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Measurement of Ferroelectric Films in MFM and MFIS Structures

Jackson D. Anderson

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A Thesis Submitted
in Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in
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R·I·T | Kate Gleason College of ENGINEERING

Department of Electrical and Microelectronic Engineering
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Measurement of Ferroelectric Films in MFM and MFIS Structures

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Soli Deo gloria.

Abstract

For many years ferroelectric memory has been used in applications requiring low power, yet mainstream adoption has been stifled due to integration and scaling issues. With the renewed interest in these devices due to the recent discovery of ferroelectricity in HfO_2, it is imperative that the properties of these films are well understood. To aid that end, a ferroelectric analysis package has been developed and released on GitHub and PyPI under a creative commons non-commercial share-alike license. This package contains functions for visualization and analysis of data from polarization, leakage current, and FORC measurements as well as basic modeling capability. Functionality is verified via the analysis of lead zirconate titanate (PZT) capacitors, where a multi-domain simulation based on an experimental Preisach density shows decent agreement despite measurement noise. The package is then used in the analysis of ferroelectric HfO_2 films deposited in metal-ferroelectric-metal (MFM) and metal-ferroelectric-insulator-semiconductor (MFIS) stacks. 13.5 nm HfO_2 films deposited on a semiconductor surface are shown to have a coercive voltage of 2.5 V, rather than the 1.9 V of the film in an MFM stack. This value further increases to 3-5 V when a lightly doped semiconductor depletion and inversion capacitance is added to the stack. The magnitude of this change is more than can be accounted for from the 10% voltage drop across the interfacial oxide layer, indicating that the modified surface properties are impacting the formation of the ferroelectric phase during anneal. In light of this, care should be taken to map out ferroelectric HfO_2 properties using the particular physical stack that will be used, rather than using an MFM stack as a proxy.

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List of Symbols

Term	Description	Units/Value
V_c	Coercive Voltage	V
E_c	Coercive Field	V/cm
P_r	Remnant Polarization Charge	C/cm^2
E_{bias}	Bias field	V/cm
E, E_α	Forward Switching Field	V/cm
E_r, E_β	Reverse Switching Field	V/cm
P_s	Saturation Polarization Charge	C/cm^2
ϵ_0	Permittivity of Free Space	$8.854 * 10^{-14}$ F/cm
ϵ_r	Relative Permittivity	
U	Potential Energy Density	J/cm^3
α_0	2nd-order Landau Parameter	cm/(F*K)
β	4th-order Landau Parameter	cm^5/(F*C^2)
γ	6th-order Landau Parameter	cm^9/(F*C^4)
T	Temperature	K
T_c	Curie Temperature	K
E_{apl}	Applied Electric Field	V/cm
V_{DS}	Drain to Source voltage	V
C_{gb}	Gate to Body Capacitance	F/cm^2
C_s	Semiconductor Capacitance	F/cm^2
C_{fe}	Ferroelectric Capacitance	F/cm^2
ρ^-	Forward Switching Polarization Charge	C/cm^2
I_D	Drain current	A
S	Subthreshold swing	mV/dec

Chapter 1

Introduction to Ferroelectricity

Ferroelectricity has been studied for years, with discussions about the phenomenon dating as far back as 1920 [1]. In fact, the first patent for a field-effect device using ferroelectric films dates back to the 1950's, not long after the invention of the transistor itself [2]. Despite this fact, ferroelectric films have remained in relative obscurity outside of a select few markets. This chapter will provide an introduction of what a ferroelectric film is, as well as some ways that ferroelectricity is quantified and modeled. Different ferroelectric materials will then be discussed, shedding some light on the challenges that have relegated traditional ferroelectric materials and devices to niche markets as well as some new developments that have shown hope for bringing new ferroelectric devices into mainstream use.

1.1 Ferroelectric Basics

Within the category of dielectric films, there are several films that are piezeoelectric, exhibiting charge generation when mechanical fields are applied. Of these piezoelectric films, a subset are pyroelectric, exhibiting charge generation upon the application of thermal fields. Likewise, a subset of pyroelectric films are ferroelectric and exhibit charge generation due to the application of electric fields. Where films fall in this heirarchy, seen in Fig. 1.1, is driven by the crystal structure of the material, with a non-centro symmetric crystal phase being necessary in order to have two stable

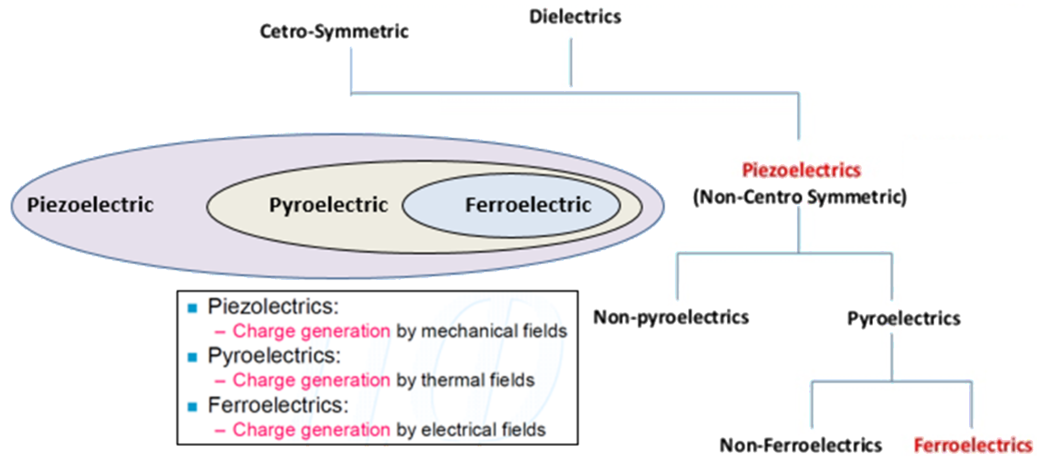
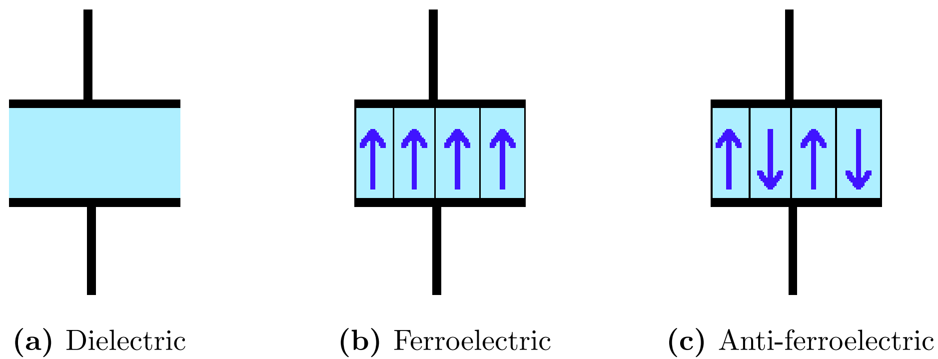


Figure 1.1: The hierarchy of dielectric materials.

polarization states for the atoms in the crystal lattice. Some materials, such as HfO_2, exist in a variety of crystal phases with only one of them being ferroelectric.

The fundamental measures of ferroelectricity are the remnant polarization charge and the coercive field of the material. The coercive field, E_c, is the electric field required to induce a change between the two stable polarization charge states. Once in either the up or down state, the material exhibits a characteristic charge even when the applied electric field is removed. This value is the remnant polarization, P_r. Sometimes, it may require more of a field to switch the film in one direction than it does the other. When this happens, the film is said to have a bias field, E_{bias}. Ideally the entire ferroelectric film would exhibit the same properties and switch at the exact same time. In reality, however, most films contain multiple ferroelectric domains that have slightly varying coercive and bias fields. In some materials, the ferroelectric dipoles that exist tend to orient in opposite directions when bias is removed. These materials are said to be anti-ferroelectric and exhibit little to no remnant polarization, despite displaying hysteretic behaviour when a field is applied. The orientation of polarization charge dipoles when bias is removed is summarized in Fig. 1.2.



(a) Dielectric **(b)** Ferroelectric **(c)** Anti-ferroelectric

Figure 1.2: Polarization charge vectors in dielectric, ferroelectric, and anti-ferroelectric films at zero applied bias.

1.2 Models of Ferroelectricity

Over the nearly 100 years of study that ferroelectric films have undergone, there have been numerous models proposed in an effort to understand the films and their behaviour in electronic systems. Covered first in this section is the Preisach model - a basic model borrowed from ferromagnetic device studies that serves as a good introduction to ferroelectric devices. Following that, the Miller model is examined. This model, extended by Lue et al., provides a mathematical framework for generating electrical behaviour similar to that seen in ferroelectric devices. Finally, a deep dive will be taken into a thermodynamic theory of phase transitions put forth by Landau in the 1960's. This relatively recent approach to characterizing ferroelectric behaviour has been instrumental in investigating some intriguing behaviour in ferroelectric transistors.

1.2.1 The Preisach Model

The Preisach model, proposed in 1935, is the oldest of the three models that will be discussed [3]. This model represents a ferroelectric film as being composed of a number of hysterons - an ideal domain of fixed remnant charge that switches instantly from one state to the other when the coercive field is reached (Fig. 1.3). The overall behaviour

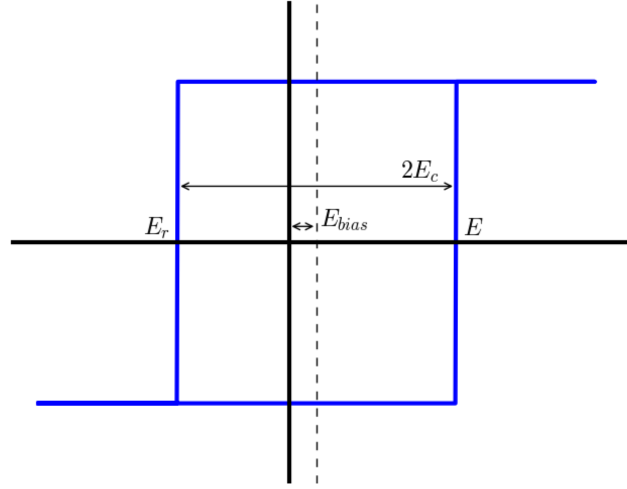


Figure 1.3: The ideal hysteron representation of ferroelectric domains.

of the film is dependent on the distribution of the bias and coercive field parameters of this collection of hysterons. This probability distribution function (PDF) of domains in E_{bias} and E_c space is known as the Preisach density. An example PDF for a film that could contain the domain from Fig. 1.3 is shown in Fig. 1.4.

While E_{bias} and E_c are typically preferred for describing the properties of a hysteron, experimental data will sometimes refer to a hysteron by its forward switching field (E or E_α) and its reverse switching field (E_r or E_β). These values can be changed to E_{bias} and E_c values via a 45 degree coordinate transform as shown in Eqs. (1.1) and (1.2) [4].

$$E_c = \frac{E - E_r}{2} \tag{1.1}$$

$$E_{bias} = \frac{E_r + E}{2} \tag{1.2}$$

When plotting the Preisach density, only the lower right half of the plotted plane is used. This is because of the fact that E is defined as being the positive-most switching

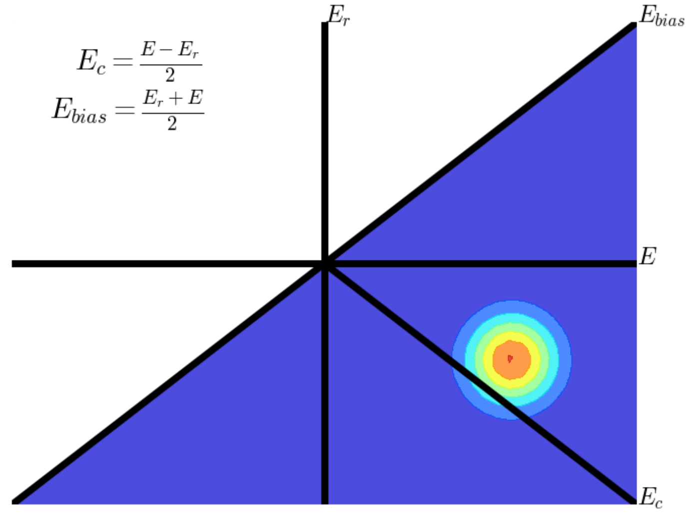


Figure 1.4: The Preisach diagram, showing the probability distribution of domains centered at positive coercive and bias fields in a ferroelectric sample.

field of the ferroelectric film and can never be less than E_r. Thus, there will never be any data left of the $E = E_r$ line. Thought of in terms of E_c and E_{bias}, there will never be a case where a ferroelectric film has a hysteresis curve of negative width - E_c will always be positive. The Preisach representation of a ferroelectric domain may be simple, but it provides a relatively easy way to model ferroelectric films using just a handful of experimentally measured parameters, something that can be extremely valuable when a highly detailed model of film behaviour is not required.

1.2.2 The Miller/Lue Model

The Miller model, proposed by Miller et al. in 1990, presents a mathematical description of the hysteresis curve seen in experimental hysteresis measurements [5]. This mathematical description, given by

$$P_{+}(E) = P_{s} tanh\left(\frac{E - E_{c}}{2\delta}\right) + \epsilon_{r}\epsilon_{0}E \tag{1.3}$$

with

$$\delta \equiv E_c \left(ln \left(\frac{1 + \frac{P_r}{P_s}}{1 - \frac{P_r}{P_s}} \right) \right)^{-1}, \tag{1.4}$$

is used to calculate half of the hysteresis loop and is then rotated 180° to give the other branch. The linear term of Eq. (1.3) represents the normal dielectric behaviour of the film while the first term represents the hysteretic component. The saturation polarization P_s and its relationship to P_r is used to modulate how quickly the ferroelectric switches from one state to the other.

This formalism was extended further by Lue et al. in 2002, who included additional terms to describe the behaviour of a ferroelectric material when an electric field is applied that switches some, but not all, domains [6]. These minor or non-saturated loops are useful for describing some ferroelectric behaviour, but are limited in their ability to describe non-saturated ferroelectric switching that is not symmetric about the origin. Such switching would occur anytime after the ferroelectric film is initially biased into a certain state and a different voltage is subsequently applied. When an electric field is applied that is sufficient to switch some but not all domains, domains that have an E_c larger than the field applied will simply remain in their current state rather than switching. If most domains are switched to the negative state but some remain in the positive state, what results is an asymmetric hysteresis loop since the film has gone from all domains being in one state to an overall mixed state. Nevertheless, the model remains a valuable tool for investigating the behaviour of ferroelectric films in memory devices.

1.2.3 The Landau Model

The symmetry-based Landau theory states that, in the vicinity of a phase transition, the Gibb's free energy density can be represented by an even power series expansion such as that given in Eq. (1.5) where α_o, β, and γ are empirical material constants, the Curie temperature T_c represents the temperature at which ferroelectric behaviour

disappears, and E_{apl} represents the applied electric field [7].

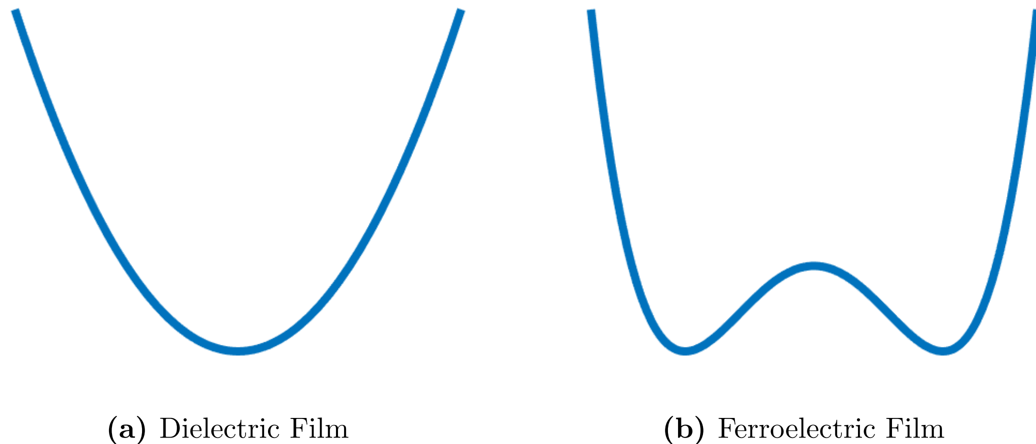
$$U_{fe} = \alpha_o(T - T_c)P^2 + \beta P^4 + \gamma P^6 - E_{apl}P \tag{1.5}$$

If $T < T_c$ while α_o, β, and γ are positive, one obtains the ferroelectric energy landscape seen in Fig. 1.5b. If $T > T_c$, the ferroelectric behaviour disappears and the film acts similar to a normal dielectric, seen in Fig. 1.5a. As bias is applied to a ferroelectric film, the energy density profile tilts until one of the two wells becomes high enough that the associated energy minimum disappears. At this point, it becomes more energetically favorable to move to the other well. When bias is decreased and subsequently forced in the other direction, it must reach a certain non-zero magnitude (the coercive field/voltage) before the previously energetically favorable well becomes high enough that the barrier disappears and the charge can move to the other well.

An antiferroelectric film can be obtained by superimposing several different ferroelectric domains with different parameters. The superposition of domain potential energy profiles results in an energy density-charge relationship where there is a well near $P = 0$ as well as at larger non-zero values. Such a relationship leads to two regions of hysteresis as bias is applied with a region of little to no hysteresis at zero applied bias.

1.3 Applications of Ferroelectricity

The uses for ferroelectric films are numerous as the models proposed to explain their behaviour. Ferroelectric properties have been taken advantage of in a variety of devices over the years including capacitor-based ferroelectric random access memory (FRAM/FeRAM), ferroelectric tunnel junctions (FTJs), and ferroelectric transistors (FeFETs) for memory and logic applications. Many of the ferroelectric memory device concepts have familiar aspects that are shared with current mainstream memories,



(a) Dielectric Film **(b)** Ferroelectric Film

Figure 1.5: Potential energy landscape comparison of dielectric and ferroelectric films.

as several ferroelectric devices replace charge storage or injection with polarization charge. Other emerging ferroelectric devices may be less familiar, with the negative-capacitance ferroelectric transistor (NC-FET or NC-FeFET) being particularly new.

1.3.1 Capacitor-Based FRAM

The use of ferroelectric capacitors in combination with traditional CMOS access transistors is the main commercial driver of ferroelectric memory devices today and has been since the 1990's. In particular, ferroelectric memory shines in applications that require low power, fast speeds, and radiation hardness such as secure ID cards, smart meters, and medical devices [8]. While several different cell structures exist, the most basic is the 1T1C cell. This cell is similar to dynamic random access memory (DRAM) in that the combination of a bit-line and word-line can be used to access any individual ferroelectric capacitor. In fact, much of the circuitry and theory of operation are shared with DRAM. The main difference, however, is in the advantages inherent in using ferroelectric polarization charge over traditional capacitive charge storage. Firstly, unlike traditional DRAM devices, capacitor-based FRAM devices are non-volatile. When power is removed from a ferroelectric device, the charge stored on the capacitor will dissipate. The ferroelectric polarization state, however, does not.

Rather, the capacitor will relax back to its remnant polarization value, a value that it will maintain for upwards of ten years in a properly engineered device [9]. This fact leads directly to a second advantage of ferroelectric memory over DRAM, which is that it does not require constant refreshing to prevent bits from flipping. This leads to dramatically reduced power consumption, something that is extremely desirable in mobile applications.

1.3.2 Ferroelectric Tunnel Junction

The ferroelectric tunnel junction is a relatively new class of ferroelectric memory, based on the concept of the memristor, that seeks to create ferroelectric memory in a compact 1C cell structure. In this approach, a ferroelectric layer thin enough to have appreciable tunneling current is sandwiched between two electrodes. The ferroelectric polarization state of the film is then used to modulate the tunneling barrier, in effect creating a resistor whose resistance is based on previously applied voltages [10]. If the ferroelectric film is composed of many domains of varying properties, such a device is able to exhibit a range of resistances between the two fully saturated polarization states - a property that is especially useful for providing weighting in neuromorphic applications. These devices have not been commercialized yet, but they have potential for use in the types of 3D crossbar memory architectures that are just now becoming mainstream [11].

1.3.3 Ferroelectric Transistors

1.3.3.1 Memory FeFET

Long theorized, the ferroelectric transistor promises to give the benefits of capacitive-based ferroelectric memory with the density of flash memory due to a 1T cell. Data is stored in the transistor via way of polarization charge in the ferroelectric gate, which then leads to a threshold voltage shift for the device. A read-out voltage is chosen

somewhere between the two states' threshold voltages such that the device turns on for readout in one state but not the other. To rewrite the cell, V_{ds} is set to zero and a gate voltage larger than the coercive voltage of the film is applied. The process designer must balance the coercive voltage of the ferroelectric gate along with the remnant polarization and capacitance to create a device that is energy efficient due to low rewrite voltages while offering robustness via comfortable read-write voltage margins.

While theoretically elegant, there are reasons that these devices have not reached mainstream use. Unlike their 1T1C counterparts, FeFETs so far have struggled to provide good data retention. This is due to interfacing issues between most ferroelectric materials and silicon. Interface problems are mitigated via the addition of a thin dielectric buffer layer, however this leads to a depolarization field that counteracts the ferroelectric polarization state [9]. The problem stems from the fact that, with the addition of a buffer layer, there now exists two capacitors in series in the gate stack. Thus, when power is removed from the device, the substrate and the gate are at ground potential whereas the interface between the two gate layers is left floating. Charge builds up on this floating interface to compensate the ferroelectric polarization charge, leading to a non-zero voltage and electric field that act to depolarize the ferroelectric film.

1.3.3.2 Logic FeFET

The most recently proposed use for ferroelectric films is in the domain of steep subthreshold slope logic transistors [12]. These devices are structurally similar to FeFETs used for memory devices but the ferroelectric film behaviour and threshold voltage of the device have been tuned such that the ferroelectric film switches states while the transistor is turning on and/or off. These devices achieve their steep switching characteristics via a transient negative capacitance phenomenon, hence their being

called negative capacitance transistors.

The idea at the heart of these devices is that, while typically unstable by itself, a negative capacitance can be stabilized when in series with another positive capacitor. This stems from the fact that the total capacitance of a series combination of capacitors in the gate of a transistor (and in general) is the harmonic mean of the individual values. That is,

$$C_{gb} = \left(\frac{1}{C_s} + \frac{1}{C_{fe}}\right)^{-1} = \frac{C_s C_{fe}}{C_s + C_{fe}}. \tag{1.6}$$

When both capacitors are positive, this typically results in a positive value that is less than either of the individual values. When one capacitor is negative but smaller in magnitude than the other, the overall expression is negative and is unstable (resulting in hysteresis). When one capacitor is negative and larger in magnitude than the other, however, the numerator and denominator of Eq. (1.6) are both negative and the overall capacitance becomes positive [13]. This is shown graphically in Fig. 1.6 for a fixed value of C_s. While this shows the relationship between a negative capacitance and an overall capacitance, it does not explain how a negative capacitance comes about in the first place. To understand that, one must look back to Landau theory.

Starting with Eq. (1.5), one can obtain the polarization charge vs. electric field relationship by differentiating with respect to polarization charge. From here, the polarization vs. voltage relationship can be given by multiplying by the thickness of the ferroelectric film:

$$V_{fe} = t_{fe} * \frac{dU}{dP} = t_{fe} * \Big(2\alpha_o(T - T_c)P + 4\beta P^3 + 6\gamma P^5 - E_{apl}\Big) \tag{1.7}$$

Using the definition of capacitance, the capacitance per unit area can then be found:

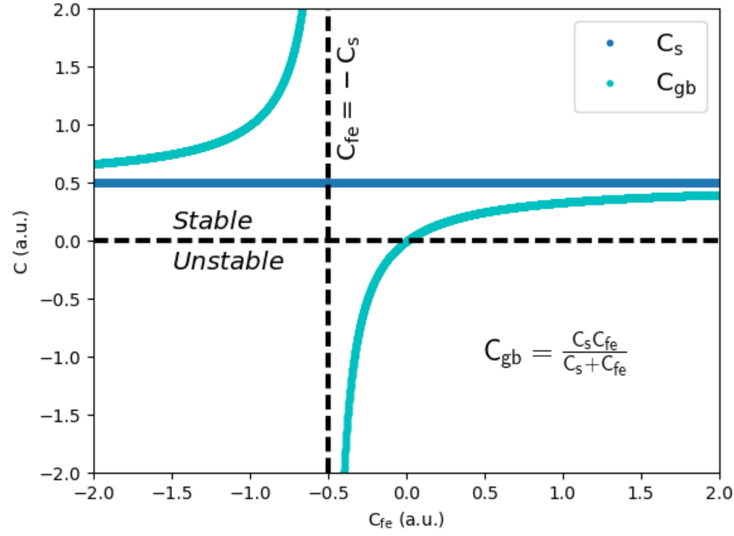
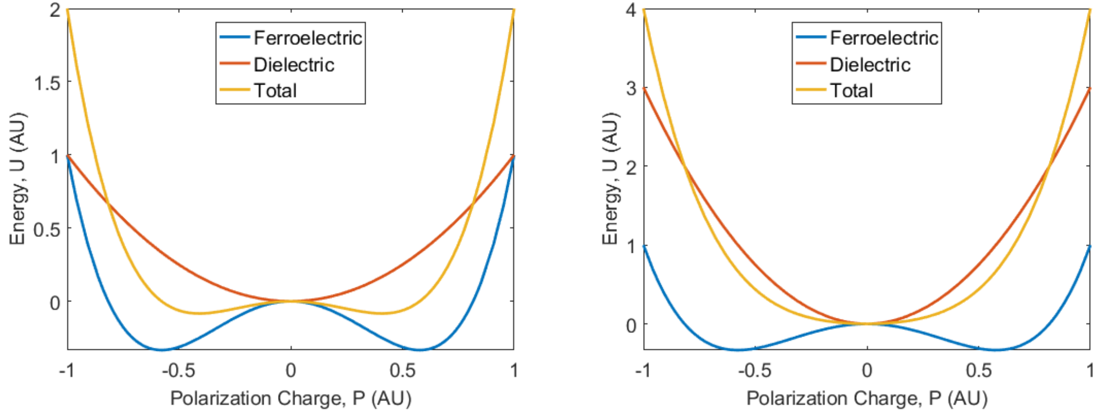


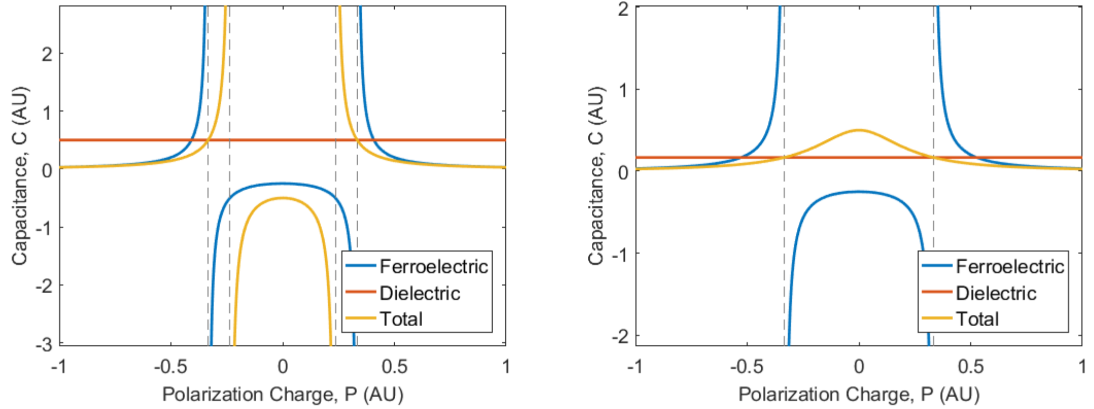
Figure 1.6: Impact of varying ferroelectric capacitance on gate to body capacitance of a FeFET.

$$C_{fe} = \left(\frac{dV}{dP}\right)^{-1} = \frac{1}{t_{fe} * \left(2\alpha_o(T - T_c) + 12\beta P^2 + 30\gamma P^4\right)} \tag{1.8}$$

Using this definition of capacitance and Eq. (1.6), the overall capacitance and effective potential energy profile of a system with a ferroelectric capacitor in series with a fixed capacitance is shown in Fig. 1.7. In the case where the negative capacitance of the ferroelectric is not larger in magnitude than its peer for all values of charge, the resulting capacitance looks similar to the original ferroelectric film, albeit with a narrower window of negative capacitance. This results in an overall ferroelectric behaviour with shallower wells (and, therefore, less hysteresis). On the other hand, when the negative ferroelectric capacitance is always greater than that of its peer, what results is a variable positive capacitance that is greater than the constant capacitance during ferroelectric switching and less than the constant capacitance otherwise. If this area of ferroelectric switching occurs at a voltage around the threshold voltage of the transistor, the polarization charge will pass through the area of negative capacitance during device turn-on, transiently giving a higher capacitance and, thus,



(a) Energy profile of unstabilized NC system **(b)** Energy profile of stabilized NC system



(c) Capacitance of unstabilized NC system **(d)** Capacitance of stabilized NC system

Figure 1.7: Energy and capacitance vs. charge characteristics (in arbitrary units) for a series combination of ferroelectric capacitance C_{FE} and dielectric capacitance C_{DE} with $C_{FE} > -C_{DE}$ (left) and $C_{FE} < -C_{DE}$ (right).

a steeper sub-threshold slope.

1.4 Ferroelectric Materials

When ferroelectric materials are referenced, most often the subject of discussion will be a perovskite material such as lead zirconate titanate (PZT) or strontium bismuth tantalate (SBT). Commercial production of ferroelectric memory devices, however, has remained at nodes >100 nm due to the large area capacitors required to generate charge differences between readout states when using these films. A typical perovskite

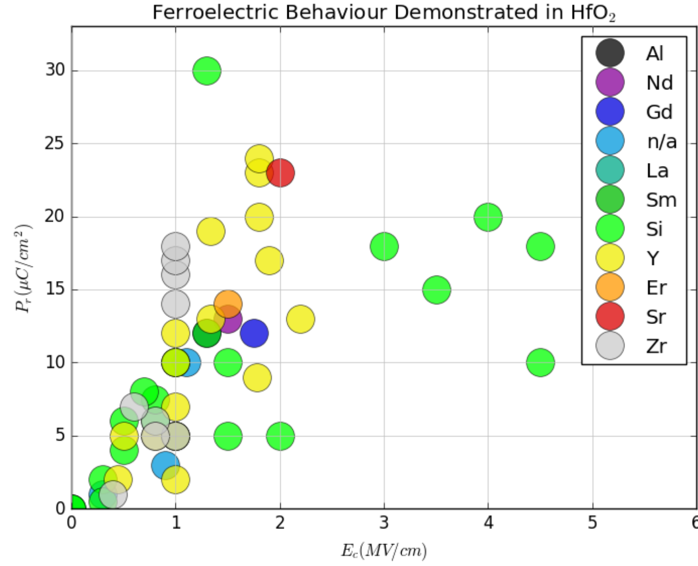


Figure 1.8: Demonstrated ferroelectric behaviour in HfO_2 thin films for a variety of dopants. [14–25]

film exhibits a remnant polarization of about 30 μC/cm^2 or $3 * 10^{-19}$ C/nm^2. Efforts have been made to scale down perovskite ferroelectrics using the FeFET architecture; however, the interfacing between these films and silicon remains a great challenge. Thick buffer layers are required, decreasing device performance. Furthermore, a coercive field of around 10^5 V/cm means that a 100 nm high gate dielectric is required to get a 1 V operating window for the device, limiting scaling [9].

An alternative to traditional perovskite materials has recently been found with the discovery of ferroelectric behaviour in HfO_2. This newly discovered behaviour comes about as a result of forcing the film into an orthorhombic phase via stress during the annealing process. This stress is applied both via the incorporation of dopants such as silicon into the crystal lattice as well as via the application of a capping layer [14]. HfO_2 exhibits a range of ferroelectric properties based on the dopants added and the anneal process that is performed, a fact that is highlighted in Fig. 1.8.

The most notable difference between ferroelectric HfO_2 and perovskite films is found in their coercive field values. HfO_2 exhibits a coercive field an order of mag-

	Perovskites	Doped HfO_2
Typical P_r (μC/cm^2)	30	5-30
Typical E_c (MV/cm)	0.1 - 0.2	1 - 2
Process Technology	130 nm	28 nm
CMOS Compatibility	Poor	Good
Fabrication	BEOL	FEOL
Memory Cell	1T-1C / 2T-2C	1T

Table 1.1: Comparison of perovskite and HfO_2 ferroelectric materials [9, 26–28].

nitude larger than that of its ferroelectric peers, making it much more suitable for scaling. It is also relatively well understood due to its years of use as a high-k gate dielectric in the CMOS industry. These facts together mean that ferroelectric transistors are for the first time becoming a potentially viable solution, with 28 nm HfO_2 FeFETs demonstrating an endurance of 10^5 cycles being manufactured on-die with traditional logic devices [26]. While this is still far away from the 10^{14} cycle endurances shown by commercial FRAM devices, it shows significant promise for a material that was just discovered six years ago [27]. A summary comparing perovskite and HfO_2 ferroelectric films is given in Table 1.1.

1.5 Summary

Knowing the current commercial applications of ferroelectric films and the potential market given the properties recently found in HfO_2, it is important that the behaviour of these new ferroelectric films is well understood. In order to evaluate these properties, however, one must have a thorough understanding of the methods used to extract the parameters from experimental samples, a topic that will be covered in detail in Chapter 2.

Chapter 2

Characterization of Ferroelectric Materials

Compared to a traditional dielectric film, ferroelectric films are quite complex, with a host of stress, temperature, and field-dependent parameters that modulate their behaviour. This chapter does not pretend to be an exhaustive primer on ferroelectric material characterization. Rather, it will focus on the types of measurements that can be used to analyze the ferroelectric properties of a film under a constant stress. While some of these will be performed at various temperatures to provide insight into the temperature-dependent behaviour of the film, the piezoelectric behaviour of the film is not discussed in the scope of this work. Covered in this chapter are four primary ferroelectric measurement techniques: the dynamic hysteresis measurement, the positive-up negative-down (PUND) measurement, the leakage current measurement, and the measurement of first-order reversal curves.

2.1 Dynamic Hysteresis Measurement

The dynamic hysteresis measurement is perhaps the most fundamental measurement of ferroelectric films, providing a hysteresis curve at a given frequency as its output. During a dynamic hysteresis measurement, the device under test (DUT) is first subjected to a pre-polarization pulse. The purpose of this pulse is to cycle the film and ensure that the ferroelectric domains are in a known state. Once this is done, a voltage pulse is applied such that the ferroelectric film switches first to one state

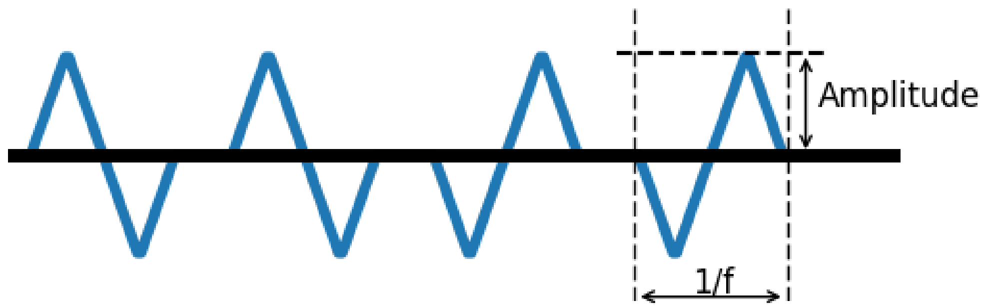


Figure 2.1: Voltage vs. time waveform for the dynamic hysteresis measurement

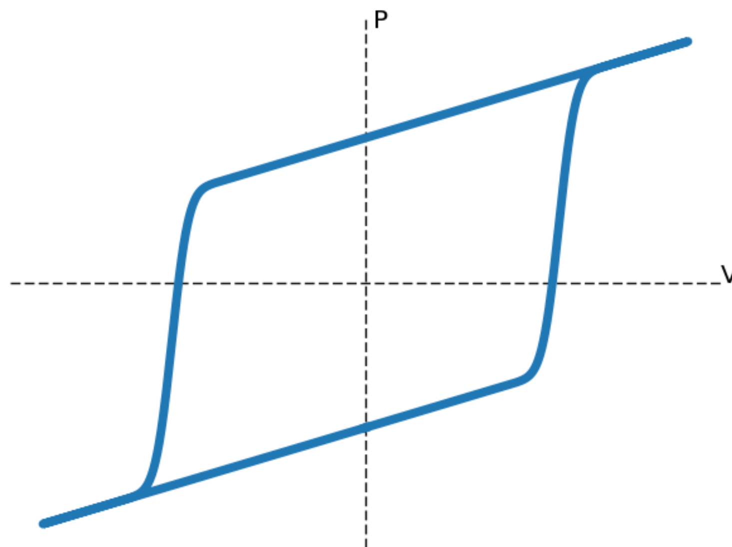
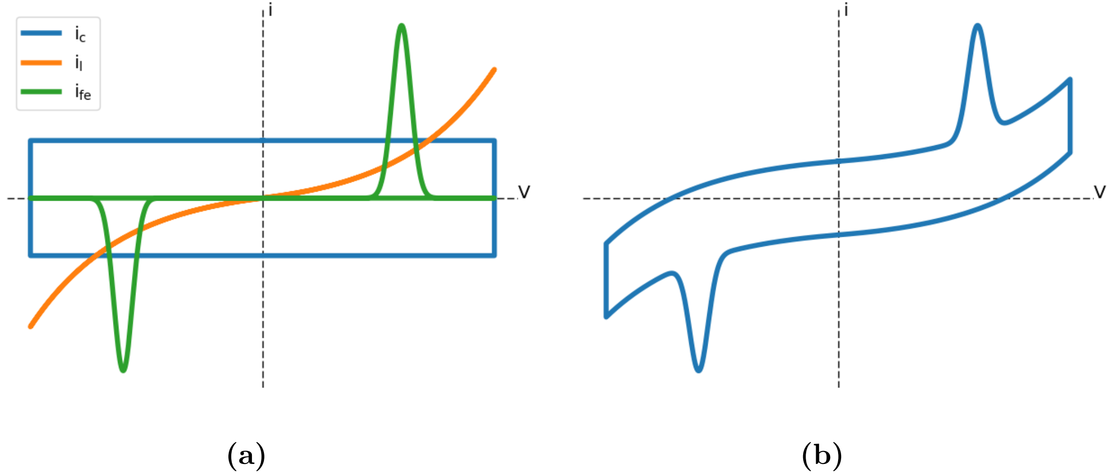


Figure 2.2: A typical hysteresis that would be seen from a sample with low leakage current.

and then to the other, resulting in a complete picture of the hysteresis of a sample. This process is then in some cases repeated going in the opposite direction around the hysteresis loop, allowing the two loops to be averaged together [29]. A typical input waveform for the measurement as described is given in Fig. 2.1, with an example of a resulting hysteresis loop given in Fig. 2.2.

While many circuits exist to measure the response of ferroelectric films, the aix-ACCT TF-1000 instrument used in this study uses the virtual ground method. This particular implementation utilizes an op-amp with selectable gain to amplify and



(a) **(b)**

Figure 2.3: Components of measured sample current (left) and overall measured current (right) for a hysteresis measurement.

measure the current passing through the ferroelectric film as a function of applied voltage [30]. The measured ferroelectric current is then integrated with respect to time to obtain the measured polarization charge. The current that is measured is not all ferroelectric switching current, however. Rather, it is a combination of the desired ferroelectric current as well as capacitive and leakage currents. That is,

$$i_{meas} = i_l + i_c + i_{fe}. \tag{2.1}$$

An example of what this measured current may look like is shown in Fig. 2.3.

The triangular shape of the applied voltage waveform is important, as it provides a constant $\frac{dV}{dt}$. This leads to the current shown in Fig. 2.3a and means that the capacitive current contribution to the measurement is constant, allowing for the ferroelectric switching current to be more easily extracted. Leakage current, if it is significant for the sample being measured, is a more complicated component to model but can be measured directly as will be discussed in Section 2.3.

Of interest to those looking to implement ferroelectric films in commercial devices is the stability of these ferroelectric parameters over many switching cycles. A so-called fatigue measurement of a film consists of taking a series of hysteresis mea-

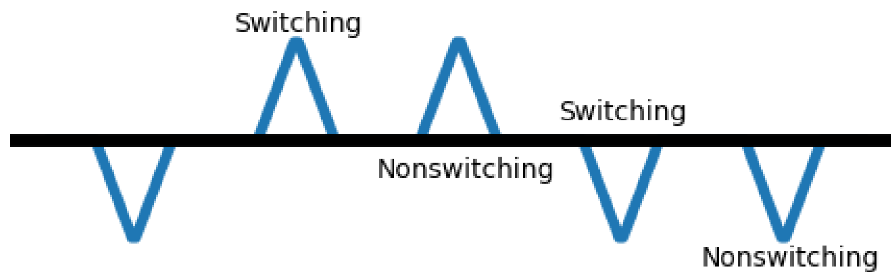


Figure 2.4: Possible voltage vs. time waveform for a PUND measurement.

surements while cycling the film in between. This allows the user to map the evolution of ferroelectric parameters over the entire cycling lifetime of a film - information that can be used to choose an optimal film and design appropriate noise margins into the final application.

2.2 PUND Measurement

Another measurement that is often used in characterization of ferroelectric materials is the positive-up negative-down, or PUND, measurement. This measurement is similar in many aspects to the dynamic hysteresis measurement discussed above. The measurement seeks to characterize the hysteresis of a sample just like before, but it does so by polarizing the film in the same direction twice. This allows for capturing both the switching and non-switching current characteristics of the film, the difference of which essentially cancels out non-ferroelectric effects, giving a cleaner view of the ferroelectric properties of the film. While this test is often performed with trapezoidal voltage pulse waveforms, it can just as well be performed as shown in Fig. 2.4 with triangular pulses similar to those used in dynamic hysteresis measurements [31].

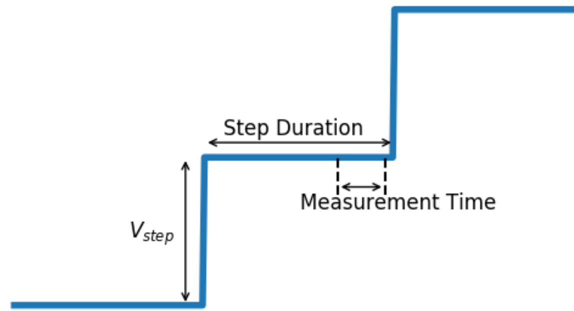


Figure 2.5: A portion of the voltage pulse used in leakage current measurements, showing the delay after a voltage step that allows capacitive current contributions to subside.

2.3 Leakage Current Measurement

As shown earlier, leakage current can cause a relatively large unwanted distortion in the total current measured in dynamic hysteresis measurements. In samples where leakage current is an appreciable fraction of the ferroelectric current, it can be helpful to analyze the leakage current component separately from the ferroelectric and capacitive currents. This is done through a leakage current measurement.

The leakage current measurement, unlike the measurements discussed up to this point, does not have a constant $\frac{dV}{dt}$. Rather, a step function with a defined duration is used to traverse voltages from a given V_{min} to V_{max}. Assuming a step duration of several time constants is chosen, the capacitive current decays to zero before the current at that voltage is recorded. This means that only resistive leakage current is measured, allowing the user to determine the influence of leakage on any hysteresis measurements for the sample.

2.4 First-Order Reversal Curves

The last type of measurement that will be discussed is the method of measuring first-order reversal curves (FORCs). This method was first applied to ferroelectrics as far

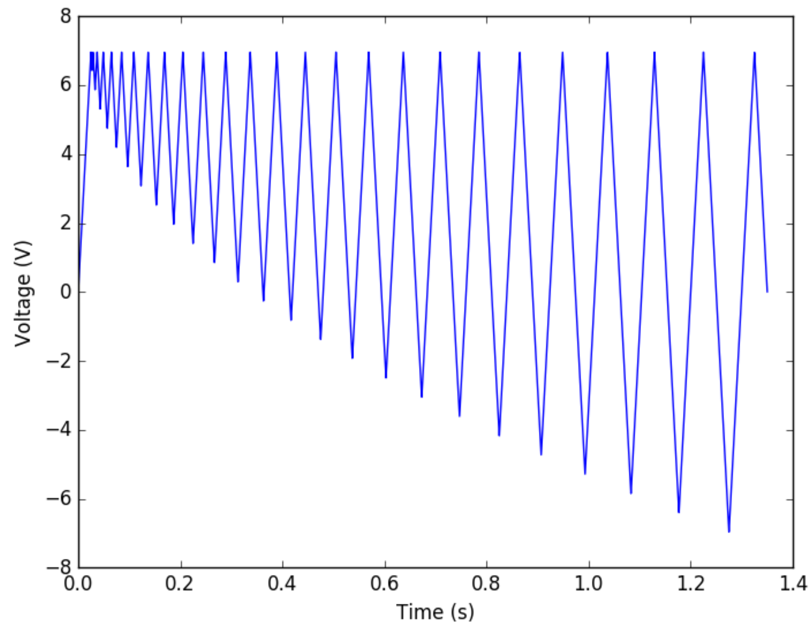


Figure 2.6: The voltage vs. time waveform used in FORC measurements.

back as the 1960's, and has more recently been applied to a variety of ferroelectric films [4, 32, 33]. The FORC measurement can be thought of as a series of hysteresis measurements starting in one polarization state and progressively moving towards the other polarization state. This waveform, shown in Fig. 2.6, leads to several nested hysteresis loops for the film and can be used to see the exact reverse bias at which the ferroelectric domains start to switch states.

From the entirety of the measured data, the polarization values going backwards along the curve are removed, leaving only the forward-sweeping values, designated ρ^- and shown in Fig. 2.7. It is this data, which represents the polarization charge during switching as a function of reverse voltage, that is used to calculate an experimental probability density function for domain switching. This is done by taking the mixed partial derivative of ρ^- with respect to the forward and reverse voltages (or fields) and normalizing the resulting landscape to have a total probability of one.

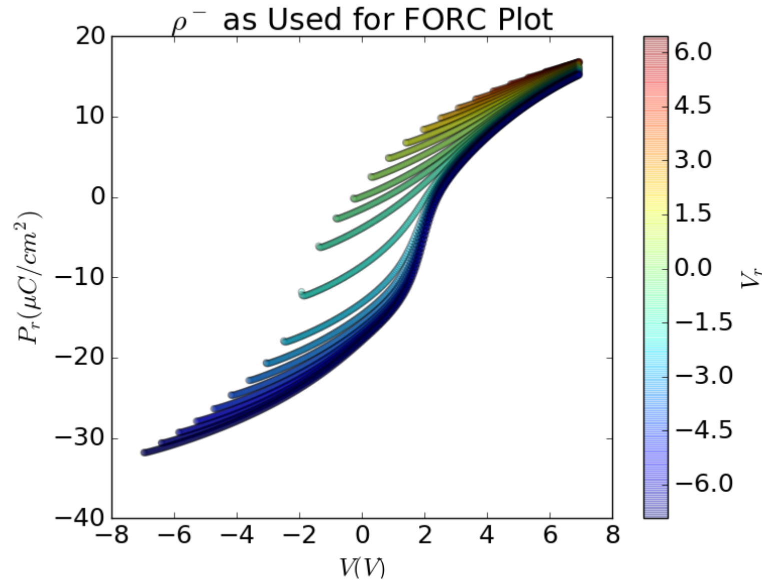


Figure 2.7: Hysteresis data from FORC measurement used to generate Preisach diagram.

2.5 Summary

The aforementioned electrical tests together can be used to obtain a picture of the overall ferroelectric behaviour of a thin film. Once this data is collected there is a good deal of analysis that can and should be performed to gain a better understanding of film behaviour. Chapter 3 will discuss in-detail a package that was specifically developed to ease this task.

Chapter 3

Developing a Framework for Ferroelectric Film Analysis

Before analysis of test data from the ferroelectric devices could be completed, the data had to be exported from the ferroelectric tester and transformed into a usable format. To that end, a Perl script was developed to parse the TF-1000 tester output files into separate tab-separated value (TSV) files for each measurement. To perform analysis on the data, a python package was created. Python was chosen for its open-source nature, allowing other research groups to easily benefit from and contribute to the code going forward. Additionally, Python has a rich set of features through modules such as scipy, numpy, and matplotlib that allow for advanced data analysis and visualization. This chapter serves as an introduction to the code that was written and will be used for the majority of device analysis in this paper. Included is an explanation of the workflow as well as the theory behind functions dealing with data analysis. The package (as well as the Perl script) is available in its entirety on the Python Package Index (PyPI) and GitHub under a creative commons non-commercial share-alike license.

3.1 Overview of Package Structure

The developed ferro package consists of two main parts and can be seen in Fig. 3.1. The first part consists of objects that represent imported data as well as methods for importing, viewing, and filtering said data. The other part of the package consists

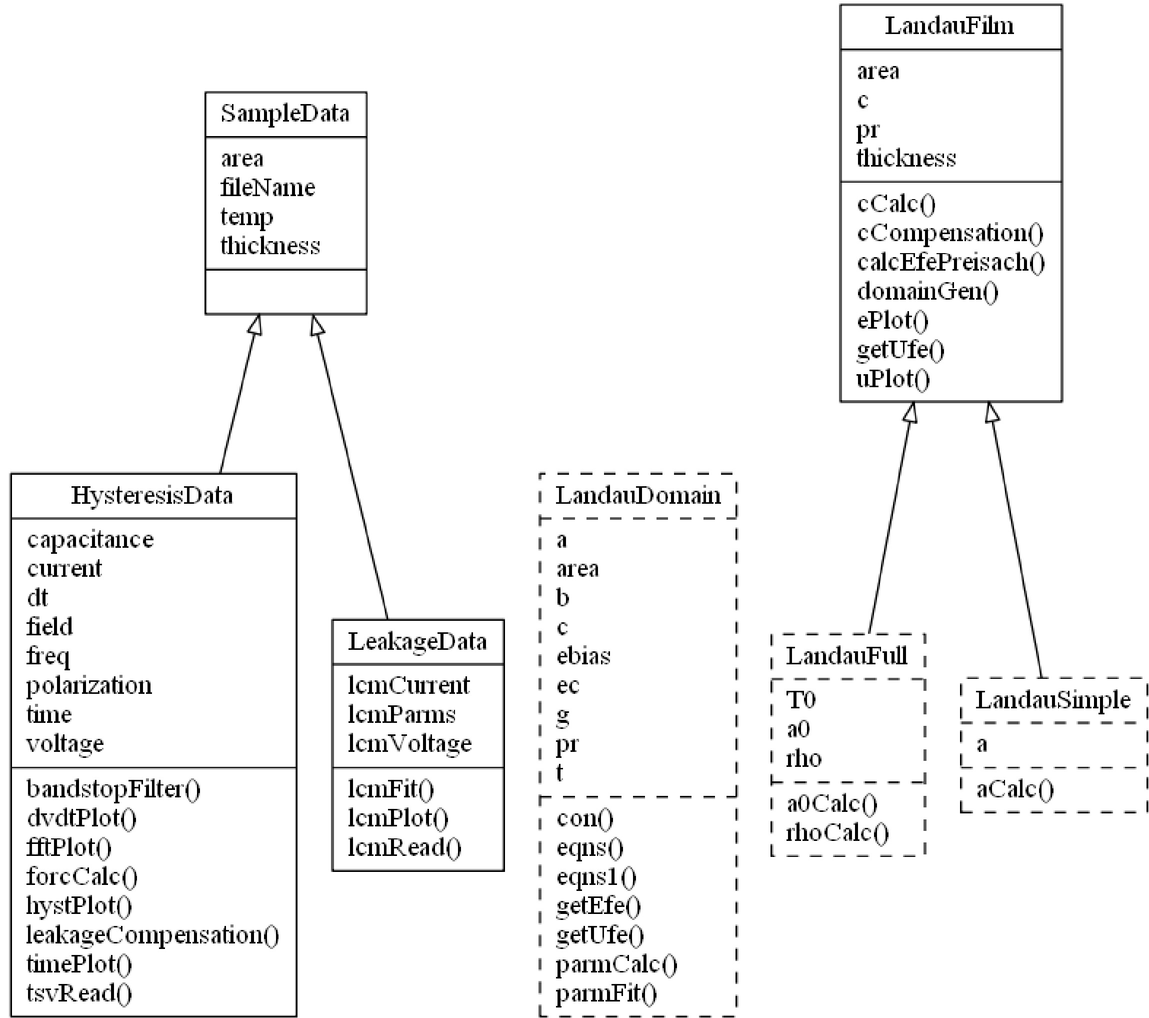


Figure 3.1: Structure of Python ferro package. Experimental features indicated with dashed borders.

of objects for modeling ferroelectric films based on acquired measurement data. The following sections will investigate both halves of the ferro package in more detail, explaining the different methods contained within and the techniques utilized.

3.2 SampleData

Data classes are used to represent a single measurement of a sample carried out under specific conditions. Currently there are two types of data implemented: hysteresis or FORC (P-V) measurement data (*HysteresisData*) and leakage current measurement

data (*LeakageData*). Both of these classes inherit the *SampleData* class, which contains certain attributes that are used by all data classes such as measurement data file name and sample characteristics such as area, thickness, and temperature during measurement.

3.2.1 HysteresisData

The *HysteresisData* class contains functions related specifically to analysis of P-V measurement data. The *tsvRead* function takes a given filename of a TSV file containing P-V data and reads the time, voltage, current, and polarization data into the current *HysteresisData* object. It will also scan the name of the TSV file for information on the temperature and frequency at which the measurement was carried out. If found, it will set the corresponding attributes appropriately. If not found, default values of 100 Hz and 300 K will be used. If the user knows that the filename does not contain information on frequency or temperature they also have the ability to specify a non-default value for the temperature and frequency when they create the *HysteresisData* object.

After the *tsvRead* function, *hystPlot* is perhaps the second most important function in the *HysteresisData* class. This function is used to view the P-V and I-V curves for the related *HysteresisData* object, allowing quick visual analysis of the measurement data complete with cursors such as would be possible on the test instrument. If desired, the user can also toggle the plotting of electric field rather than voltage by setting $plotE =$ True. An additional *hystPlot* function is implemented outside of the HysteresisData class that takes a list of *HysteresisData* objects as input. This allows for overlaying several P-V and I-V (or P-E and I-E) curves on each other to show the impact of a changing parameter on hysteretic behaviour. This method also takes a list of strings as an optional argument which, if provided, will create a legend for the data.

Closely related to *hystPlot* is *dvdtPlot*, a function which plots the absolute value of dvdt versus time. Also displayed on the plot is the mean value of the data. This function can be used to evaluate the validity of *cCalc*, a *LandauFilm* function that will be described in detail in the following section.

The *fftPlot* and *bandstopFilter* functions are available in *HysteresisData* to visualize and provide mitigation of noise in measurement data. Both of these functions take the data to be displayed/filtered as their required input. The *fftPlot* function will plot the frequency components of the given signal up to the Nyquist limit while the *bandstopFilter* function can be used to eliminate any spurious signals seen in measurement data, with the default behaviour filtering between 50 and 70 Hz to mitigate line noise. The user can also toggle a plot of the filter frequency response on or off by calling the function with the plot parameter set to true.

If there is a large amount of known leakage current in the *hysteresisData* object, the *leakageCompensation* function can be used to clean up the data before further analysis. This function takes a leakage current measurement of the sample (a *leakageData* object) and subtracts the modeled leakage current from the measured current, recalculating the hysteresis curve from the new current values. This compensation is done on a new copy of the data which is then returned, leaving the original data intact.

The last part of *HysteresisData* is contained in the *forcCalc* function, which deals with the handling of FORC data, the generation of domain probability distributions, and the display of FORC diagrams. In order to do this, the function first looks at the series of hysteresis curve measurements and notes the minima and maxima in the triangular voltage waveform. This allows it to determine which of the data constitute forward sweeps as well as the reversal voltage that should be associated with that data. The function then takes the measured data and fits a surface to it such that values are linearly spaced. After this, the mixed partial derivative with respect to the

forward and reverse field are taken and the distribution is normalized to give a total probability of one.

If the plot input parameter is set to true, the function will display a FORC diagram showing the calculated probability distribution of domain parameters as well as the data that it is based on. If the PDF is particularly noisy, a rolling average filter can be applied by setting the *filtIter* input to the desired number of passes and specifying the number of values to use in the E and E_r direction using the *filtDim* input (a list of length two). A linear parameter also exists that can be used to select the method of grid interpolation. If true (the default value), a linear grid interpolation is used. Otherwise, natural neighbor interpolation is used via the Natgrid library. Note that this non-default option requires the separate installation of Natgrid. More details can be found in the documentation for *forcCalc*.

3.2.2 LeakageData

Closely mirroring the structure of *HysteresisData* is the *LeakageData* class, which provides functions for the import and handling of leakage current measurement data. The *lcmRead* function is analogous to *tsvRead* in the *HysteresisData* class. This function takes a file path that points to a TSV and imports the voltage and current data into the *LeakageData* object. It also attempts to find a temperature in the filename and, if it does not, defaults to 300K. This data can then be viewed with *lcmPlot*, a function similar to *hystPlot* which plots voltage vs. leakage current. One difference between *lcmPlot* and *hystPlot* comes from the fact that *lcmPlot* can also plot the modeled leakage current if the user has fit parameters to the experimental data. This is accomplished with the last function in the *LeakageData* class: *lcmFit*.

While *lcmFit* is itself a simple function, it embodies the most complex part of *LeakageData*: fitting the experimental data so that it can be useful in data analysis. The *lcmFit* function takes two inputs: a reference to a function that you would like to

fit the data to and a list of initial values to pass to the given function to start the curve fitting process. As the source of leakage current is dependent on device structure and fabrication, the default function for *lcmFit* is a 5th order polynomial. This allows for a good fit of leakage currents caused by a variety of physical phenomena. If a user wishes to study the leakage current from a single source more in-depth, they are able to define their own function and pass that to *lcmFit* instead.

3.3 LandauFilm

Once sample data has been imported using the *SampleData*-derived classes, the user can next attempt to model and extract parameters from it. The first class in development for this purpose in the ferro package is *LandauFilm*, which aims to implement the Landau-Khalatnikov model discussed in Section 1.2. As the base class for the Landau model, *LandauFilm* contains parameters such as film area, capacitance, remnant polarization, and thickness that are common to both approaches that are being implemented. It also contains a host of functions shared by the underlying classes including *cCalc*, *cCompensation*, *calcEfePreisach*, *domainGen*, *ePlot*, *getUfe*, and *uPlot*.

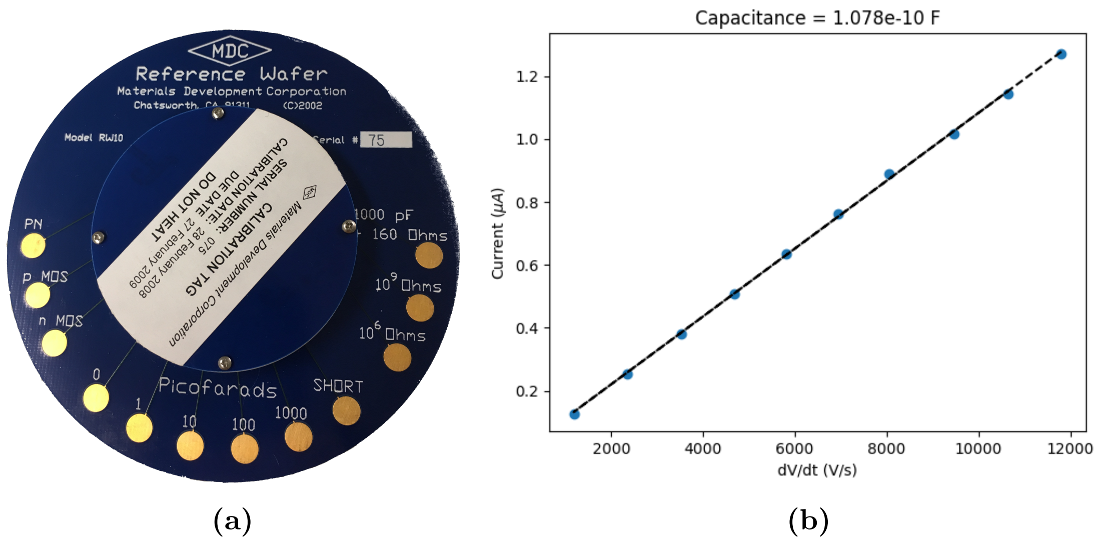
LandauFilm is the base class for two proposed models: *LandauSimple* and *LandauFull*. The *LandauSimple* class neglects ρ and lumps $\alpha_0(T - T_c)$ into a simple α parameter, modeling a ferroelectric film at a particular temperature. *LandauFull*, on the other hand, can be used when hysteresis data for the film is available at different temperatures. These models are only partially implemented and should be taken as a starting point for future work rather than as a working product. In place of these, *calcEfePreisach* will be used to test the functionality of the rest of the modeling code.

The first function in *LandauFilm*, *cCalc*, is used to model the capacitive contribution to the hysteresis measurement. This is done via a linear fit to the mean of the absolute value of $\frac{dv}{dt}$ vs. the median absolute value of the ferroelectric current

for several different measurement frequencies. The slope of this line represents the capacitance of the sample. Since a hysteresis measurement consists of a sawtooth voltage waveform, the absolute value of the slope of this waveform is theoretically a constant value (minus the discontinuities at the corners of the waveform). Taking the mean of this absolute value minimizes noise present in the measurement system. Likewise, taking the absolute value of measured current allows the use of the entire hysteresis loop to calculate a capacitive current. Since ferroelectric switching represents a small portion of the time captured by a hysteresis measurement, the median value of measured current is very likely to fall in the non-switching region, giving a good estimation of capacitive current contribution. Note that user caution must be taken for very leaky samples, as the leakage current in these samples may mask the capacitive current. In this case, it may be desirable to subtract out the leakage current before performing capacitive current analysis.

The function takes a list containing *HysteresisData* measurements taken at different frequencies as its primary input and outputs a float representing the calculated capacitance value. The function also takes an optional boolean input, plot, which toggles plotting of the analyzed data as well as the calculated line fit. The default value for plot is false. This function was verified with a Materials Development Corporation reference wafer, seen in Fig. 3.2a. A value of 107.8 pF was extracted from hysteresis data (see Fig. 3.2b) for a capacitor with a stated value of 103.4 pF.

After calculating a capacitance value, the *cCompensation* function can be used to subtract the capacitive current contribution from a *HysteresisData* object. After compensation is performed, polarization is recalculated by integrating the new *HysteresisData* current. Inputs include the *HysteresisData* object which is to be compensated as well as an optional boolean to turn plotting on. If plot is set to true, the function will run *hystPlot* on the *HysteresisData* object before and after compensation. Outputs include a copy of the *HysteresisData* object with capacitive current



(a) (b)

Figure 3.2: Capacitance standard (left) with extracted 100 *pF* value (right).

removed as well as a remnant polarization value calculated from the gap between the maximum and minimum polarization values left after compensation. Note that this may differ slightly from a remnant polarization calculated from another method such as PUND measurements.

Outside of the handling of capacitance-related functions, *LandauFilm* also has functions dealing with the handling of ferroelectric domains, a third class that represents the individual domains found within a ferroelectric film[1]. The first of these, *domainGen*, takes the field, reverse field, and probability values output by *HysteresisData.forcCalc* and creates randomly sampled *LandauDomains* based on them. The number of domains generated can be user specified, with a default value of 100. The actual number of domains in a ferroelectric film can be quite a bit higher, but the resolution of multi-domain modeling is limited by that of the FORC measurement, leading to diminishing returns for greater numbers of domains. An optional plot input can be set true to show a plot of the sampled domains' parameters. Additionally, a *retParms* boolean can be set true to return a matrix containing the experimental

[1] *LandauDomain* itself has several functions for the fitting of Landau parameters to the given properties. As these are used exclusively by *LandauFull* and *LandauSimple*, they are not given further discussion in this work. Interested parties can contact me for further information.

field and reverse field values for the domains as well as coercive and bias field values calculated from the experimental data.

The list of domains generated by *domainGen* can next be passed to the *calcEfePreisach* function, which represents the domains as ideal hysterons and generates a hysteresis curve for the film based on an input electric field sweep. If no initial state is defined for the hysterons, they are assumed to all be negatively polarized. The *esweep* vector is next incremented through and each field value is compared with the coercive field plus the bias field of each domain. If the field value is greater than that required to switch the domain, the hysteron switches states. Otherwise the hysteron will stay in its current state. Once all domains have been checked for possible switching, the sum of the domain states is taken and stored as the polarization at that electric field value. The calculated polarization values are returned along with the final state of the hysterons after *esweep* is completed. If plot is set to true, a hysteresis curve is generated from the data. If the *cAdd* input is set to true, the output polarization values will also include the contribution of charge from capacitive behaviour.

The final three functions in *LandauFilm* are simple functions related to the viewing of film parameters. The first function, *getUfe*, takes an array of polarization charge values and a list of domains and returns the sum of the domain potential energy landscapes at those polarization values. This value can then be passed to *uPlot*, which takes an array of polarization values and associated potential energies as its input and generates a plot. This can be used to plot a sum of potential energies from *getUfe* or to plot the potential energy of individual ferroelectric domains. The final function, *ePlot*, handles the plotting of electric field vs. polarization charge curves given an array of polarization values and their associated electric fields. The user can also specify a coercive field and bias field when calling the function. If these are specified, lines will be plotted showing where the electric field local maxima/minima

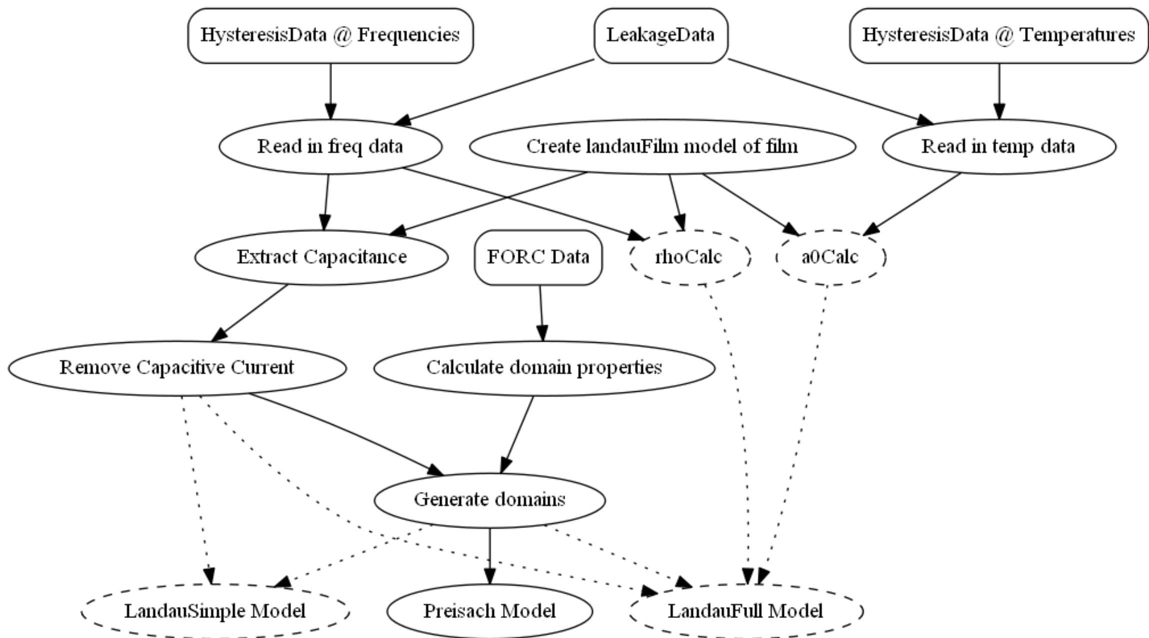


Figure 3.3: Typical data analysis workflow using ferro package. Experimental features indicated with dashed borders.

should be located. This is of use primarily when viewing single-domain behaviour and can be used as a visual method of checking the integrity of mathematical calculations of the landau parameters of the domain. If a coercive field is specified without a bias field, a default bias field of 0 will be used.

3.4 Summary

This chapter has focused on providing a detailed description of the various functions in the ferro package as well as their inputs and outputs. While there are many pieces of the package to be considered, a typical data analysis workflow can be summed up as seen in Fig. 3.3. This basic workflow is used to analyze the data presented in the following chapters and will display results all the way from immediately after read-in to the very end of the process.

Chapter 4

Analysis of PZT Ferroelectric Capacitors

In order to validate the ferro package during development, a ferroelectric capacitor with well-documented properties was tested and analyzed. The capacitor, commercially available from Radiant Technologies, consists of 255 nm of ferroelectric PZT deposited in seven layers between two platinum electrodes and packaged in a TO-18 package [34]. The results obtained from a 10,000 um^2 area sample are presented in the following sections.

4.1 Hysteresis Characterization

Before taking any measurements, the first action performed on the packaged device was to cycle the film with a 9 V 1 Hz square wave as recommended to recover it from imprint [34]. While the required 100 cycles did not quite eliminate the bias field for the device, it did increase and stabilize the remnant polarization. The resulting performance can be seen in Fig. 4.1, which shows the hysteresis behaviour of the device from 100 to 1000 Hz. Leakage current of the sample was measured to be less than one nanoamp, making its influence on the hysteresis curve negligible.

In examining the current as a function of frequency, it is tempting to think that the polarization loop should be getting larger due to the large increase in the size of the ferroelectric switching peak. This is deceptive, however, as polarization represents the integral of the current over time, not over voltage. There is in fact a great deal more

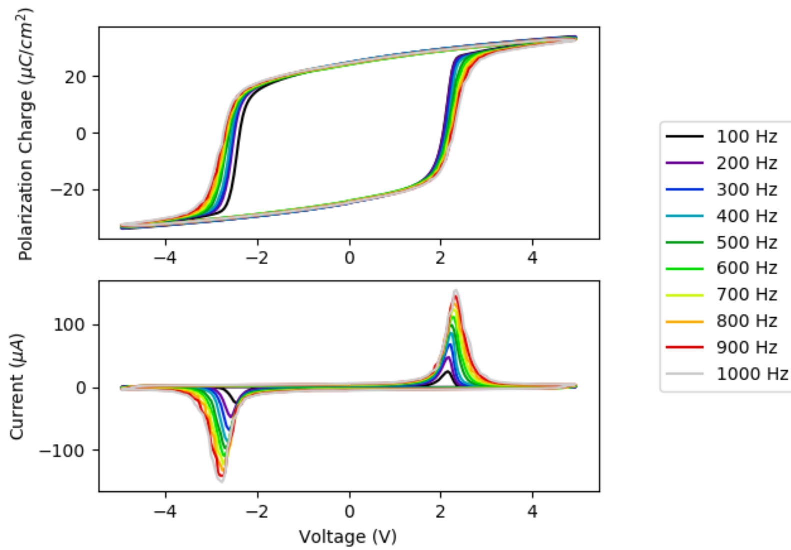


Figure 4.1: Comparison of PZT capacitor hysteresis curves at various frequencies.

switching current, but this current is happening over less and less time as frequency increases, giving an equivalent amount of total charge.

The relative lack of leakage current made the PZT capacitor the perfect sample for evaluating the effectiveness of *cCalc* with ferroelectric data. The extracted capacitance, seen in Fig. 4.2, is 2.36 $\frac{\mu\text{F}}{\text{cm}^2}$, which is similar to the value reported in [34]. The hysteresis data was then put through the *cComp* function, resulting in the hysteresis curve shown in Fig. 4.3. The remnant polarization value of 20 $\frac{\mu\text{C}}{\text{cm}^2}$ is used for modeling the film later on.

One thing to note when using *cCalc* is that the precision of the parameter extraction is dependent on the amount of noise present in the physical measurements. For instance, the test instrument used in this study had a maximum frequency of 1 kHz and noise in $\frac{dV}{dt}$ significantly increased as this limit was approached. This is illustrated in Fig. 4.4.

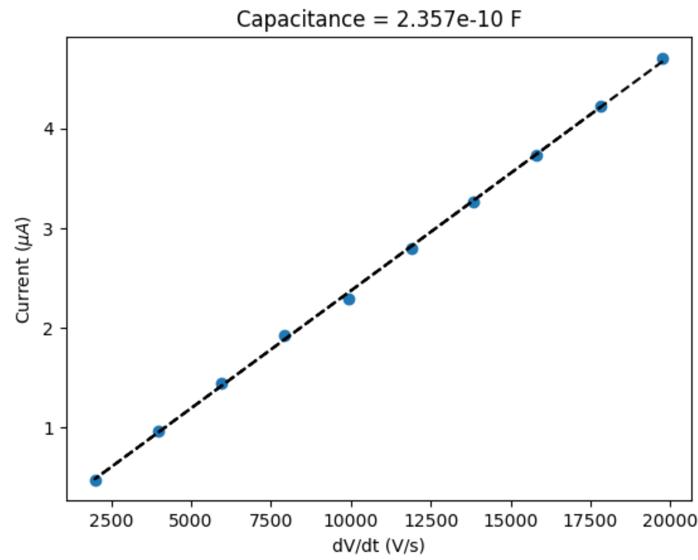


Figure 4.2: Capacitance extracted by *cCalc* from PZT capacitor hysteresis data.

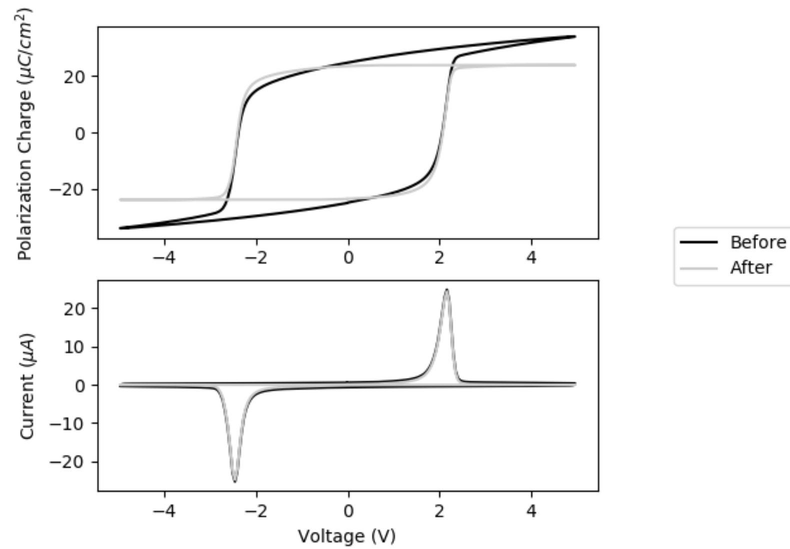
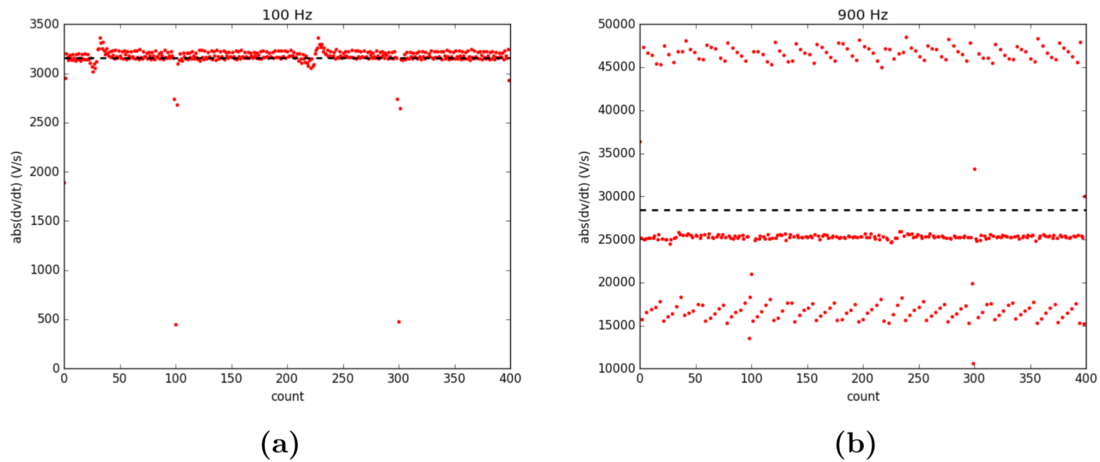


Figure 4.3: PZT capacitor hysteresis before and after compensation.



(a) (b)

Figure 4.4: Noise in $\frac{dv}{dt}$ increases with increasing measurement frequency (mean value shown as dashed line).

4.2 FORC Measurements

FORC measurements were carried out via a custom defined hysteresis waveform that was imported to the tester software. The waveform was created with a constant $\frac{dV}{dt}$ equivalent to that of a normal 100 Hz hysteresis measurement. The resulting domain probability distribution is shown in Fig. 4.5. A staircase-like effect can be seen at the values near $E = E_r$. This is caused by the numerical differentiation of the experimental data and the limited resolution in E_r. Since the tester used had a maximum of 10,000 data points per measurement, a trade off had to be made between E and E_r resolution. The results shown have twenty five E_r steps and an average of 400 E steps.

FORC measurements were also attempted with 100 E_r steps and an average of 100 E steps but significantly different device behaviour was seen, as shown in Fig. 4.6. This prevented any meaningful comparison of the resulting probability distribution functions. The significant difference in experimental results stems from an issue that can be seen most clearly by looking at the voltage and current signals versus time, as shown in Fig. 4.7. From this data, it is apparent that the measurement with 100 E_r

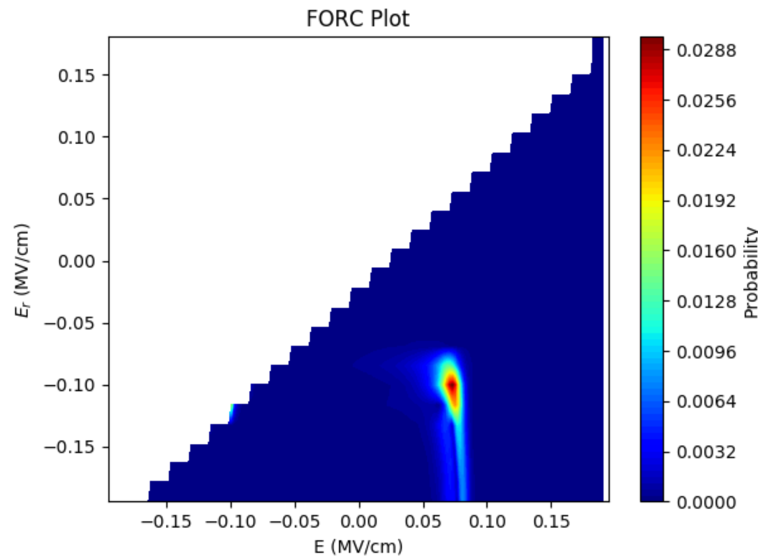


Figure 4.5: Probability distribution of domains in PZT capacitor calculated from FORC data.

steps mysteriously requires a significantly longer time for the ferroelectric switching current to decay. This is the result of a hardware filter in the test instrument which automatically activates for measurements longer than 2 s in an attempt to limit high frequency noise. As this filter cannot be disabled, all subsequent FORC measurements will be shown with only twenty five E_r steps.

Using the probability density function seen in Fig. 4.5, 100 domains were randomly generated and a triangular electric field sweep was used to simulate a hysteresis measurement using calcEfePreisach(). The resulting behaviour, compared with an actual hysteresis measurement, is shown in Fig. 4.8. In comparison to the measured behaviour, the simulated hysteresis has a much more pronounced tail on the negative slope. The highest probability in the FORC PDF is centered at the correct value of E and E_r, but there is also a tail in the probability function that exists across many E_r values at $E = 0.08$ MV/cm. This tail is caused by an anomaly in the measurement where, as the tester sweeps across E values for a particular E_r, there exists an E at which $\frac{\partial^2 \rho^-}{\partial E_r \partial E}$ reverses sign for a short region, followed by a region of the correct

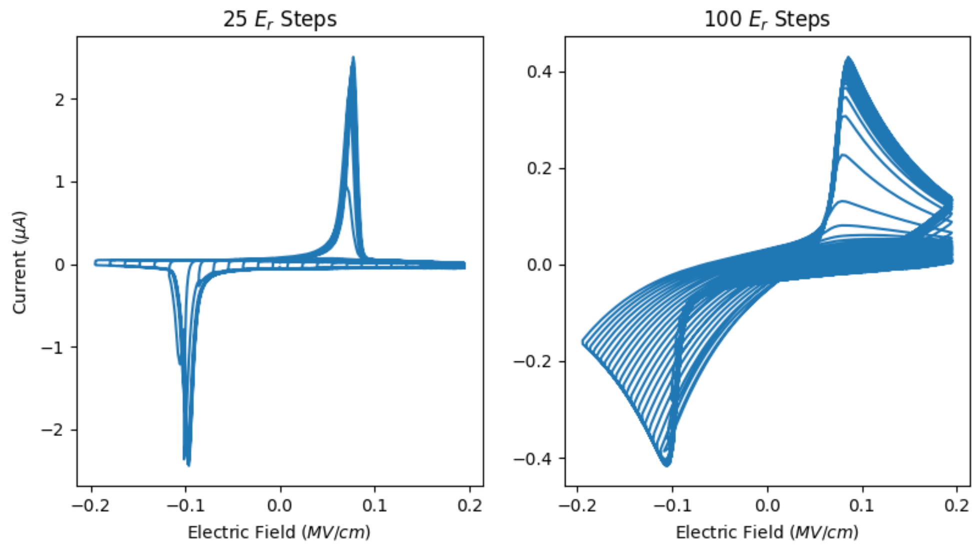


Figure 4.6: Comparison of the measured currents from FORC measurements on the same sample with varying numbers of E_r steps.

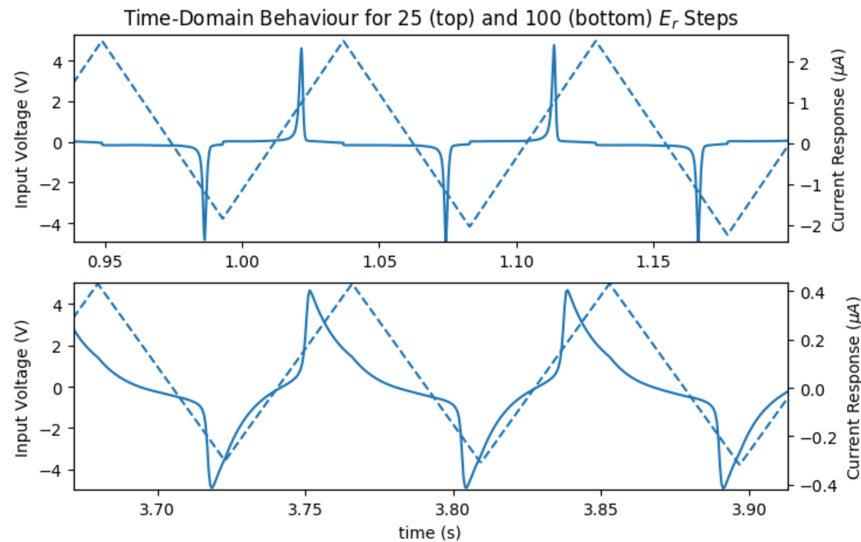


Figure 4.7: Comparison of current vs. time characteristics for the two FORC measurements with varying numbers of E_r steps shows significant inductive behaviour after ferroelectric switching. Input voltage for hysteresis measurement shown as dotted line.

sign and a larger than expected magnitude. What this leads to is a higher than normal probability for the region, causing the tail seen in the measurement. This phenomenon only occurs when the ferroelectric film is past the point of complete switching and correlates to the E values where the film is starting and finishing switching and ρ^{-} is abruptly changing slope (see Fig. 4.9). One way to mitigate the impact of this tail is to apply a smoothing filter to average out the values of opposing sign. The downside of this is that unless it is applied selectively, it will also spread out the "real" portion of the PDF, resulting in a less abrupt overall switching for the ferroelectric film when modeled later on. Another alternative could be to find the highest probability point of the data and then fit a probability distribution to that point, changing skew, kurtosis, and/or standard deviation until an optimum fit is found. This would have the added benefit of allowing for interpolation of domain probability between sampled points, creating a smoother final hysteresis curve. With such interpolation, one could run a multi-domain simulation with something closer to the actual number of domains in the film and weigh the benefits of increased accuracy against the additional computational time necessary.

4.3 Summary

While there are challenges inherent with the non-ideal nature of measurement data, the ferroelectric PZT capacitor has confirmed much of the overall functionality of the ferro package, allowing it to be used with confidence. The data from this device will also serve as a reference against which the experimentally derived properties of ferroelectric HfO_2 will be compared. The effectiveness of leakage compensation - something that was not necessary for the PZT samples analyzed - will be examined through the analysis of ferroelectric HfO_2 data in Chapter 5.

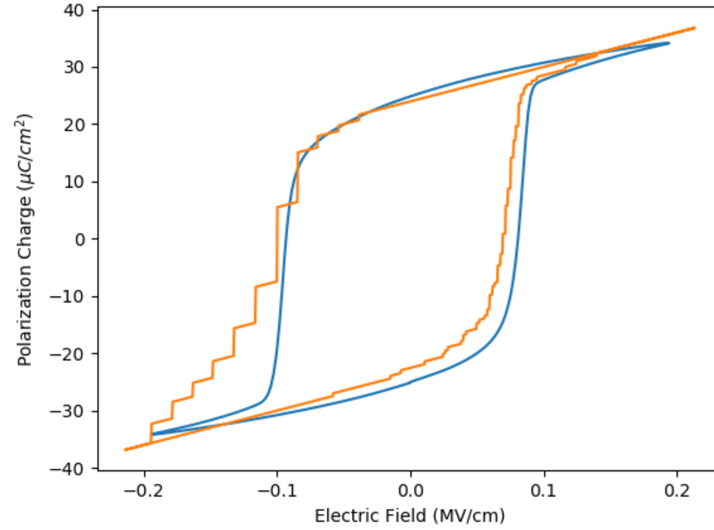


Figure 4.8: Comparison of measured hysteresis and hysteretic behaviour derived from FORC probability distribution using ideal hysterons.

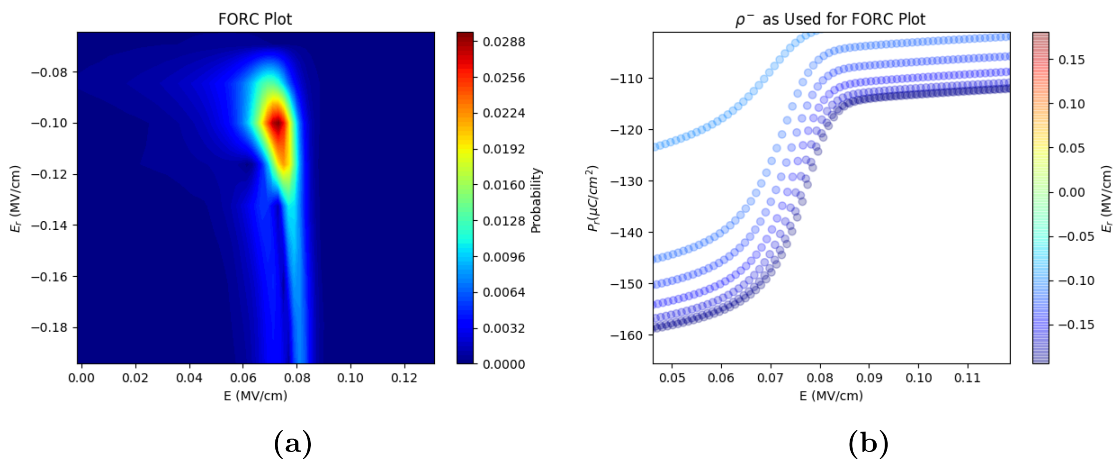


Figure 4.9: The area of the FORC PDF (left) and FORC polarization data (right) corresponding to the erroneous tail in the probability density function.

Chapter 5

Analysis of HfO_2 Ferroelectric Films and Devices

As was highlighted in Chapter 1, there are many applications where the properties of HfO_2 make it uniquely suited compared to traditional perovskite ferroelectrics. One of these applications, the FeFET, will be highlighted later on in this chapter. Before that, however, the ferroelectric properties of HfO_2 will first be investigated in an MFM and MFIS+ film stack. The fabrication of the various devices under discussion is as follows.

5.1 Fabrication Details

5.1.1 MFM Capacitors

The MFM capacitors used in this study are a subset of those studied previously in [35] and consist of 13.1 nm of 3.8 mol. % Si-doped HfO_2 sandwiched between two TiN electrodes. The bottom TiN electrode was deposited on a degenerately doped p-type wafer via reactive sputtering with a thickness of 13.1 nm. Si:HfO_2 was then deposited via ALD by NaMLab in Dresden, Germany. The 12 nm top TiN electrode was deposited via chemical vapor deposition and the samples were rapid thermal annealed in an N_2 ambient for 1 s at 1000 °C before metalization and patterning were carried out at RIT. The samples were patterned using a CV test mask, shown in Fig. 5.1. Testing was performed using the chuck contact as the bottom electrode.

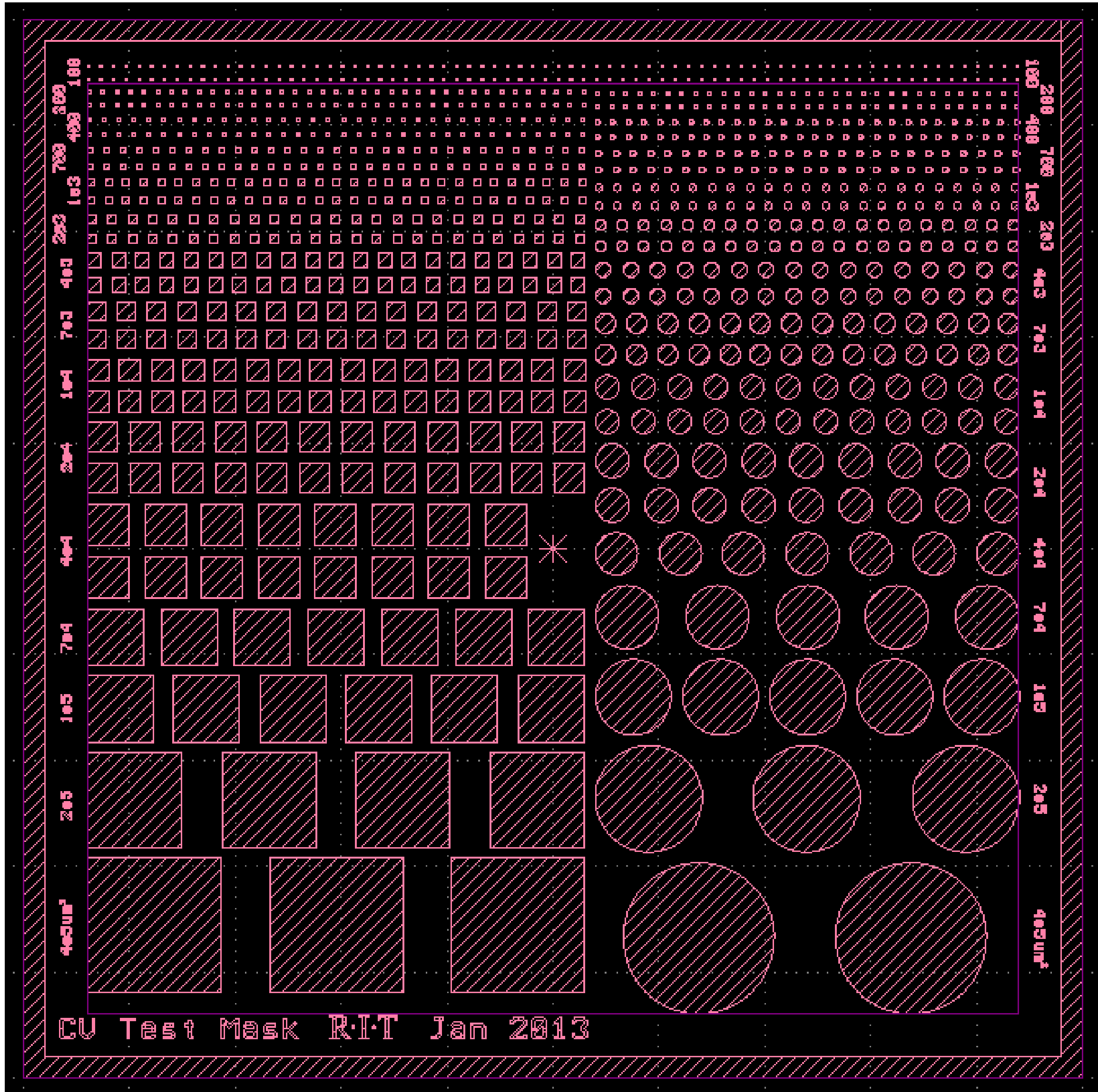


Figure 5.1: Layout of the mask used to pattern MFM capacitors.

5.1.2 FeFETs and MFIS+ Capacitors

In addition to the MFM structures discussed above, ferroelectric transistors were fabricated for analysis using a process flow developed in-house with the gate deposition performed at NaMLab as detailed in the previous section, but with HfO_2 deposited at both 3.8 and 5.6 mol. % Si. The higher silicon doping percentage is known to produce anti-ferroelectric behaviour in HfO_2, presenting another type of sample for analysis [22]. The HfO_2 thickness, measured via X-ray reflectivity, was reported as 13.5 nm for the 3.8 mol. % film and 10.5 nm for the other. The difference in sample thicknesses is due to the fact that a different number of total cycles is needed to get the doping percentages specified above. The complete process flow used is outlined in Appendix A.

Patterning of the devices was performed using the mask seen in Fig. 5.2. The top half of this mask includes several N-channel FeFETs ranging in size from $L = 40$ μm, $W = 20$ μm down to $L = 2$ μm, $W = 2$ μm. The bottom half of the mask consists of a variety of electrical test structures, resolution marks, and overlay analysis verniers. In the middle of the mask towards the right side are capacitors of various sizes. These capacitors consist of the gate stack deposited on top of a silicon substrate that has been degenerately doped via the source/drain implant masking layer. This allows for the study of any effects such as the formation of interfacial layers that may occur when ferroelectric HfO_2 is placed on silicon rather than between two conducting TiN layers.

Previous work estimated an etch rate of 5.5 nm/min or less for Si:HfO_2 in the chlorine-based plasma that was used [36]. A steady decrease in the etch rate over multiple minutes was noted. This etch rate was calculated based on ellipsometric data taken on a Film Sense FS-1 multi-wavelength ellipsometer; however, it seemed odd that the etch rate slowed significantly over time. In an attempt to better characterize the etch rate, the samples discussed in this study were etched with the same plasma

Figure 5.2: Layout for masks used in fabrication of FeFETs and MFIS+ Capacitors.

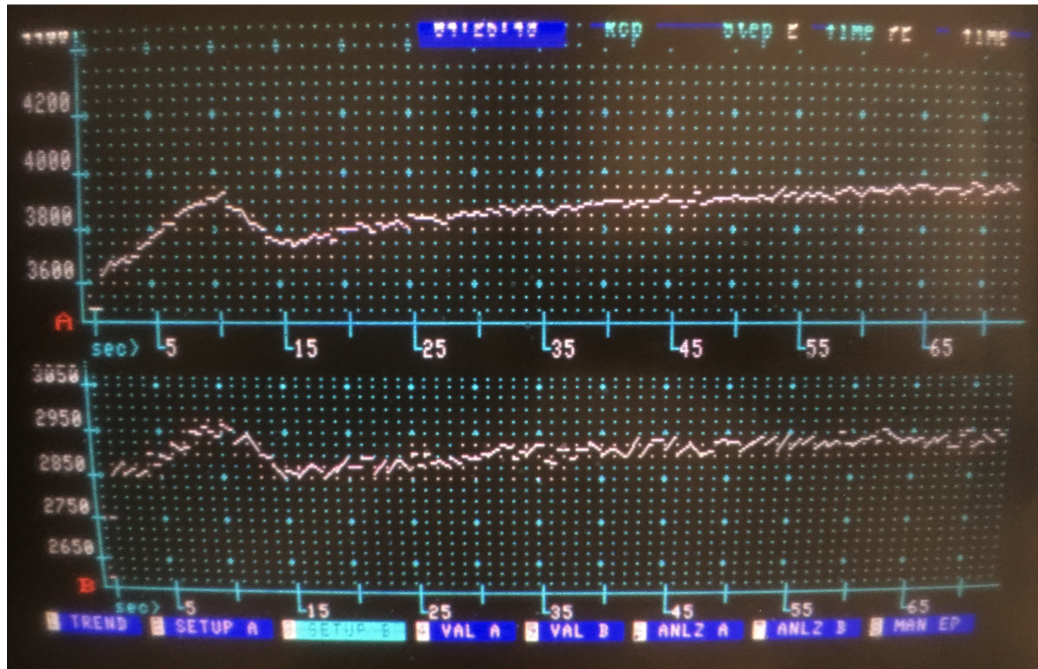


Figure 5.3: Channel A (520 *nm*) and channel B (703 *nm*) optical endpoint signals during the FeFET gate stack etch.

used previously but with altered timing and were monitored during the gate etch via optical endpoint detection. The antiferroelectric sample was first etched twice for 75 seconds, giving a total time 30 *sec* less than that done previously. The optical endpoint signal seen during the first half of the etch is shown in Fig. 5.3. The first peak is thought to be caused by the TiN etching away with the slow upward slope being caused by the HfO_2 etching. The second half of the etch gave a relatively constant signal. Based on this but still erring on the side of caution to ensure good electrical contact to the source and drain regions, the etch for the ferroelectric sample was done in one step for 90 seconds.

Among the test structures placed on the FeFET mask were resistors of fixed width and various length for transmission line measurements. After the completion of processing, these resistors were probed to determine the impact of the etch on contact resistance. The resulting calculated source/drain sheet and contact resistances are shown in Fig. 5.4. The fact that the ferroelectric sample with the shortened etch time

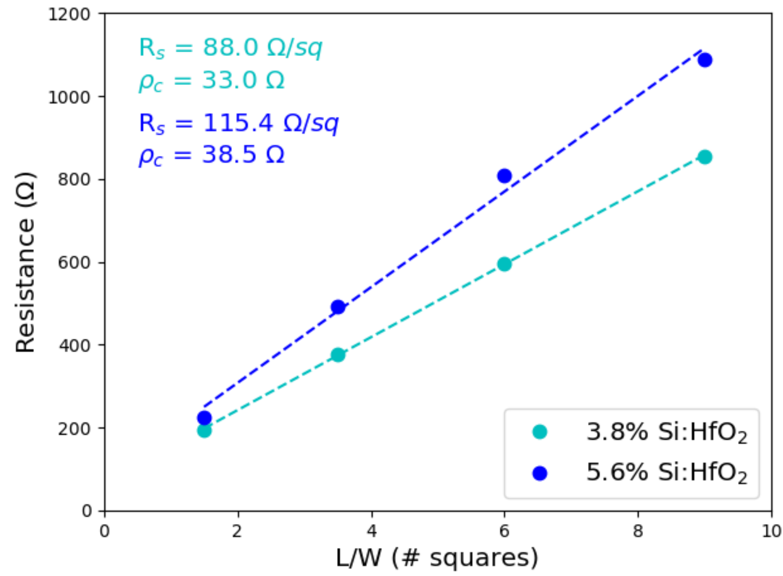


Figure 5.4: Sheet and contact resistances extracted from transmission line measurements of the two FeFET wafers.

had 5.5 Ω less contact resistance is promising, although additional experimentation should be done to see if this trend holds across a larger sample size. The fact that sheet resistances are so different between the two wafers, in particular, raises some suspicion, as both wafers received the same source/drain implant and diffusion. Even if the change is statistically insignificant, however, this still represents identical characteristics for a halving of the etch time - a good thing from a processing point of view.

5.2 Hysteresis Characterization

5.2.1 MFM Capacitors

The MFM capacitors that were fabricated show good ferroelectric behaviour across several frequencies, with distinct switching peaks and low leakage current (see Fig. 5.5). This quickly changes as sample temperature is increased and additional parasitic trapped carriers are excited. While the presence of leakage current is undesirable, it

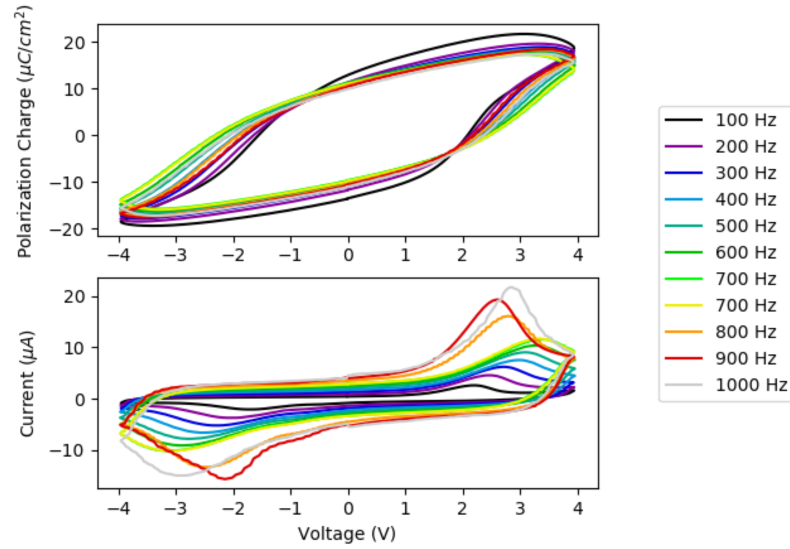


Figure 5.5: Comparison of hysteresis in HfO_2 MFM sample at various frequencies.

provides an excellent opportunity to test the capability of the ferro package to fit the current and subtract it out of measurement data. One such calculated fit is shown in Fig. 5.6 with the raw temperature-related hysteresis data and its compensated counterpart seen in Fig. 5.7. The compensation performs fairly well at lower temperatures but begins to fail as leakage current increases. This is not a mathematical error, but rather an impact of the leakage current measured via a leakage measurement differing from that present in the sample during a hysteresis measurement. This is likely due to the fact that the sample was beginning to break down since this was the last measurement made where the device was working.

Previous work reported ferroelectric behaviour in HfO_2 up to 200 °C (473 K), with the orthorhombic phase disappearing around 450 °C (723 K) [37, 38]. In the tested samples, leakage current grew to overpower ferroelectric switching current before 200 °C was reached. If the Curie temperature of HfO_2 is to be directly measured, further work will need to be done on reducing this parasitic current.

FORC measurements were next carried out on the sample at room temperature, resulting in the domain distribution shown in Fig. 5.8. This distribution shows a

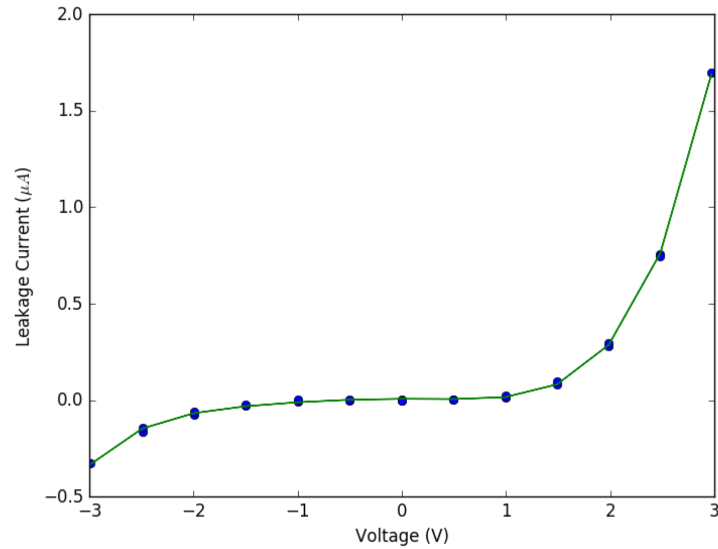


Figure 5.6: Measured leakage current at 352 K with *lcmFit* polynomial fit.

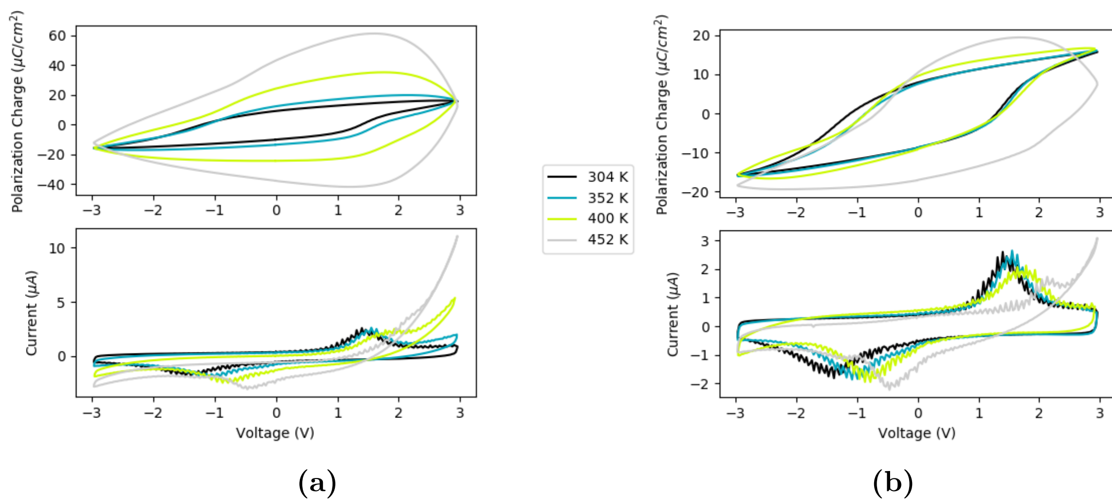


Figure 5.7: Comparison of hysteresis in HfO_2 MFM sample at various temperatures.

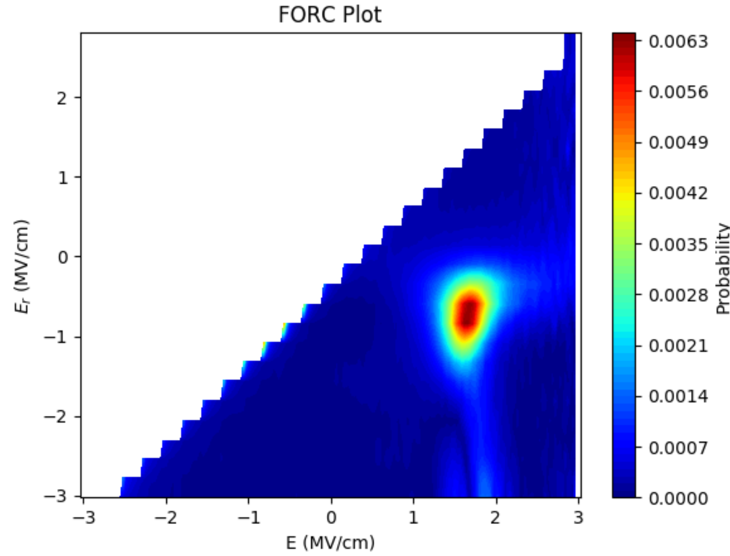
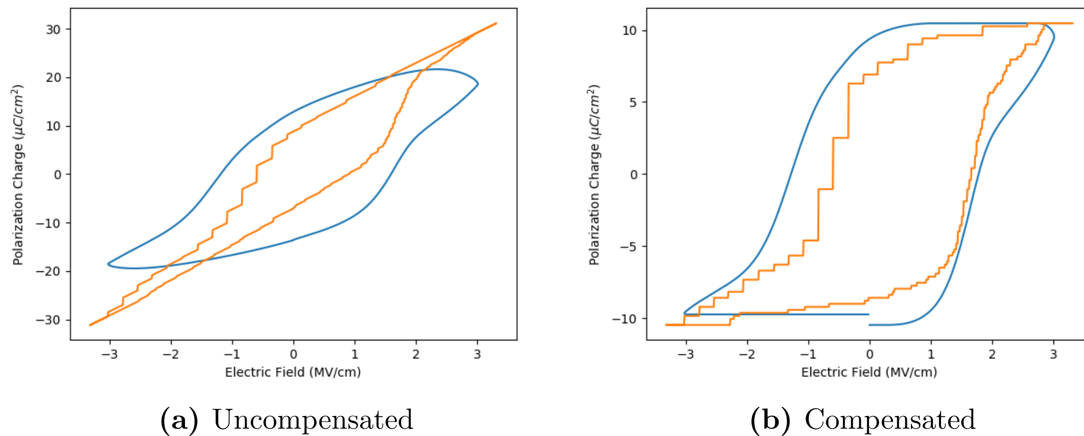


Figure 5.8: Ferroelectric domain distribution in MFM samples.

slight positive bias field, as well as the "tail" around $E = 2$ MV/cm at the more negative reverse field biases that was seen in the PZT data. This will lead to some mismatch between modeled and experimental data at negative electric fields. There also seems to be some noise present along the coercive field axis ($y = x$), which will cause early switching of the sample.

Due to the effects stated above, some degree of mismatch between model and data was predicted when results were plotted. What was not anticipated, however, was the vast difference that is present in Fig. 5.9a. The difference in slope indicates that it can largely be attributed to a mismatch in capacitive current contribution between the experimental and modeled data. The extracted relative permittivity from the frequency data was around 70, a value much larger than expected. This may be due to leakage current, which causes a larger current in the sample than would otherwise be present for a given $\frac{dv}{dt}$, leading to a higher extracted slope.

Capacitance being the source of the mismatch is confirmed by plotting the Preisach modeled domains without capacitive current against the experimental data with capacitive current removed, as shown in Fig. 5.9b. Without the difference in slope,



(a) Uncompensated **(b)** Compensated

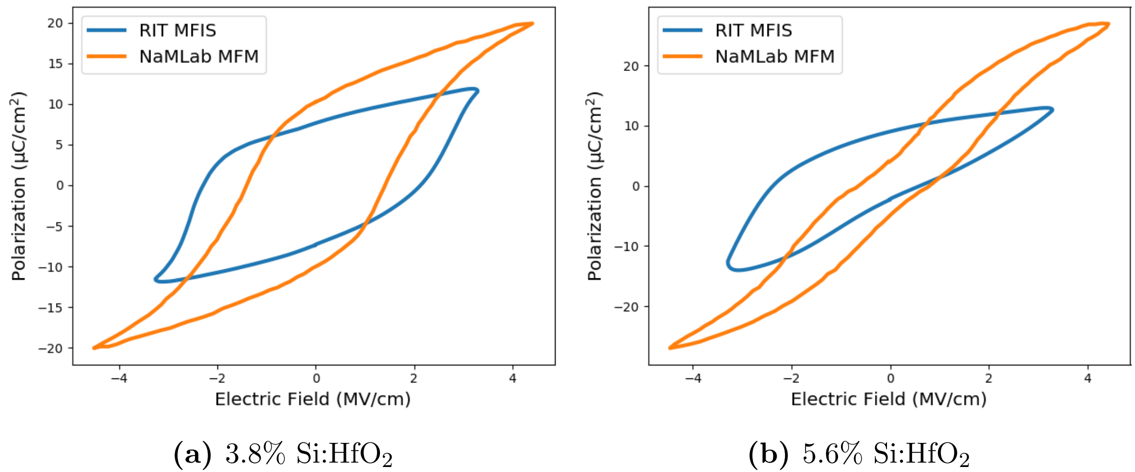
Figure 5.9: Preisach modeling of MFM capacitors using raw data (left) and capacitance compensated data (right).

the two hysteresis loops match up much better (minus the issues discussed above). This comparison is not without its own errors, however, as a small degree of offset is present in the capacitance-compensated experimental data. This problem occurs when capacitance is overestimated and the compensation algorithm prevents the gap between the forward and reverse currents from going below zero. Since this safeguard disrupts the symmetry of the current subtraction, the symmetry between the two halves of the polarization loop is broken and a gap appears.

5.2.2 MFIS+ Capacitors

In addition to the device wafers, monitor samples were also included during gate stack processing to obtain ferroelectric film characteristics in an MFM stack. This enabled a direct analysis of the impact of growing the HfO_2 on a silicon surface rather than on TiN. The results, seen in Fig. 5.10, show a markedly different device performance. In particular, the HfO_2 grown directly on silicon seems to have a larger coercive field, a smaller remnant polarization, and a smaller capacitance.

In order to accurately characterize the capacitance of the MFIS+ samples, a variety of the different sizes and shapes that were on the mask design were tested. Many

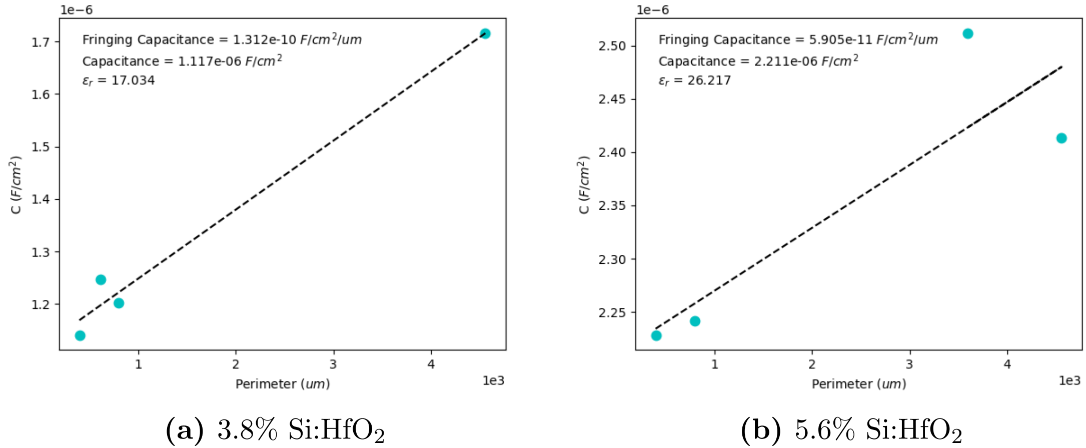


(a) 3.8% Si:HfO_2 **(b)** 5.6% Si:HfO_2

Figure 5.10: Comparison of measured MFIS+ hysteresis with hysteresis of MFM monitor sample.

of the results obtained were higher than expected, so the capacitances were normalized with respect to area and plotted versus perimeter as shown in Fig. 5.11. From this, a real capacitance was extracted from the y-intercept of a line fit to the data. The slope of this line represents an estimate of the parasitic capacitance contributed by fringing fields. From the y-intercept, relative permittivities were then calculated using the known thickness of the ferroelectric film. As these values were slightly lower than those reported from the MFM stack, the MFIS+ capacitors were next modeled as a series combination of an SiO_2 layer and a HfO_2 layer with a relative permittivity equal to that extracted from the MFM capacitors. This gave an interfacial oxide thickness of between two and three Angstroms for the two wafers. The fact that this thickness is quite small is due to an RCA clean that was performed before the HfO_2 ALD. An additional HF dip at the end of the RCA clean could further reduce this interfacial layer, although it is suggested that such a thin layer is beneficial for obtaining a good HfO_2-Si interface [39].

As the electric displacement field must be equal at the boundary between the two layers (assuming any interfacial charge is negligible), the field in the SiO_2 will be four to nine times greater than that in the HfO_2. This means that a measurable portion of



(a) 3.8% Si:HfO_2 **(b)** 5.6% Si:HfO_2

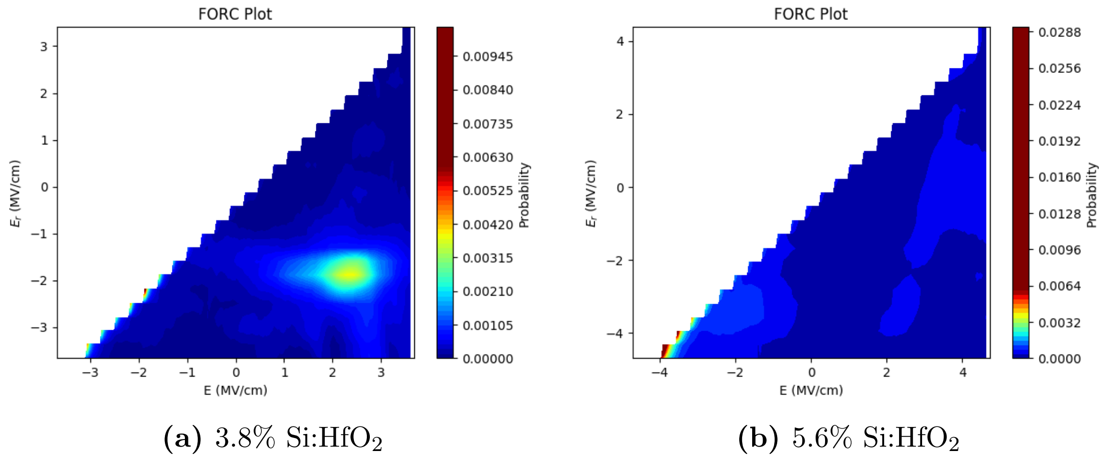
Figure 5.11: Separation of real and parasitic capacitance from measurement of various sized devices on the same die.

	MFM ϵ_r	MFIS+ ϵ_r	SiO_2 Thickness ($\AA$)	Voltage Across SiO_2
3.8% Si:HfO_2	18.5	17.0	2.5	8.1%
5.6% Si:HfO_2	30.0	26.2	2.0	12.8%

Table 5.1: Analysis of SiO_2 layer in MFIS+ stack.

the voltage applied will be dropped across this layer rather than the ferroelectric film, a result summarized in Table 5.1. Nevertheless, this voltage drop and the resulting change in capacitance alone cannot explain the difference in behaviour between the MFM and MFIS+ capacitors.

Given the relative lack of an interfacial oxide between the HfO_2 gate and the substrate, the remainder of the difference in ferroelectric behaviour must come from the HfO_2 film itself. This may come about as a result of having a different film stack during the annealing step, where the development of ferroelectric properties is known to be stress-dependent. The film stack could also lead to the presence of a non-ferroelectric HfO_2 layer at the silicon interface, further reducing the polarization charge present. The extent to which the coercive field of the stack has changes is highlighted in Fig. 5.12a, where the 3.8% Si:HfO_2 domain distribution has shifted by nearly $1MV/cm$ away from the coercive field axis. The distribution is also spread out more as a result of some of the applied voltage being dropped across a non-ferroelectric



(a) 3.8% Si:HfO_2 **(b)** 5.6% Si:HfO_2

Figure 5.12: Comparison of measured MFIS+ first order reversal curves.

layer. Fig. 5.12b shows the antiferroelectric sample not even fully switching within the applied field region, with the distribution running into the edge of the measured area. Both of these plots show significant noise along the coercive field axis, which could be caused by the presence of higher levels of leakage current in the sample. Note that the color scale of these two plots has been fixed to that of Fig. 5.8 to allow the ferroelectric switching to be seen despite the high values residing at the edge of the field.

5.3 Analysis of FeFET Performance

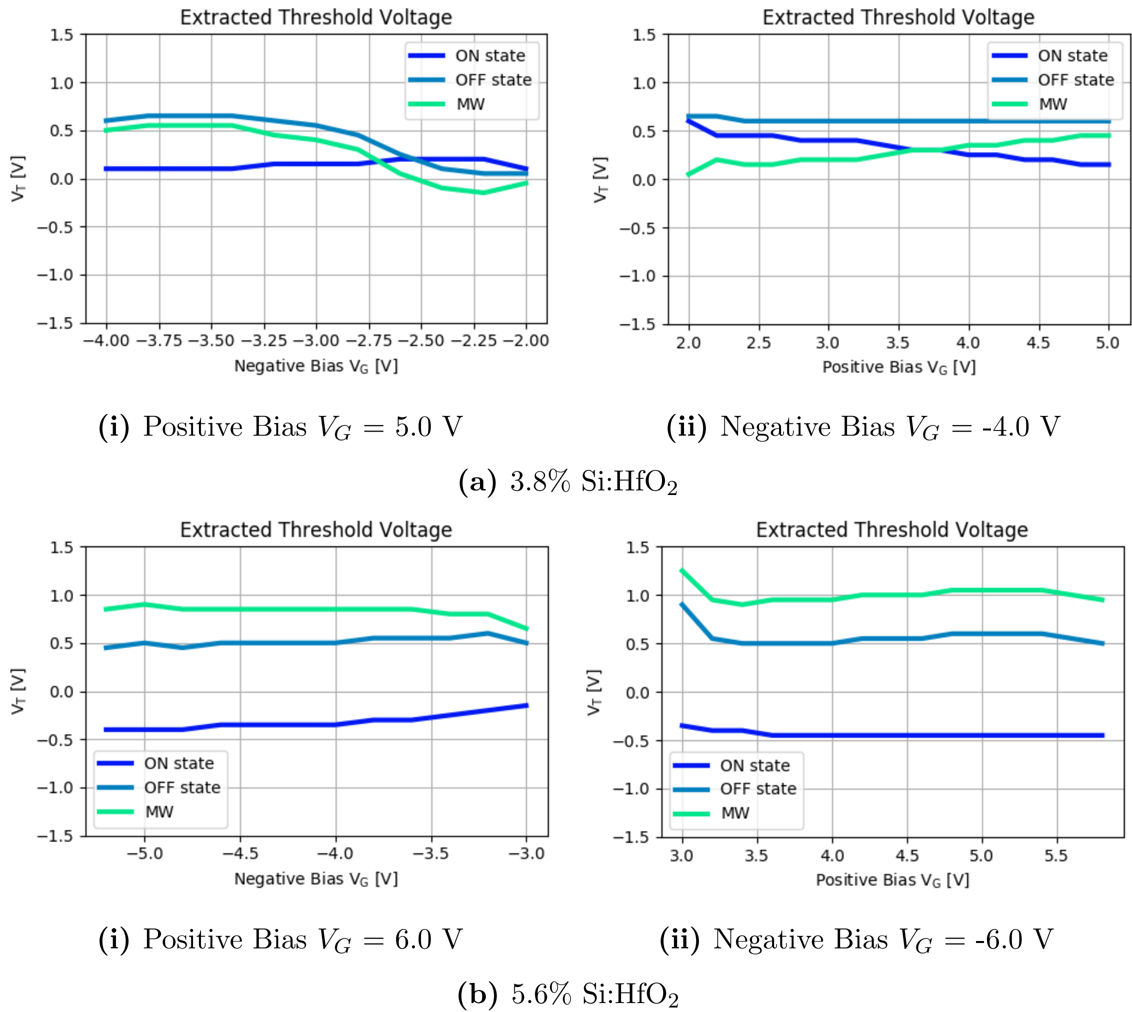
Despite the unwanted effects of leakage current, interfacial layers, increased coercive fields, and decreased remnant polarization, there is no doubt that some ferroelectric behaviour still remains in the Si:HfO_2 films. In analyzing the FeFET, there is yet another confounding factor: the variable capacitance of a lightly doped semiconductor. Beyond the change in capacitance that occurs during depletion, the semiconductor layer also drops 0.95 V when in inversion and -0.4 V when in accumulation (see Appendix B). This means that even less of the total voltage drops across the ferroelectric layer, stretching out the hysteresis curve when viewed as a function of applied

voltage.

Given this fact, it may be seen as desirable to apply a greater voltage to the gate of the FeFET than was applied to the ferroelectric capacitors. One must be careful when doing so, however, as to not break down the gate dielectric. The FeFETs were measured at a drain voltage of 0.1 V and a gate bias sweeping from -1 to 2 V to capture the transfer characteristics of the device. Between sweeps, the gate was held at a bias voltage for 10 ms to switch the state of the ferroelectric film. In order to select appropriate bias voltages, the bias voltage of one state was fixed at a high value while the bias voltage of the other state was swept from low to high magnitude. The minimum bias voltage that could be evaluated was limited by the voltage range required for the $I_D - V_G$ sweep while the upper limit was dictated by the breakdown voltages of the gate stacks, which were measured to vary between 6.25 and 7.5 V across the two wafers. The results of this process, which was carried out for both states with both films, are shown in Fig. 5.13. Interestingly, only small changes were seen in the memory window of the antiferroelectric sample across the measured voltages. This indicates that the film is primarily switching at lower voltages, perhaps even during the $I_D - V_G$ sweep.

As a result of this analysis, bias values of -3.5 and 4.5 V were chosen for the ferroelectric sample. Values of -5.5 and 5.0 V were chosen for the antiferroelectric sample to see if any additional shift would be seen as a result of cycling the film. The resulting $I_D - V_G$ characteristics of both devices over fifty cycles are seen in Figs. 5.14 and 5.15.

After a negative gate bias, the ferroelectric sample domains are aligned with the positive pole pointing towards the top of the gate (polarization vector pointing towards the substrate). This means that there is a voltage drop across the gate, lowering the voltage seen by the channel and apparently increasing the threshold voltage. After a positive bias, the negative pole of the gate is oriented at the top of the stack,



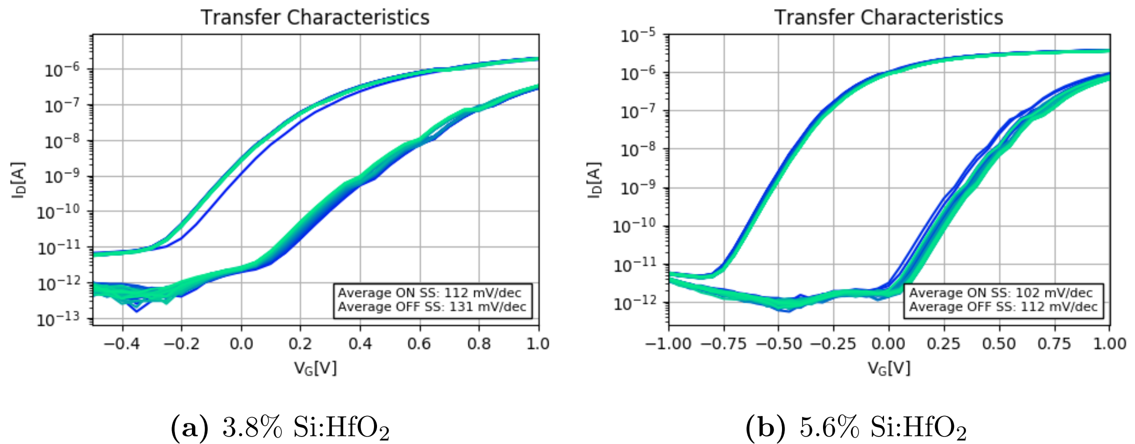
(i) Positive Bias V_G = 5.0 V **(ii)** Negative Bias V_G = -4.0 V

(a) 3.8% Si:HfO_2

(i) Positive Bias V_G = 6.0 V **(ii)** Negative Bias V_G = -6.0 V

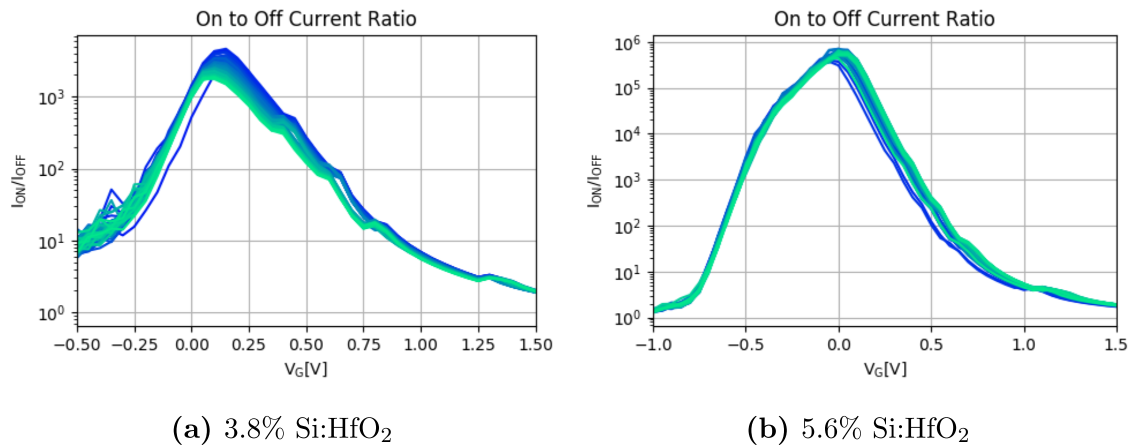
(b) 5.6% Si:HfO_2

Figure 5.13: Threshold voltages as a function of applied voltage for L=40 um, W=20 um FeFETs.



(a) 3.8% Si:HfO_2 **(b)** 5.6% Si:HfO_2

Figure 5.14: $I_D - V_G$ characteristics over 50 cycles of devices seen in Fig. 5.13.



(a) 3.8% Si:HfO_2 **(b)** 5.6% Si:HfO_2

Figure 5.15: Current ratio between the two states as a function of gate voltage for the data seen in Fig. 5.14.

providing voltage gain across the gate and lowering the apparent threshold voltage of the device.

Interestingly, the antiferroelectric device shows state behaviour that is opposite that of the ferroelectric sample, with a positive bias moving the sample into the ”off” state and a negative bias moving it into the ”on” state. This is believed to be due to the stretching of the hysteresis curve via voltage division, a phenomenon mentioned previously and discussed in depth by Miller and McWhorter [40]. Upon examination of the switching currents of the two ferroelectric films from the MFM samples, shown in Fig. 5.16, it can be seen that the antiferroelectric sample exhibits two ferroelectric switching peaks in each direction. Now consider the case where the hysteresis curve is stretched far enough such that only the two peaks closest to 0 V fell within voltage range that can safely be applied to the gate while avoiding breakdown. In this case, the resulting antiferroelectric film would appear to act like a ferroelectric film but with a positive switching peak at a negative voltage and a negative switching peak at a positive voltage - the opposite of typical behaviour. That being said, this direction of threshold voltage shifting is also consistent with the presence of mobile positive charges in the gate oxide, so further work should be done to validate or disprove this theory.

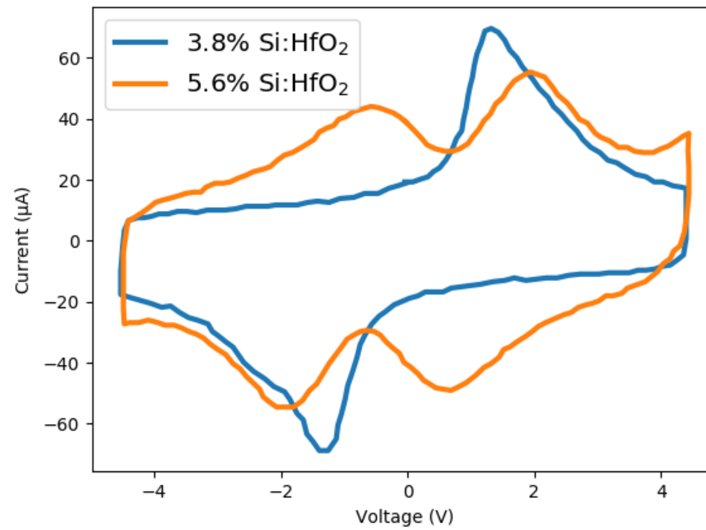


Figure 5.16: Current vs. voltage characteristics of the ferroelectric and antiferroelectric films present in the FeFETs, measured in an MFM stack.

5.4 Conclusion

While the reported ferroelectric behaviour of HfO_2 may not be as noise-free as that observed in PZT films, the hysteretic nature of the film is undeniable with 0.6 V and 1.0 V threshold voltage shifts demonstrated in the 3.8% Si:HfO_2 and 5.6% Si:HfO_2 FeFETs respectively. Whether mobile charges play a significant role in this hysteresis is yet to be determined. The voltage required to switch the ferroelectric film, which was around 1.9 V (E_c=1.4 MV/cm) in the MFM stack, was shown to increase to 3-5 V in a FeFET gate stack. It is suspected that only half of the domains in the 5.6% Si:HfO_2 switched in the FeFET gate stack, resulting in behaviour opposite what was shown in the 3.8% Si:HfO_2 sample. While the larger threshold voltage shift of the 5.6% Si:HfO_2 sample resulted in an on-to-off current ratio almost three orders of magnitude larger than the other sample, additional testing will need to be done to ensure that reading the state of the device does not impact the stored ferroelectric state. This is extremely important if one wants to reduce power consumption by

eliminating a refresh of the memory cell after every read operation.

Chapter 6

Concluding Remarks

Ferroelectric devices are one of a host of technologies competing for a role in next-generation memory and logic devices. The future for ferroelectric devices looks promising with the demonstration of HfO_2 devices at the 28 nm node [26]. Whether or not ferroelectric films find a place in nm-scale devices, however, they will continue to occupy a small but important niche at older nodes [8, 27]. This work has presented a modeling framework to ease analysis of ferroelectric test data, accelerating researcher learning. The implemented multi-domain Preisach model serves as a guide for interested parties to implement their own models going forward and also highlights some of the challenges present in working with real experimental data.

Beyond simply developing and validating the Ferro modeling package, this work has also analyzed the behaviour of ferroelectric HfO_2 thin films on several different bottom electrodes. Ferroelectric properties are clearest on a TiN bottom electrode, which demonstrates a coercive voltage of 1.9 V for a 13.5 nm film. Both capacitors tested with a silicon bottom electrode showed significantly increased coercive voltage beyond what would be expected from either silicon depletion or an interfacial oxide. This highlights the important role that the physical capacitor structure plays in formation of the ferroelectric phase in HfO_2. What is yet to be explored is whether this difference is primarily due to the physical stresses exerted on the HfO_2 film during annealing or whether the material composition also plays a role. Also useful would

be a cross-sectional analysis of the physical structures of the devices, which would allow for more accurate modeling of the interfacial layer in the MFIS device stacks.

Transistors fabricated with the micron-scale RIT NMOS FeFET process flow demonstrated memory windows between 0.6 and 1.0 V, with especially interesting behaviour seen from the 5.8 % Si:HfO_2 sample. This behaviour may stem from incomplete polarization of the ferroelectric domains in the anti-ferroelectric film. Mobile charges in the HfO_2 may also play some role, as the direction of threshold voltage shifting in the 5.8 % sample is the same as would be exhibited by positive ions moving in the gate. There certainly exists some amount of fixed charge, as the threshold voltage was measurably shifted from the calculated flat-band voltage of -0.24 V. In this light, further studies quantifying the impact of charges on device performance would be prudent and would allow a more accurate depiction of the extent of ferroelectric behaviour in the devices.

Once the impact of charges on device characteristics is better understood, efforts can be made to improve device processing to mitigate their presence. There is certainly room for process improvements in the gate stack etch and anneal, but the devices fabricated with the current process have proven quite valuable in allowing for the analysis of ferroelectric behaviour. With these devices characterized and a framework for data analysis established, the door is now open for future device modeling and process optimization informed by the results that have been presented. These will allow continued study of a class of devices that may yet have an important role to play in mainstream consumer electronics.

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Appendix A: NMOS FeFET Process Flow

Process Step	Tool - Description
0	Substrates - p-type, 20 $\Omega * cm$
1	Zero Level Litho
2	10:1 BOE - Etch native oxide
3	Drytek Level Zero Etch
4	Gasonics Asher - Resist Strip
5	RCA Clean
6	FURNACE04 - Pad oxide growth (tgt 50 nm)
7	Back Side Implant (B^{11} $2 * 10^{15}/cm^2$ @ 50 keV)
8	ASM LPCVD - (Si_3N_4) Nitride (tgt 150 nm)
9	SSI/ASML - Process Lvl 1 Mask - Active Region
10	LAM 490 - Etch Nitride for exposing field regions
11	Channel Stop Implant (B^{11} $8 * 10^{13}/cm^2$ @ 100 keV)
12	Gasonics Asher - Resist Strip
13	RCA Clean
14	FURNACE01 - Field Oxide Growth (tgt 650 nm)
15	Hot Phos - Etch Nitride
16	10:1 BOE - Etch Pad Oxide
17	FURNACE01 - Kooi Oxide Growth (tgt 100 nm)
18	V_T Adjust Implant (skipped for these devices)
19	SSI/ASML - Process Lvl 2 AND Lvl 3 Mask - S/D and N+ Region
20	S/D Implant (P^{31} $2 * 10^{15}/cm^2$ @ 75 keV)
21	Gasonics Asher - Resist Strip
22	RCA Clean
23	S/D and Backside Anneal (1000°C in N_2, 75 min soak)
24	10:1 BOE - Etch Kooi Oxide
25	NaMLab - ALD Fe-HfO_2 and TiN (annealed)
26	SSI/ASML - Process Lvl 5 Mask - Gate Definition
27	LAM 4600 - TiN & HfO_2 Etch to form Gate
28	Resist Strip
29	10:1 BOE Dip
30	Al Deposition - CVC 601 Sputter or PE 4400 (tgt 750 nm)
31	SSI/ASML - Process Lvl 6 Mask - M1
32	LAM 4600 - Al Etch
33	Resist Strip
34	Backside Al Deposition - CHA Flash
35	FURNACE01 - Al Sinter (400°C in N_2/H_2)

Appendix B: Calculation of Semiconductor Surface Potential

From Kirchoff's voltage law and charge balance, it can be shown that the total voltage drop across the gate stack of the transistor is given by

$$V_{GB} - V_{FB} - \Psi_s + Q'_c/C'_{ox} = 0. \tag{B.1}$$

The flat band voltage, neglecting parasitic charges, can be calculated based on the materials used in the gate stack of the transistor:

$$V_{FB} = \phi_m - \chi_s - \frac{E_g}{2} - \phi_f \tag{B.2}$$

where

$$\phi_f = \phi_t ln\left(\frac{N_A}{n_i}\right) \tag{B.3}$$

The semiconductor charge is given by

$$Q'_c = -sgn(\Psi_s)\sqrt{2q\epsilon_s Na}$$
$$\sqrt{\phi_t\left[exp\left(\frac{-\Psi_s}{\phi_t}\right) - 1\right] + \Psi_s + \phi_t exp\left(\frac{-2\phi_f}{\phi_t}\right)\left[exp\left(\frac{\Psi_s}{\phi_t}\right) - \frac{\Psi_s}{\phi_t} - 1\right]}. \tag{B.4}$$

For the derivation of these relationships, the reader is directed to [41]. Using these equations and the values for the fabricated devices shown in Table B.1, ϕ_f and V_{FB} were calculated as 0.18 and -0.24 V respectively[1]. A range of Ψ_s were defined and passed into Eq. (B.4) to solve for Q'_c, which was then used to solve for V_{GB}. From this point, the voltage drop across the gate oxide was calculated as

$$\Psi_{ox} = V_{GB} - V_{FB} - \Psi_s \tag{B.5}$$

[1] These values were taken from the process given in Appendix A, from measured capacitances, and from Silvaco Athena simulations of channel dopant depletion during processing. Athena simulations were done with an SiO_2 gate, so actual doping may differ slightly in these devices.

N_A	$1.36 * 10^{13}$ cm^{-3}
ϕ_m	4.55 eV
χ_s	4.05 eV
E_g	1.12 eV
ϵ_{fe}	18.5
ϵ_{de}	3.9
C'_{ox}	$1.117 * 10^{-6}$ F/cm^2
t_{fe}	13.5 nm
t_{de}	0.2 nm

Table B.1: Values used in MFIS capacitor voltage analysis.

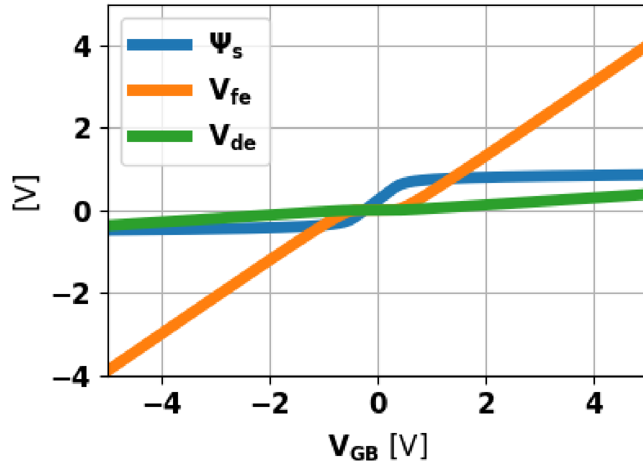

Figure B.1: Voltage analysis of 3.8 % Si:HfO_2 FeFET gate stack.

which represents the drop across both the ferroelectric and interfacial layers. The actual voltage drop across the two layers can be solved for by solving Eqs. (B.6) and (B.7), which are derived from electrostatic boundary conditions and Kirchoff's voltage law. The calculated results for the 3.8 % Si:HfO_2 FeFET stack (neglecting polarization charge) are shown in Fig. B.1.

$$\epsilon_{fe} E_{fe} = \epsilon_{de} E_{de} \tag{B.6}$$

$$\Psi_{ox} = E_{fe} t_{fe} + E_{de} t_{de} \tag{B.7}$$