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Ultra-Shallow Phosphorous Diffusion in Silicon using Molecular Monolayer Doping

Astha Tapriya
axt2750@rit.edu

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Astha Tapriya

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Approved by:

Dr. Santosh K. Kurinec (Thesis Advisor)

Dr. Scott Williams (Thesis Committee)

Dr. Ivan Puchades (Thesis Committee)

Dr. Robert Pearson (Director, Microelectronic Engineering Program)

Dr. Sohail Dianat (Head, Electrical and Microelectronic Engineering)

DEPARTMENT OF MICROELECTRONIC ENGINEERING

KATE GLEASON COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

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To my family, friends and colleagues…

Abstract

Controlled doping of semiconductor material with high atomic accuracy and minimum defects in silicon is needed for next generation nanoscale and solar devices. The molecular monolayer doping (MLD) strategy is a novel technique based on the formation of self-assembled monolayer of dopant –containing molecule on surface of crystalline silicon, followed by rapid thermal annealing. MLD helps to form damage free junctions which are conformal. It is capable of nanometer scale control of dopant introduction and formation of ultra-shallow diffused profile. MLD can be used for conventional planar devices, FinFETs and nanowires, since both bottom-up and top-down approaches are feasible making it highly versatile. It also finds applications in solar cell industry, to fabricate selective emitters and increases the efficiency of the crystalline silicon solar cell along with reduced contact resistance.

Phosphorus MLD on p-type silicon is formed using diethyl 1-propylphosphonate (DPP) as dopant source in this work. It involved demonstrating the formation of monolayer on silicon piece and 6-inch wafer. The setup is designed, assembled and implemented successfully to achieve monolayer formation on full wafer. The presence of phosphorous on the surface is detected by Auger electron spectroscopy and confirmed by X-ray photoelectron spectroscopy on the same silicon sample. The phosphorous monolayer on the surface is diffused in the silicon surface using rapid thermal anneal at 1000^{o}C for 180 seconds. The diffusion profile is characterized by Secondary ion mass spectrometry (SIMS), spreading resistance profile and sheet resistance measurements. The result show successful creation of diffusion profile with high surface concentration, junction depth of 20 nm extracted at 1 x 10^{18} cm^{-3} base doping and sheet resistance is 920 Ω/sq. The total dose of phosphorous in the silicon is dependent on the number of bonds

formed using DPP and dose is increased by multiple rounds of MLD and annealing, sheet resistance for double MLD is reduced to 670 Ω/sq. N+P junctions are fabricated using MLD and current-voltage characteristics are measured and analyzed using unified model. It is found that the specific contact resistivity of MLD doped wafer is lower than the implanted wafer. It is also reported that MLD doping can be masked by a thin oxide layer giving a possibility of patterned doping.

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Term	Description	Units
q	Charge	C
k	Boltzmann's constant	eV/K
T	Temperature	K
Q	Dose	atoms/cm^2
n_i	Intrinsic concentration	cm^{-3}
D	Diffusion constant	cm^2/sec
D_o	Pre exponential factor	cm^2/sec
E_a	Activation energy	eV
R	Resistance	Ω
ρ	Resistivity	Ω-cm
a	Area	cm^2
R_s	Sheet resistance	Ω/sq
t_o	Thickness of layer	cm
V	Voltage	V
I	Current	A
ϕ	Potential	V
ϵ	Electric field	V/cm
ε	Permittivity	F/cm^2
N_A	Acceptor density	cm^{-3}
N_D	Donor density	cm^{-3}
p	Electron density	cm^{-3}
n	Hole density	cm^{-3}
V_{bi}	Built in potential	V
J	Current density	A/cm^2
τ	Minority carrier lifetime	s
L	Diffusion length	cm

n	Ideality factor	
Ec	Conduction band energy	eV
Ev	Valence band energy	eV
χ	Electron affinity	eV
ρ_c	Specific contact resistivity	Ω-cm^2
R_c	Contact resistance	Ω
L_T	Transfer length	µm
d	Spacing	µm

Chapter 1

Introduction and Motivation

In 1965, Gordon Moore predicted that the number of transistors on a chip would double every two years. This technology advancement in the semiconductor industry has only been possible due to the continuous efforts to scale metal-oxide-semiconductor field effect transistor (MOSFET) to smaller physical dimensions [3]. In order to increase the device packing density, improve the speed of transistor and ultimately increase the performance of the device, channel length, gate oxide thickness and junction depth are scaled.

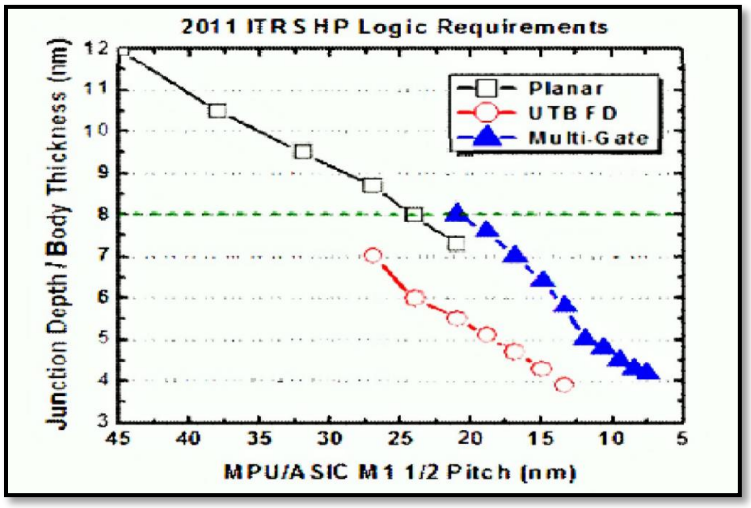


Figure 1.1: Junction depth versus the pitch for planar, fully depleted and multi-gate devices. [6]

Ultra-shallow junctions (USJ) are difficult to achieve in 2D structure due to severe short channel effects, excessive threshold voltage variations, and high off-state leakage. The introduction of 3D structures helps to achieve better device performance at 22nm and beyond nodes, the junction depth and source/drain sheet resistance are of critical importance. In Figure

1.1, the International Technology Roadmap for Semiconductors (ITRS) calls for the adoption of the ultra-shallow junction to maintain the short channel integrity [4].

Doping plays a crucial role in the fabrication of CMOS/finFETS and Silicon solar cell for junction formation. The performance of the device is directly dependent on the quality of junction formed. Therefore there is a tremendous need of well-defined, uniform nanoscale doping of Si structures. The current doping techniques like ion implantation result in damage during processing all of which cannot be corrected by annealing. The uniformity and control over the dose of the dopants is compromised when using solid source diffusion.

There have been tremendous efforts in recent years to develop new technology for introducing dopants in the semiconductor with minimum damage and shallow junctions. Molecular Monolayer Doping is one such technique which involves the formation of a self-assembled monolayer on the surface of hydrogen-terminated silicon by forming covalent bonds between dopant containing chemistry and Silicon. The dopants are diffused into the semiconductor by thermal treatment. The covalent bonds formed at the surface helps to control the dopant dose. The technique results in high atomic accuracy, minimum defects, and no crystalline damage.

1.1 Reported Work on MLD for Silicon Substrate

Molecular monolayer doping on Silicon was first reported in 2008 by Ho et al, group based out of University of Berkley, California. Allylboronic acid pinacol acid ester was used in 1: 25 v/v with mesitylene to form boron dopant containing monolayer on the surface of silicon, followed by rapid thermal anneal at high temperature for few seconds to form the ultra-shallow junction [1]. The same group applied MLD process to fabricate bottom up grown intrinsic nanowires and applied to silicon on insulator substrate in order to fabricate field effect transistor [2].Ho and co-

workers tried to investigate the effect rapid thermal anneal parameters on MLD diffused silicon, Temperature and time for spike anneal were varied to fabricate ultra-shallow junctions, which were later characterized and analyzed using non-contact sheet resistance measurement [4].

In 2011, CNSE Albany and Sematech first used phosphorous MLD, and fabricated FinFETS with 20 nm fin width on 300 mm silicon wafer, uniform silicide contacts were formed on MLD doped junction as compared to poor quality silicide formed due to damage caused by ion implantation [26]. .MLD technique was combined with lithography by Voorthuijzen and coworkers to achieve patterned monolayer and control the positioning of the monolayer on the surface. Bottom up and top down nano-imprint lithography approach was combined with existing MLD technique on the hydrogen terminated silicon substrate [22].

The control of dopant concentration in MLD has been limited by thermal conditions for very long, but it can also be tuned downwards by mixing dopant containing molecule along with an alkene that lacks dopant, thus diluting the chemistry. Ye and co-workers reported a linear relationship existed between the dopant molecule in the initial chemistry and dopant molecule on the surface [11]. The dose can be increased by using dopant rich chemistry. Javey et al, in their research found that the packing density of diethyl 1- propyl phosphonate (DPP) was 8.3×10^{14} cm^{-2}, higher than diethyl vinyl phosphonate (DVP) which was later verified using TOF-SIMS. Boron and phosphorous containing chemistry have been used to form the monolayer on silicon surface, recently O'Connell et al reported Arsenic containing chemistry and doped planar Si and nanowires.

Monolayer Contact Doping (MLCD) was first introduced by Hazut et al, the techniques involved formation of dopant containing monolayer on a donor substrate, which was then later brought in contact with device wafer and annealed, the technique eliminated the need of capping oxide and its subsequent etch. MLCD was used to dope intrinsic silicon nanowires were contacted

by two terminals. It was observed the MLCD resulted in decrease in the sheet resistance of the nanowires as compared to conventional doping techniques [8].

MLD also finds application in photovoltaic industry, Puglisi and coworkers reported about MLD dopes Si nanowires which were integrated into the solar cell had higher short circuit current and fill factor than Si planar solar cells [10].

1.2 Thesis Outline

The work is focused on achieving phosphorous doping of p-type silicon using MLD followed by surface and electrical characterization. Chapter 2 presents the existing doping techniques, their disadvantages and need for a new technique Monolayer Doping. Chapter 3 discusses the various application of MLD like the ultra-shallow junction, selective emitter, and contact engineering via selective doping. In Chapter 4, the elemental and electrical characterization of monolayer dopant diffused layer are described. Chapter 5 elaborates on the diode theory, specific contact resistivity of metal-semiconductor contacts and transmission line method. Chapter 6 describes about the reaction mechanism for MLD, apparatus designed for silicon pieces, its conversion to 6-inch setup, chemicals, and process flow to achieve MLD. Chapter 7 presents the results obtained through elemental characterization XPS, AES, SIMS, sheet resistance measurement and SRP. Chapter 8 elaborates on the fabrication steps for N+P diode and TLM patterns. The results of the diode I-V characteristics, comparison with unified model and specific contact resistivity among others are also discussed .Experiments to pattern monolayer along with the results are discussed in chapter 9, followed by conclusion and future work in chapter 10.

Chapter 2

Background

In this chapter the doping mechanism in silicon, current doping techniques – ion implantation, spin on doping and others are explained. A new technique Monolayer Doping is introduced.

2.1 Doping in Silicon

Silicon belongs to IV group and has four valence electrons in its outer shell which are covalently bonded to the other valence electrons of adjacent silicon atoms. The valence electrons at 0^oK are covalently bonded therefore do not contribute to electrical conductivity of the silicon, as the temperature increases the bonds break and valence electrons/holes are released. In the intrinsic silicon which is chemically pure the number of electrons is equal to the number of holes. Electrical properties of the semiconductor can be altered by adding impurities this method is called doping.

If the impurities added to the silicon are from group V like Phosphorous, Arsenic, Antimony and Bismuth it forms n-type semiconductor. The elements in group V have five valence electrons, when they displace silicon atom four of the valence electrons form covalent bonds with the valence electron in Si atom. The fifth valence electron does not form any covalent bond and can leave the atom as a free electron. The number of electrons in the silicon is higher than the intrinsic silicon and therefore alters the electrical properties. The impurity added to the semiconductor are from group III (Boron, Aluminum and Gallium). They have three valence electrons in the outer shell and forms three covalent bond out of four valence electrons from the Silicon atom thus creating hole. These impurity are also called acceptors and form p-type

semiconductor as the hole is considered positively charge. The resistivity of the semiconductor depends on the dopant concentration as shown in Figure 2.2 and can be altered easily.

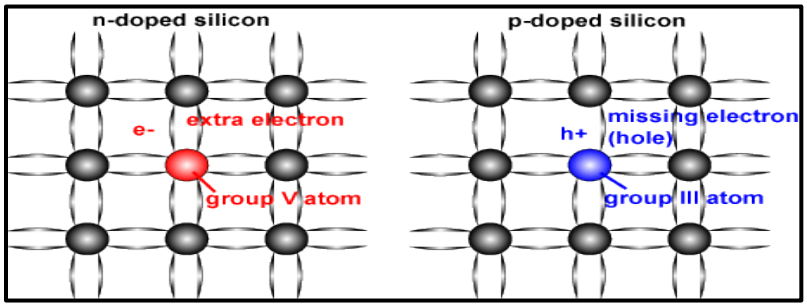


Figure2.1: Schematic of silicon crystal doped with impurities [2].

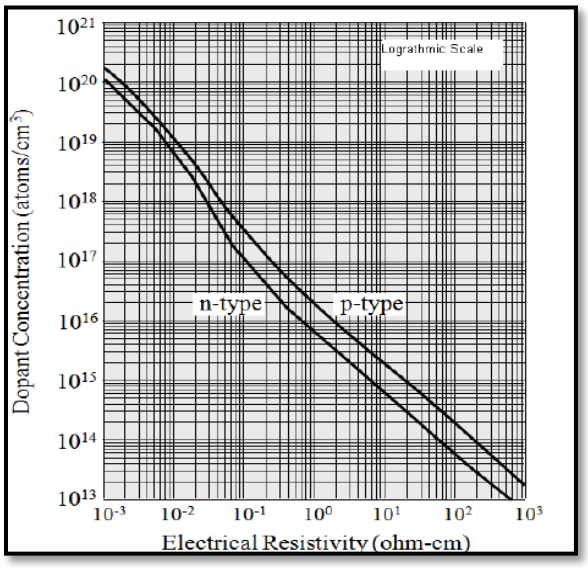
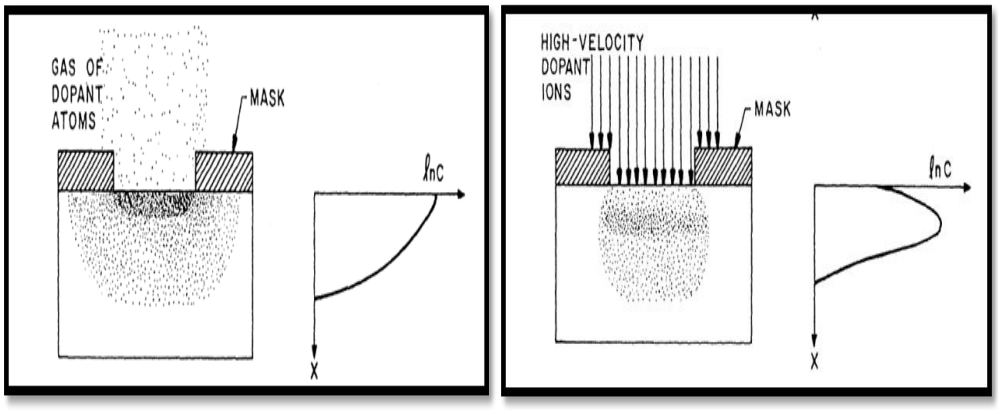


Figure 2.2: Dopant concentration versus resistivity of silicon [3].

2.2 Current Doping Techniques

Diffusion and Ion Implantation are two commonly used doping techniques used in the industry to add impurities in the semiconductor are shown in Figure 2.3. Diffusion involves the movement of dopant particles from higher concentration to lower concentration regions in random

motion whereas ion implantation involves bombarding accelerated ions on the surface of the substrate.



(a) (b)

Figure 2.3: Doping techniques (a) Thermal diffusion and (b) Ion implantation [18].

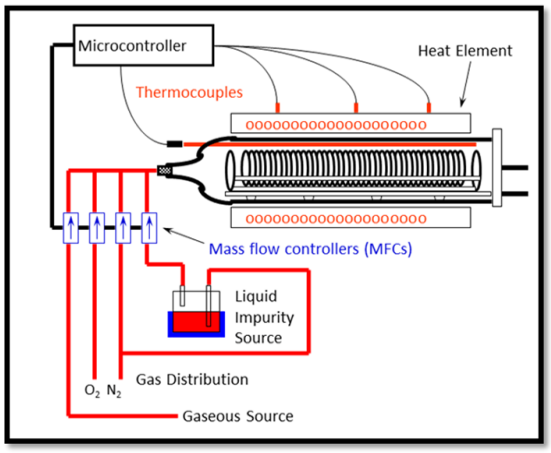


Figure 2.4: Schematic showing the general diffusion system. [18]

In Figure 2.4, the general diffusion system is shown, the dopant source can be either gaseous (Diborane, Phosphine, Arsine, Silane), spin on glass (Pockel) or liquid (Arsenosilica, Phosphosilica and Borosilicate).

2.2.1 Spin on Doping

Spin on dopant is another method that provides a dopant source for fabrication of junctions. The dopant is applied to the surface of the substrate followed by spinning to form a uniform layer of dopant containing film, the excess solvent is removed by a pre-bake step followed by diffusion at elevated temperature to form desired junction profile. Spin on dopant has lack of control over the areal dose of dopants and forms non-uniform junctions.

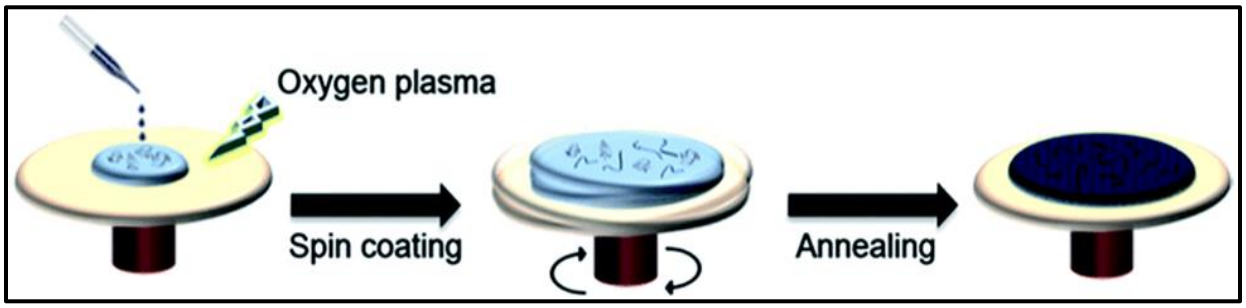


Figure 2.5: Diagram of spin on coating of dopant [7].

The process of two-step diffusion is described in Figure 2.6, the first step is the introduction of impurities into the substrate called pre-deposition, it follows constant source mechanism and the impurity in the region is determined by calculating area under the curve in Figure 2.7.

$$C(x,t) = C_{ssb} erfc\left(\frac{x}{2\sqrt{D_1 t_1}}\right) \tag{2.1}$$

$$Q = \frac{2}{\sqrt{\pi}} C_{ssb}\sqrt{D_1 t_1} \tag{2.2}$$

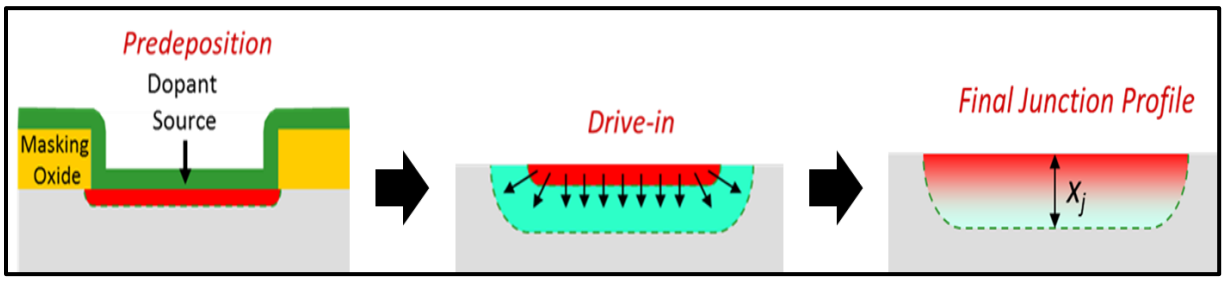


Figure 2.6: Two step diffusion process [18].

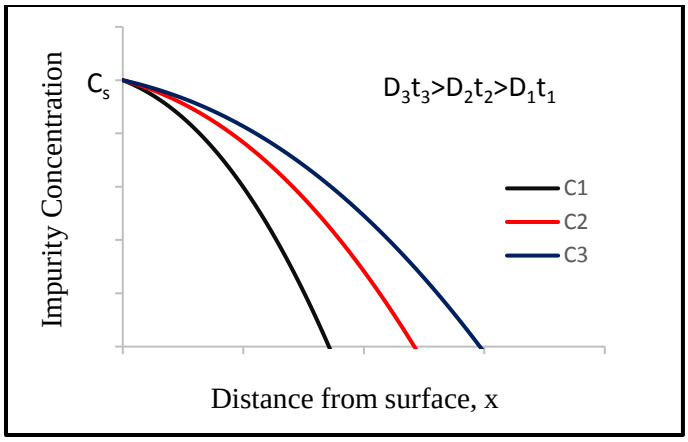


Figure2.7: Constant source diffusion

The second step is to drive-in dopants which determines the surface concentration and junction depth. The drive-in is limited source diffusion and forms a Gaussian profile calculated using equation 2.3. The drive in diffusion profile for varying time is given in Figure 2.8, the surface concentration decreases with time and whereas junction depth increases with time.

$$C(x) = \frac{Q}{\sqrt{\pi D_2 t_2}} \exp\left(-\frac{x^2}{4D_2 t_2}\right) \tag{2.3}$$

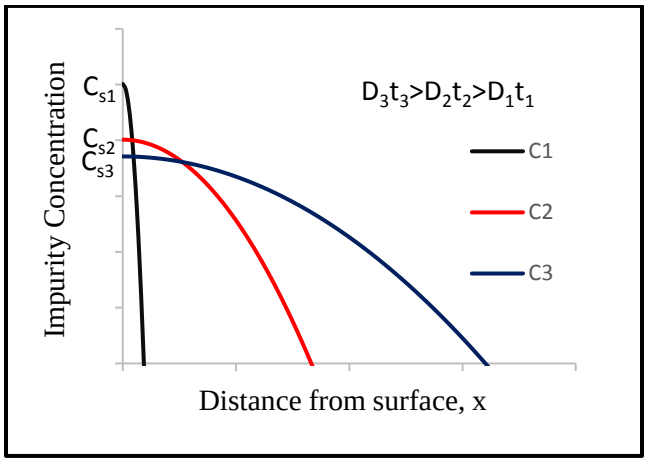


Figure 2.8: Limited source diffusion

2.1.2 Ion implantation

Ion Implantation is the technique used for introduction of dopant into the semiconductor, and it was patented by William Shockley in 1954. Although the patent was issued in 1954, it was used in manufacturing much later. It is a low-temperature process and has more advantage over thermal diffusion. The dopant atoms are volatilized, ionized, accelerated, separate by mass to charge ratio and directed towards the substrate or target. When the atoms are bombarded on the surface of the substrate, the atoms collide with the host atoms, lose energy and finally come to rest at a certain depth. The light ions like Boron loose energy by columbic interaction, it is called electronic stopping power, whereas heavier ions like Phosphorous and Arsenic loose energy by nuclear collision called nuclear stopping power.

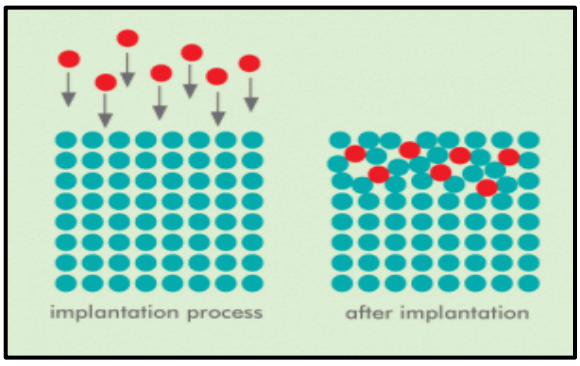


Figure 2.9: Arrangement of atoms before and after implantation [8]

Profile after implantation and drive –in is calculated using equation 2.4, where R_p and ΔR_p are projected range and straggle.

$$C(x) = \frac{Q}{\sqrt{2\pi}\sqrt{\Delta {R_p}^2 + 2Dt}} exp\left[-\frac{(x - R_p)^2}{2(\Delta {R_p}^2 + 2Dt)}\right] \quad (2.4)$$

The dose is the time integral of the current density, the implanted profile can be approximated by a gaussian function as given in figure 2.10.

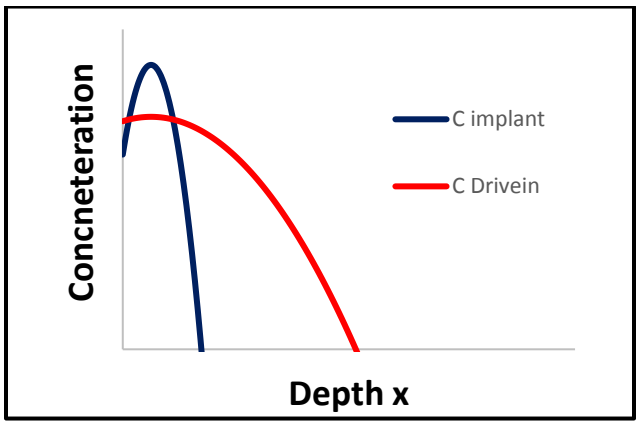


Figure 2.10: Implanted and drive-in profile

Table 1: Strengths and weakness of current doping techniques

Doping Techniques	**Strengths**	**Weaknesses**
Conventional Diffusion	No damages created	Forms glassy skin that needs etching
		Limited to solid solubility
	Well studied and employed	Low dose predeps are difficult
		High temperature process
	Batch fabrication possible	Shallow junctions are Difficult
		Involves hazardous material
Ion Implantation	Complex profiles can be achieved by multi-energy implants	Deep and shallow profiles are difficult
		Not all the damages created can be corrected by annealing
	Precise Dose Control	Involves hazardous materials
		Implant Diffusion enhances diffusion
	Extensively used in IC industry	Implant Diffusion enhances diffusion
		Can be expensive

In Table 1, the strength and weakness of current doping technology i.e. conventional diffusion and ion implantation are described.

2.1.3 Other Techniques

The other doping techniques include plasma doping and gas immersion laser doping. In plasma doping the accelerated dopant ions are extracted from the plasma at high voltage and bombarded on the substrate which is attached to the other electrode. Plasma based ion implantation forms shallow junction as compared to beamline implant. In gas Immersion Doping the impurity is introduced into the silicon substrate during regrowth step, using XeCl pulsed excimer laser beam. The important feature of this of this technique is that no high temperature anneal is required to activate and diffuse the dopant.

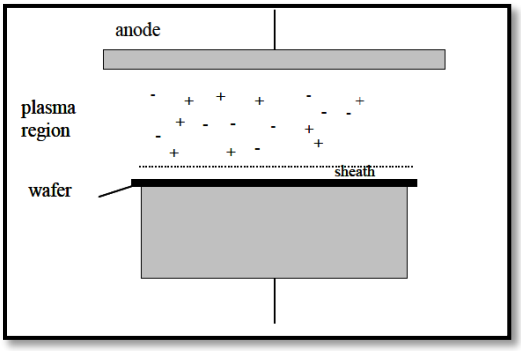


Figure 2.11: Schematic of plasma doping setup [31].

2.3 Molecular Monolayer Doping

Molecular Monolayer Doping is a two- step approach which is based on the formation of self-assembled monolayer of dopant coating molecules on the surface of crystalline Silicon followed by rapid thermal anneal to diffuse and activate the dopant to form a junction. The covalently attached monolayer featuring chemically substitute dopant atoms on the silicon surface

is well defined. The monolayer and silicon interface when exposed to high-temperature thermal diffusion it results in the breakage of the bonds formed between silicon and dopant containing chemical and desirable junction depth is achieved.

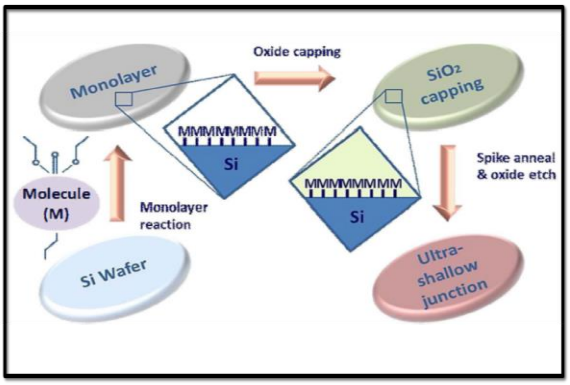


Figure 2.12: Schematic showing the monolayer doping process. [4]

Controlled doping of semiconductor material with high atomic accuracy and minimum defects is the main aim of monolayer doping technique which can be used at nanoscale technologies. MLD can be used for both n and p-type doping of either bottom-up or top-down structure thus making it highly versatile for various applications. Due to the formation of bonds on the surface it helps to control dopant dose which is not possible with other technologies, in spin-on dopant the thickness of the material whereas in ion implantation the gas flow rate control the dose of the dopant. The monolayer formation involves self-limiting reaction on the crystalline silicon surface resulting in well-defined monolayer formation with high molecular accuracy. Moreover, doping profile can also be tuned by different annealing conditions. Therefore MLD can be used for conventional planar devices, FinFETs and nanowires, it can also be used for both bottom-up and top-down approaches making it highly versatile. It is currently examined by the industry for ultra-shallow junctions for silicon and III-V substrates.

Chapter 3

Application of Monolayer Doping

MLD finds application in both Integrated Circuit and Photovoltaics industry. It can be used to achieve ultra-shallow junctions in planar and three-dimensional electronic devices. In PV industry MLD can help to fabricate selective emitter thus increasing the efficiency of solar cell.

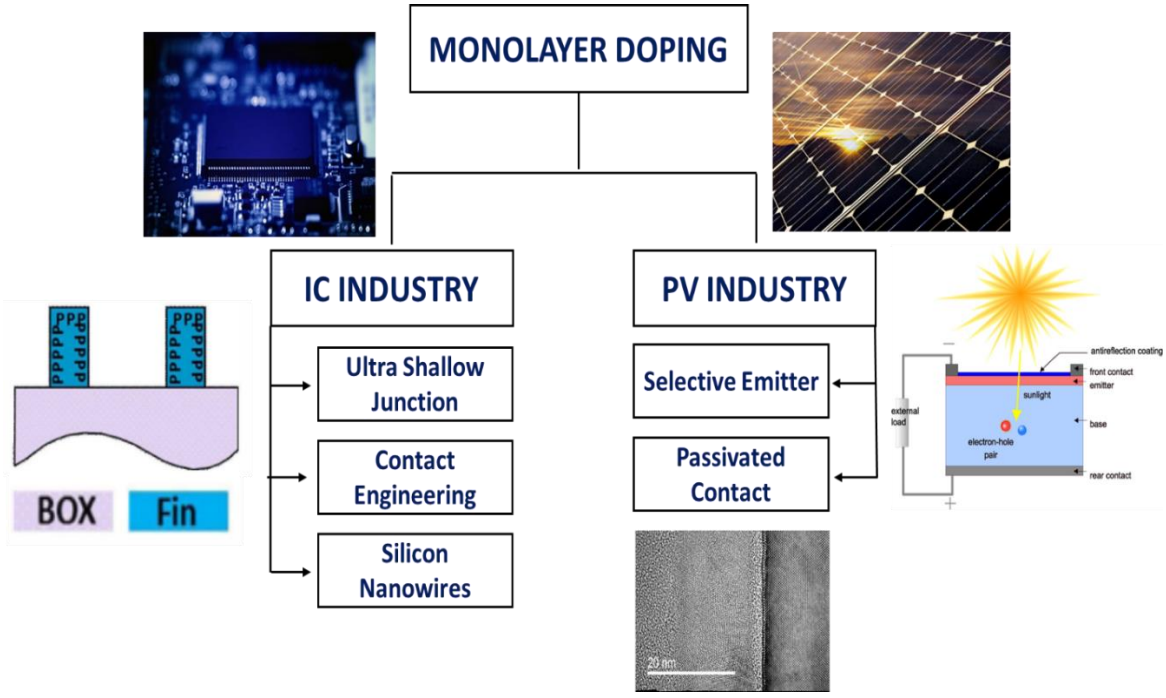


Figure 3.1 Applications of monolayer doping

3.1 Electronic devices

In this section, the possible application of MLD in IC industry are discussed. MLD is a uniform, controlled and conformal doping technique and can be used fabricate ultra-shallow junction, 3-D devices and silicon nanowires for better performance.

3.1.1 Formation of Ultra-Shallow Junction

The technological advancement in the semiconductor industry has been governed by device scaling. To achieve faster transistor speeds and higher packing density junction depths along with gate length is continuously scaled. In Figure 3.2 the junction depth versus sheet resistance for different doping and annealing technique, MLD results in low junction depth along with lower sheet resistance.

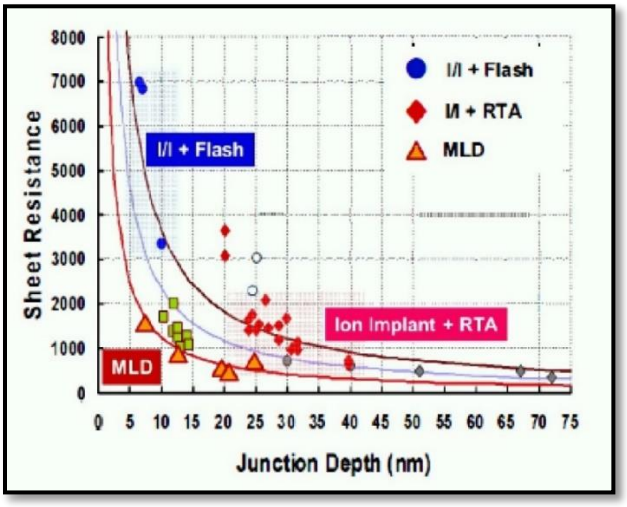


Figure 3.2: Junction Depth- Sheet resistance for doping and annealing techniques. [5]

It is important to realize ultra-shallow junctions (USJ) with low sheet resistivity, if not it would result in short channel effects like drain induced barrier lowering, surface scattering, velocity saturation, impact ionization and hot electrons. The modification of the threshold voltage due to the scaling of channel length and limitation imposed on electron drift characteristics in the channel result degraded device performance. One method to solve this problem is by scaling the gate dielectric thickness to maintain control over short channel effects (SCE) but it increases power consumption and gate leakage current. Another alternative to minimize the short channel effects is to decrease the junction depth. In Figure 3.3, the effect of shallow and deep junction depth on the device performance is described.

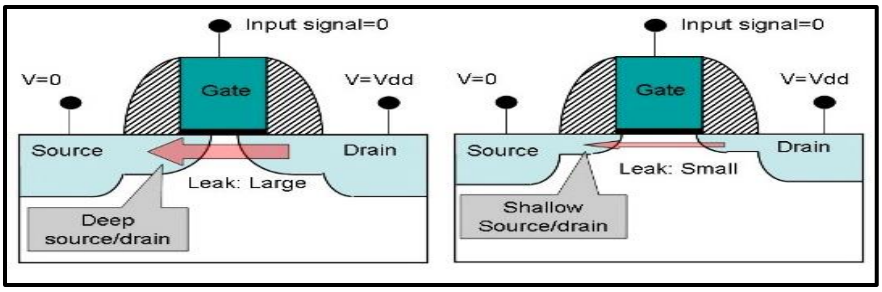


Figure 3.3: Effect of source/drain junction depth on leakage current.

In Industry, USJ are achieved by forming abrupt channel doping from techniques like plasma doping, conventional implantation, infusion and molecular implantation. Shallow profiles can be achieved using low energy implant, the n+ junction is formed using As (arsenic) ion and p+ junction using BF2 (boron fluoride) ion. They are larger atoms as compared to P (phosphorous) or B (boron) therefore has lower implantation range. The disadvantage to this technique is extremely low energy is required and it takes hours to implant required dose .Moreover larger ions cause excessive damage throughout the implanted region.

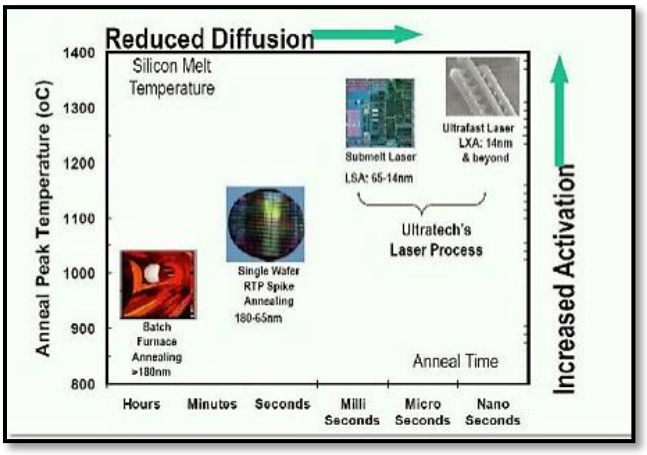


Figure 3.4: Evolution of thermal anneal [16]

High dopant activation and reduced thermal budget is required to achieve USJ, in Figure 3.4 anneal temperature and time of different techniques and their effect on diffusion and activation are described.

3.1.2 Doping of Silicon Nanowires

Silicon nanowires have one-dimensional architecture and unique electrical, optical and mechanical properties, therefore they find applications in electronic devices and photovoltaics. These properties of silicon nanowires are dependent on the doping concentration, thus a controlled technique to achieve desired doping dose is crucial. The existing doping techniques are either destructive or non-uniform. MLD is suitable for doping silicon nanowires, it forms well defined and uniform junction. The can be tuned downward by using mixed MLD which is mixing dopant containing chemistry with the 1-undecene. Dopant dose in increases by using dopant atom rich chemistry.

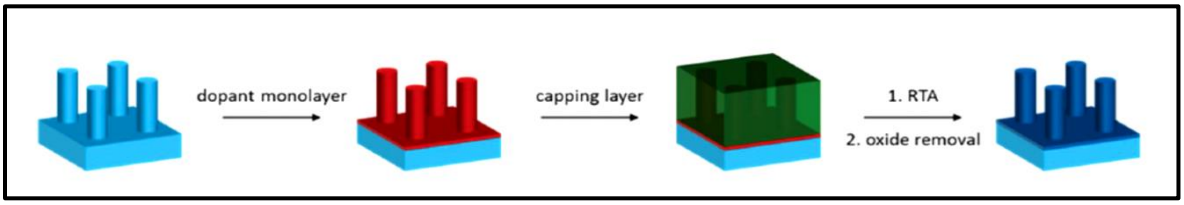


Figure 3.5: Silicon nanowires doped using MLD. [38]

3.1.3 Contact Engineering

The external parasitic resistance is one of the main components that degrade the performance of FinFETs with continuous scaling. The main contributor to the resistance is contact resistance which is between the diffused layer and metal silicide layer. Low specific contact resistivity is desired with scaling of devices, which can be achieved by lowering the Schottky barrier or by increasing the dopant concentration of the diffused region. MLD provides high dopant concentration at the surface which can be used to lower specific contact resistivity as seen in Figure 3.6.

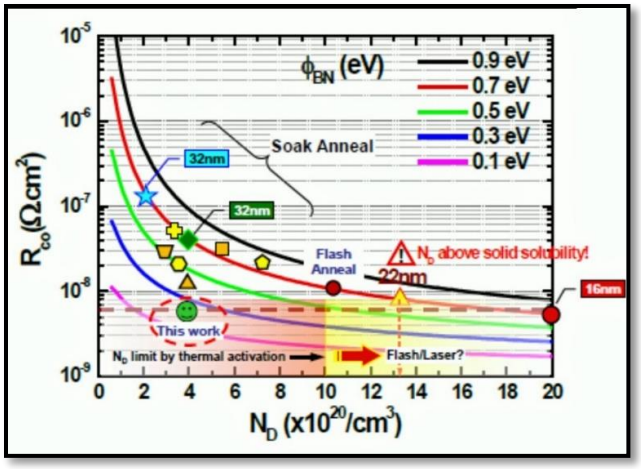


Figure 3.6: Specific contact resistivity versus concentration for various technology nodes. [5]

3.2 Solar Cells

A solar cell directly converts sunlight into electricity, when light shines on the cell it results in the generation of carriers, which produce current and voltage to generate power. The generation of current in the solar cell is a two-step process, first absorption of light, which results in the generation of electron-hole pairs. The cell efficiency can be improved by forming a heavily doped region under the contact called as selective emitter; MLD is a suitable technique for fabricating selective emitter.

3.2.1 Selective Emitter

Increasing the efficiency of solar cell and reduction in the cost of fabrication are the two main aspects of research in PV industry. The cell efficiency can be improved by optimizing passivation layer to reduce recombination, surface texturing to increase light trapped effects and redistributing emitter profile. The higher efficiency of the solar cell depends on the type and quality of emitter. The commonly used solar cell consists of crystalline silicon with a thin layer of a heavily doped region to form planar diode structure, the heavily doped region is called emitter, while the moderately doped region is the base of the cell.

The homogenous emitter in the fabrication of silicon solar cell is one of the main limiting factors of the efficiency of screen-printed solar cell. The incorporation of selective emitter structures results in enhanced efficiency, especially at shorter wavelengths. Surface recombination depends on the number of minority carriers at the junction edge, their movement away from junction and recombination with majority charge carriers. It affects both short circuit current and open circuit voltage.

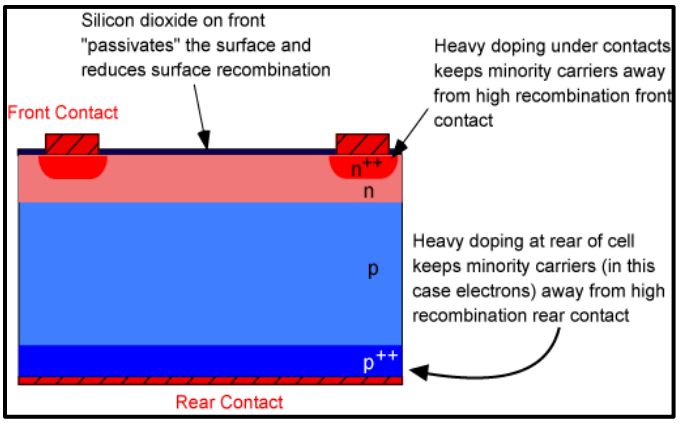


Figure 3.7: Selective emitter as an application of MLD. [2]

In the conventional solar cell, high doping is desirable in order to obtain good ohmic contact, thus contact resistance decreases and fill factor increases. However, it affects both short circuit current and open circuit voltage, The J_{SC} is also affected by recombination, it reduces the charge carriers that reach the contact. Further, when the emitter is lightly doped, the recombination of electrons and holes reduces thus increasing J_{SC} and V_{OC}, but the contact resistance increases which in turn affects fill factor of the cell. The advantages of both heavily and lightly doped emitter are realized in the selective emitter. It is heavily doped region under the contacts which result in good ohmic contact and also keeps minority carriers from recombining at the front surface due to field.

3.2.2 Passivated Tunneling Contact

Passivated contacts (low Jo, contact) are required for high efficiency solar cells. One way to realize carrier selective contacts (thus low Jo,contact) is to form tunnel oxide passivated contacts (TOPCon) consisting of an ultra-thin tunnel oxide and a heavily doped poly-crystalline silicon (poly-Si) layer as shown in Figure 3.8. Doping the thin poly-Si layer is currently achieved by in-situ growth by PECVD or by ex-situ ion implantation. Heavily doped polysilicon can be used as passivated layer since it is sensitive to sample preparation, tolerate high thermal budget and low contact resistance. MLD can be used to heavily dope polysilicon. [25]

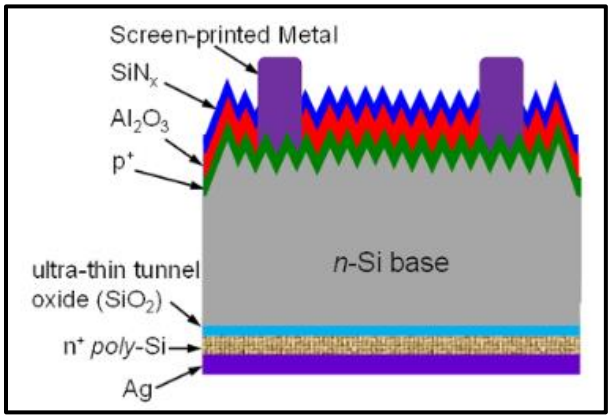


Figure 3.8: Schematic of a solar cell structure with rear passivated tunnel contact. [41]

Chapter 4

Characterization of Diffused Layer

4.1 Elemental Characterization

In this chapter, the techniques used to characterize MLD before and after annealing are discussed. Elemental characterization like Auger Electron spectroscopy, X-ray photoelectron spectroscopy, and Secondary ion mass spectroscopy are described. The electrical characterization of the MLD doped layer is performed using spreading resistance profile and sheet resistance measurement.

4.1.1 Secondary Ion Mass Spectrometry (SIMS)

SIMS is commonly used technique for surface analysis; it helps to detect impurity elements in a surface layer and bulk. The surface of the sample is bombarded with high energy ions which result in charged or neutral particles being ejected out of the surface and are transferred into a mass spectrometer across electrostatic potential, therefore the particles are also called as secondary ions. The particles could be in the form of atoms, cluster of atoms or molecular fragments.

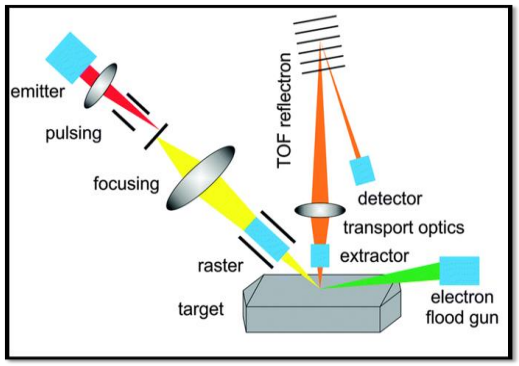


Figure 4.1: Secondary ion mass spectroscopy. [18]

The mass spectrometer consists of both magnetic and electrostatic analyzer; the energy of the secondary ions is reduced by the electrostatic analyzer filter, which helps to separate the ions by the magnetic analyzer on the basis of their charge/mass ratio. The advantages of using SIMS are that the analysis requires only small sample. Further samples with low concentration levels can also be analyzed due to very high sensitivity, which also allows the depth profiling of the sample.

4.1.2 X-Ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is surface analysis technique is commonly used technique to determine quantitative atomic composition and chemistry. It provides information about the chemical state of the element detected, by irradiating sample with monochromatic x-ray that results in ejection of photoelectrons, the energies help to characterize the sample. XPS analyses surface layer or thin films of about 5 nm average depths. The sample is excited with the x-ray that results in emission of photoelectrons from the surface of the sample. An electron energy analyzer measures the energy of the emitted photoelectron. The binding energy and the intensity of a photoelectron peak help to determine the element, chemical state, and quantity.

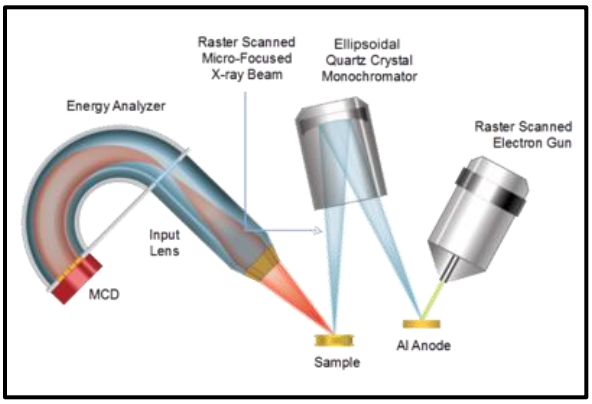


Figure 4.2: X-ray photoelectron spectroscopy. [42]

4.1.3 Auger Electron Spectroscopy (AES)

The technique uses the emission of low energy electrons through auger process and helps determine the surface composition of the sample. It involves three steps, first is atomic ionization which involves the sample being exposed to high energy electrons that results in ionization of all levels of lighter elements and higher core levels of heavier atoms. The ionized atoms are in excited state and try to relax to lower energy either by x-ray fluorescence or by Auger emission, which is the second step. The energy when the ionized atom relaxes to lower atom if transferred to the second electron, it utilizes fraction of this transferred energy to overcome the binding energy and the remaining is used as kinetic energy. The chemical state and elemental identity of the sample are determined by the kinetic energy and intensity of the Auger peak.

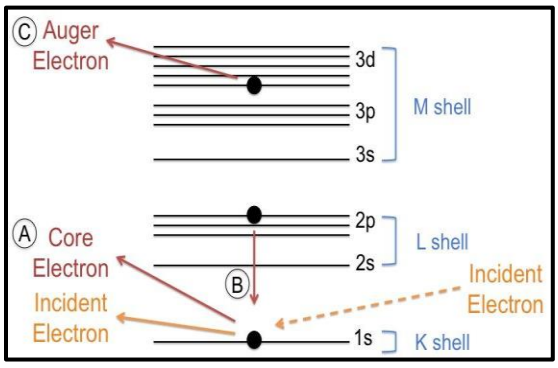


Figure 4.3: Schematic of the auger process [42].

4.2 Electrical characterization of Profile

4.2.1 Diffusion Profile

The dopants attached to the surface using MLD process rely on thermal process to diffuse; the dopants atoms occupy either substitutional or interstitial position in lattice. Impurity atoms such as Boron, Phosphorous and Arsenic occupy substitutional position in which the dopants

atoms contribute free electrons or holes to silicon lattice, during high-temperature processing impurity profile is redistributed through random thermal motion and this process is called diffusion.

The diffusion process in MLD is described using Fick's law, it relates the diffusion flux across the boundary to the concentration gradient in the system. It is seen that regions with higher concentration diffuse more rapidly. Fick's law explains the change in concentration with time at a definite location. The boundary conditions are solved to determine the impurity profile. The two conditions are constant dose and constant concentration. MLD uses constant dose as primary mechanism for diffusion of dopants, the fixed amount of dopant is incorporated silicon during annealing step. It is considered that there is no loss of impurity during diffusion and impurity dose introduced at the surface boundary gives following solution

$$C(x,t) = \frac{Q}{\sqrt{\pi D t}} \exp\left(-\frac{x^2}{4Dt}\right) \tag{4.1}$$

, where Q is impurity dose in atoms/cm^2, t is drive in time (sec) and D is diffusion constant.

$$D = D_o \exp\left[-\frac{E_a}{kT}\right] \tag{4.2}$$

Table 2: Diffusion coefficient of phosphorous in silicon varying temperature

Temperature (^{o}C)	Diffusion Coefficient cm^2/sec
950	6.60 x 10^{-15}
1000	2.60 x 10^{-14}
1050	9.31 x 10^{-14}
1100	3.03 x 10^{-13}
D_o = 10.5 cm^2/sec and E_a= 3.69	

In Figure 4.5, the impurity profile, which is the concentration of an impurity versus depth into the silicon is plotted. The impurity profile can be used to determine the junction depth. Silvaco, Athena is used to model MLD diffusion. Constant dose mechanism is used for 1 x 10^{13} cm^{-2}, 5 x 10^{13} cm^{-2} and 1 x 10^{14} cm^{-2} dose. Diffusion profile, sheet resistance and junction depth were generated. (See Appendix)

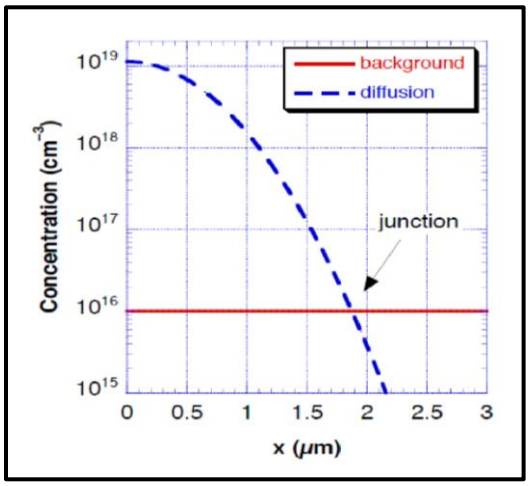


Figure 4.4: Concentration versus depth and junction depth. [16]

The diffusion of phosphorous impurity atoms in the silicon is vacancy dominated. In Figure 4.5 the Phosphorous profile is illustrated, it has three distinct regions. The first is high concentration region where the total phosphorous concentration exceeds the free carrier concentration, followed by kink in the profile and finally a tail region of enhanced diffusion. In the region of high concentration of phosphorous a fraction of phosphorous ions pairs with vacancies, the concentration is directly proportional to the surface electron concentration cubed. The difference in tetrahedral radius of phosphorous and silicon results in a mismatch ratio which at higher concentration results in defect formation due to strain on phosphorous lattice. A study proposed by Fair and Tsai suggest that the tail formation in the phosphorous diffusion profile is

due to dissociation of phosphorous and vacancies pair when the surface concentration drops below 10^{20} /cm^3.

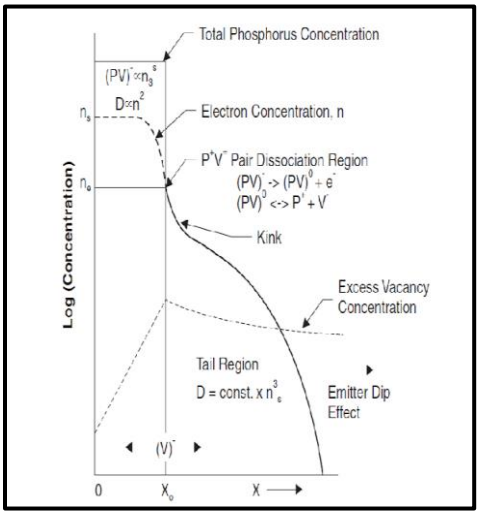


Figure 4.5: Phosphorous diffusion profile. [36]

4.2.2 Sheet Resistance

The sheet resistance is used to characterize thin-doped layers as well as the substrate given by Ω/sq, it is dependent on the resistivity ρ which is an intrinsic property of the material and thickness of the layer t_o as given in equation 4.3. The mobility μ is dependent on the doping density n cm^{-3}. The sheet resistance of doped region is a function of surface dopant concentration, average mobility and junction depth given in equation 4.4.

$$R_s = \frac{\rho}{t_o} \tag{4.3}$$

$$R_s x_j = \frac{1.13 \left[\ln \frac{C_s}{C_B}\right]^{1/2}}{q C_s \bar{\mu}} \tag{4.4}$$

$$\rho = \frac{1}{q\ \mu\ n} \tag{4.5}$$

Four point probe is most common method to measure the resistivity or sheet resistance of the film. The resistance is measured by measuring the current flows between the probes for a given applied voltage. Four probes are used instead of two since it reduces current spreading and gives more accurate results. The current is forced between the two outer probes and voltage drop is measured across the two inner probes and thus avoids any problems with probe contact.

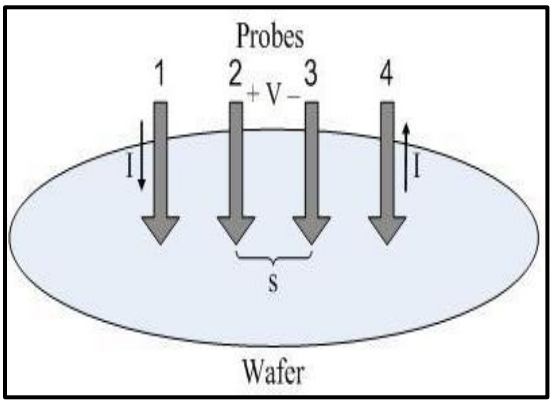


Figure 4.6: Four point probe to measure sheet resistance. [29]

For a thin sample where thickness (t) of the sample is much smaller than the spacing (s) between the probe (t<<s), the resistivity is given by equation 4.6. The sheet resistance measurement were carried out on CDE Resmap 4 point resistivity mapping tool.

$$R_s = \frac{\pi}{ln2}\frac{V}{I} \tag{4.6}$$

4.2.3 Spreading Resistance Profiling (SRP)

Spreading Resistance Profiling is a technique that is used to analyze the resistivity versus depth profile in semiconductor. The voltage is applied between two metal needles that are some distance apart and are pressed into the surface of the semiconductor. The resistance is measured between the two needles and is given by equation 4.7.

$$R = \frac{\rho}{2a} \tag{4.7}$$

, Where R is the resistance measured in ohms, ρ is the resistivity of the sample measured in Ω-cm and a is the radius of the contact area in cm^2. The spreading resistance profiling provides information about the active dopant in the substrate whereas SIMS gives total dopant in the substrate.

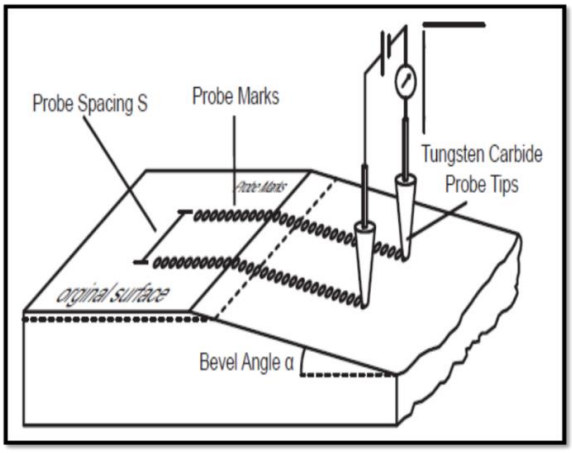


Figure 4.7: Spreading resistance profiling. [19]

Chapter 5

Diode and Contact Resistivity Measurement Structures

The PN junctions are most widely used in electronic device structures such as diodes, transistors, solar cells and temperature sensors. The diode theory, ideal diode current equation, influence of high injection voltage on the characteristics and unified model are discussed. The specific contact resistivity is an important parameter in contact engineering and is measured using transmission line method is described in this section.

5.1 Diode Theory

When p-type and n-type semiconductor are brought in intimate contact carriers diffuse across the junction forming a fixed charge layer on either side due to ionized impurity atoms. The depletion region or space charge region is formed and is depleted of mobile carriers. The electrostatic analysis of p-n diode provides information about charge density and electric field in the depletion region.

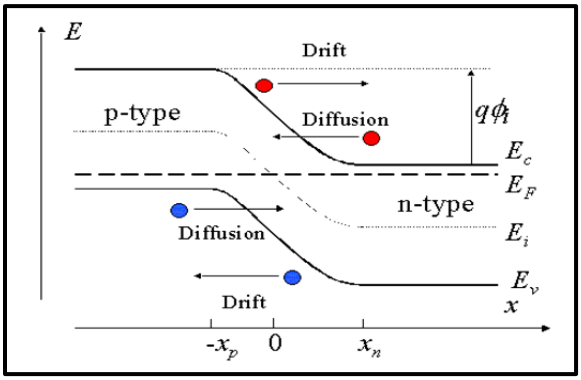


Figure 5.1: Energy band diagram of a p-n junction in thermal equilibrium. [18]

In Figure 5.1 energy band diagram of p-n junction at thermal equilibrium is shown, there is an internal potential at thermal equilibrium that is due to the difference between the n and p-type semiconductors called built-in potential given in equation 5.1.

$$V_{bi} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{5.1}$$

5.1.1 Total Current Density

The ideal diode characteristics of PN diode are based on some assumption like there is low-level injection which means majority charge carrier is much greater than the minority charge carrier. Further, the diode has abrupt boundaries and semiconductor outside the boundaries is neutral and the electron and hole concentration is constant in depletion region. The J-V characteristics of the diode are found by solving the boundary condition for diffusion current density.

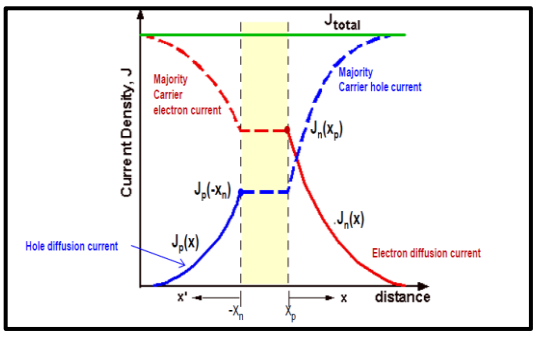


Figure 5.2: Total current density in the PN junction. [2]

The total current density for ideal long diode (quasi neutral width on each side is >> respective minority carrier diffusion length) is given in equation 5.2:

$$J_{np}(-x_p) + J_{pn}(x_n) = qn_i^2 \left[\frac{D_n}{L_n N_D} + \frac{D_p}{L_p N_A}\right]\left[\exp\left(\frac{qV_a}{kT}\right) - 1\right] \tag{5.2}$$

The space charge region is assumed to have no free carrier and the dopant concentration is constant in this region that in turn means there is no recombination or generation in the space charge region thus the current density remains constant. When these assumptions are not considered the general diode current voltage characteristics is given in equation 5.4 where $J_{s,QNR}$ and $J_{s,SCR}$ are current

density in quasi neutral region and space charge region. The ideality factors are given by n1 and n2. The total current density is current density in neutral region and in depletion region.[15]

$$J = J_{NR} + J_{DR} \tag{5.3}$$

$$J = J_{s,QNR}\left[\exp\left(\frac{qV}{n_1 kT}\right) - 1\right] + J_{s,SCR}\left(1 - \frac{V}{V_{bi}}\right)^{\frac{1}{2}}\left[\exp\left(\frac{qV}{n_2 kT}\right) - 1\right] \tag{5.4}$$

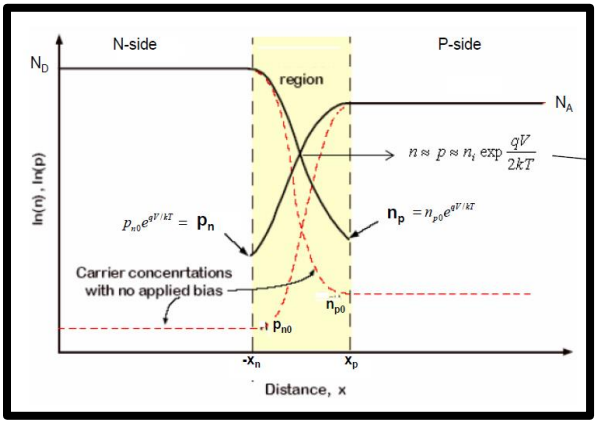


Figure 5.3: Carrier concentration in forward bias. [2]

The intrinsic carrier concentration remains same on the both sides (n_i), the emitter is considered to be heavily doped ($x_p >> x_n$) and surface recombination velocities are considered to be infinite. For a one step abrupt N+P diode, current density can be written as:

$$J = qn_i^2\left\{\frac{D_n}{N_A L_n}\right\}\left[\exp\left(\frac{qV}{n_1 kT}\right) - 1\right] + \frac{qx_p n_i}{2\tau_n}\left(1 - \frac{V}{V_{bi}}\right)^{1/2}\left[\exp\left(\frac{qV}{n_2 kT}\right) - 1\right] \tag{5.6}$$

It must be noted that equation 5.6, assumes low-level injection i.e. minority carrier concentration injected is less than the majority carrier concentration in the base.

In the forward bias I-V curve of the diode at higher current densities there is a shift from the ideal diode curve as seen in Figure 5.4, one of the reasons for this deviation could be high-level injection. When the minority carrier concentration injected in the neutral region is much higher the low-level

injection conditions are not applied, this condition is called high-level injection. The onset of high-level injection happens for condition stated in equation 5.9, where V_{hl} is defined as the voltage at which high-level injection would be observed.

$$\delta n = n_{po} exp\left(\frac{qV_{hl}}{kT}\right) = N_A \tag{5.8}$$

$$V_{hl} = \frac{kT}{q} ln\left(\frac{N_A}{n_{po}}\right) = \frac{2kT}{q} ln\left(\frac{N_A}{n_i}\right) \tag{5.9}$$

In order to account for high-level condition, a unified model has been developed by M.J. Cristea and is employed in this study. [40]

5.1.2 Unified Model

The unified model analyzes low injection, medium injection, high injection and ohmic region of current-voltage characteristics of p-n junction together instead of analyzing them separately. The general formula for minority carrier concentrations at the boundary of space charge region in n and p side of junction is given by equations respectively.

$$p_n(x_n) = \sqrt{n_i^2\, exp\left(\frac{qV}{kT}\right) + \frac{N_D^2}{4}} - \frac{N_D}{2} \tag{5.10}$$

$$n_p(x_p) = \sqrt{n_i^2 \exp\left(\frac{qV}{kT}\right) + \frac{N_A^2}{4}} - \frac{N_A}{2} \tag{5.11}$$

The following equations can be modified depending on the injection level, at low injection level the majority carrier concentration is equal to the acceptor/donor concentration whereas at high injection level both the minority and majority carrier concentration is higher than the doping of the semiconductor and charge equilibrium condition results in equal magnitude ($n_p = p_p \gg p_{po} = N_A$).The current equations at low injection and high injection level is given in (5.12) and (5.13)

$$J = -q\frac{D_n}{L_n}n_p(x_p) = \frac{qD_n}{L_n}\frac{n_i^2}{N_A}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{5.12}$$

$$J = 2q\frac{D_n}{L_n}n_p(x_p) = \frac{\sqrt{2}qD_n}{L_n}n_i\left[\exp\left(\frac{qV}{2kT}\right)\right] \tag{5.13}$$

The current at low injection and high injection level have dependence on the $n_p(x_p)$, the general formula for current is derived using equation 5.14, which will not depend on the injection level.

$$J = q\frac{D_n}{L_n}\sqrt{2n_i^2\left[\exp\left(\frac{qV}{kT} - 1\right)\right] + N_A^2} - N_A \tag{5.14}$$

The generalized equation of I-V characteristics of long diode using unified model is given in equation 5.15.

$$J = \frac{qn_i x_p}{2\tau_n}\left(1 - \frac{V}{V_{bi}}\right)^{1/2}\left[\exp\left(\frac{qV}{2kT}\right) - 1\right] + q\frac{D_n}{L_n}\sqrt{2n_i^2\left[\exp\left(\frac{qV}{kT}\right) - 1\right] + N_A^2} - N_A \tag{5.15}$$

Table3: Parameters for diode analysis

Parameters	Value
ni (cm-3)	1 x 10^{10}
NA (cm-3)	1 x 10^{15}
T (K)	300
τ (s)	1 x 10^{-7}
µn (cm2/V.s)	1.37 x 10^{3}
µp (cm2/V.s)	4.08 x 10^{2}
Dn (cm2/s)	35.4
Ln (µm)	19

In Table 3, the parameters and constants used for general diode analysis using unified model for varying substrate doping, minority carrier lifetime and series resistance are given. In Figure 5.4,

the current-voltage characteristics for varying substrate doping and minority carrier lifetime are plotted using high-level injection separately and unified model. The substrate doping was varied from 10^{14} cm^{-3}, 10^{16} cm^{-3} and 10^{18} cm^{-3}, rest of the parameters were kept constant. Similarly the minority carrier lifetime was varied from 10^{-3} s, 10^{-5}s and 10^{-7}s respectively. The substrate doping and other parameters were kept constant as given in Table 3.

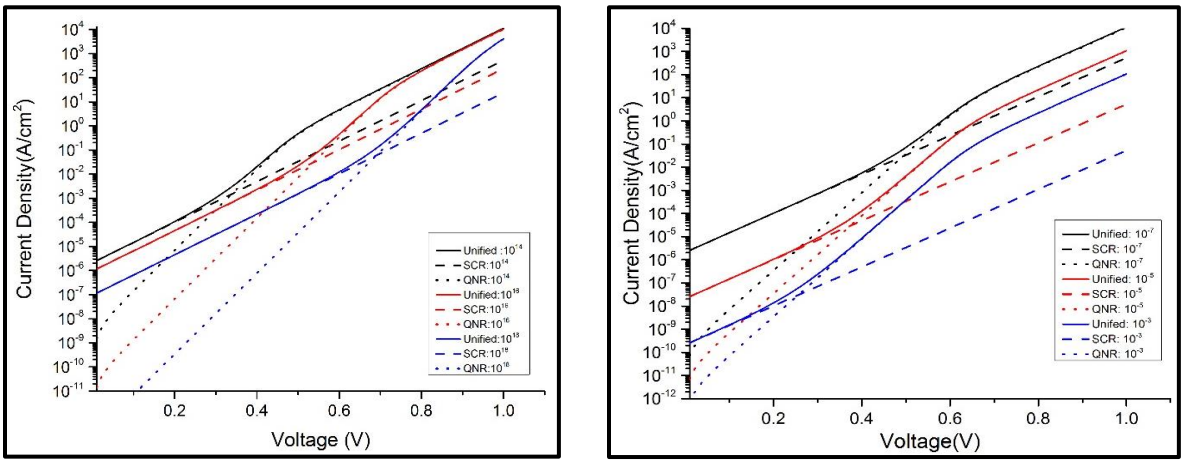


Figure 5.4: J-V characteristics for varying substrate doping and minority carrier lifetime using unified model.

Unified model includes both high and low injection level. As the substrate doping increases the voltage at which high level injection sets in increases. The change in the minority carrier lifetime has effect on the current in the depletion region and the voltage at which the SCR and QNR region intersects. The series resistance of the semiconductor material bends the exponential dependence of current on the forward bias voltage to ohmic dependence that is included in generalized equation 5.16.

$$J = \frac{qn_i x_p}{2\tau_n}\left(1 - \frac{V}{V_{bi}}\right)^{1/2}\left[\exp\left(\frac{qV}{2kT}\right) - 1\right] + q\frac{D_n}{L_n}\sqrt{2n_i^2\left[\exp\left(\frac{V - AJR}{kT/q}\right) - 1\right] + N_A^2} - N_A \tag{5.16}$$

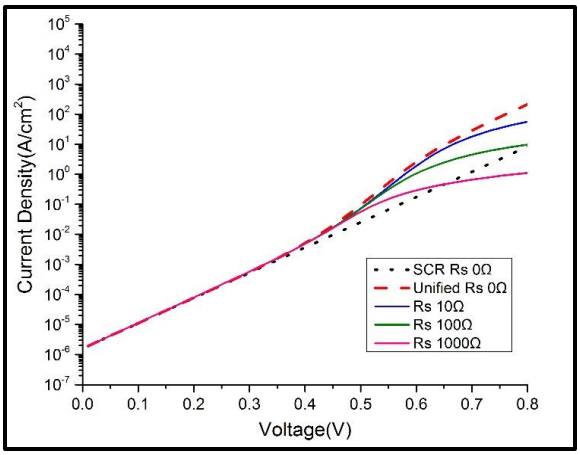


Figure 5.5: The effect of series resistance on the J-V curve of diode using unified model.

In Figure 5.5, the effect of series resistance on the current-voltage characteristics of a diode is simulated using standard parameters. The unified model can be used to extract the value of series resistance in the diode. The increase in the resistance results in increase in the bending of the curve.The four regions in real diode, i.e SCR recombination, ideal, high Injection level and series resistance current – voltage characteristics in forward bias is given in Figure 5.6

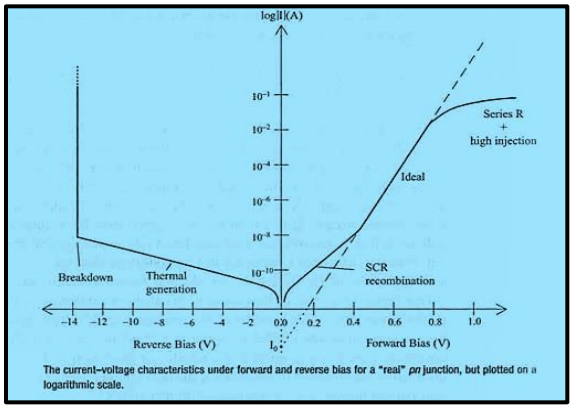


Figure 5.6: Current-Voltage characteristics under forward and reverse bias for diode.

5.1.3 Ideality Factor

The ideality of the diode is defined as a measure of how intently takes after an ideal diode. While determining the basic diode conditions assumptions are made to find the current-voltage characteristics, moreover there are some second order effects which results in diode not following the ideal diode regime and the ideality factor helps to determine these causes. The general diode current voltage equation given in 5.6 can be rewritten as follow

$$I_{NR} = I_{s,QNR}\left[\exp\left(\frac{qV}{n_1 kT}\right) - 1\right] \tag{5.17}$$

For voltages greater than 100mV the -1 term in equation 5.18 is ignored, followed by taking log of both sides we can plot the natural log of the current against the voltage, the slope is equal qV/nkT which determines the ideality factor. It can be plotted as a function of voltage or as a single value.

$$\ln(I_{NR}) = \ln(I_{s,QNR}) + \frac{qV}{n_1 kT} \tag{5.18}$$

5.2 Metal-Semiconductor Contact

Metal-Semiconductor contacts are one of the components of the modern semiconductor devices and various processes and designing methods are applied to improve its performance. Ohmic contacts are preferred connection since it provides low resistance junction, which allows current conduction between metal and semiconductor in both directions. However to form ohmic contact appropriate metal is required, therefore contacts with heavily doped semiconductor which results in carriers tunneling through the semiconductor are formed. The ohmic contact is non-rectifying metal semiconductor contact with low resistance which is independent of voltage applied, it conducts current in both direction from metal to semiconductor and vice versa.

5.2.1 Conduction Mechanism

When metal and semiconductor is brought together to form contact, the conduction in the junction formed is dependent on the doping concentration of semiconductor. The conduction

mechanism in metal/ semiconductor contacts can be described using thermionic emission, field emission and thermionic field emission as shown in Figure 5.6.

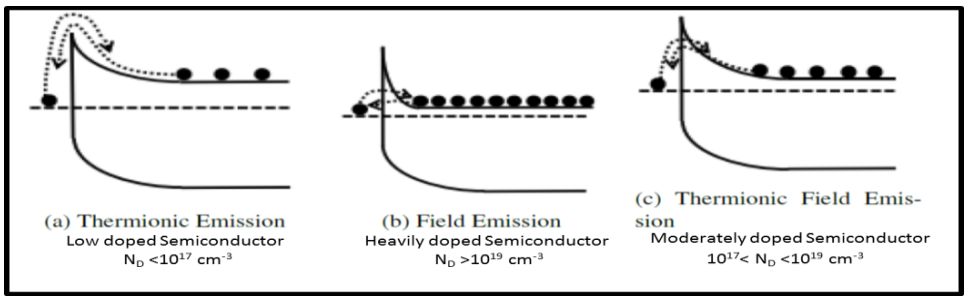


Figure 5.7: Current conduction mechanisms in metal-semiconductor junctions. [21]

Thermionic emission dominates when the semiconductor has low doping density (N_D <$10^{17}cm^{-3}$). For moderately doped semiconductor ($10^{17}cm^{-3}$<N_D <$10^{19}cm^{-3}$) thermionic field emission is the conduction mechanism where carrier is thermally excited to higher energy level but the electrons don't have enough energy to overcome the barrier so it tunnels through the barrier. For heavily doped semiconductor with dopant density N_D >$10^{19}cm^{-3}$ the electrons tunnel through the barrier.

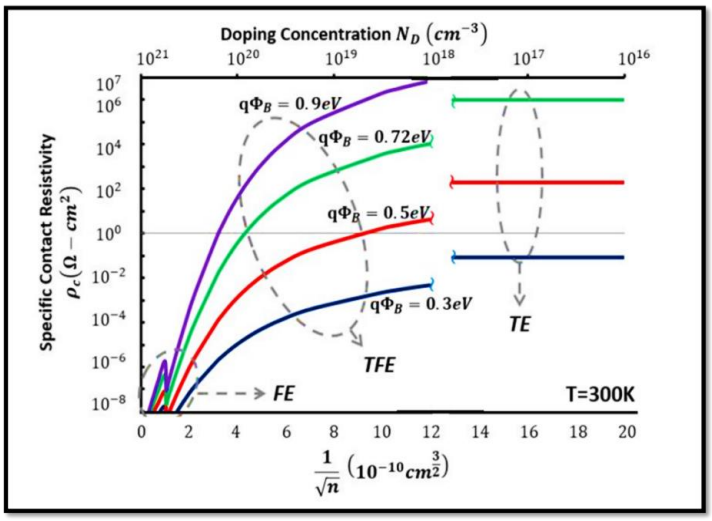


Figure 5.7: Concentration versus specific contact resistivity for different barrier height. [17]

The effect on specific contact resistivity with doping concentration and barrier heights is shown in Figure 5.7. As the doping concentration increases the specific contact resistivity decreases for given barrier height, the field emission conduction mechanism dominates as it has prevalent at higher doping concentration.

5.2.2 Specific Contact Resistivity

Specific contact resistivity (ρ_c) is defined by the component resistance and is a figure of merit for ohmic contacts. The units of ρ_c is Ω-cm^2 and it is defined as the slope of the I-V curve at V=0. In the equation 5.19 J is the current density with voltage at zero bias.

$$\rho_c = \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \tag{5.19}$$

The specific contact resistivity is independent of contact area therefore contacts of different sizes can be measured. It includes contact resistivity of interface and also region above and below interface. The ease with which current flow across a metal-semiconductor interface is defined as contact resistance and can be expressed in terms of contact resistivity and cross sectional area (A) as given in equation 5.20.

$$R_c = \frac{\rho_c}{A} \tag{5.20}$$

5.2.3 Transmission Line Method (TLM)

The specific contact resistivity can be measured using various techniques like two terminal, six terminal techniques etc. Transmission line method was proposed by Shockley, is used to measure the sheet resistance and contact resistance of metal-semiconductor contacts. In this method, total resistance between contacts spaced by a distance d as illustrated in Figure 5.8 is plotted with respect to spacing d. The TLM array have Z and L as width and length respectively.

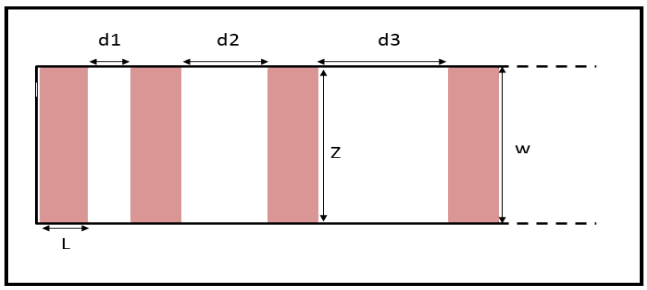


Figure 5.8: Top down view of TLM structure

The TLM structure consists of a diffused semiconductor region with sheet resistance R_{sh} on bare silicon substrate. Metal contacts are fabricated over the diffused region, to separate the contacts insulating oxide is used. The specific contact resistivity is extracted by carrying out I-V measurements on adjacent contacts. The total resistance obtained from this measurement is plotted as a function of distance between the contacts d.

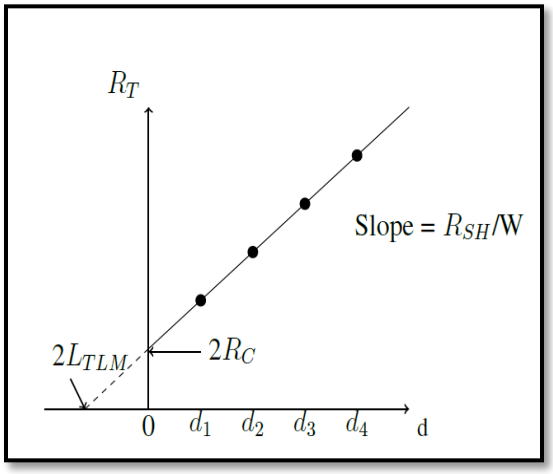


Figure 5.9: Parameter extraction through TLM measurement. [21]

The transfer length (L_T) is the half the x-intercept of the total resistance versus spacing plot and sheet resistance is determined by slope of the line. The transfer length is defined as the

characteristic length obtained when the voltage is 1/e of its value. The equation of the line formed for total resistance is given by equation 5.22

$$L_T = \sqrt{\frac{\rho_C}{R_{sh}}} \tag{5.21}$$

$$R_T = 2R_C + \left(\frac{R_{sh}}{W}\right) d \tag{5.22}$$

The flow of current under metal region and in semiconductor region is illustrated in Figure 5.10, it is observed for low doped semiconductor and thus low ρ_C the current flows quickly into the contact at the edge of the contact area whereas for highly doped semiconductor the current flow is expanded due to high transition resistance.

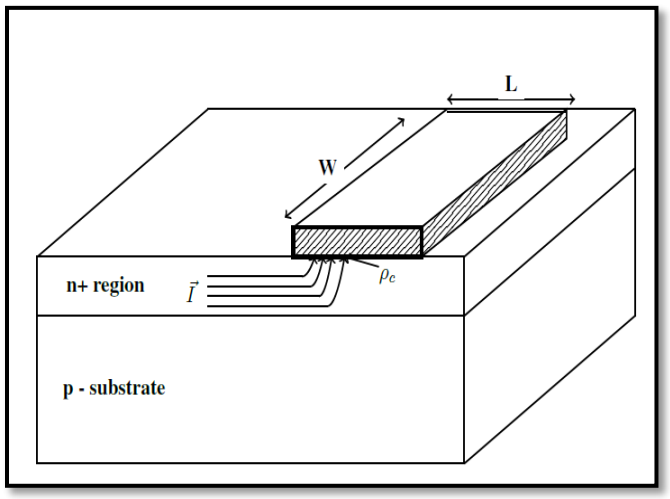


Figure 5.10: Conduction path for metal-semiconductor contact. [21]

If the metal resistivity is low it can be neglected and the contact resistance from lumped circuit model, can be rewritten as

$$R_C = \left[\frac{\rho_c}{L_T Z}\ coth\left(\frac{L}{L_T}\right)\right] \tag{5.23}$$

Since the contact resistance has coth dependence, two limiting cases between L and L_T can be observed short contact approximation and long contact approximation.

- When $L < 0.5L_T$, the specific contact resistivity is dependent on the length of the contact and is called short contact approximation.

$$coth\left(\frac{L}{L_T}\right) \approx \frac{L_T}{L} \ , \quad \rho_c = R_C W L$$

- When $L > 1.5L_T$, the specific contact resistivity is dependent on the transfer length of the contact and is called long contact approximation

$$coth\left(\frac{L}{L_T}\right) \approx 1, \rho_c = R_C W L_T$$

The long contact approximation has some limitation the extraction of ρ_c could be incorrect if appropriate contact geometry is not used. Further the effect of width of the contact is neglected on the extraction of ρ_c. Spreading resistance and current crowding at the edge of the contact is not considered. The sheet resistance and ρ_c are assumed to be uniform throughout the structure.

5.2.4 TLM Optimization

The optimization of TLM structures can be achieved by optimizing the errors in the measurement. The errors are classified into two main-types - random and systematic error. The optimum width for systematic error is given by equation 5.47. The δW and δR are chosen with respect to anticipated error in experimental values. The dependence of specific contact resistivity on width studied by Sidhant Grover will be used to find the optimum width for given sheet resistance and target specific contact resistivity [16].

$$W_{opt} = \sqrt{4\left(\frac{\delta W}{\delta R}\right)\sqrt{\rho_c R_s}} \tag{5.24}$$

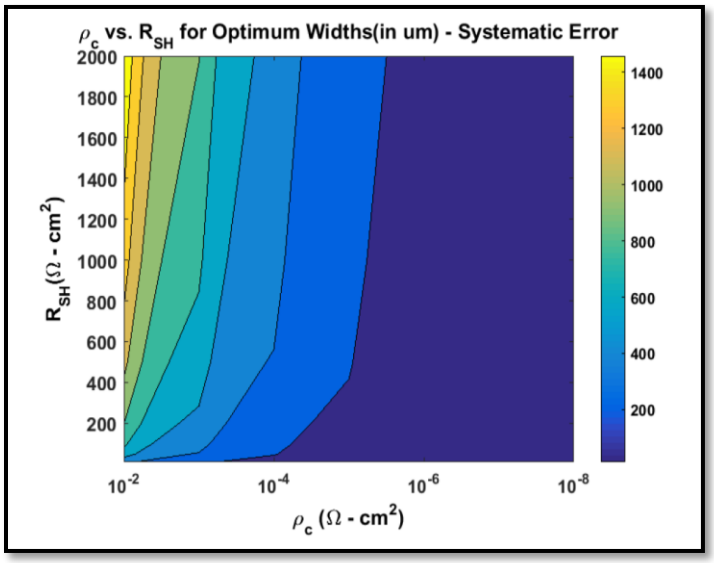


Figure 5.11: Contour map of optimum width for sheet resistance and specific contact resistivity. [22]

Chapter 6

MLD Process Development

Monolayer Doping is defined as the formation of self-assembled monolayer on the surface of hydrogen-terminated silicon and subsequent thermal step to activate and diffuse the dopants in the surface. The schematic flow of MLD process is described in Figure 6.1. In this chapter, the reaction mechanism, setup required for reaction, conversion to full wafer setup and complete process flow is described.

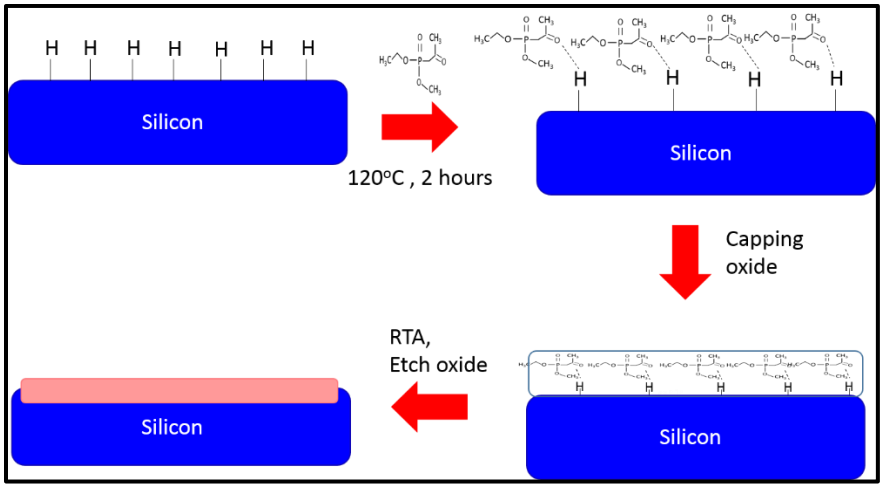


Figure 6.1: Process flow of MLD

6.1 Hydrosilylation Reaction

Organic well-ordered monolayers on the crystalline silicon surface can have various potential applications. The monolayers can be formed either by alkylation of halogen terminated silicon surface with organo-magnisium or organo-lithium compounds. The other method to form monolayer is the reaction between the hydrogen-terminated silicon surface and an alkene or alkyne. The monolayers formed by both these methods are dense, well ordered and linked to the

surface by the stable Si-C bond. The monolayer formation using halogen terminated silicon and then reacting it with organometallic reagents is used less often due to some strong limitation like the presence of Lithium and Magnesium, which is undesirable in the semiconductor industry since it degrades the device performance.

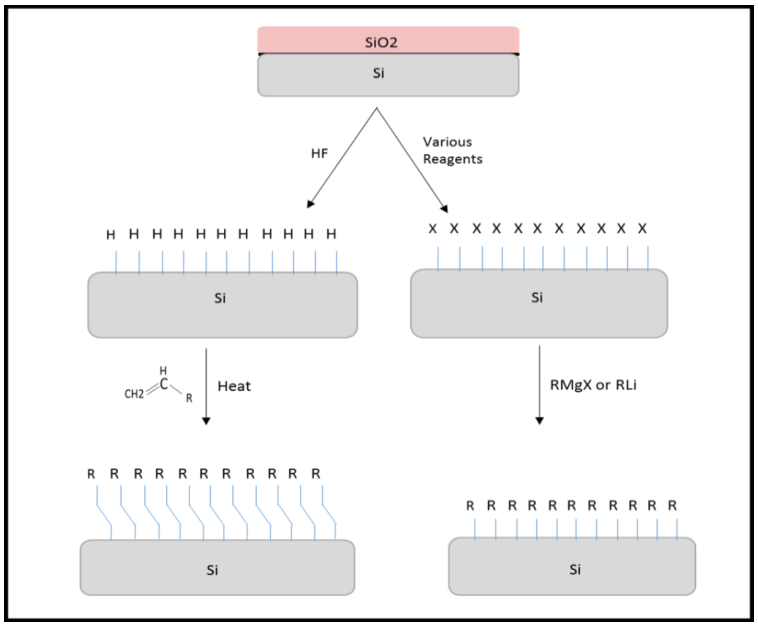


Figure 6.2: Schematic representation of monolayer formation on silicon using two methods. [21]

The surface was cleaned prior to the hydrosilylation reaction, the native oxide was etched off the Si surface using HF or NH4F to create hydrogen-terminated surface. The Si substrate was submerged into the aqueous solution of dopant containing organic compound usually an alkene. The reaction was initiated either by thermal treatment or by irradiation of light; the mechanism to form radical using dopant containing chemistry and hydrogen-terminated silicon initiated by thermal treatment is shown in Figure 6.3. The reaction propagates until the densely packed monolayer is formed.

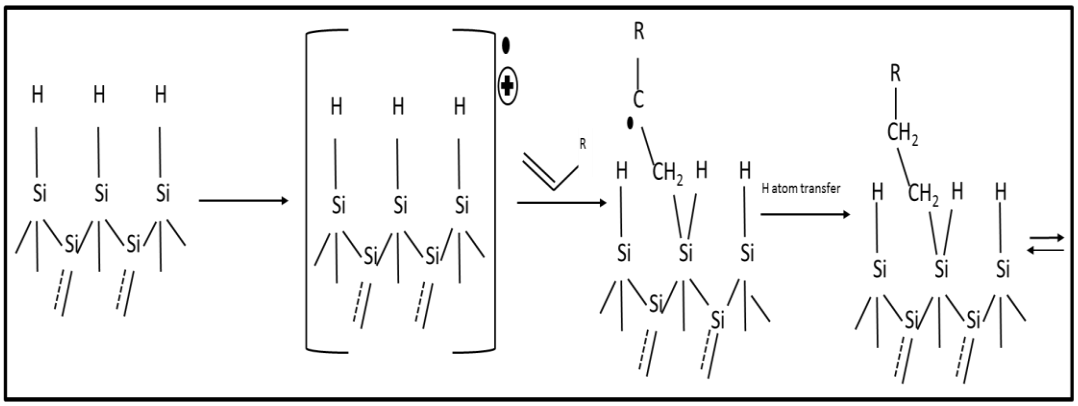


Figure 6.3: Radical chain reaction initiated by thermal conditions on silicon substrate. [21]

6.2 Chemistry Preparation

MLD is dependent on hydrosilylation mechanism to bind the dopant-containing chemical to the hydrogen-terminated surface of silicon substrate; the chemical needs to have at least one dopant atom attached to it. The commonly used Boron source for p-type doping is Allyl boronic acid Pinnacol ester (ABAPE). The n-type phosphorous dopant sources commonly used are diethyl vinyl phosphonate (DVP) and diethyl 1-propylphosphonate (DPP), the chemical formulas are seen in Figure 6.4. The dopant-containing adsorbate usually contains alkene or alkyne but DPP lacks that and still has demonstrated to function as phosphorous source. It seems plausible that DPP forms monolayer using adsorption on the surface of hydrogen terminated silicon. The preparation of chemistry was done in the glove bag, which was filled with inert gas argon or nitrogen. All the glassware used, were cleaned and thermally dried using torch so that water evaporates. The weighing scale, gloves, pipettes, wipes and chemicals were kept inside the glove bag, followed by sealing it. The glove bag was deflated using vacuum pump attached to pipe on one side of the bag , once deflated inert gas is filled in from the other side of the bag, this process was repeated three

times to ensure the environment was inert and no oxygen was present in the glove bag. The inert gas was partially filled the third time in order to give some space to work effortlessly.

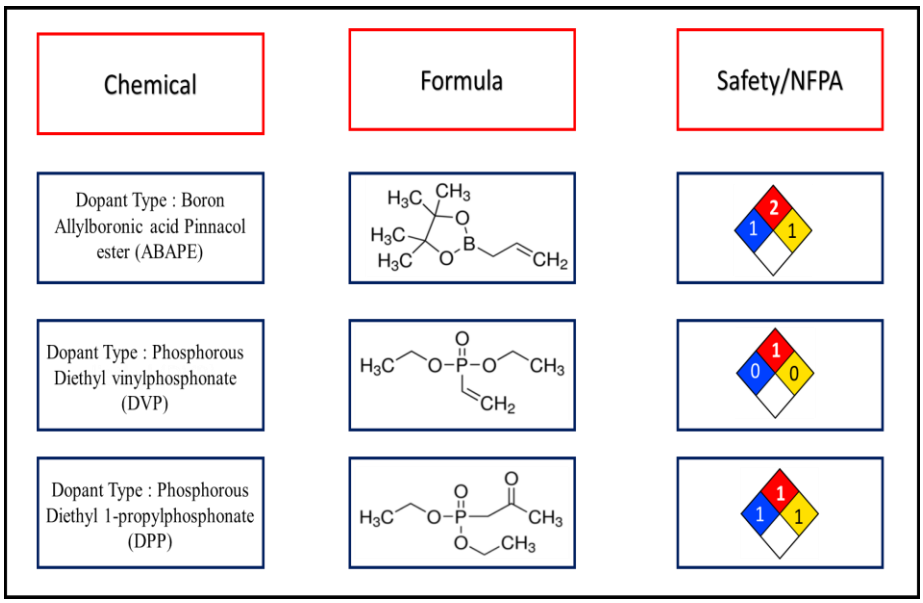


Figure 6.4: Dopant containing adsorbate with their chemical formula and NFPA safety data

Figure 6.5: Glove bag sealed and partially filled with inert gas

The dopant-containing chemical was mixed with Mesitylene that was used as solvent to increase the volume of the total chemistry, both the chemicals were mixed in 1:25 ratio volume by volume

(v/v). After the chemistry was prepared the flask was covered with Para-film and the bag was deflated. The mixed chemistry was sparged for twenty minutes with inert gas; it was the process by which insert gas was bubbled into the chemistry. This serves two purposes; first it ensures that the chemistry remians oxygen free and also keeps inert gas in the remainder of the test tube keeping oxygen out of the ambient.

6.3 Setup Description

The reaction between silicon substrate and mixed chemistry can be slow and might take a long time for any visible response to occur so heating was used to increase the rate of reaction and thus decrease the time of reaction. The temperature for the chemistry used for the experiment conducted was 120-170^{o}C.

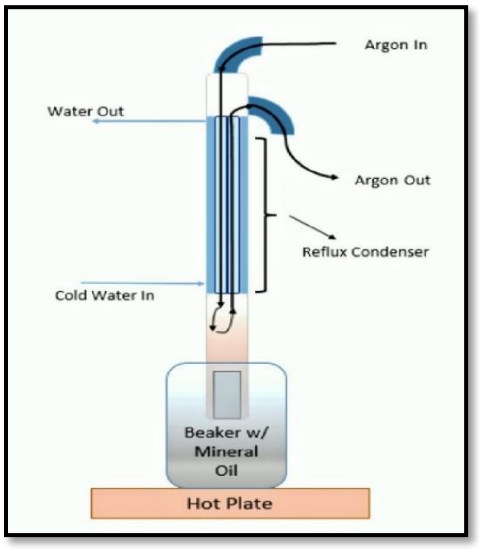


Figure 6.6: Set up requirement for MLD experiment

However, organic compounds with low boiling point when exposed to heat will evaporate and will result in incomplete reaction. The boiling point of Mesitylene and DPP are 164.7^{o}C and 94^{o}C respectively. Therefore, reflux system was used to prevent losing the chemistry, the reflux

technique was used to condensate the vapors formed back into the system. The reflux system has two parts, it is wrapped with a jacket for cold water to flow through this allows for any vapors from the mixture to be condensed back, keeping the solution in steady state. All the chemistry preparation and reaction were carried out under argon to ensure oxygen-free environment, so that silicon does not form any native oxide on the surface and monolayer is successfully formed. The reflux system serves to bring argon into and out of the system making sure the ambient remains inert. The setup for MLD reaction on silicon pieces is shown in Figure 6.7.

Figure 6.7: Apparatus for MLD on silicon pieces

6.4 Apparatus Design for 6-inch Wafer

The apparatus designed earlier could only fit silicon pieces to do MLD, new design idea was required to hold 6-inch wafer. The container requirements were as following, it should withstand high temperature, resistant to chemicals used, should be able to attach a reflux system to it and minimum chemistry volume should be used in order to keep the cost low. The container

used is shown in Figure 6.8, it is made from aluminum and therefore can withstand the high temperature and is chemically resistant to mesitylene-based chemistry. The container would hold wafer horizontally and would require about 200mL of total chemistry to fully submerge one wafer.

Figure 6.8: Vessel for wafers to perform MLD

Figure 6.9: PLA printed sleeve for glass joint

The reflux condenser which serves dual purpose of condensing the chemical vapors and providing ambient inert atmosphere to the entire system was made of glass joints and a connector was required to join it with aluminum container. The glass connectors could not be used as they are easily breakable, therefore 3D printing was used to solve this problem. A sleeve was designed and printed as a prototype to ensure the correct sizing and fit with standard 3D printing filament

polylatic acid (PLA) as seen in Figure 6.9, the sleeve printed using the PLA filament cannot be a long-term solution as it was unable to withstand temperature and chemicals.

Nylon has higher mechanical strength and superior resistance to organic chemicals and can be used to replace PLA filament. In Figure 6.10, the nylon sleeve printed using 3D printer and implanted into the system design to check its feasibility.

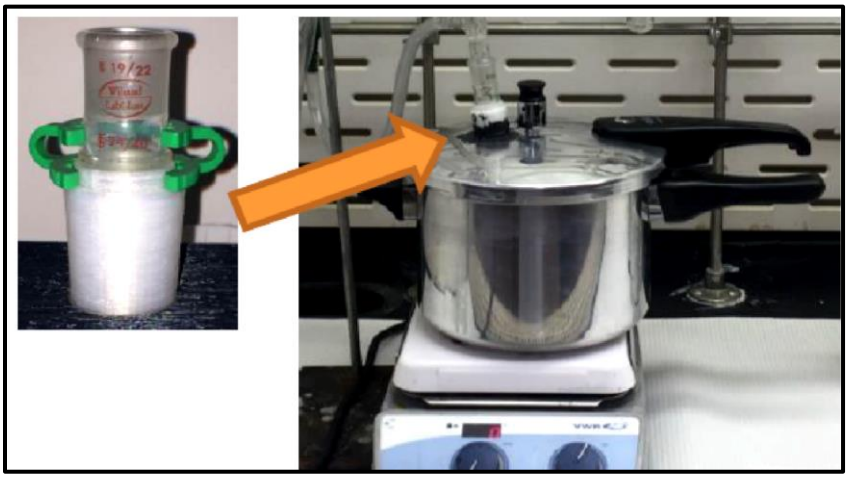


Figure 6.10: Nylon sleeve print and implementation on MLD apparatus

Several test runs were done on the new MLD apparatus for 6-inch wafer with both water and chemistry. Leaks were discovered around the top of the container since the seal inside the container could not withstand the temperature and expanded, it was replaced with room temperature vulcanized (RTV) silicon which solved the problem. The leaks in system were examined using glass slide, if observed RTV paste was used from time to time to avoid any leaks in the system. The apparatus designed was a low cost, uses minimum volume of chemistry and fulfills all the requirements for the system to successfully perform MLD on 6-inch wafers. The container was able to withstand temperature and chemical, inert gas ambient in the chamber and vapors are condensed, to ensure minimum loss of chemistry.

Figure 6.11: 6inch setup for MLD

6.5 Monolayer Doping Process Flow

The process flow to achieve monolayer doping is described in this section, the technique involves formation of dopant containing monolayer on the surface of the substrate, followed by deposition of capping layer to ensure no loss of dopant during thermal heating. Subsequently, the substrate was annealed to diffuse dopants and form junction. The native layer of silicon dioxide (SiO2) was etched using 10:1 BOE for 10 sec to form hydrogen terminated silicon surface. The samples were then immediately transferred in dopant containing chemistry. The samples were reacted with diethyl 1-propylphosphonate (DPP) which is a phosphorous dopant source and mesitylene as solvent for 2.5 hours at 170^{o}C. All the reactions were carried under argon medium to ensure oxygen free environment. After the reaction was completed the chemistry was left to cool down. The samples were cleaned using Toluene, Acetone, Methanol and DI water in the given order to remove any physisorbed material on the surface of silicon.

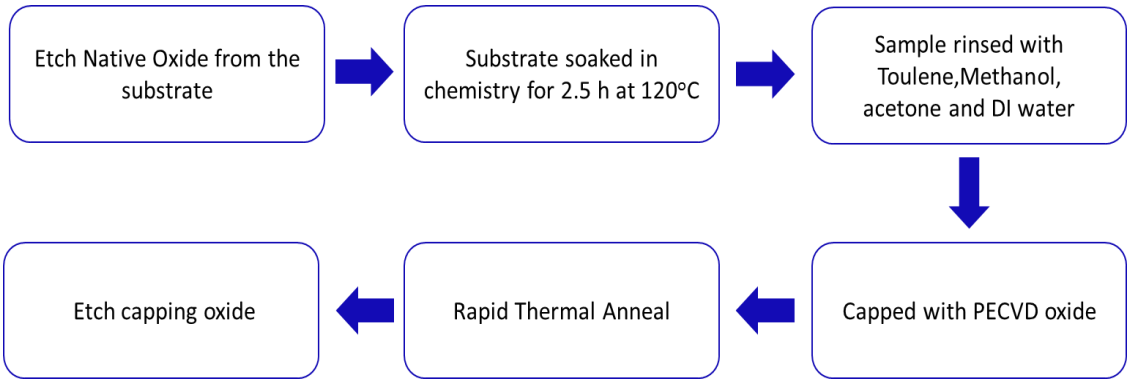


Figure 6.12: Complete steps to achieve doping through MLD

The samples were capped with SiO2 using Plasma enhanced chemical vapor deposition (PECVD), which involves deposition of thin film from gas/vapor phase to solid state on the surface of the substrate. The precursor used to deposit SiO2 is tetraethylorthosilicate (TEOS) for plasma-enhanced deposition. The capping layer ensures that there was no loss of the dopant molecules into surrounding during anneal. The thermal process was used to diffuse the dopant adsorbate molecule. Finally, the capping oxide was etched using BOE to achieve desired junction and diffusion profile using MLD.

6.5.1 Annealing

The dopants were diffused in silicon with thermal process, the junction depth and diffusion profile of the dopants is dependent on annealing time and temperature. The solid solubility and diffusivity increase with temperature. In Figure 6.13, the advanced annealing techniques and their dependence on temperature and drive in time are described. As the temperature increases the dopant activation increases, whereas the decrease in anneal time results in less diffusion of dopants. The ultra-shallow junction is achieved by annealing for short time at high temperature so as to avoid the dopant being driven deep into the substrate.

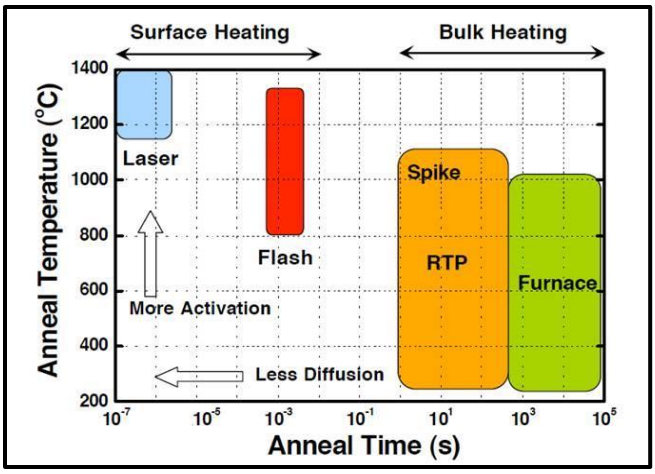


Figure 6.13: Advanced annealing techniques

The laser and flash annealing technique having higher temperature ramping rate and could be used to achieve ultra-shallow junction. However, at high temperature the melting and recrystallization of capping layer makes these techniques less favorable. Rapid thermal anneal was used to diffuse dopants into the silicon substrate for the purpose of our experiment. The samples were annealed at 1000ºC for 5 min in nitrogen ambient in AG 610A RTP. To understand the change in doping profile with change in annealing conditions a temperature and time study was done.

6.6 Double MLD

In order to study more about MLD, experiments were conducted in order to understand the effect of more than one MLD on the dose and surface concentration. In Figure 6.14 the process flow for double MLD is described, native oxide was etched from the surface of silicon followed by MLD1 and cleaning. The surface of silicon was capped with oxide and substrate was annealed for dopant to diffuse in the surface. Subsequently the capping oxide was etched and sheet resistance was measured to make sure MLD1 was successful. The complete process was again repeated to achieve second MLD.

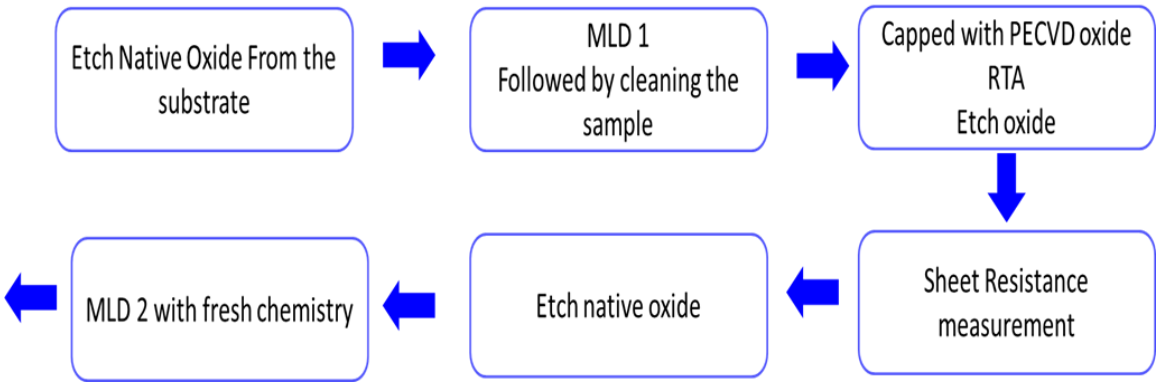


Figure 6.14: Steps to perform double MLD

The dose is dependent on the number of bonds between silicon and dopant containing chemistry and amount of dopant diffused in the substrate, which in turn is dependent on annealing conditions. If <100> silicon was used for the purpose of experimentation. The maximum number of silicon atoms on the surface is given by following equation 6.1 where the number of atoms/plane will be 2 since for <100> planes are mutually perpendicular to each other and a is lattice constant.

$$\rho_{(100)} = \frac{\#\frac{atom}{plane}}{a^2} \tag{6.1}$$

Therefore the maximum dose for <100> plane silicon is

$$\rho_{(100)} = 6.78 * 10^{14}\ \frac{atoms}{cm^2}$$

Chapter 7

Results from MLD Diffused Layer

In this chapter, the results obtained from elemental and electrical characterization of MLD diffused layer are discussed.

7.1 AES and XPS for Elemental Characterization

The surface of monolayer sample was characterized using AES and XPS for successful covalent bond formation. The samples were analyzed using AES after the reaction between DPP and hydrogen terminated silicon. The samples were analyzed without etching and silicon, carbon and native oxide were detected. After etching the sample for 1 min phosphorous, silicon carbide, silicon and silicon dioxide were detected as seen in Figure 7.1. The carbon to phosphorous ratio is 6:1 similar to ratio of these elements present in DPP.

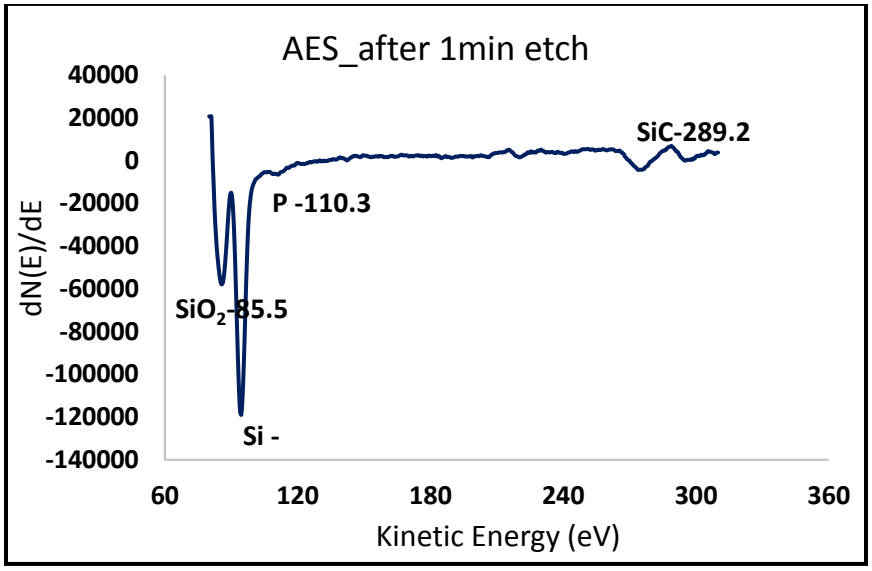


Figure 7.1: AES of MLD sample

To confirm the presence of small phosphorous in the sample XPS measurement was performed on the same sample. As seen in Figure 7.2, phosphorous peak is observed at 131.5 eV binding energy. Silicon, silicon carbide, and carbon are also detected similar to the AES results.

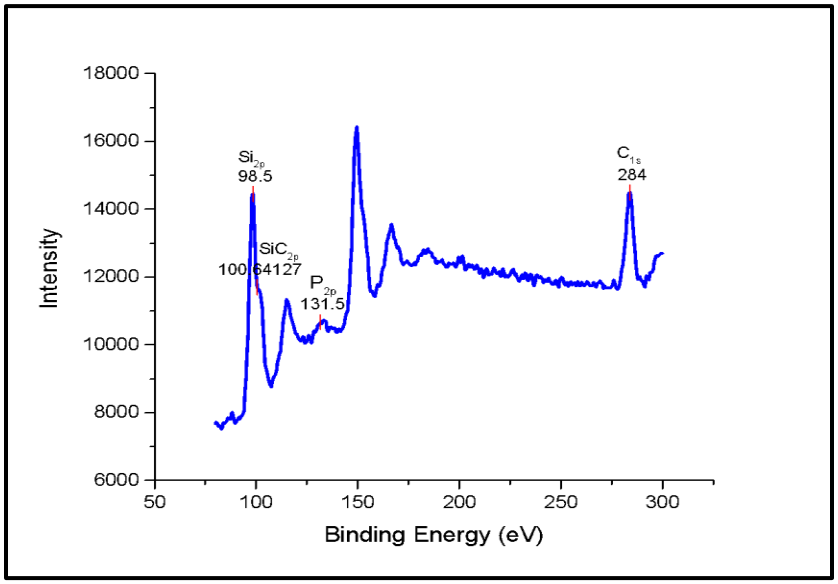


Figure 7.2: XPS of MLD sample

7.2 Doping Profile Characterization

Secondary ion mass spectroscopy (SIMS) measurements was used to characterize the doping profile of the thermally diffused phosphorous atoms. The silicon sample measured were reacted with dopant containing chemistry to form monolayer, followed by the deposition of 50nm of capping TEOS layer and anneal to diffuse the dopant into the substrate. In Figure 7.3, the doping profile of phosphorous in silicon, which was annealed at 1000oC for 5 min in RTA system, is shown. The surface concentration is 3 x 10^{20} cm^{-3} that sharply decreases to 10^{18} cm^{-3} at 26 nm depths. The kink and tail feature is observed due to lower diffusivity of P at higher concentration, which is also observed in conventional doping techniques.

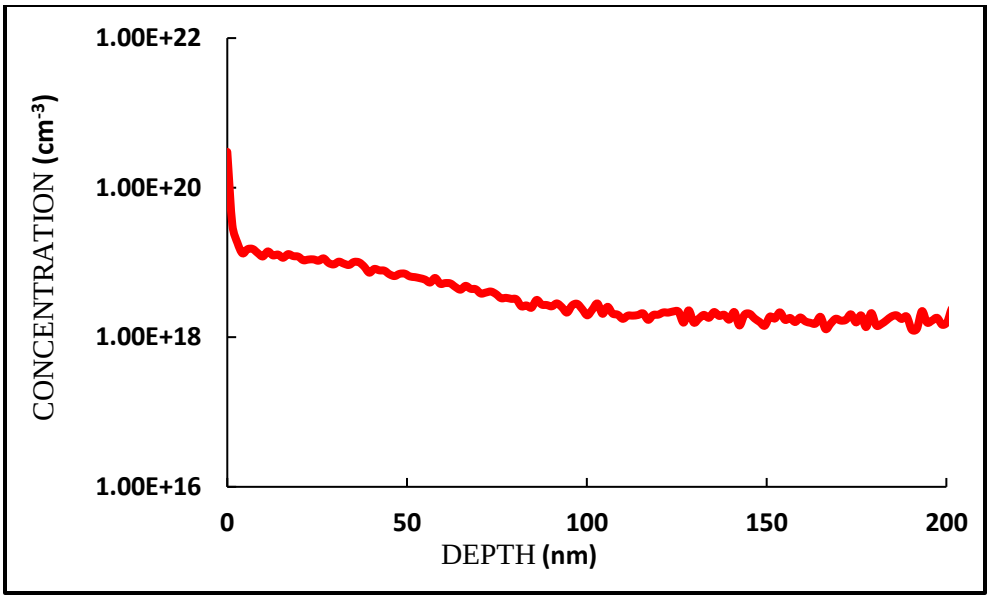


Figure 7.3: SIMS on MLD processed sample

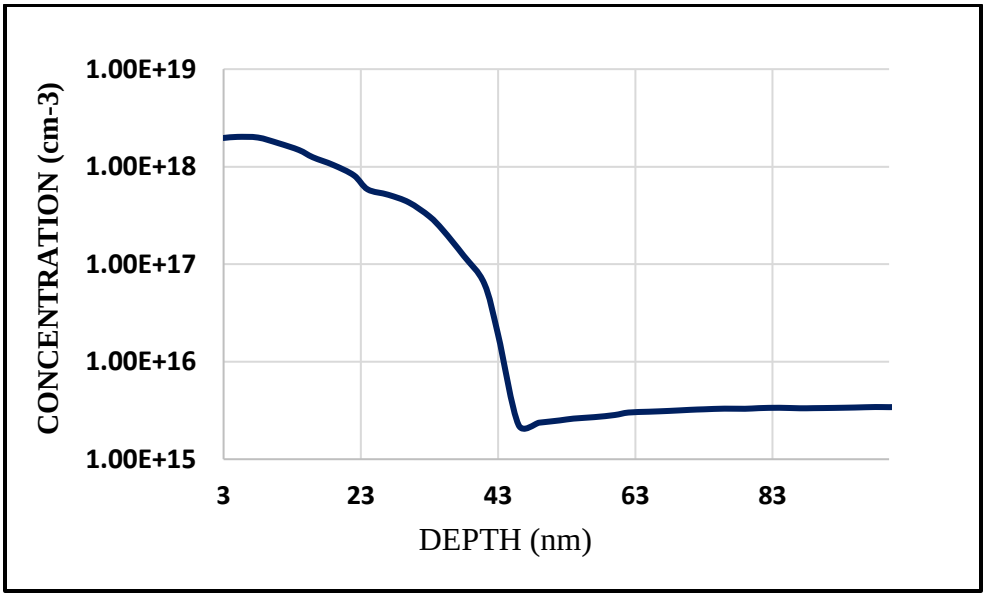


Figure 7.4: Spreading resistance profile of phosphorous doped p type silicon using MLD

The active dopant concentration and junction depth from spreading resistance profiling is 2.5 x 10^{18} cm^{-3} and 45 nm with substrate doping 2 x 10^{15} cm^{-3}respectively as shown in Figure 7.4. The dose calculated from the data is 1.12 x 10^{13} cm^{-2}. The maximum dose obtained from one MLD

can be 6.7 x 10^{14} cm^{-2} as discussed in chapter 6. The limitation of SRP technique is that a bevel of typically 0.1 or 0.05 µm deep on the surface was created for measurement, this result in active dopant present on surface not accounted in calculation.

In Table 4, the comparison between calculated parameters from SIMS profile and experimental parameters from SRP are compared. N–type Gaussian Irvin curve was used to determine the junction depth of 50 nm using surface concentration 10^{20} cm^{-3} from SIMS profile and sheet resistance 1000 Ω/sq . The dose for the profile is calculated from SIMS data is 4.5 x 10^{14} cm^{-2}. It is observed that not all dopant was activated during thermal anneal.

Table 4: Comparison between calculated and experimental diffusion profile parameters

	Calculated/SIMS	Experimental/SRP
Dopant Concentration (cm^{-3})	10^{20}	2.5 x 10^{18}
Junction Depth (nm)	45	47
Dose (cm^{-2})	4.5 x 10^{13}	1.2 x 10^{13}

The container and process developed to dope a 6-inch wafer, as discussed in chapter 6 was characterized using SIMS. Leaks were observed around the top of the container during the first run due to seal that was incompatible with chemistry and couldn't withstand the temperature. The seal was replaced using RTV, many experiments have been successfully conducted after the leak in the first run. The doping profiles were measured using SIMS as shown in Figure 7.4 for 6-inch wafer and piece that were both annealed at 1000ºC for 5 minutes. For the 6-inch sample, discrepancy is observed for first 30 nm which can be attributed to SIMS artifact is was observed on the surface, other than that the profile is very similar to MLD processed silicon piece.

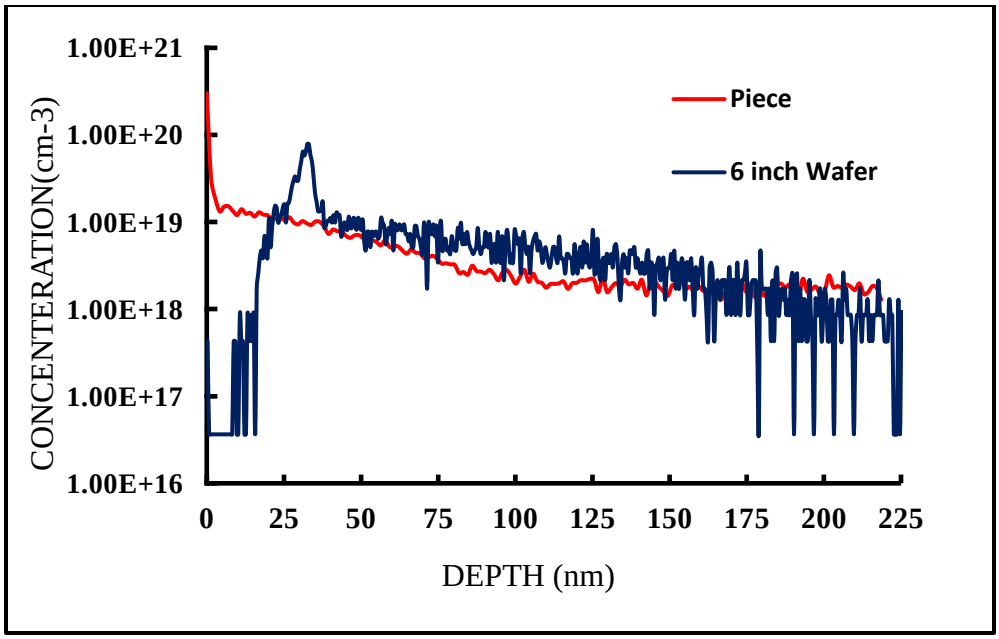


Figure 7.5: SIMS data comparison between 6-inch wafer and silicon piece

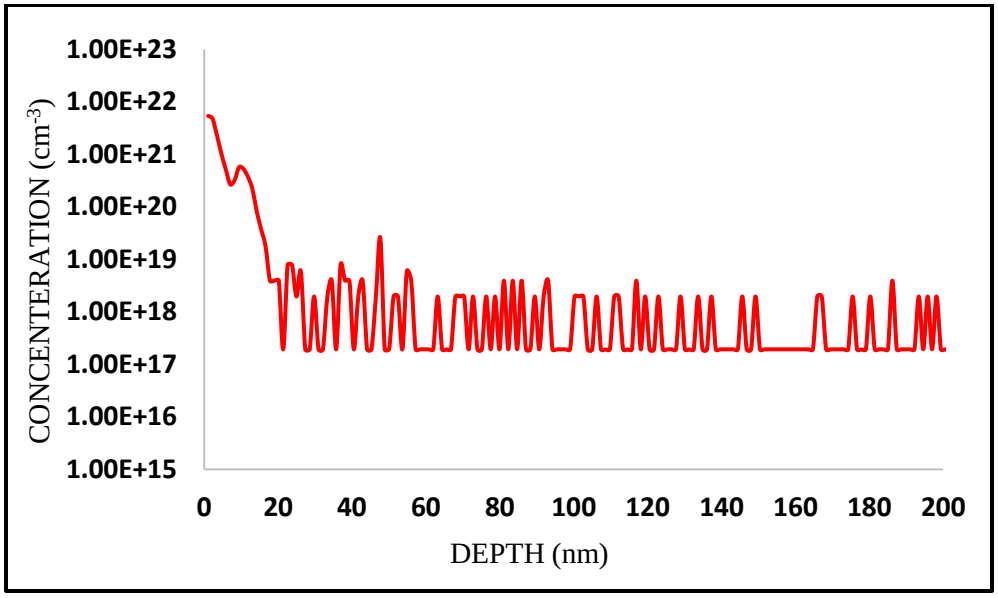


Figure 7.6: SIMS data for double MLD sample

The double MLD was used to introduce more dopant into the substrate, and increase the dose. The silicon sample was doped using double MLD as per the process discussed in chapter 6. SIMS was used to characterize the doping profile; the surface concentration is 5.6 x 10^{21} cm^{-3}, which is higher

than the concentration from single MLD as shown in Figure 7.6. Discrepancy and noise was observed until 25 nm due to the sensitivity of the tool.

7.4 Sheet Resistance

To further characterize the MLD samples, four point probe measurements were done to obtain the sheet resistance.

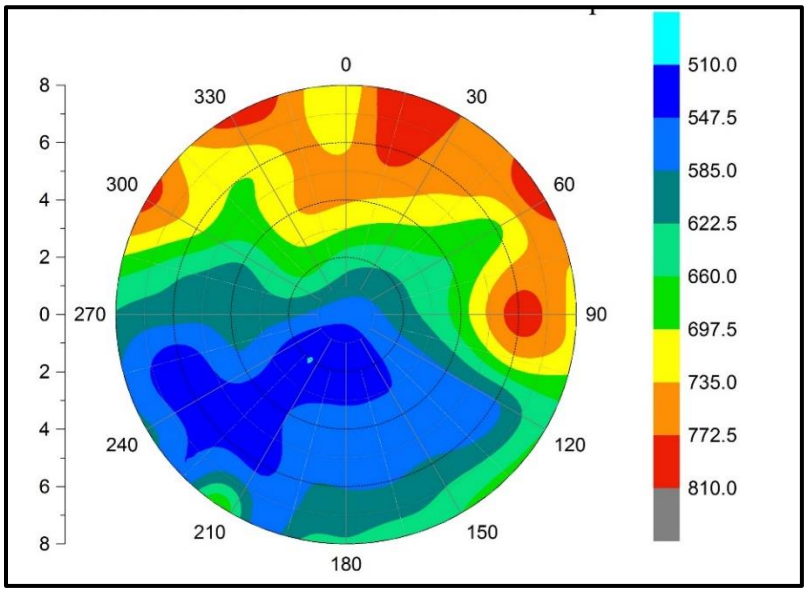


Figure 7.7: Sheet resistance contour map of 6-inch wafer

The sheet resistance contour map for 6-inch wafer is shown in Figure 7.7, it was observed that near the notch of the wafer the sheet resistance was higher as compared to rest of the wafer, the plausible reason for the non-uniformity were the leaks encountered during processing and change in cleaning process. The wafer was held using tweezer and toluene, acetone and methanol was sprayed around the wafer, rather than dumps and rinse strategy used for silicon pieces so far. The issue with leak was resolved using RTV and the wafer were dump rinsed during cleaning process, it was observed that the sheet resistance was uniform across the wafer with standard deviation of 4% as shown in

Figure 7.8. In Table 5, the average sheet resistance of single and double MLD of the 6-inch wafer and the silicon piece sample were compared.

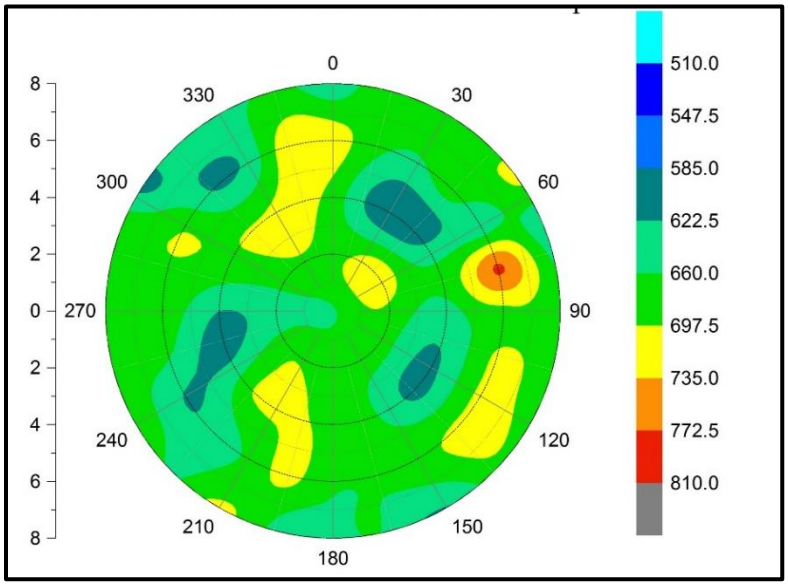


Figure 7.8: Sheet resistance contour map after resolving issues with leak and cleaning process.

Table 5: Sheet resistance for various MLD cases

	Single MLD	Double MLD
Piece (Ω/sq)	962	655
Wafer (Ω/sq)	1126	670

7.5 Anneal Time and Temperature Study

Once the setup for doping 6-inch wafer was successfully implemented, various experiments could have been possible. This study involved measuring the sheet resistance by varying the anneal time and temperature conditions to understand the effect. After the monolayer was formed and capping oxide was deposited on the samples, they were treated at three

temperatures 900ºC, 1000ºc and 1100ºC for 1 min, 3 min and 5 min respectively followed by etching capping oxide and measuring sheet resistance. As shown in Figure 7.9, the sheet resistance is very high due to the incomplete activation of phosphorous, whereas at higher temperature and longer diffusion time the junction depth and activation both increase, thus decreasing the sheet resistance value. Similar experiments were conducted by Ho et al [1], and sheet resistance followed a similar trend as shown in Figure 7.10.

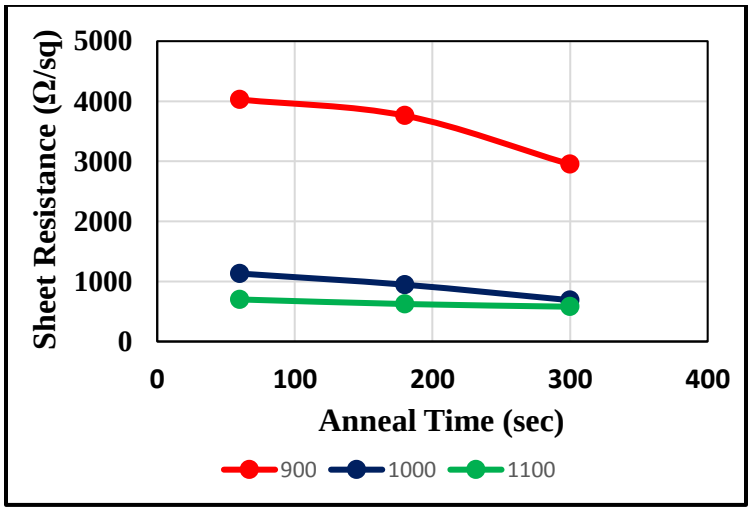


Figure 7.9: Sheet Resistance versus anneal time and temperature

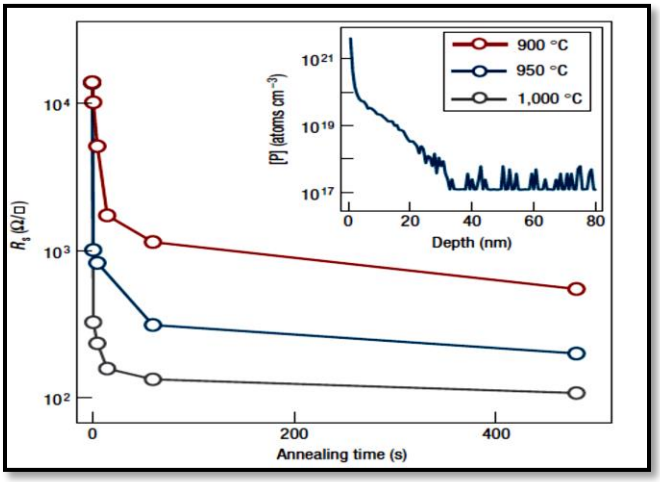


Figure 7.10: Sheet resistance versus annealing temperature. [1]

Chapter 8

Device Fabrication and Electrical Characterization

In this chapter, the process flow to fabricate diode and contact resistivity structures and results obtained through electrical testing are discussed.

8.1 Diode and TLM Fabrication

Diode and Transmission Line Structures were fabricated using photolithography, etch, deposition and thermal process. The predefined levels for photolithography were MESA isolation, contact cut and metal. The N+ region was formed using double MLD process on p-type silicon substrate of base resistivity 7 Ω-cm. The sheet resistance measured after double MLD and rapid thermal anneal for 5 min at 1000^{o}C was 670 Ω/sq. ASML was used to form MESA isolation lithography pattern followed by etching using LAM 490 as shown in Figure 8.1.

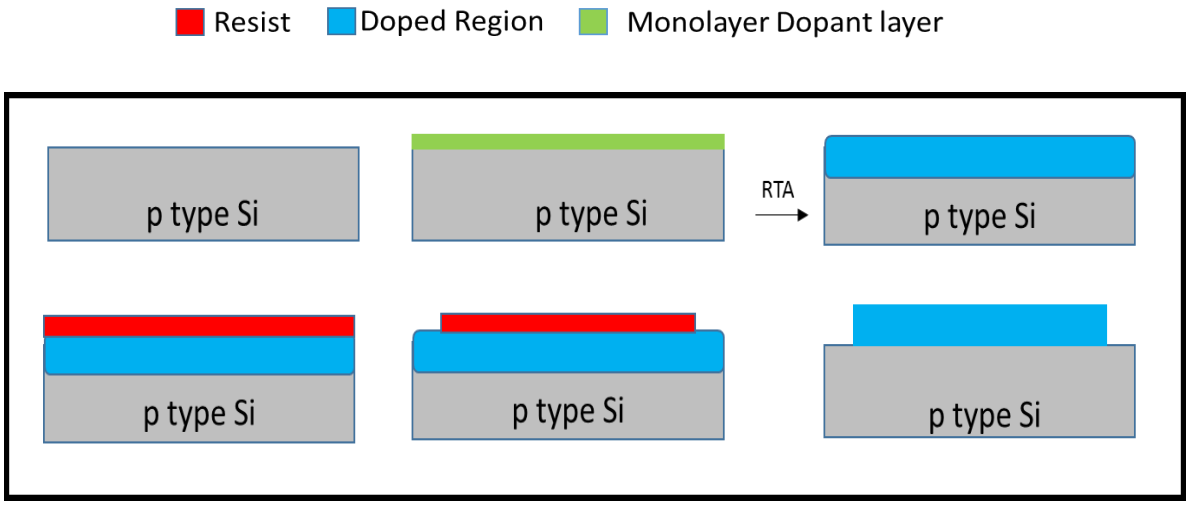


Figure 8.1: Process flow for patterning of the monolayer using MESA isolation

Further, insulating PECVD oxide was deposited using P5000 that was patterned to form contact cuts. NiSi contacts were formed using two step self-aligned process discussed in section 8.2,

Aluminum was sputter deposited in PE4400, ASML was used to pattern and followed by etching in LAM 4600 Rainbow etcher to form contact with the bond pads. The TLM pattern fabricated have variable width ranging from 10 μm – 2000 μm, the length of all the TLM structures were 10 μm.There were two different size of diode 520 μm x 520 μm and 118 μm x 128 μm which were fabricated using the same mask and levels as TLM structure [16]. The schematic of fabrication process is described in Figure 8.2.

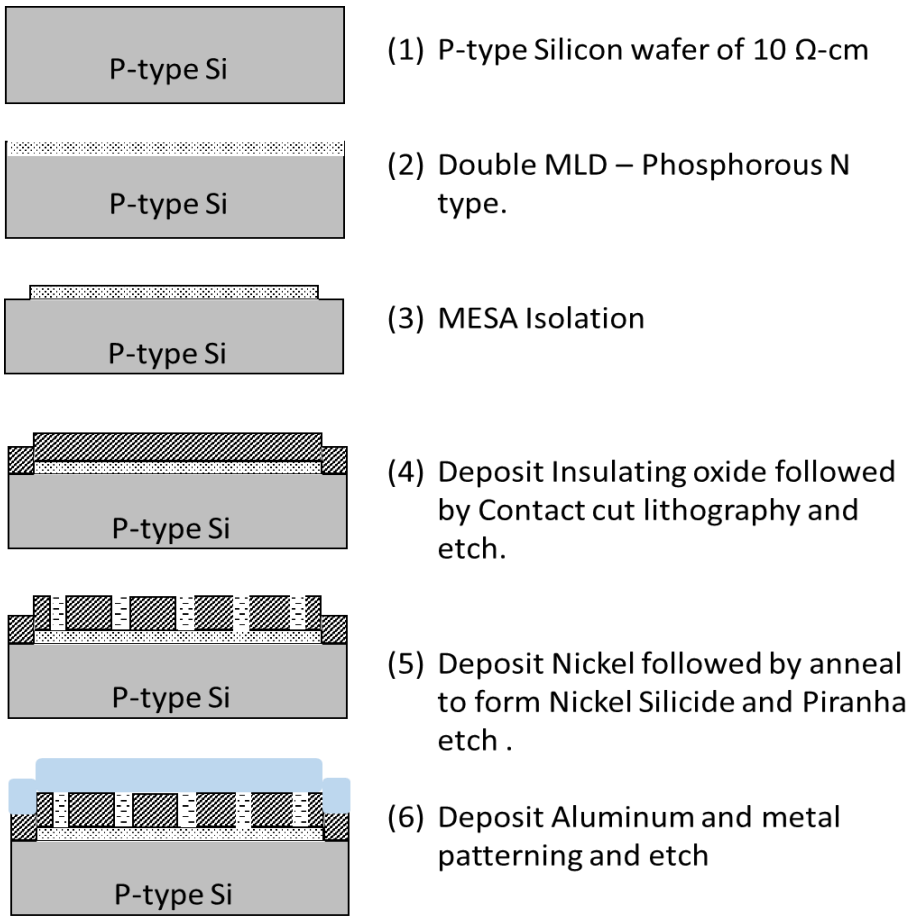


Figure 8.2: Diode and TLM fabrication process flow

8.2 Self- aligned Silicide (SALICIDE) and NiSi Technology

Self-aligned silicide technology was developed to reduce the parasitic resistance which helps to lower the resistance in gate, source and drain areas in modern MOS transistors. The performance of the transistor is improved as it forms a low contact resistance contact without the need of additional lithographic step as it simultaneously forms silicide at source/drain and gate region of transistor. Transition metal layer is deposited followed by annealing which results in reaction in metal being reacted with silicon to form silicide. The annealing is performed at low temperature to avoid formation of silicon bridges that might cause electrical shorts, further the unreacted metal is etched. Finally a high temperature anneal is performed to achieve desired low resistivity silicide. Titanium, Cobalt and Nickel are some metal that form silicide, they have low resistivity, good adhesion to silicon and when silicon is heavily doped they have low Schottky barrier.

The Ni/Si phase formation sequence is complicated; it can form up to 11 phases with 8 phases stable at room temperature. The phase formation is dependent on multiple factors like processing parameters, dopant type, dopant concentration and cleaning conditions. The low resistivity NiSi is formed at low temperature due to its higher concentration and diffusivity and therefore the process to form NiSi is diffusion controlled. In this study, 7 nm thick nickel was sputter deposited using PE4400 followed by rapid thermal anneal at 550^{o}C for 1 minute to form nickel silicide. The unreacted nickel is etched using piranha solution at 90^{o}C.

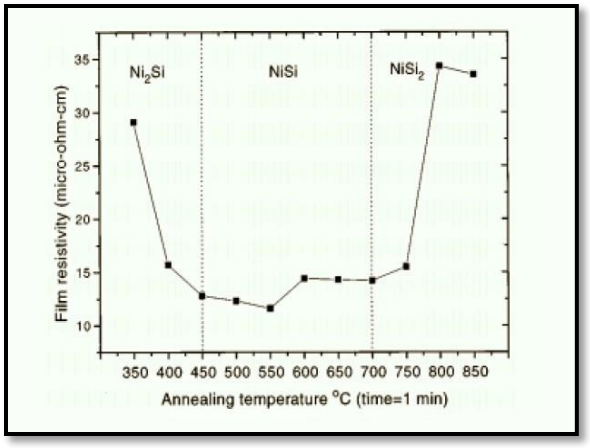


Figure 8.3: Film resistivity of NiSi versus annealing temperature. [19]

8.3 Electrical Testing

The fabricated devices were tested using the ICS metrics software and HP4145 semiconductor parameter analyzer. The diodes were tested using manual station with 2-point probe I-V measurement out by sweeping voltage from -1 to 1Volts and measuring the current across the diode. The TLM structures were measured using automated station using 4-point probe I-V measurements to reduce errors in resistance measurement. I-V curves for TLM structures with different width were generated, which were used to extract transfer length and specific contact resistivity.

8.4 I-V Characteristics and Analysis

The diodes were fabricated using the steps described in chapter 6, the N+P junction was formed using monolayer followed by contact formation and 5 nm nickel was deposited. Annealing at 550^{o}C for 1 minute formed the nickel silicide. Further, metal was deposited, patterned and etched. The current-voltage characteristics were measured in forward bias as shown in Figure 8.4.

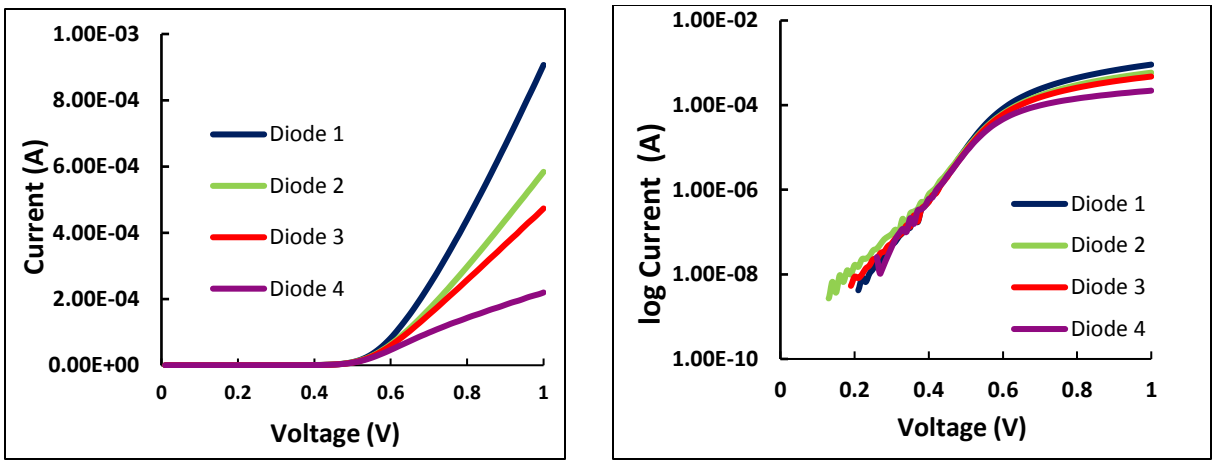


Figure 8.4: I-V in forward bias characteristic in linear and log scale.

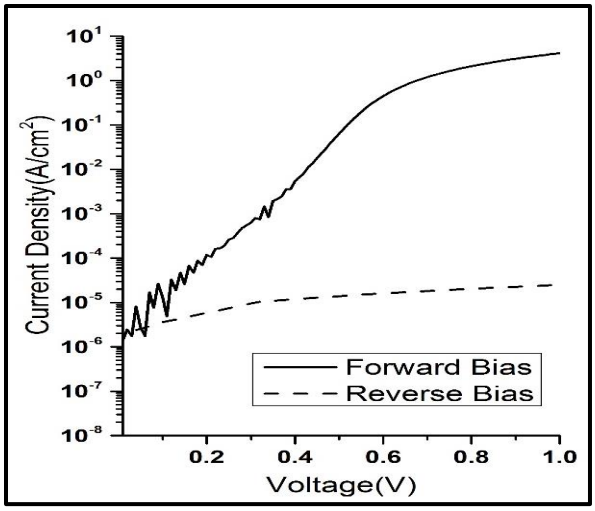


Figure 8.5: J-V characteristics in forward and reverse bias

In Figure 8.5, the forward and reverse bias current density versus voltage characteristics of a diode with area of N+ contact was 118 µm x 120 µm, whereas the backside of the substrate was used as P side contact is shown. In reverse bias it is observed that the current changes so slowly with the voltage. The depletion region current increases with the reverse bias which follows an approximate $-V^{1/2}$ relationship. The heavily doped N + abrupt junction was fabricated on p type substrate with resistivity 13 Ω-cm and acceptor density 2 x 10^{15} cm^{-3}. The built-in voltage is

calculated using equation 5.1 is 0.901V.In Table 6, the constants and parameters which were used in diode analysis are given.

Table 6: Constants used in diode analysis

Constants	Value	Units
Intrinsic Concentration (n_i)	1.5×10^{10}	cm^{-3}
Boltzmann Constant (k)	8.617×10^{-5}	eV/K
Temperature (T)	300	K
Electron Mobility ($\mu_{n)}$	1370	cm^2/V-s
Hole Mobility ($\mu_{p)}$	408	cm^2/V-s
Area	1.4×10^{-4}	cm^2
Acceptor Doping Density(N_A)	1×10^{15}	cm^{-3}

It is observed that the depletion region current dominates at low bias since space charge current (I_{SNR}) is higher than quasi neutral region current (I_{QNR}). The ideality factor for quasi neutral region at 0.28 V and space charge region at 0.41 V is 1.57 and 2.16 respectively. In Figure 8.5 the exponential of QNR and SCR current for varying forward bias voltage is calculated using equation 7.3 and 7.4, and plotted along with the experimental data. The forward biased I-V characteristics is plotted in semi-log current and linear voltage scale, the three different regions can be distinguished from our plot, first depletion region recombination where the current is dominated by recombination effects in the depletion region, the ideality factor is close to two. The second region is ideal diode; the current increases one order magnitude when voltage is increased by 90 mV. High injection level effects and series resistance dominates the third region current. It is observed that the effect of series resistance is very high and therefore the region with ideality factor 1 is small.

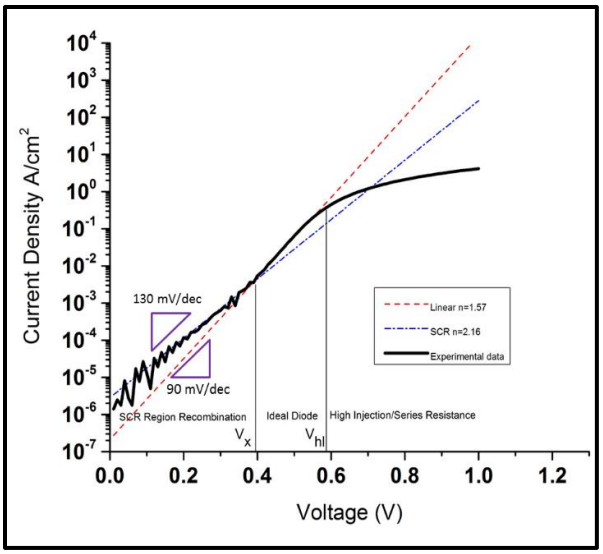


Figure 8.6: log J-V characteristics analysis for N+P diodes

The voltage at which the QNR and SCR current intersect is Vx, and it used to determine the minority carrier lifetime of the diode. The width of the ideal diode region can be found from the difference of high injection voltage region and intersection of SCR and QNR current voltage Vx. The width depends on the base doping and minority charge carrier.

$$At\ V_x \quad J_{SCR} = J_{QNR}$$

$$V_x = 0.05\sqrt{\frac{N_A * 3.08 * 10^{-14}}{\mu_n \tau_n} ln\frac{N_A}{10}} \tag{8.1}$$

$$V_{hl} - V_x = \frac{2kT}{q} ln\left(\frac{N_A}{n_i}\right) - \frac{2kT}{q} ln\left[\frac{1}{2n_i}\left(\frac{N_A}{L_n}\right)\sqrt{\frac{2\varepsilon_s}{qN_A}\frac{kT}{q} ln\frac{N_A}{10}}\right] \tag{8.2}$$

$$V_{hl} - V_x = 0.05\ ln\frac{5.5 * 10^{-4}\sqrt{\mu_n \tau_n}}{\sqrt{\frac{1}{N_A} ln\frac{N_A}{10}}} \tag{8.3}$$

The minority carrier lifetime is calculated using equation 6.30, the intersection voltage when SCR is equal to QNR current is 0.392 V and is used to calculate minority carrier lifetime (τ_n) 0.12 µs. The high level injection initiates at 0.6 V calculated using equation 6.9.

8.5 Experimental and Unified Model

The current density - voltage characteristics at low level and high level injection using the experimental data obtained from analysis of N+P diode were calculated and analyzed together. The unified model combines the low injection, medium injection and high injection levels of I-V characteristics in one equation. In Figure 8.8, the comparison between the experimental and data calculated using unified model is shown. The J-V characteristics using unified model were calculated using equation 5.15 and 5.16, the series resistance component of 580 Ω is added into the plot generated from unified model and similar bending as the experimental data is observed.

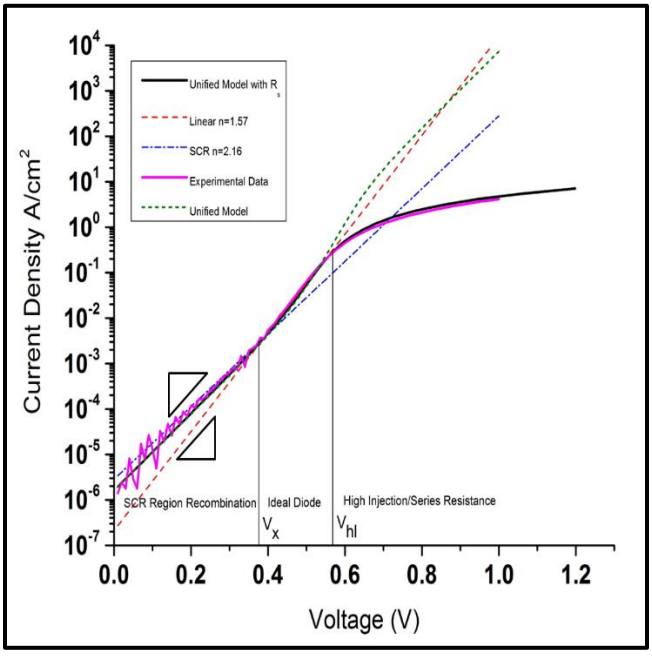


Figure 8.8: J-V characteristics of experimental data, unified model and with series resistance

Table 7: Experimental/Calculated parameters for Diode Analysis

Parameters	Experimental /Calculated	Units
n_1	1.57	
n_2	2.16	
D_n	35.4	cm^2/s
Ln	20.2	μm
τ_n	1.15×10^{-07}	s
V_x	0.38	V
V_{hl}	0.56	V
J_{QNR}	2×10^{-07}	A
J_{SCR}	3×10^{-6}	A
Rs	588	Ω

8.6 Specific Contact Resistivity of MLD and Implanted TLM Structure

TLM measurements were performed on MLD diffused regions and phosphorous implant wafers with NiSi contacts and Al metallization. The dose for the phosphorous implant was 2×10^{13} cm^{-2} which is comparable to MLD dose and was annealed for 30 min at 900ºC.The measurements were performed for constant length 10μm and varying width ranging from 10μm - 350μm TLM structures. Lumped Circuit Model was used to determine specific contact resistivity, the resistance was calculated at varying spacing and transfer length was determined from the equation 7.21. The sheet resistance, transfer length, contact resistance and specific contact resistance are shown in Table 8. The sheet resistance of the N+ diffused region for MLD and implanted wafer were 670.46 Ω/sq and 55 Ω/sq, which is comparable to the sheet resistance obtained by TLM measurement.

For the particular specific contact resistivity and sheet resistance there is optimum value of TLM structure width that would provide least systematic error. The optimum width for the sheet resistance 600 Ω/sq and specific contact resistivity 10^{-6} Ω-cm^2 is 88 µm, calculated using equation 7.24 and δW and δR is 1.5 µm and 0.2 Ω respectively.

The specific contact resistivity of TLM structures doped with phosphorous implant and NiSi contacts is 2 x 10^{-4} Ω-cm^2 whereas the MLD doped structure has lower specific contact resistivity 3 x 10^{-5} Ω-cm^2.

Table 8: Comparison between TLM structures measurement of MLD and implant wafer.

	Sheet Resistance (Ω/sq)	**Transfer Length (µm)**	**Contact Resistance (Ω)**	**Specific Contact Resistivity (Ω-cm^2)**
MLD	531	2.35	15.7	2.9 x10^{-05}
	721	1.13	8.16	9.2 x10^{-06}
	584	2.83	10.3	4.7 x10^{-05}
Implant	54	14.2	6.38	1.09 x 10^{-04}
	76	13.2	4.98	1.31 x 10^{-04}
	47	18.8	8.82	1.66 x 10^{-04}

Chapter 9

Patterning of Monolayer

The photolithography process is used to pattern different layers for fabrication of devices. It usually begins with growth or deposition of thin film like silicon dioxide, polysilicon, metal on the surface of the wafer, followed by coating thin layer of photoresist, which is exposed and developed. The desired pattern is achieved by etching the area that is not protected by the resist.

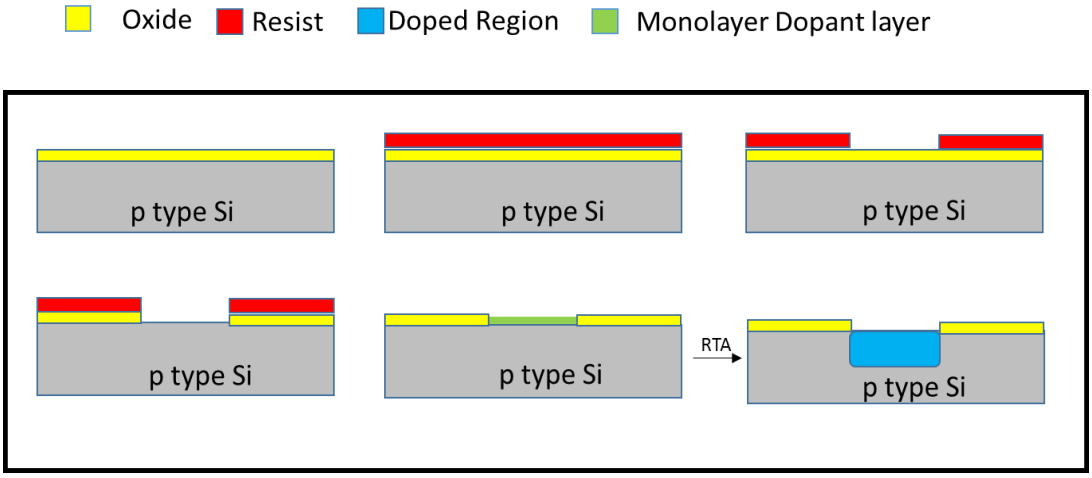


Figure 9.1: Process flow for patterning of the monolayer with oxide as masking layer

Experiments were conducted to determine if localized doping could be achieved using monolayer. Silicon dioxide was used as masking layer, to prevent diffusion of dopants into the silicon. In the Figure 9.1, the process to pattern a wafer is described. The SiO_2 was deposited/grown on the surface of silicon followed by photolithography and etch. Subsequently MLD was performed which results in dopant containing chemistry forming monolayer on the surface and thermal process to diffuse the dopants deep in the surface. The patterning of monolayer was done using two different approaches; MESA isolation was used to fabricate diodes and TLM, and is discussed

in detail in Chapter 8. The second approach was to use Silicon dioxide as masking layer to form pattern. The initial investigation was done on Si pieces, one with 200 nm thick oxide and other as bare hydrogen terminated silicon. Both samples were reacted with chemistry at the same time followed by capping oxide and anneal at 1000^{o}C for 5 minutes. After etching oxide off the surface, sheet resistance was measured using four-point probe. As shown in Table 9, the sheet resistance value of silicon under the oxide is comparable with measurements done before doping.

Table 9: Sheet resistance comparison of silicon under oxide and bare silicon after doping

Sample	**Sheet Resistance (Ω/sq)**
Bare Silicon	194
Doped Silicon	1031
Silicon under oxide	219

The 4-inch Si wafer was used to investigate the patterning of monolayer using oxide as masking layer on full wafer with pattern formed using photolithography. A 250 nm thick oxide was deposited followed by lithography and etch. The feature sizes were 3 cm x 3 cm, 2 cm x 2 cm, 1.5 cm x 1.5 cm and 0.5 cm x 0.5 cm. The wafer was etched using 10:1 BOE for few seconds just before the reaction to form monolayer, followed by deposition of capping oxide and anneal at the same condition as the Si pieces. The sheet resistance was 219 Ω/sq all across the wafer except at the center of largest feature the sheet resistance was 1125 Ω/sq.

The reason for the same sheet resistance of MLD exposed silicon and oxide protected silicon could be either that oxide on the surface repels the chemistry or thickness of the oxide is affecting the bond formation. The boundary layer formed between the chemistry and the Si surface might have viscosity effect that would be dominant at the interface of silicon and oxide.

The latter was eliminated by measuring the contact angle between mesitylene, silicon and silicon dioxide surface respectively. It was observed that the angle was so small that it could not be measured. To investigate the boundary layer issues two wafers with 20 nm and 50 nm oxide thickness were patterned followed by doping. Stirrer was used during the reaction in order to create agitation. After the reaction was complete, wafers were cleaned followed by capping oxide deposition, anneal and etching oxide.

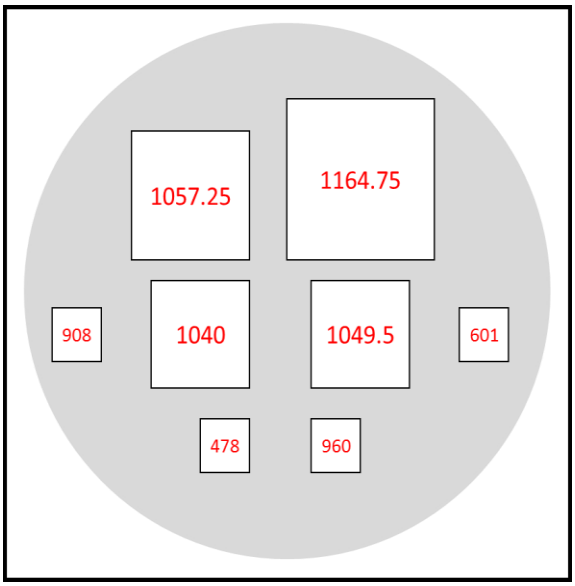


Figure 9.2: Average sheet resistance of bare silicon region after MLD

Sheet resistance measurements were performed and it was observed that for thinner oxide the silicon patterns were uniformly doped everywhere whereas for thicker oxide the interface between silicon dioxide had no doping especially at the smaller features. In Figure 9.2, the grey and white area are Si under oxide and doped Si respectively. The average sheet resistance of grey area is 189 Ω/sq and the doped region is 968 Ω/sq.

Chapter 10

Conclusions and Future work

Monolayer doping a novel technique based on formation of covalent bonds through hydrosilylation reaction between dopant containing chemistry and silicon substrate was demonstrated. With the geometry of the devices becoming smaller, the existing technology spin on dopant and ion implantation pose a challenge for uniform doping. Spin on dopant glass often cracks at high temperature thermal treatment and lacks uniformity and control over the dose of dopants. On the other hand, the ion implantation result in severe crystal damage, transient enhanced diffusion and random dopant fluctuation for 3-D structures.

10.1 Conclusions

Monolayer doping has the capability to form ultra-shallow junctions and abrupt boundaries at nanometer range. The technique forms damage-free junctions semiconductor substrate and devices. The conformity and self-limiting property of the molecular monolayer provides well defined dose and therefore an ideal candidate for thin body devices and 3D structures.

In this work, phosphorous monolayer doping was performed successfully performed on silicon pieces sample. XPS and AES gave information about the presence of phosphorous and silicon carbide on the surface. Therefore confirming the formation of monolayer on the silicon substrate. The doping profile formed after annealing the sample was characterized using SIMS, which was performed at NREL, SRP and sheet resistance measurement. The dopant concentration is high at surface and decreases rapidly with increase in depth; it seems plausible that constant dose is the primary mechanism of diffusion in MLD. The surface concentration and the sheet resistance measured using 4 point probe gave 4.5 x 10^{13} cm^{-2} dopant dose and junction depth 45 nm. All

dopant is not activated during the thermal treatment as the dopant dose from SRP was 1.2 x 10^{13} cm^{-2}.

In order to better study the characteristics and fabricate devices using monolayer doping a system was designed and assembled to hold full size wafer. The system was tested and issues with leaks were resolved using RTV. The wafer processed using the system was compared using SIMS and sheet resistance measurement. Other than the first few nanometers the profile were similar to each other. The dopant concentration in the substrate was tuned upward by multiple runs of MLD and subsequent anneal which decreased the sheet resistance from 1100 Ω/sq for one MLD run to 670 Ω/sq for double MLD. The sheet resistance across the wafer was uniform, the standard deviation is 4% and average sheet resistance is 670 Ω/sq.The effect of anneal time and temperature on the diffusion of dopants was studied, and higher temperature results in higher activation and time determines the junction depth of the dopants.

N+P junction diodes were fabricated using phosphorous MLD and current-voltage characteristics were measured and analyzed. The effect of series resistance was very high and therefore the region with ideality factor 1 was small. The experimental data was compared with unified model that combines the low and high-level injection. The series resistance measured from experimental data was 588 Ω. To understand the bending due to ohmic dependence, unified model was modified and effect due to series resistance was added. The specific contact resistivity for n-type MLD doped was higher than the implanted wafer, measured using lumped circuit model .The sheet resistance obtained from TLM measurement were comparable with the sheet resistance of the diffused region measured earlier.

The ρ_c based on sheet resistance and optimum width of 100 µm is 9.3 x 10^{-6} Ω-cm^2 and 2 x 10^{-4} Ω-cm^2 for MLD and implanted structures respectively.

Patterning of a dopant monolayer by selective etch and oxide as masking layer has provided localized doping. Thinner oxide results in uniform monolayer formation due to mild effect of boundary layer between solid and fluid.

10.2 Future Work

MLD has shown the capability of controlled, conformal and uniform doping technology, and in order to further understand the applications of MLD, future studies are suggested. Doping of source/drain region and polysilicon gate in 2D planar CMOS can be investigated. In this work n-type phosphorous doping was demonstrated to fabricate diodes and TLM structure, organic chemistry for Boron and Arsenic doping are available and should be used in future as p-type and n-type dopants. Mixing the dopant containing chemistry with an alkene that lacks dopant atom can control dopant dose.

Doping of nanostructures and non-planar device like FinFETs. Silicon nanowires were doped using phosphorous MLD and in figure 10.1 the SEM image of the nanowires after MLD and anneal is shown. Energy-dispersive X-ray spectroscopy detected presence of phosphorous. Further, characterization needs to be done to confirm phosphorous doping.

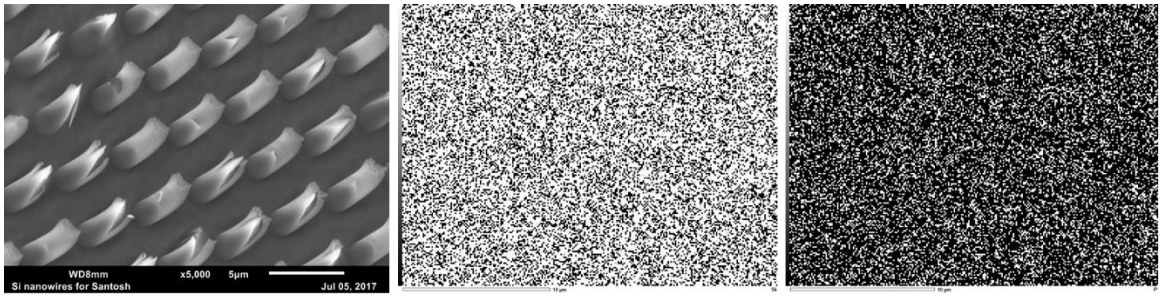


Figure 10.1: SEM and EDS image of MLD doped silicon nanowires

Aside from IC industry, MLD process can also be applied to applications in PV industry to fabricate heavily doped region under the contact called selective emitter to achieve higher efficiency. MLD can find application in fabricating passivated tunneling contacts and interdigitated back contact solar cell for higher efficiencies.

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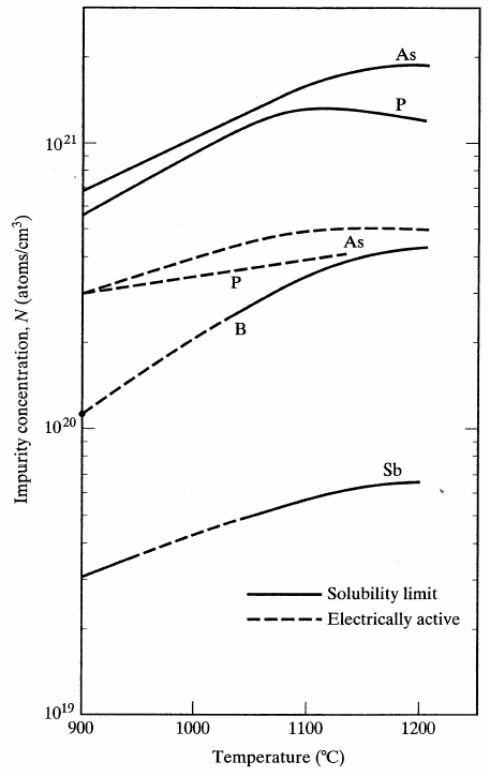
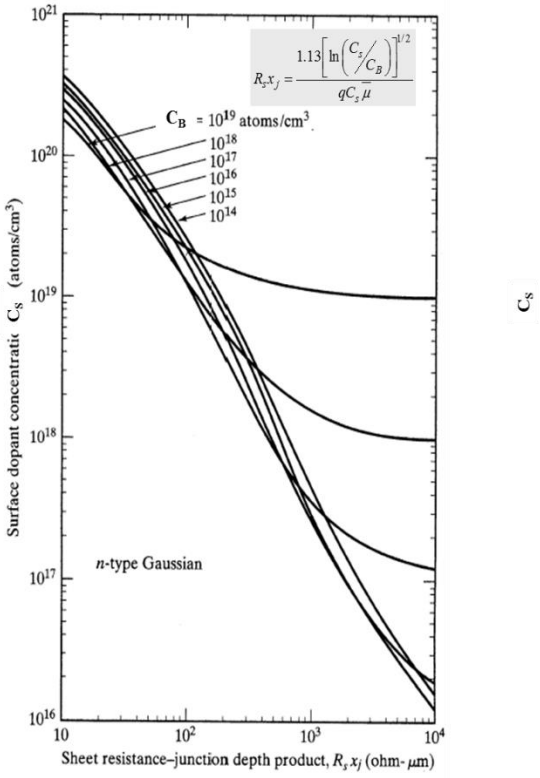
Appendix A

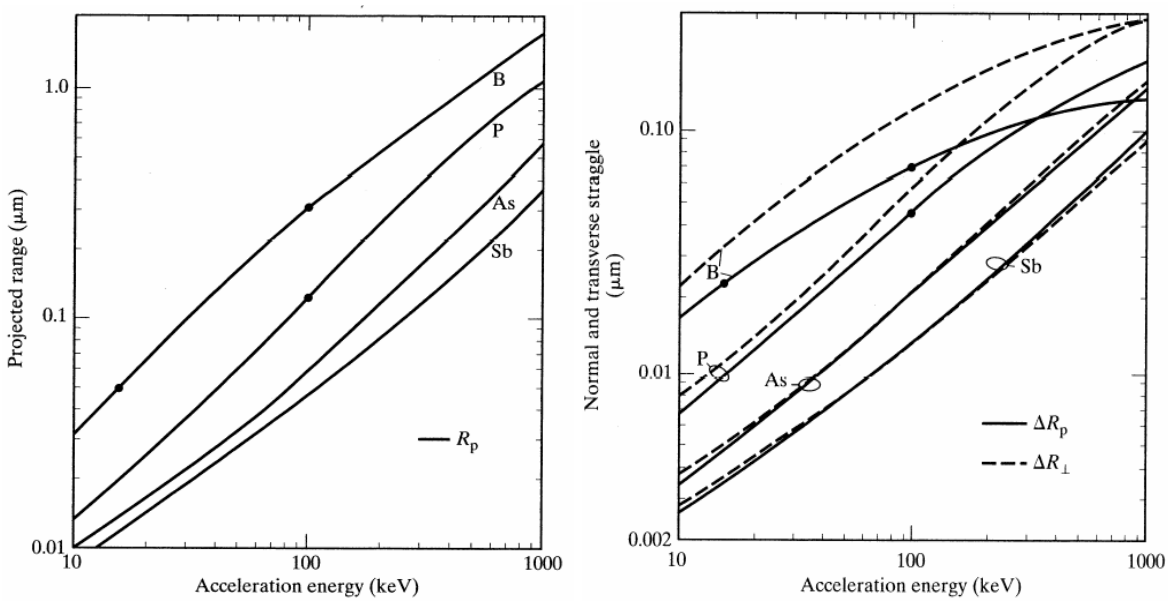
Phosphorous Properties

Properties	
Atomic Weight	30.97
Atomic Number	15
Density (g/cm^3)	1.83
Diffusion Coefficient (cm^2/sec)	10.5
Activation Energy (eV)	3.69
Solid Solubility (@ 1000°C) (cm^{-3})	9×10^{20}





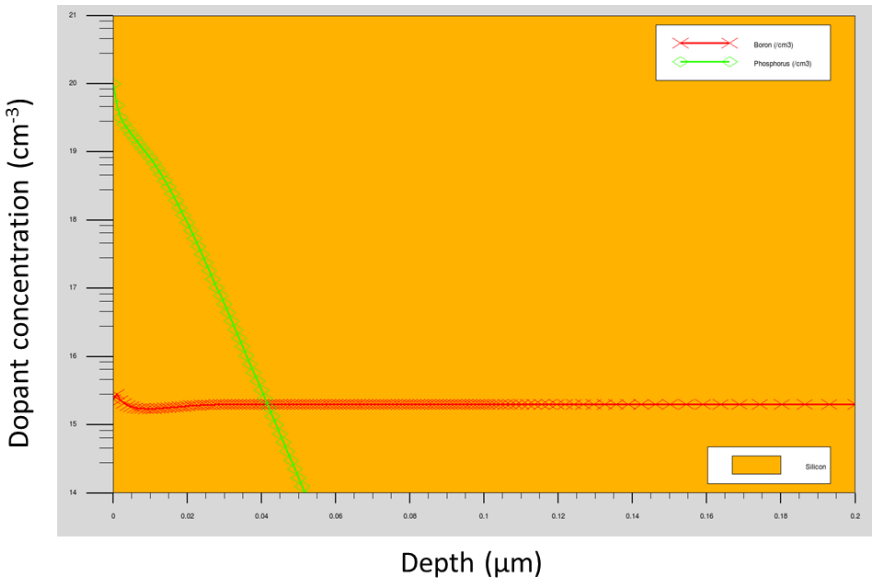
Solid Solubility and n-type Gaussian Irvin curve



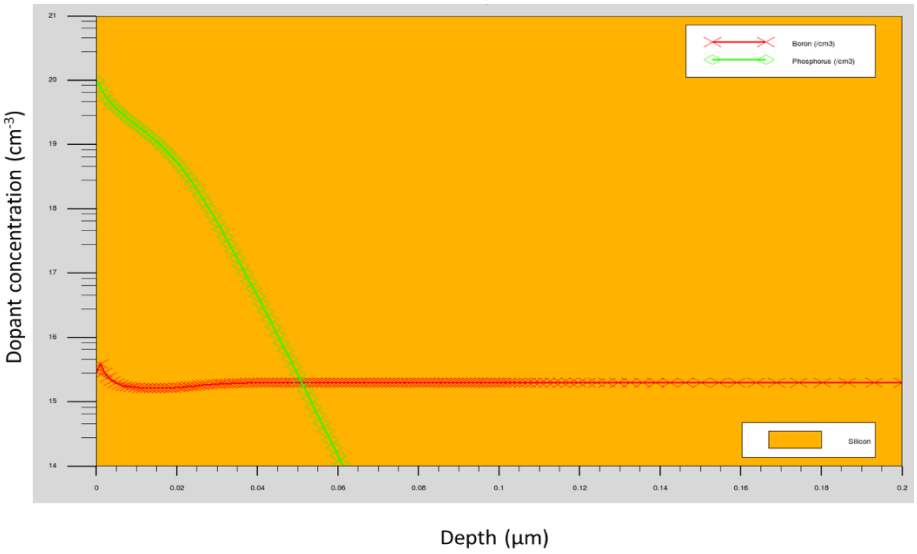
Projected Range and Straggle

Simulation plots

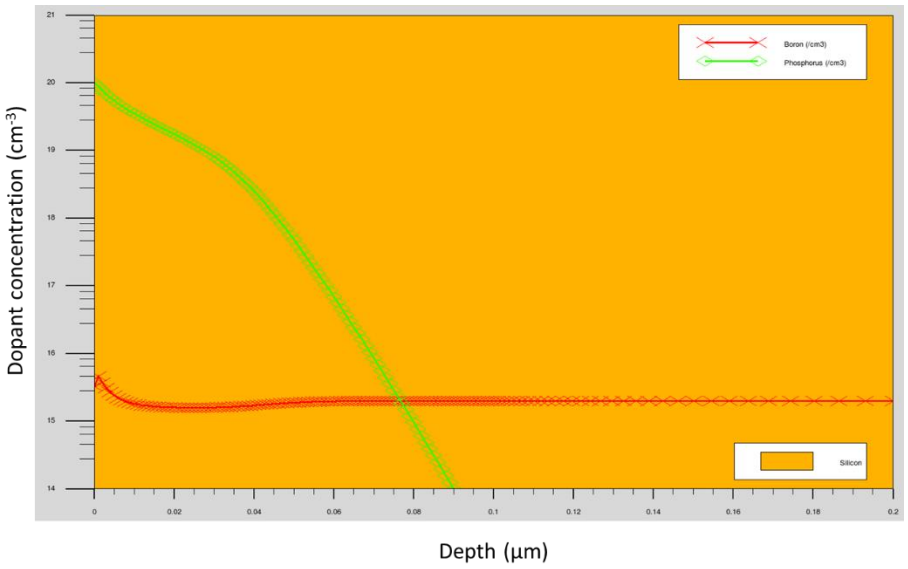
Dose (cm-3)	Junction Depth (nm)	Sheet Resistance (Ω/sq)
2e13	35	2000
5e13	50	1000
1e14	76	745


Boron (/cm3)
Phosphorus (/cm3)
Silicon
Dopant concentration (cm-3)
Depth (µm)

(1)


Boron (/cm3)
Phosphorus (/cm3)
Silicon
Dopant concentration (cm-3)
Depth (µm)

(2)


Boron (/cm3)
Phosphorus (/cm3)
Silicon
Dopant concentration (cm-3)
Depth (µm)
21
20
19
18
17
16
15
14
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0.16
0.18
0.2

(3)