# PMOS OPERATIONAL AMPLIFIER

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## ABSTRACT

This project was an evaluation of a PMOS op amp characteristics. Due to nonworking op amps, SPICE simulation and design layout were investigated. Results show that new design and fabrication are needed.

## INTRODUCTION

The op amp, designed to operate with +/- 9 volts power supplies, has been fabricated at RIT for possible commercial applications. It consists of two gain stages with an overall gain of 2000. The first gain stage is a differential input stage with a gain of 50. One of its differential outputs is level shifted using a source follower .Its other output is used to establish a reference bias voltage for the source follower through a saturated load. The second gain stage has a gain of 40 with its output bufferred by an output stage to enable the op-amp to drive low impedance loads. The op amp circuit is shown in Figure 1,and its layout is given in Appendix I.

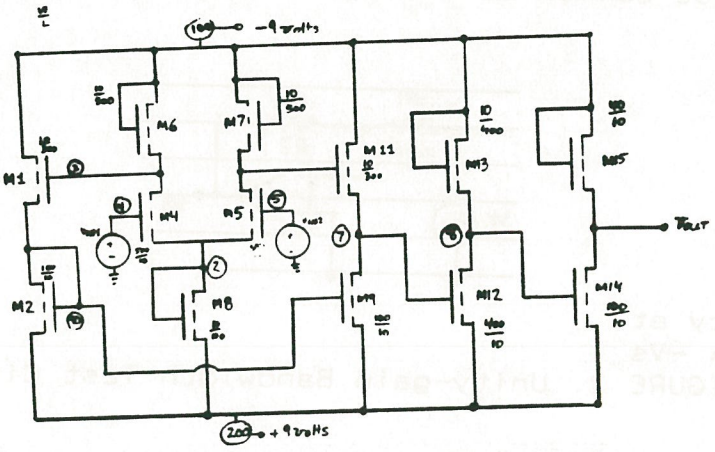



FIGURE 1. PMOS Op Amp Schematic Diagram

The operational amplifier parameters to be evaluated were broken down into four categories: open-loop differential characteristics,output signal response,input error signals,and common-mode characteristics. In this section,these parameters will be defined. And in each case,practical test circuits for parameter measurement are presented and described.

The open loop gain of the op amp is measured by plotting the input voltage versus output voltage with a load resistance of 20K [1]. The input signal (sweep) has enough amplitude to drive the output into saturation in both the plus and minus directions. Gain is equal to any output voltage change divided by the input voltage change that causes it. The slope of the curve at any point depicts the small signal gain near that point.

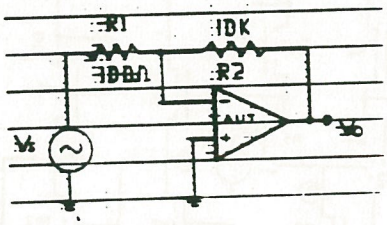
Output resistance of an op amp is the effective output source resistance when operated open loop. Using the open-loop parameter test method above, the output resistance of an op amp is measured by observing the low frequency gain decrease produced by the load [2]. The gain decrease results from the output voltage division across the output resistance and the load resistance, and the loaded gain is

$$Ao' = ((Rload/(Ro+Rload))Rload$$

Then the output resistance will be

$$Ro = ((Ao/Ao')-1)Rload$$

Unity-gain bandwidth is the frequency range from direct current to that frequency at which the open loop gain crosses unity. Because of slewing rate limiting, only small-signal response is achieved at this frequency,and the output test signal should be observed to ensure that the amplifier is in linear operation. The unity gain bandwidth is measured in a closed-loop circuit as in Figure 2 to avoid being affected by the highly amplified noise common to the open-loop test circuits.




fc = frequency at
which Vo = -Vs

FIGURE 2. Unity-gain Bandwidth Test Circuit

Slewing rate is the maximum rate of change of output voltage. In general, slewing rate is measured in the unity-gain voltage follower circuit of Figure 3. The amplifier is driven by a high frequency square wave . The slew rate is found as the slope of the transition between the output extremes.

Offset voltage is an important parameter when an op-amp is used to amplify small direct voltages . This is the differential dc input voltage required to provide zero output voltage with no input signal or source resistance. The offset value is measured

at room temperature. To facilitate the measurement of the input offset voltage a high-gain test circuit is used to amplify the offset as indicated in Figure 4 [2].

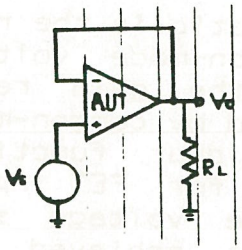
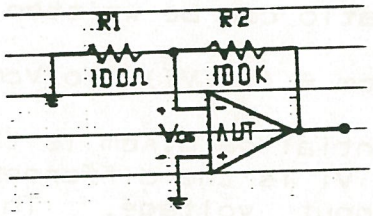



FIGURE 3. Test Circuit For Slew Rate




Vos = -(Vo/1001)
Vo = -((R1+R2)/R1)Vos

FIGURE 4. Input Offset Voltage Test Circuit

Input offset current is the DC biasing current required at either input to provide zero output voltage with no input signal or offset voltage. The input bias current is the gate leakage current of an input FET. The input bias currents are measured by forcing them to flow in large resistors, as in the test circuit of Figure 5,which are bypassed to reduced noise. The output voltage is essentially the product of one of the resistors and the associated current. It is typically necessary to null the input offset voltage [2].

| Switches open | Vo |
|---|---|
| S1 | Ib1*Rg |
| S2 | _Ib1*Rg |
| S1,S2 | Ios*Rg |

For Vo much larger than Vos

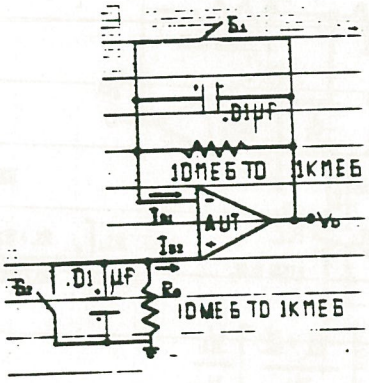



FIGURE 5. Measurement Circuit for Input Bias Currents and Input Offset Current

Input offset current is the difference between two input bias currents. This difference current is measured as indicated in Figure 5. Since the measurement takes the difference between two currents which are of the same order of magnitude, it is necessary to match the two resistors to within about .1 percent.

Common mode rejection ratio is the ratio of the differential voltage gain to the common-mode voltage gain. The CMRR is a figure of merit comparing the gain received by differential signals with that received by common-mode signals. The common mode gain is often a non linear function of the common-mode voltage level, especially for FET input amplifiers. For this reason the full common-mode voltage swing must be used in measuring CMRR . This is achieved by using the difference amplifier circuit of Figure 6. For well-matched or balanced resistors as indicated, the signal at the two inputs is essentially a common-mode signal. However, the common-mode unbalance of the amplifier produces an output error voltage and an associated differential input voltage Vi=Vo/Ad. Then the common-mode rejection ratio can be written [2]

$$CMRR = Ad/Acm = (Vo/Vi)/(Vo/Vcm) = Vcm/Vi$$

where Ad is the differential gain, Acm is the common-mode gain Vo is the output voltage, Vi is the differential input voltage, Vcm is the common-mode input voltage. This can be rewritten considering

$$Vo = ((R1+R2)/R1)/Vi$$

$$Vcm \sim Vs \text{ for } R2 \text{ very large compared to } R1$$

The common-mode rejection ratio is then expressed simply in terms of the input and output signals by combining the last three relationships to get

$$CMRR = ((R1+R2)/R1)Vs/Vo$$

where Vs is the input voltage

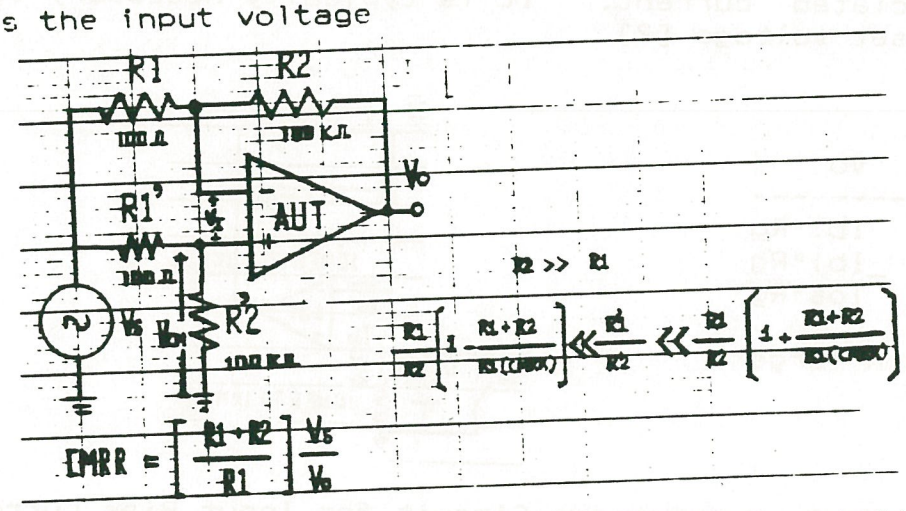



FIGURE 6. Common Mode Rejection Ratio Measurement Circuit

Power supply rejection ratio may also be plotted and measured with a curve tracer. PSRR shows the effects that a change in power supply voltage may have on the output of an op-amp. Either the positive or negative supply may be changed to show the effect. The output of the op-amp is held close to zero volts during these changes by applying the right amount of voltage between its inputs. Input voltage is plotted against power supply voltage [1].

## EXPERIMENT

Prefabricated PMOS op amp were diced,mounted,and wired bonded for testing. The op amp were inoperable even at other values of VDD and VSS. Threshold voltage of discrete P-ch transistors were obtained (Appendix II) and compared to the designed value. Several on-wafer op amp were probe tested showing non working op amps. SPICE simulation using actual threshold voltage was done (Appendix II). Design layout was also checked.

## RESULT/DISCUSSION

Table 1 is a summary of the testing and simulation results. The discrete P-ch transistor threshold voltage ranged from -4.5 to -5 compared to -3 volts as designed. Design layout checking revealed that transistor M8 was improperly designed with ratio

TABLE 1. SPICE Simulation Results

| NSS \ POWER SUPPLY | +/-9 volts | | +9/-5 volts |
|---|---|---|---|
| 8.28E11 (Vth=-3v) | W/L = 10/100 | W/L = 100/10 | W/L = 10/100 |
| | GAIN = 73DB | OUTPUT CONSTANT AT 5.43V | |
| 1.55E12 (Vth=-4.6v) | CURRENT SOURCE IS OFF | CURRENT SOURCE IS OFF | CURRENT SOURCE IS OFF |

W/L inverted. The SPICE simulation results,using +/-9 volts power supply, showed that for the designed W/L ratio of 10/100 and threshold voltage of -3 volts, the op amp functions as expected though with a higher gain than was designed (i.e. 73DB instead of 66DB). This is due to the non unity gain of the source follower and the output stage. SPICE simulation using the

W/L of 100/10, i.e.actual layout, with the same -3 volts threshold show a constant DC transfer curve of Vout constant at 5.43 volts for any value of Vin from -2 to 2. For NSS value of 1.55E12 which gives an equivalent threshold voltage of -4.6 volts. The current source M8 is off. The op amp was also simulated at supply power of -9/+5 volts with threshold voltage of -4.6 volts. Again, the current source M8 is off. In summary, SPICE simulation showed that, with the wrong W/L ratio for M8 and actual Vth,non of the op amp would work.

## CONCLUSION

Actual measurements of the op amp parameters were not possible due to the non working op amps. However, a revision of the layout with the change of W/L ratio for transistor M8 from 100/10 to 10/100 together with a tighter controlled process to produced the wanted threshold voltage of -3 volts would fix the problem.

## ACKNOWLEDGEMENTS

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## REFERENCES

1. John Mulvey, IEEE SPEC 74 Sep. 53-58.

2. Operational Amplifier,Design and Applications, edited by Tobey,Graeme and Huelsman(McGraw-Hill Book Company, New york)