EVALUATION OF INTEGRATED INJECTION LOGIC DEVICES AT RIT

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ABSTRACT

IIL logic gates were fabricated using a two diffusion, four mask process. The functioning of NOR and OR gates were evaluated, and suggestions for improving the process are given.

INTRODUCTION

IIL was invented back in 1972 by two different groups working independently of each other; one at IBM Laboratories in Germany, and the other at Philips Research Labs in the Netherlands. Both groups had the same goal which was to develop a bipolar logic that combined the high spped of a BJT with the high packing density of MOS. The result was Integrated Injection Logic.

The IIL design evolved by shrinking direct-coupled transistor logic (DCTL) shown in Figure 1a. The emitter-grounded output transistor pair was replaced by a single multi-collector vertical npn transistor. A lateral pnp transistor was used as the current injector source, and replaces the diffused resistor of the DCTL gate by also acting as an active load. As a result, no large space consuming resistors are required on the chip for either the source or load function. Thus the DCTL gate shown in Figure 1a has been reduced to a single IIL transistor pair as shown in Figure 1b.

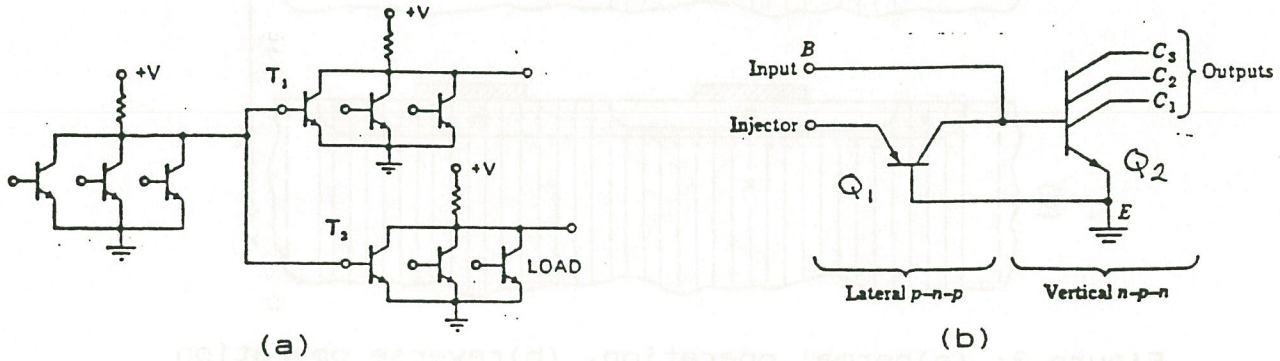


Figure 1: (a)DCTL inverter (b)IIL equivalent inverter

The end result of these modifications was to reduce the size of the logic gate down so that it takes up less real estate on the chip. Furthermore, the base of the npn and the collector of the pnp share a "p" diffusion, and the base of

the pnp and the emitter of the npn share a "n" diffusion as shown in Figure 2. This sharing of common regions between two transistors is called "merging" and further enhances the conservation of silicon area on the chip. Consequently, this makes IIL desireable for MSI and LSI applications. Other advantages of using IIL are that only four masks are required (two diffusions, contact, and metal) and there is no need for isolation or ion implantation which simplifies the processing.

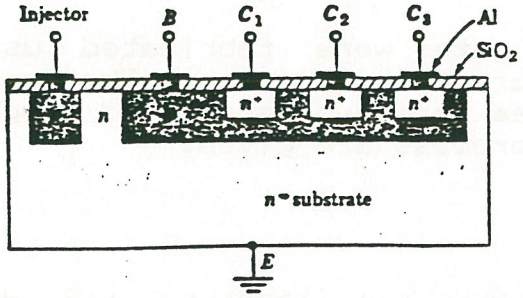


Figure 2: Cross-section of IIL inverter.

Although IIL has many advantages, there are a few tradeoffs. First of all, in order for the "merged" design to work the npn vertical transistor must operate in the reverse or "up" mode. In other words, the collector acts as the emitter and the emitter acts as the collector. This concept is shown in Figures 3a and 3b. For normal operation, the current flow lines are downward as shown in Figure 3a, whereas the current flow lines are upward for reverse operation as shown in Figure 3b.

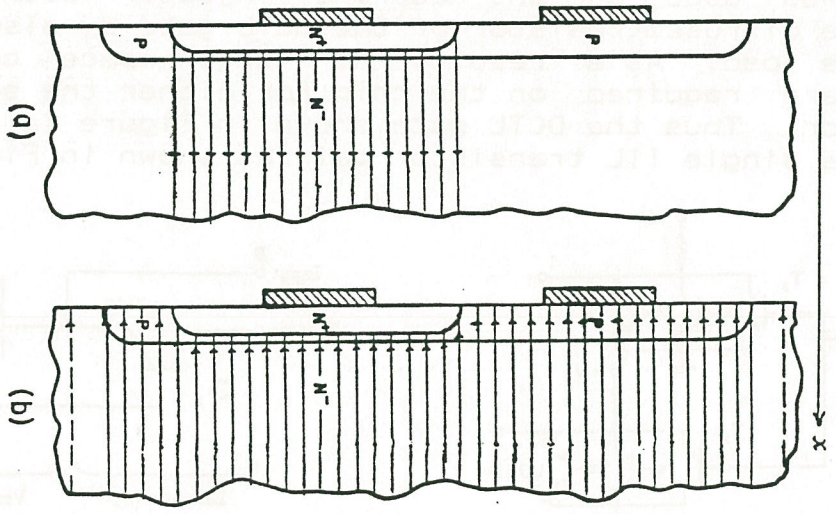


Figure 3: (a)normal operation, (b)reverse operation

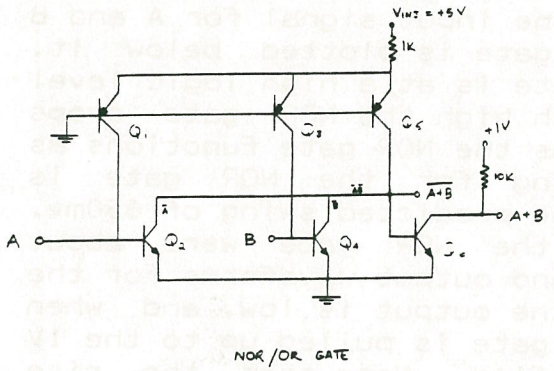
Since the collector is the substrate for normal operation, then the collecting area is very large with respect to the base area and most of the current from the emitter gets collected and high gains are easy to achieve. In contrast, for the reverse mode the collector area is small, and the

emitter is the substrate, so a large portion of the substrate current recombines in the base and is not collected. Therefore the reverse gain is considerably reduced. Furthermore, the gain is also proportional to the ratio of the emitter doping (Ne) to the base doping (Nb), as shown in Equation 1.

$$\text{Beta} = \frac{Ic}{Ib} = \frac{Ne\ Dnb\ Lpe\ Ac}{Nb\ Dpe\ Wb\ Ab} \qquad (1)$$

Since we are using the substrate as the emitter, and it is lightly doped at about 2.0E+15 then the reverse gain is reduced even further. A reverse gain of at least one is needed in order for IIL to be used in LSI applications where a large number of gates will be chained together. If the gain is less than one, then the small signal gain of the chain will be degraded with each stage until it cannot be distiguished from the background noise.

This project involved the testing of the NOR/OR gate circuit shown in Figure 4.



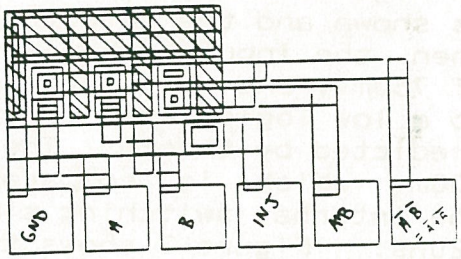


Figure 4: NOR/OR gate schematic Figure 5: NOR/OR gate ICE layout

With a high input signal on A and B (A,B>800mv), current is injected from Q1 and Q3 into the base of Q2 and Q4 which are consequently driven into saturation. The voltage at the output of Q2 and Q4 is VCE sat, which corresponds to a low signal of approximately 100mv. Thus the NOR function has been realized. This low input of VCE sat is then the input to the next gate, Q6. Therefore, Q6 is off and the output of Q6 is pulled up to the 1V supply via the 10K pullup resistor, and the OR function is demonstrated.

However, if the input signal for A and B is low, then Q2 and Q4 are off, and current is injected from Q5 into the base of Q6; saturating it. Now the output of Q2 and Q4 are at VBE sat of Q6. This corresponds to a high signal of 750mv for the NOR gate. Since Q6 is saturated then the otput of Q6 is VCE sat or 100mv, which is the low logic level for the OR gate. Thus the internal logic swing of the circuit from high to low is 650mv.

EXPERIMENT

The simple IIL logic gates decribed above, were fabricated and tested for proper functioning using a probe card setup. The NOR/OR gate shown in Figure 5 was tested to verify the operation of a IIL circuit. The circuit was tested using a 1.5V pulse at a frequency of 5KHz applied to inputs A and B, Vinj=5V, Rinj=1K, Vp=1V, and Rp=10K. A Tektronix 2430A digital oscilloscope, and HC100 color plotter were used to obtain plots of the input and output waveforms. The forward and reverse beta's of the npn vertical transistor were also investigated using the HP 4145A Parameter Analyzer.

RESULTS/DISCUSSION

The NOR and OR logic functions are verified by the plots in Figures 6 and 7. In Figure 6, the input signal for A and B is shown and the output of the NOR gate is plotted below it. When the inputs are low the NOR gate is at a high logic level of 750mv, and when the inputs switch high the NOR gate drops to a low logic level of 150mv. Thus the NOR gate functions as predicted by theory. The logic swing for the NOR gate is 600mv which is comparable to the predicted swing of 650mv. The internal switching times for the NOR gate were about 120ns. Figure 7 shows the input and output waveforms for the OR gate. When the inputs are low the output is low, and when the inputs switch high, the OR gate is pulled up to the 1V supply, and the OR function is verified. Note that the rise time for the OR gate was 4us and is much greater than the fall time of 120ns. The rise time is longer, since the 10K resistor limits the speed at which charge can be removed from Q6, whereas the fall time is shorter due to the stauration of transistor Q6 which pulls the output down. In order to reduce the rise time, an active pullup could be used in place of the 10K resitor.

The forward and reverse gain of the npn transistor was obtained from the plots in figures 8 and 9. The forward gain was 34 and the reverse gain was only 0.07. For the process used, the predicted reverse gain was 0.046, using the values shown below.

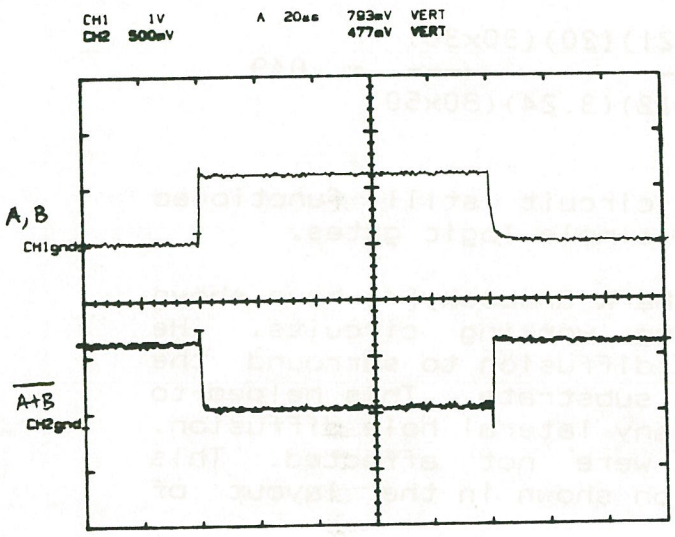


Figure 6: NOR gate function

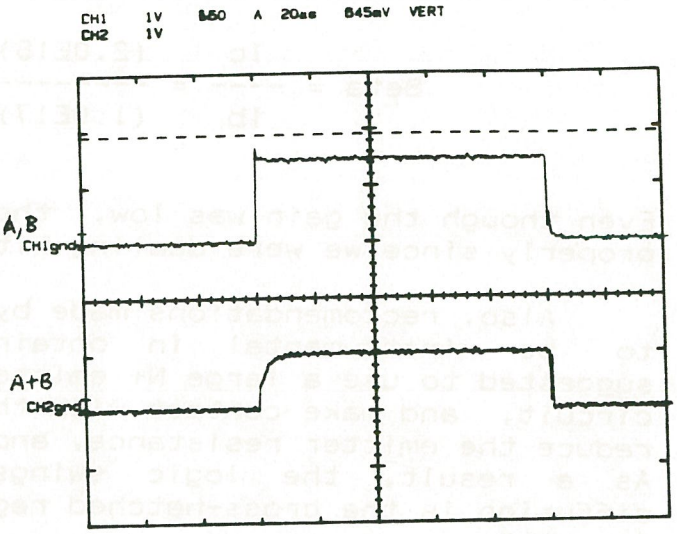


Figure 7: OR gate function

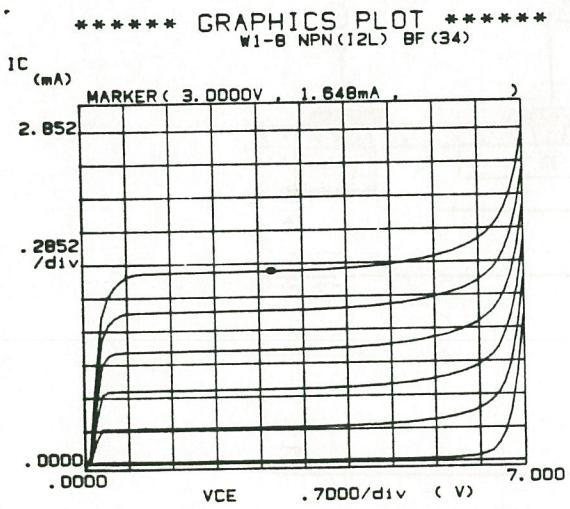


Figure 8: NPN forward beta

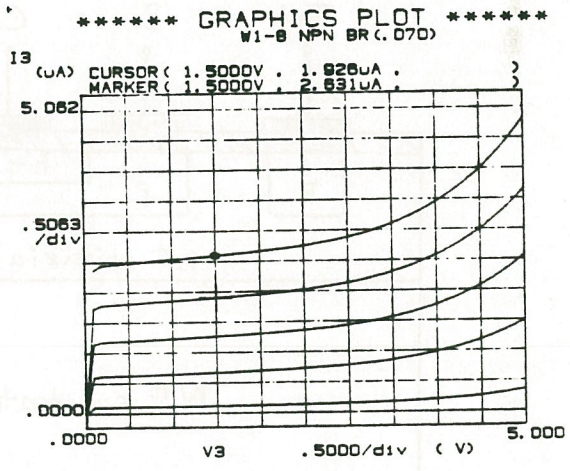


Figure 9: NPN reverse beta

$$\text{Beta} = \frac{Ic}{Ib} = \frac{(2.0E15)(21)(20)(30\times30)}{(1.0E17)(12)(3.24)(80\times50)} = .049$$

Even though the gain was low, the circuit still functioned properly since we were dealing with simple logic gates.

Also, reccomendations made by Mark Grabosky[4] have shown to be instrumental in obtaining working circuits. He suggested to use a large N+ emitter diffusion to surround the circuit, and make contact with the substrate. This helped to reduce the emitter resistance, and any lateral hole diffusion. As a result, the logic swings were not affected. This diffusion is the cross-hatched region shown in the layout of Figure 5.

CONCLUSIONS

The results show that functioning IIL circuits can be made at RIT. Although the circuits were simple logic gates, more complicated designs can be made if the reverse gain is increased. One way of doing this is to start with an N+ substrate and grow an N- epitaxial layer on top of it for fabricating the circuit, as shown in Figure 10. Note, wafers such as these can be purchased from companies like Spire or Eaton.

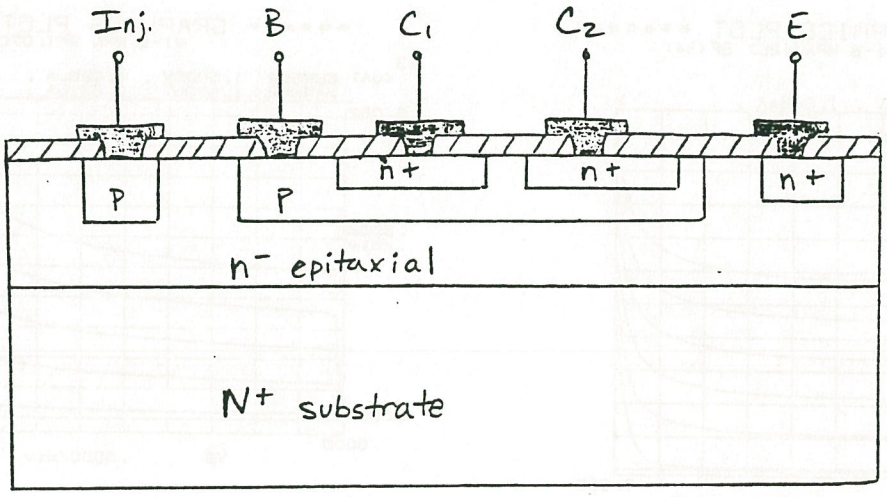


Figure 10: Improved IIL structure.

The N+ substrate will now act as the emitter, and its doping can be used in equation 1 to calculate the gain. Substituting a value of 5.0E18 for the emitter doping results in a reverse gain of 2.45 which is greater than one.

Other ways of increasing the reverse gain are to maximize the ratio of collector area to the base area, and to minimize the base width.

ACKNOWLEDGEMENTS

C.E. Conrad for setting up the probe card station which facilitated the testing of these circuits.

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