

# REDESIGN OF AN EIGHT-BIT, ECL DAC TO FACILITATE SPEED AND FUNCTIONALITY TESTING OF A BI-CMOS PROCESS

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## ABSTRACT

The redesign and layout of a clocked eight-bit digital to analog converter using emitter coupled logic is examined based on testing of the original circuit, simulation of ground node resistance and pinout compatibility to a produced part. The completed layout is subjectively compared to the original circuit design. Production and evaluation is pending at this time.

## INTRODUCTION

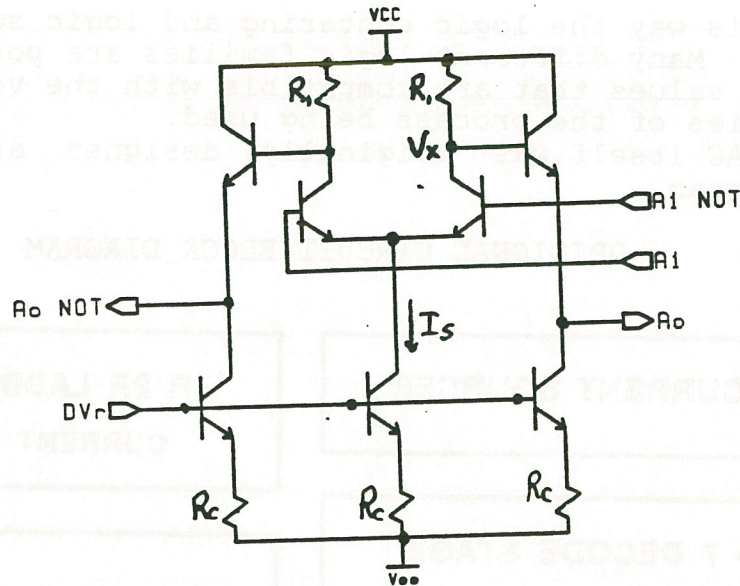
ECL is an acronym for Emitter Coupled Logic, a high performance bipolar logic family. ECL is used for maximum speed without regard for power consumption. The layout is area consuming and not conducive to operating with large logic arrays because a typical gate requires seven to nine transistors and five to six resistors where as the same gate in CMOS can be accomplished with two transistors. As the main virtue of ECL is performance and speed, it is typically biased at the maximum limits of the process, since performance increases with power consumption. ECL is capable of much greater performance than CMOS, however CMOS has a great advantage in density and power consumption on average. Even though the per stage power consumption of CMOS is increasing, taken as a whole there is a significant amount of time where gates remain static for several clock cycles where CMOS power consumption is nearly zero.

Bi-CMOS is a developmental process scheme that combines both bipolar and CMOS onto a single integrated circuit. One such process being developed at National Semiconductor uses the modular approach where CMOS is the baseline. The Bipolar transistor module was initially developed with a test pattern that in addition to parameter monitoring structures and Delay line circuits, incorporated a functional circuit designed in ECL, the DAC.

ECL itself is a current switching logic that is complementary in nature, where performance is maintained by running the maximum current per stage without saturating the differential pair. What this implies is that a large current is always flowing in two of the three branches of the typical logic gate. This is true because when one side of the circuit is off the remaining side has the current flowing.



FIGURE 1  
TYPICAL ECL CELL



Using the gate shown above in Figure 1 for discussion, the branch current  $I_s$  is set by  $DV_r$  where;

$$I_s = (DV_r - V_{be}) / R_c. \quad (1)$$

This is both the controlling current that is switched and the level selecting current in the output stages.  $V_x$ , an internal node to the circuit, has its voltage controlled by which branch the current flow is in. The low logic level,  $V_{x1}$  is the voltage at node  $x$  when the current is flowing;

$$V_{x1} = (V_{cc} - I_s \cdot R_1). \quad (2)$$

The other case is when the current is not flowing and the high logic level,  $V_{xh}$ , exists;

$$V_{xh} = (V_{cc} - 0.0 \cdot V_g) = 0.0 \quad (3)$$

These give the two logic levels at node  $x$  for either input conditions. The output stages then shift these levels down by a base emitter junction drop,  $V_{be}$  to make them compatible with the input logic levels. Saturation becomes a danger when the highest input level,  $A_{ih}$ , becomes greater than  $I_s \cdot R_1$ . In normal operation the stages are cascaded with the input of the stage being considered ( $A_{ih}$ ) being set by the output of the previous stage ( $A_{oh}$ ).  $A_{oh}$  itself is set by  $(V_{xh} - V_{be})$  or  $-V_{be}$ . In this condition the voltage on the collector of the input transistor is  $V_c = -(I_s \cdot R_1)$  and the voltage on the base is  $V_b = -V_{be}$  for any  $I_s, R_1$  combination. Because the output of the previous stage was set by  $A_{oh}$  the onset of saturation occurs in the case where  $V_c$  starts approaching  $V_b$ . Therefore with a known  $R_1$ ,  $I_s$  is calculated to be as near as possible to saturation but still keeping a safety margin. The maximum  $I_s$  is;

$$I_s = +V_{be} / R_1. \quad (5)$$

This gives a maximum  $DV_r$  of;

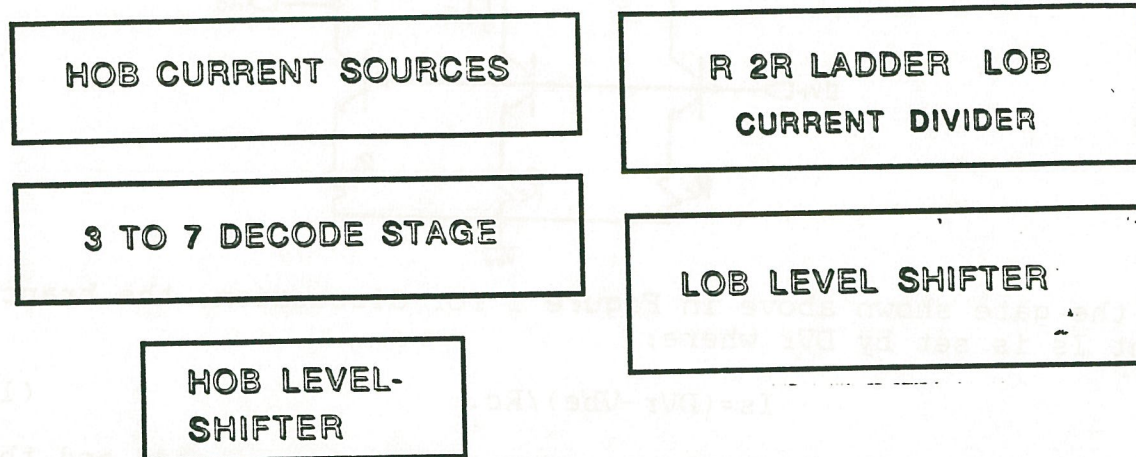
$$DV_r = (I_s \cdot R_c) + V_{be} = (V_{be} \cdot R_c / R_1) + V_{be} \quad (6)$$



In this way the logic centering and logic swing of the family is set. Many different logic families are possible by choosing  $R_c$  and  $R_l$  values that are compatible with the voltage and current capabilities of the process being used.

The DAC itself was originally designed around this logic block diagram.

FIGURE 2 ORIGINAL CIRCUIT BLOCK DIAGRAM



The balance of accuracy to area was addressed in the number of bits directly decoded as compared to the number of bits that were decreased in significance by current division on the R-2R ladder. For the original circuit, bits D0 D1 and D2 were decoded from three binary bits to seven current sources. These are labelled the HOB or higher order bits. The HOB are decoded 3 to 7 by this truth table;

FIGURE 3 HOB TRUTH TABLE AND LOGIC EQUATIONS

INPUT CODE			SEVEN CURRENT STAGES						
A	B	C	I1	I2	I3	I4	I5	I6	I7
0	0	0	--	--	--	--	--	--	--
0	0	1	ON	--	--	--	--	--	--
0	1	0	ON	ON	--	--	--	--	--
0	1	1	ON	ON	ON	--	--	--	--
1	0	0	ON	ON	ON	ON	--	--	--
1	0	1	ON	ON	ON	ON	ON	--	--
1	1	0	ON	ON	ON	ON	ON	ON	--
1	1	1	ON	ON	ON	ON	ON	ON	ON

#### CURRENT SOURCE LOGIC EQUATIONS

$$I1 = A + B + C$$

$$I2 = A + B$$

$$I3 = A + (B * C)$$

$$I4 = A$$

$$I5 = A * (B + C)$$

$$I6 = A * B$$

$$I7 = A * B * C$$

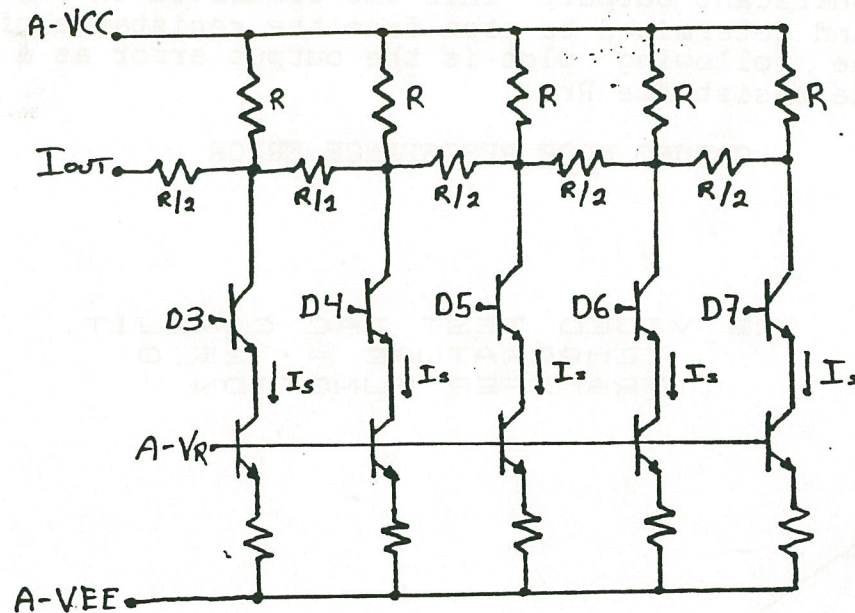


This has the effect of portioning the input code into seven regions. When the first three bits A, B and C are in any combination the decoder stage turns the appropriate number of output current sources on to reflect the significance level of those three inputs. This portioning helps reduce the level of current that needs to be switched during operation as compared to using a pure R-2R ladder.

The remaining five bits D3 to D7 are on the resistor ladder and are labeled the LOB or lower order bits. A schematic of one half of the R-2R ladder is shown here;

FIGURE 4

R-2R LADDER



This ladder performs the function of decreasing the significance of a true signal in progression from D3 to D7. Each resistor is either R or R/2 in value and is configured to divide the current in half once for each of the five stages. The LOB output drivers are of the same value as the HOB output drivers which is  $32 \cdot I_{lsb}$ . This value arises from the fact that the significance of the sixth bit is two to the fifth power which is 32. Bit D3 is divided once for a value of  $16 \cdot I_{lsb}$ , and bit D7 is divided five times to give just  $I_{lsb}$ . The input resistance looking into the ladder is 75 ohms, which corresponds to video cable and video amplifier applications.

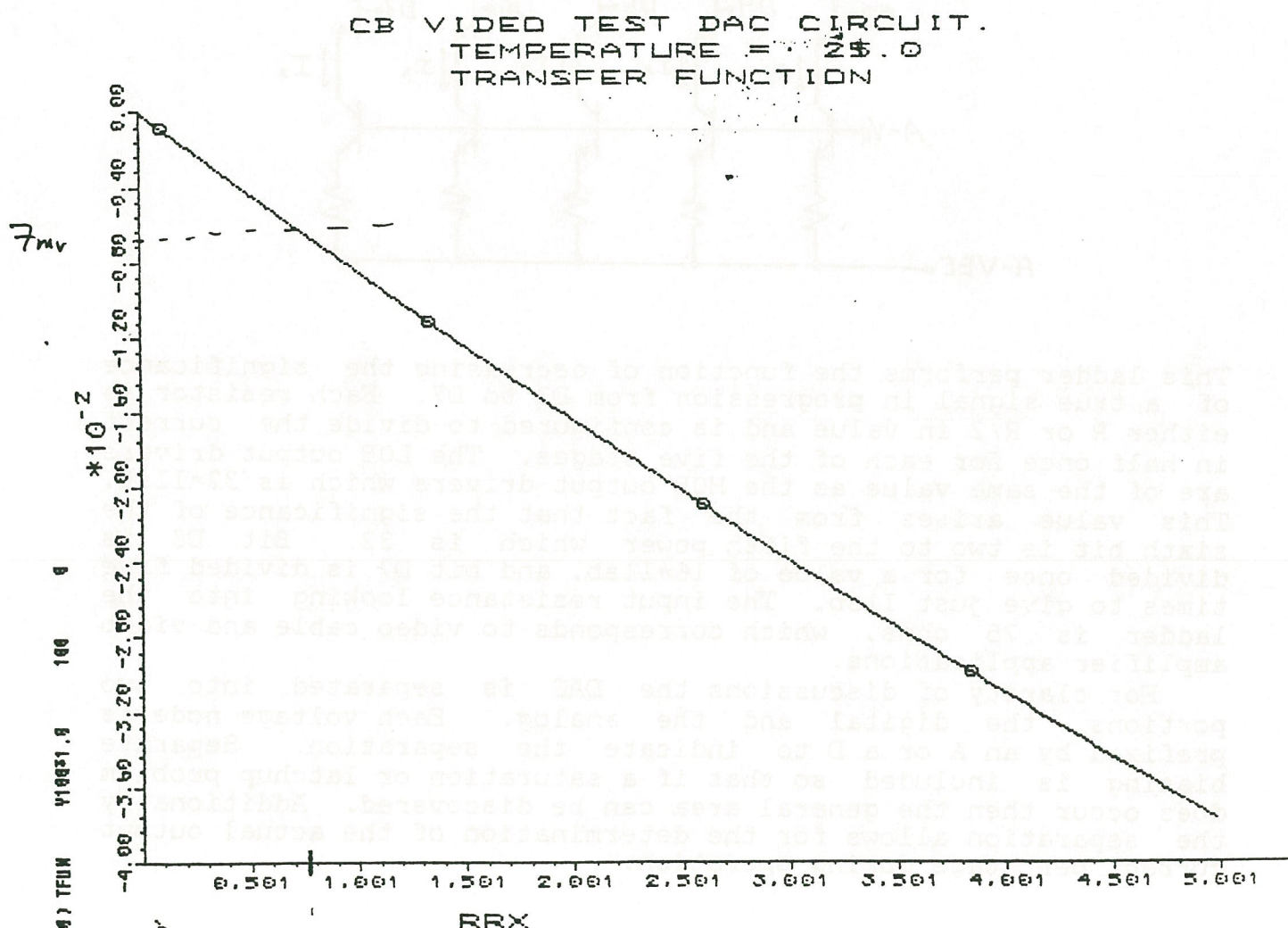
For clarity of discussions the DAC is separated into two portions, the digital and the analog. Each voltage node is prefixed by an A or a D to indicate the separation. Separate biasing is included so that if a saturation or latchup problem does occur then the general area can be discovered. Additionally the separation allows for the determination of the actual output current per stage during operation.

The remaining two blocks in the original diagram are for the setting of the logic levels and directing of the logic flow. They do not directly contribute to the functioning of the circuit.

## EXPERIMENTAL

The first step in the procedure was to determine the best method of redesign through testing of the original circuit. This testing was facilitated by building several test jigs and then driving a sampling scope as the load. The first form of error found was a zero code offset, that is to say that a zero input gave a significant output. This was simulated on SNAP, a version of SPICE and determined to stem from the resistance of the ground node. The following plot is the output error as a function of ground node resistance  $R_{rx}$ .

FIGURE 5 GROUND NODE RESISTANCE ERROR





Since the Iout(not) line is drawing full scale current when a zero is given as the input a resistance of only one ohm in the physical ground line will give an error of seven millivolts as shown in the figure. Since the fullscale swing is supposed to be a 1-volt peak signal through 75 ohms, 13.3 milliamps is a fullscale deflection. When fullscale is divided into 256 even divisions, the LSB or single increment value is 52 microamps and 3.9 millivolts. This gives a 2 LSB offset for a one ohm ground node resistance. Ground Node grouping and layout about the R-2R ladder is a prime consideration factoring into the control of resistance. Another problem observed was the glitches or timing mismatches that were consistently observed at the counting division between the LOB and HOB. The errors were consistent and nearly even for each of the seven transitions. These glitches were observed to have a pulse width of nearly one stage delay for the ECL gate type in use. Examination of the original circuit shows a disparity in the number of stages seen by the HOB and the LOB. The HOB had another logic stage to contend with, and hence an added delay. The addition of an evening stage is therefore a consideration. Several other smaller changes to the global design were;

- A balancing of the HOB logic bus through readjustment of the decoder.
- A minimization of process gradients in current source resistors by placement changes.
- A latched and clocked buffer stage to remove the on and off chip delay from the bits due to very uneven line lengths.
- An input stage to generate the complement immediately after coming on chip, to limit pinout and increase gain for the latch.

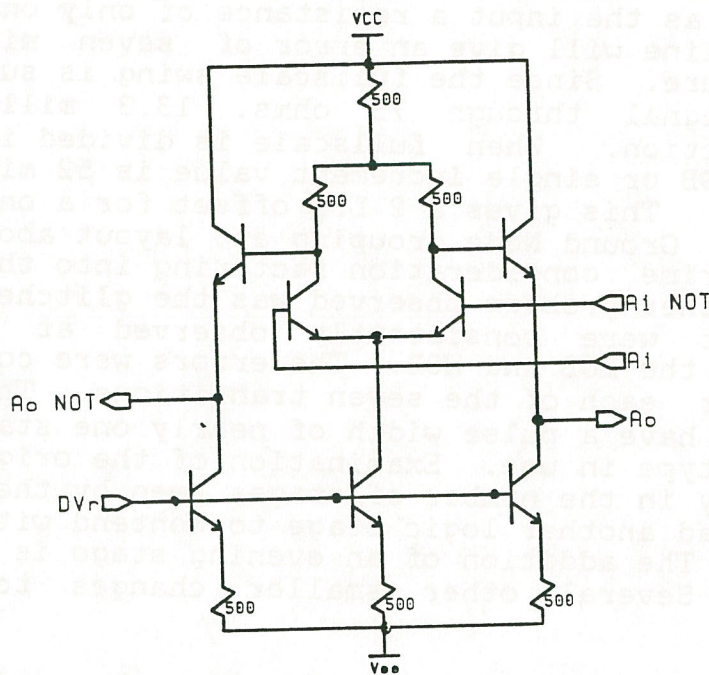
These changes were implemented to match the pinout of a standard production part to aid in comparison of performance. The final change made was to alter the basic gate function and family type. The new circuit differs only in the center push down resistor  $R_p$  shown here.

Testing of other circuits following the original test chip layout had shown that by decreasing the amount of voltage the parasitic input capacitors had to change during an input transient the performance could be increased. The original logic swing was  $V_{be}$ , the new one is cut in half by the center push down resistor to  $V_{be}/2$ . The original core of the circuit remained intact with the 3 to 7 decode and R-2R ladder portions of the circuit being integral to operation.



FIGURE 6

# REDESIGNED ECL CELL - BUFFER

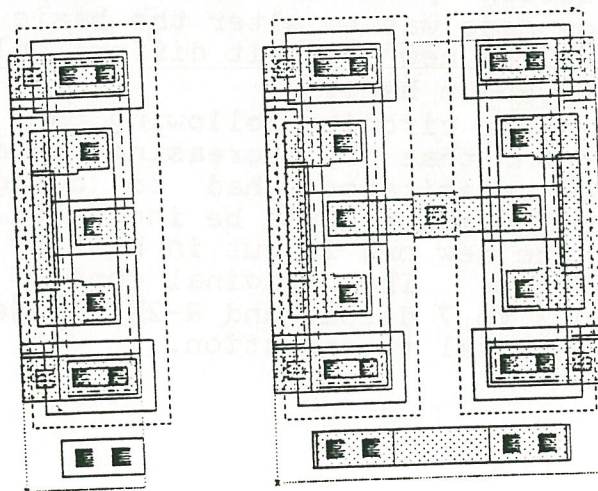


## RESULTS/DISCUSSION

The first step in the layout was the creation of the single transistor and the differential pair. The single transistor was given a double base and collector configuration to enhance performance. Since layout size was not a constraint each transistor was also given a substrate connection. Shown below is the basic differential pair and a 1-x transistor as layed out.

FIGURE 7

## LAYOUT OF 1-X AND DIFFERENTIAL TRANSISTORS

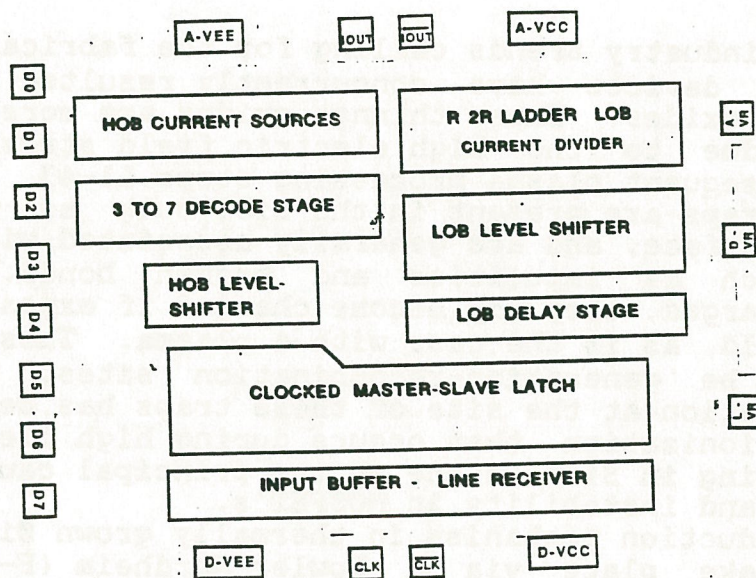




The double contacts and substrate connections may be redundant in a well controlled process but this design is for inclusion into a test pattern. As such information from imperfect runs in terms of process parameters is still desired. The layout of each cell is similar and differs only in the functionality. For ease of discussion and representation the schematics will be shown. There are three level shifter types used in the circuit; HOB, LOB, and 3-7 decode bus driver. Each performs the function of altering the logic levels so that the following stage is matched. There are several levels available that relate to the number of Vbe or diode drops in the output stage. They are labeled A1, A2, and A3 where A would be the logical variable and 1, 2, or 3 is the number of diode drops for that level. All the internal standard logic is at A1, and all the analog output drivers are at A2. The decoder stage in the HOB section requires all three levels for each of D0, D1, and D2. The final layout is approximately 3 mil square, and is shown here in block diagram form.

FIGURE 8

# FINAL BLOCK DIAGRAM



The new design will be included on the next generation of test chip masks to be produced at National. Further estimation of the improvement of the circuit design will not be possible until the devices are fabricated.

## ACKNOWLEDGEMENTS

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