DESIGN OF TEST DIE FOR MONITORING MANUFACTURING AT RIT

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ABSTRACT

This project developed a test chip designed to standardize the testing requirements and characterize bipolar, PMOS and CMOS processes at Rochester Institute of Technology. The common process monitors were designed to test resistivity, opens and shorts, contact resistance and capacitance. The photolithographic monitors were designed to test image resolution and alignment. Process specific discrete devices were designed to test parametrics and leakage currents. The test chip dies were primarily designed to be inserted onto the mask to eliminate the the need for process monitors on each die and secondly, to periodically monitor the performance of a student run integrated circuit factory.

INTRODUCTION

A student run integrated circuit factory processes a significant quantity of wafers each quarter. The wafers are predominately manufactured using either bipolar or PMOS processes. Presently, the wafers are tested and characterized based on the student's individually designed test structures. Statistical data would then be collected from the wafers by testing each die. A test die that would standardize some common process monitors could be implemented and integrated into student's projects for extraction of process data. In addition, the test die could be used exclusively on a wafer as a monitor of the health of the factory.

The design of the test die should include monitors for the bipolar and PMOS processes. With the advent of a polysilicon gate CMOS process, additional process monitors will be required. Each process will have a dedicated test die mask set. The test dies will occupy a 4000 m x 4000 m area and the process monitors will be built on common 2x6 probe pads. The test dies will allow for additions of new test devices.

The test dies will include a variety of photolithographic monitors, process monitors and electrical tests, each of which will be implemented onto the three dies for the parameters that require monitoring. The photolithographic parameters of interest include image alignment and image resolution. Process parameters that require monitoring include capacitance, opens and shorts,

resistivity, linewidth variations, minimum resolvable contacts, contact resistance and contact chain yield. Electrical structures will be used to monitor parameterics and leakage currents.

TEST DIE LAYOUT

The test dies were generated in ICE (Integrated Circuit Editor) which is an in house CAD package used for the layout of the test monitors. The common (*) monitors to all three of the test dies are:

* Alignment marks
* Alignment verniers
* Resolution targets
* Serps/Combs
* Contact holes
* Contact chain
* Van der Pauws
* Linewidths
* Resistors

The specific monitors for each process are:

Bipolar Test Die	PMOS Test Die	CMOS Test Die
Big contact vertical NPN	Capacitors	Capacitors
Normal vertical NPN	1/3 gate	
Lateral PNP	NOR gate	
Diode	NAND gate	
I2L structure		

The structures and their intended purpose follow:

Alignment marks.....to aid aligning to previous mask.
Alignment verniers.....to check alignment to previous mask down to 1 m.
Resolution targets.....to determine minimum resolvable lines and spaces.
Serps/Combs.....to determine opens/shorts in metal.
Contact holes.....to determine the minimum resolvable contact hole.
Contact chain.....to determine yield on contacts between 1st metal and diffusion.
Van der Pauws.....to determine sheet resistance of diffusions or implants.
Linewidths.....use with van der Pauws to determine linewidth variation in diffusions.
Resistors.....to measure direct resistance.
Big contact vertical NPN...to determine hfe before metal.
Normal vertical NPN.....to determine transistor parameters.
Lateral PNP.....to determine the effects of lateral junctions.
Diode.....to determine diode parameters.
I2L structure.....R S flip flop and D flip flop to determine functionality.
1/3 gate.....to determine MOS parameters with a L/W ratio of 1/3.
NOR gate.....to determine MOS functionality.
NAND gate.....to determine MOS functionality.

Table 1 is a summary of the actual layout and a brief description of the monitor.

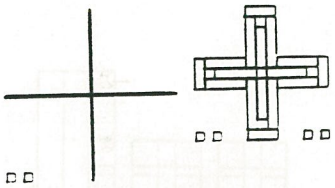

Figure 1
GCA MANN Stepper and
Kasper/Perkin Elmer
alignment targets

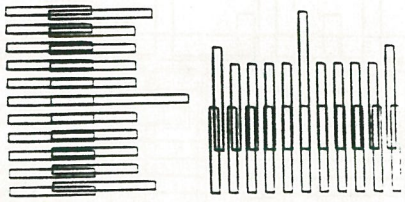

Figure 2
Alignment verniers

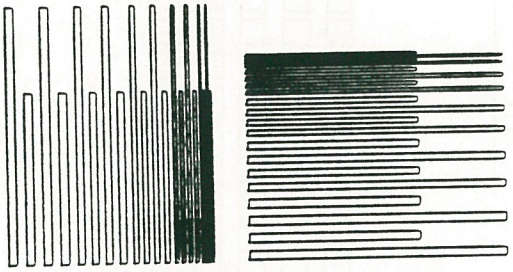

Figure 3
Resolution targets [4]
2,4,6,8,10um lines/spaces

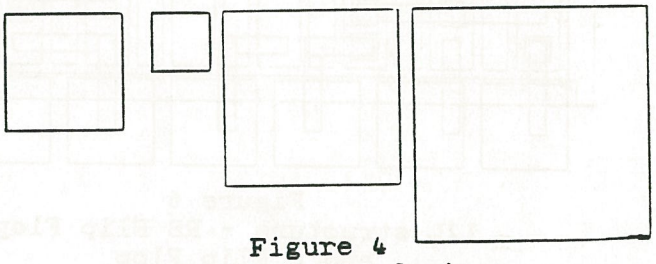

Figure 4
Capacitors MOS devices
800,600,400,200um square

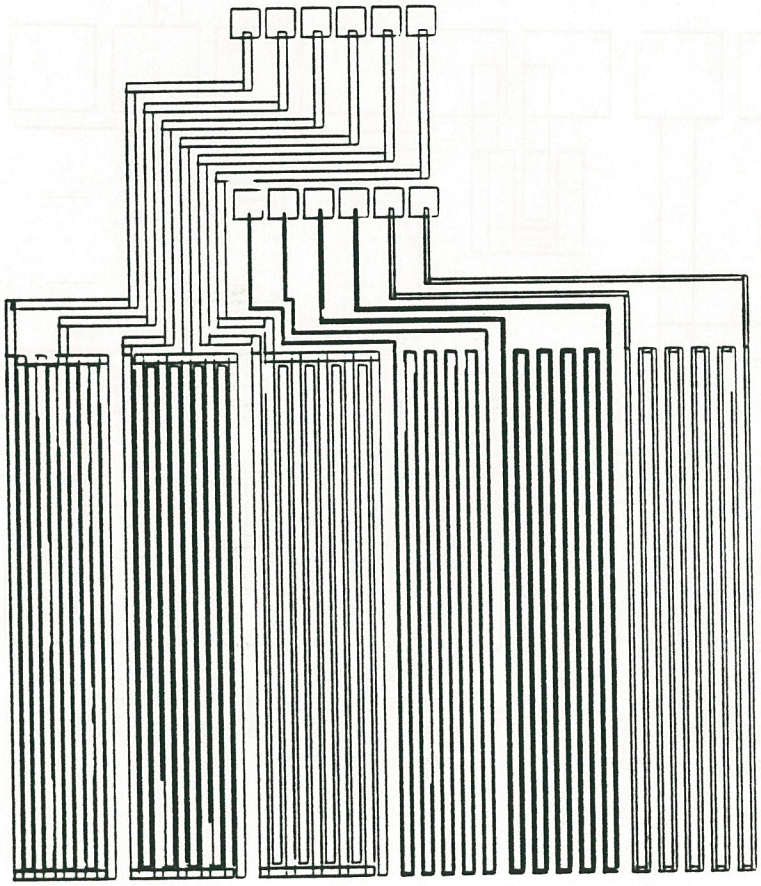

Figure 5
Serp/Comb structure
5,10,15um lines/spaces [4]

Table 1 (cont.)

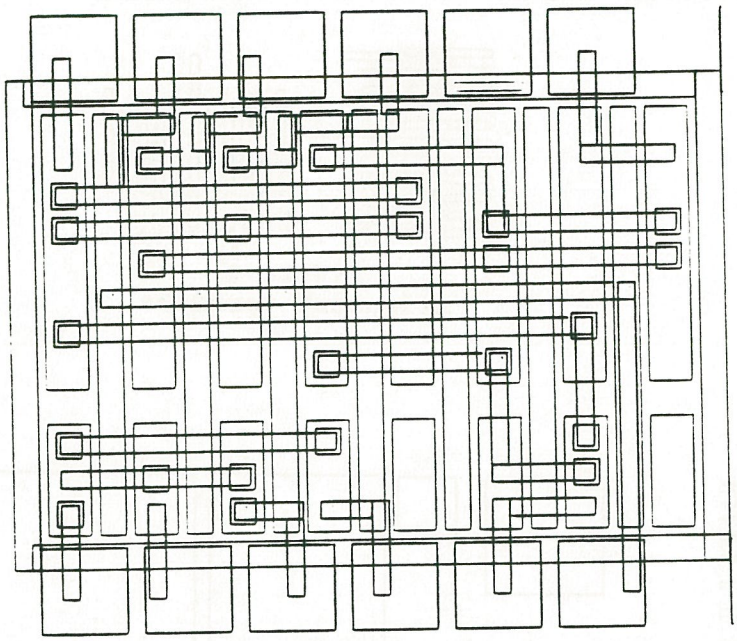

Figure 6
I2L structure - RS Flip Flop
and D Flip Flop

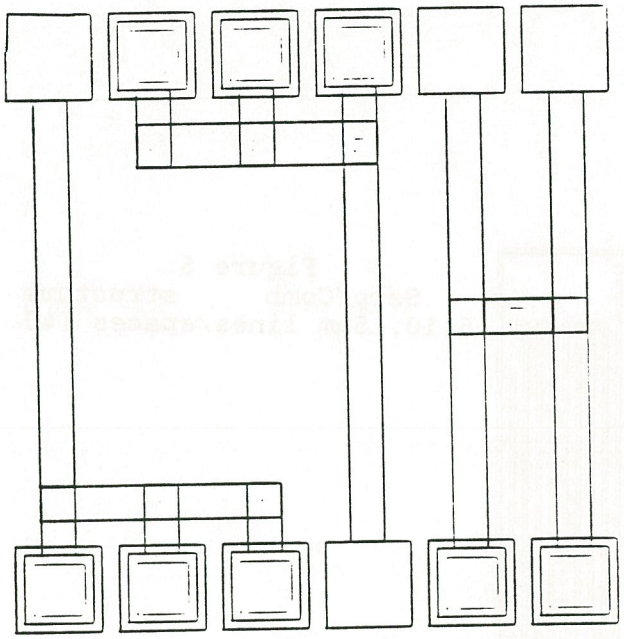

Figure 7
3,5,7,10,12,15um contact hole
test structure [4] with 20x20um
contact resistance structure [4]

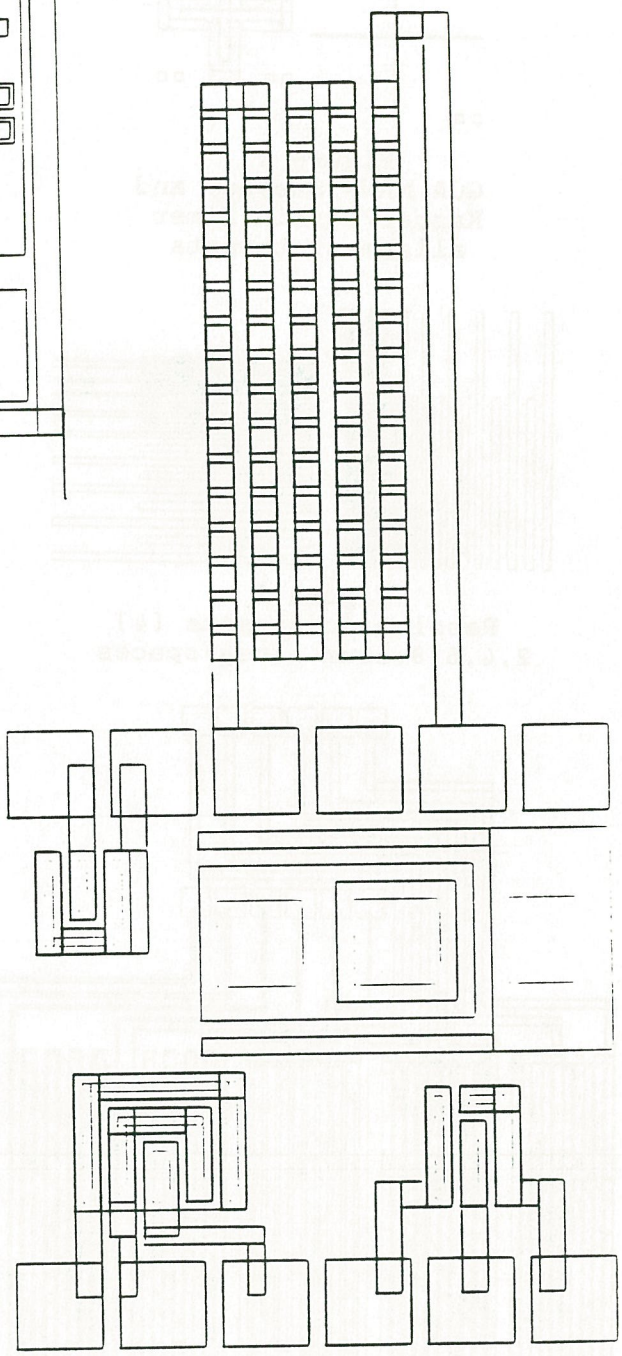

Figure 8
Contact chain [2] with Diode,
Large NPN, Normal NPN
and Lateral PNP

Table 1 (cont.)

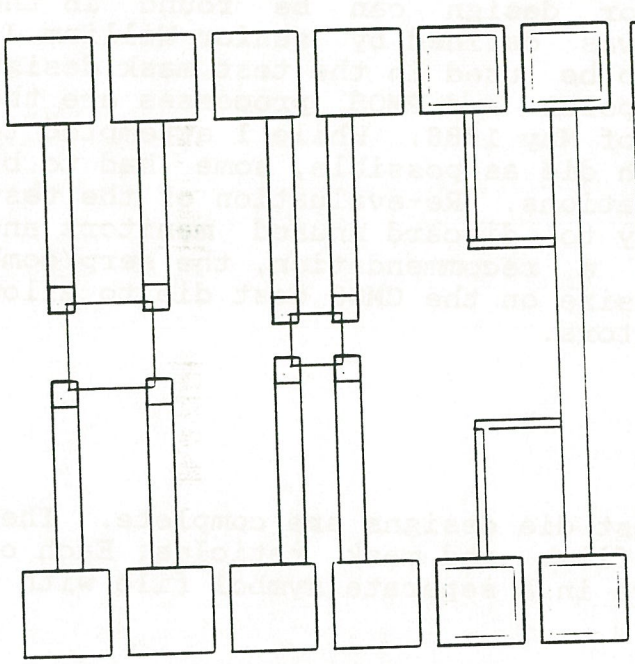

Figure 9
P-diffusion
100x100um and 60x60um
Van der Pauws [3] and
Linewidth structure [4]

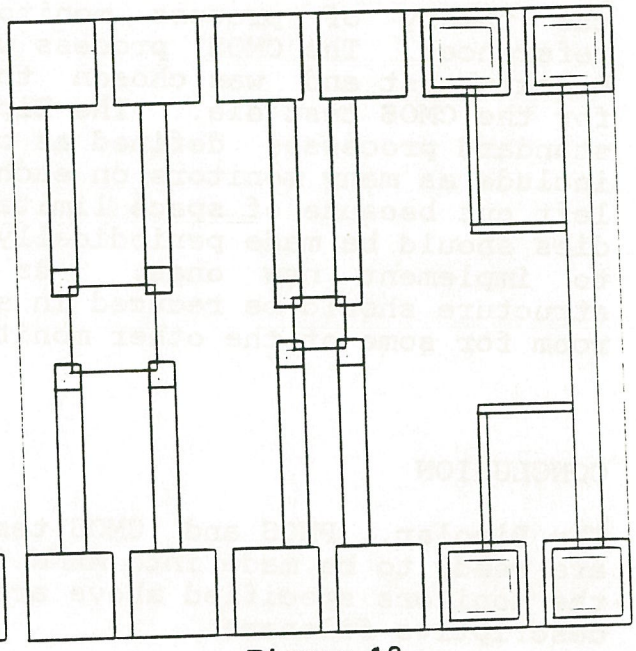

Figure 10
N-diffusion
100x100um and 60x60um
Van der Pauws [3] and
Linewidth structure [4]

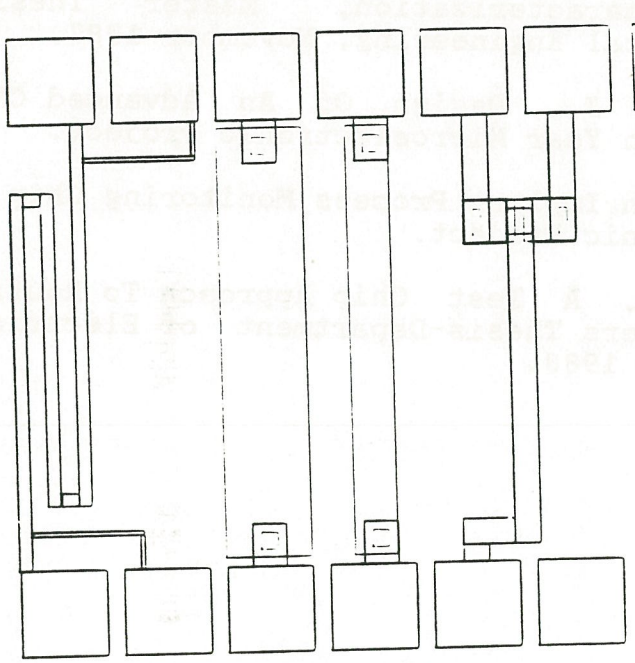

Figure 11
Metal Linewidth structure [4]
with P-diffusion resistors and
L/W of 1/3 PMOS transistor

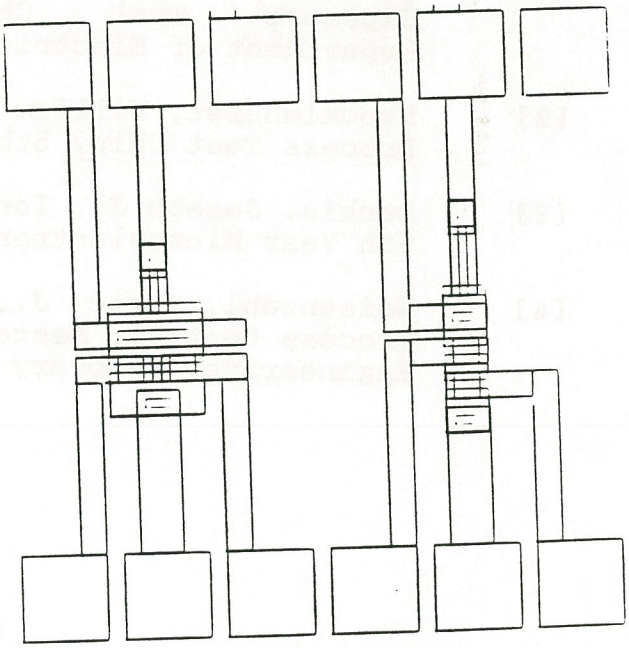

Figure 12
PMOS NOR and NAND gates
with L/W of 1/3 for the
driver transistors

RESULTS/DISCUSSION

The focus of this project was to put together the most used process monitors onto one test die per process. The details on the theory of process monitor design can be found in the references. The CMOS process was defined by senior William J. Brocklehurst and was chosen to be used in the test mask design for the CMOS test die. The Bipolar and PMOS processes are the standard processes defined as of May 1988. While I attempted to include as many monitors on each die as possible, some had to be left out because of space limitations. Re-evaluation of the test dies should be made periodically to discard unused monitors and to implement new ones. As a recommendation, the serp/comb structure should be reduced in size on the CMOS test die to allow room for some of the other monitors.

CONCLUSION

The Bipolar, PMOS and CMOS test die designs are complete. They are ready to be made into MANN files and mask reticles. Each of the monitors specified above are in a separate symbol file with a descriptive filename.

REFERENCES

[1] Benamanti, Brian L., A Multipurpose Test Mask For Exposure Tool Characterization, Master Thesis-Department of Electrical Engineering, November 1987.

[2] Brocklehurst, William J., Design Of An Advanced CMOS Process Test Chip, 5th Year Microelectronic Project.

[3] Burkis, Joseph J., Ion Implant Process Monitoring Chip, 5th Year Microelectronic Project.

[4] Meisenzahl, Eric J., A Test Chip Approach To Routine Process Control, Masters Thesis-Department of Electrical Engineering, February 1988.