FABRICATION OF A SINGLE LEVEL METAL CCD SHIFT REGISTER

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ABSTRACT

Using a "shadow mask" technique, a single level metal 3-phase CCD shift register was fabricated with electrode separations of 2 microns. Testing is pending at this time.

INTRODUCTION

A Charge-Coupled Device, or CCD, is essentially a linear array of closely spaced MOS capacitors. A three phase CCD shift register is realized by terminating such an array with a diode at each end (to inject and detect minority carriers), and connecting every third gate to a common conductor. A cross section of a three phase CCD shift register is shown in Figure 1.

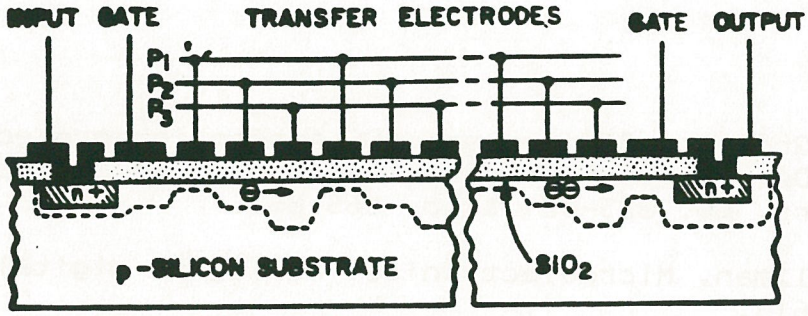


Figure 1: Cross section of a three phase CCD shift register.[1]

Consider such a device fabricated on a P-type substrate. When a large positive voltage is present on the first electrode in the array, a depletion region is formed in the underlying silicon, temporarily creating a potential well for electrons, as shown in Figure 2a. Electrons injected from the input diode accumulate in the potential well formed under the electrode. If a positive voltage is simultaneously applied to an adjacent electrode, the potential wells overlap and any charge stored under the first electrode is now shared between the two, as shown in Figure 2b (hence the term "charge-coupled"). It follows that when the bias is removed from the first electrode, the charge is transfered completely under the second, as shown in Figures 2c and 2d. A similar transfer moves the packet of charge under the third electrode. When the electrodes are pulsed with overlapping clock pulses, as shown in Figure 2e, a moving array of potential wells is established. In this fashion, packets of electrons supplied from the input diode are shifted sequentially through the device, to be detected at the output diode.

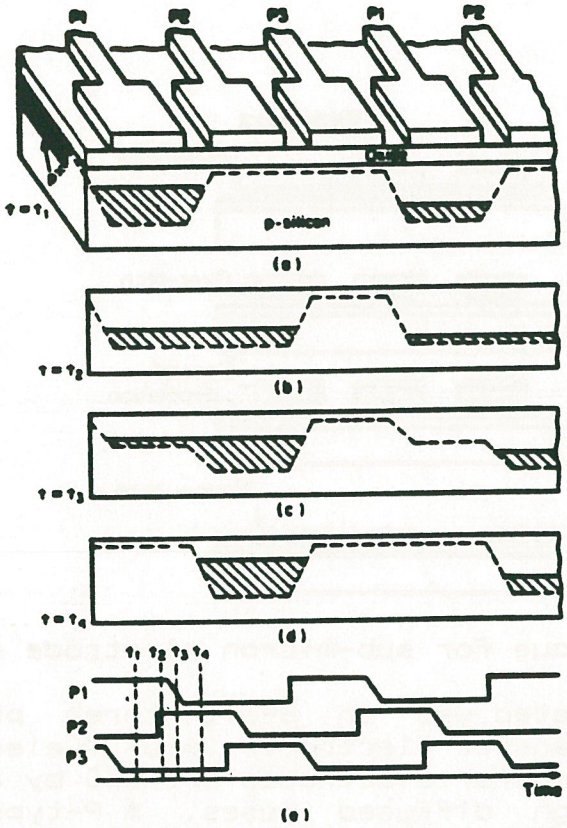


Figure 2: Operation of a three-phase CCD.[1]

The potential wells do not last indefinitely, and eventually, thermally generated electrons fill the well completely. Thus the CCD is a dynamic device, in which charge may be stored for times shorter than the thermal relaxation time of the capacitors. This time varies from one second to several minutes, depending on the processing.[2]

Critical to the operation of the device is spacing the electrodes close enough so that their depletion regions overlap. If they do not overlap no charge-coupling takes place and the device fails. For transfer efficiencies compatible with today's technology, this spacing must be less than three microns[2], which presented a problem. Silver halide masks are currently employed at RIT and as a result the current minimum feature size restriction is ten microns. This restriction was overcome by employing a "shadow-mask" technique developed by Browne and Perkins.[3,4] The technique involves defining every other electrode in the array with photoresist on a thick layer of aluminum. The metal is then etched to clear, and carefully overetched, producing an overhang structure. A second thinner layer of metal is deposited over the entire wafer. By virtue of the overhang, solvent access to the photoresist is guaranteed and the unwanted metal over the resist is lifted off in an ultrasonic acetone soak. The remaing device features are defined in a subsequent photoresist application. The result is a linear array of electrodes, with the seperations between them determined by the degree of overetch. Using this technique it is possible to fabricate single level metal structures with spacings as close as one half of a micron. This lower limit is imposed to allow for possible lateral surface migration of aluminum during the second metal deposition, which could short the device.An outline of this technique is shown in Figure 3.

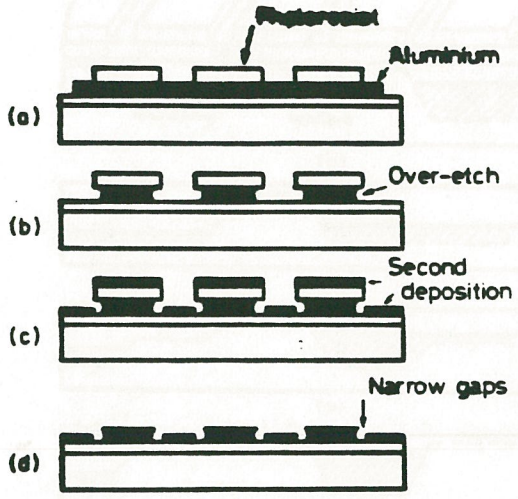
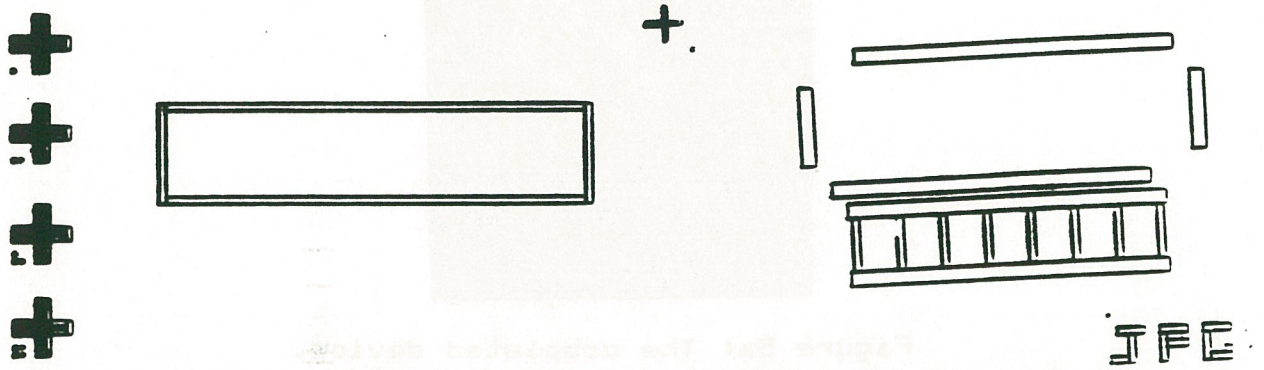


Figure 3: A technique for sub-micron electrode spacing.[3]

The device fabricated was an 8-bit three phase CCD, and therefore has 24 transfer electrodes, plus 4 electrodes for the input/output. The transfer electrodes are 250 by 40 microns and are contacted through diffused buses. A P-type substrate was chosen for two reasons. First, in a P-type substrate the minority carriers are electrons, which have higher mobility than holes and should therefore result in higher transfer efficiencies. Second, for a silicon dioxide insulator on P-type substrate the fixed charge held near the surface is positive and the silicon at the interface is held in depletion even at zero volts bias, again improving the efficiency of the device. The transfer channel was surrounded by a P-type channel-stop diffusion. The resulting high majority carrier density prevents the formation of a depletion region of any significant width, creating a surface potential wall around the transfer channel. This serves to laterally confine the direction of charge transfer, and electrically isolate the device.

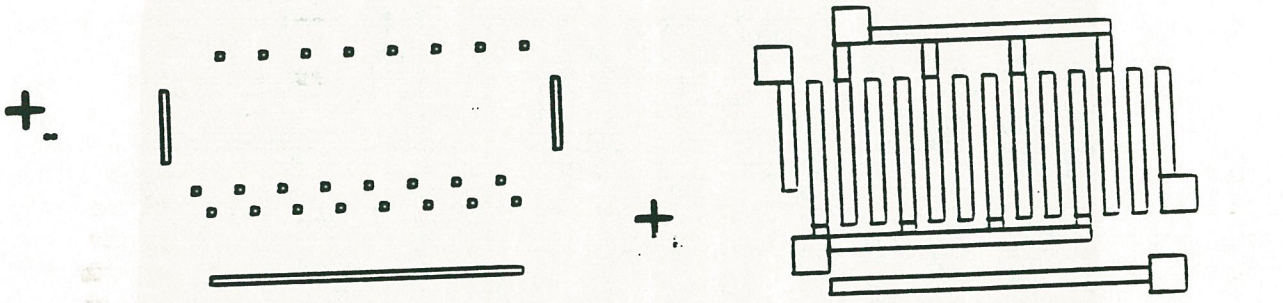
EXPERIMENT

Fabrication commenced with the growth 5000 angstrom masking oxide on a P<100> 14-22 -cm substrate at 1100C in wet O2 for one hour. Windows were opened in the oxide and boron was diffused using Allied B150 spin-on dopant source to define the P-type channel-stop. The masking oxide was removed and again regrown to 5000 angstroms and windows opened to define the input/output diodes, as well as the phase one, two and three clock buses. Phosphorous was diffused into these regions using Emulsitone N-250 spin-on dopant source. The oxide was again stripped and a 700 angstrom gate oxide was grown at 1100C in dry O2 for 25 minutes, through which contact cuts were opened. The wafer was coated with a thick layer of aluminum, and using the shadow mask technique, the electrode structure was fabricated. Figure 4 displays the five mask levels.



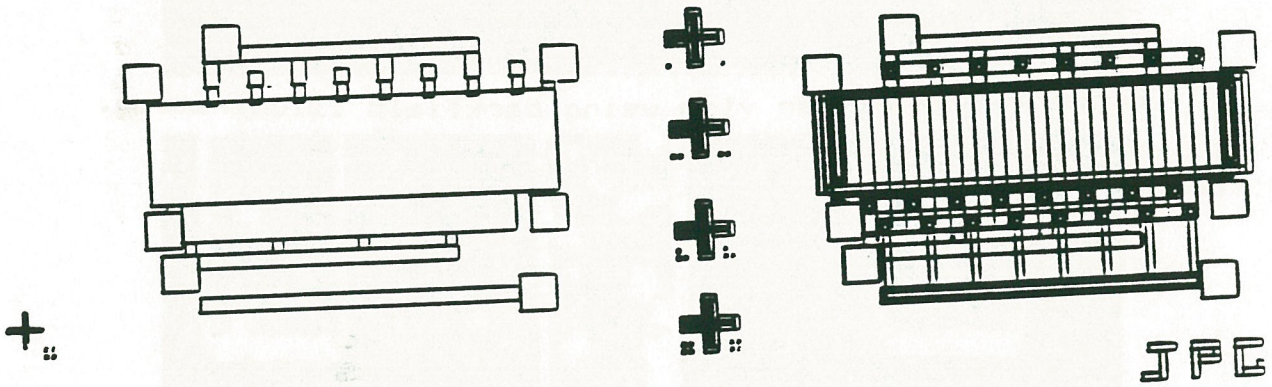
LEVEL 1: P-type channel stop.

LEVEL 2: Diode and clock bus.



LEVEL 3: Contact Cuts.

LEVEL 4: Every other electrode.



LEVEL 5: Remaning device features.

An overlay of all levels.

Figure 4: Masking levels for single level metal CCD.

RESULTS/DISCUSSION

Figure 5a shows a micrograph of the completed device, 5b a closer view using darkfield illumniation, and 5c displays a close-up of the electrode structure, also using dark field. Using the "shadow-mask" technique, electrode separations of approximately two microns were obtained for a three and half minute time to clear and a one minute overetch. Yield was very high for this proess step. Subsequent attempts may obtain closer spacing using a shorter overetch time.

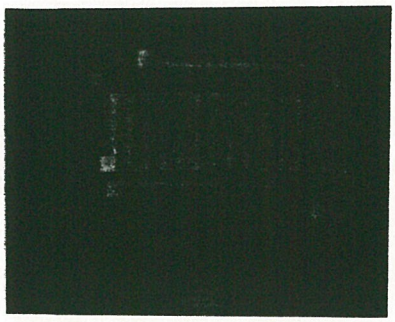


Figure 5a: The completed device.

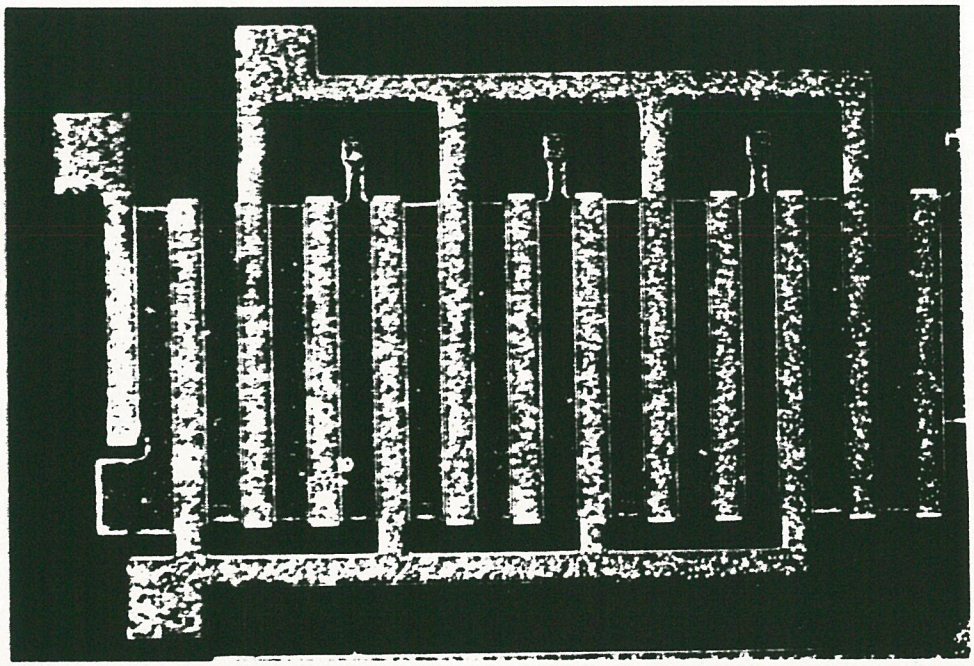


Figure 5b: A closer view using darkfield illumination.

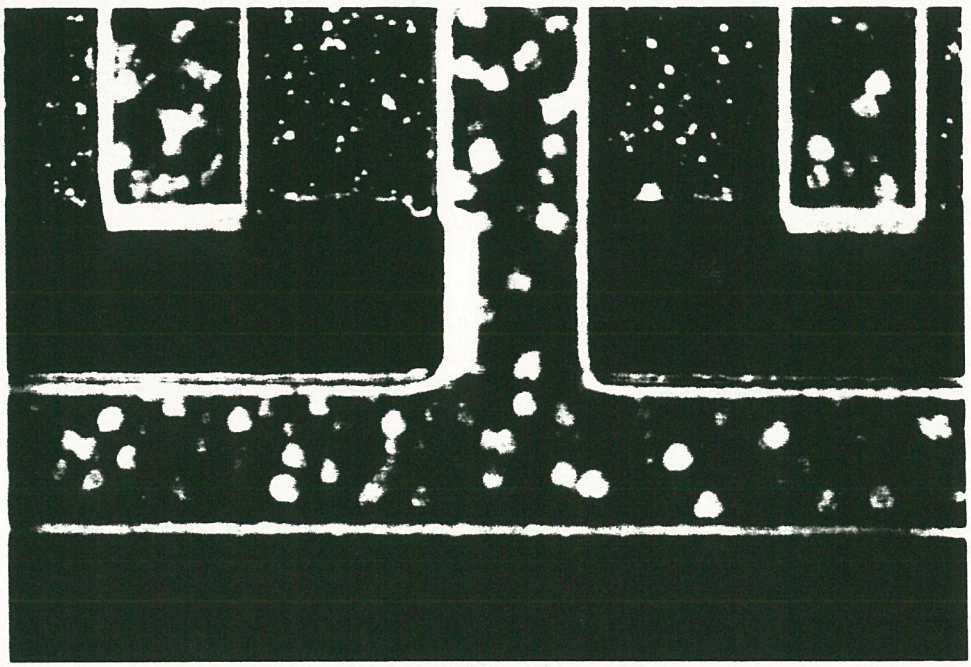


Figure 5c: A close-up of the electrode structure. Electrodes are 40 microns wide, separation 2 microns.

CONCLUSIONS

An 8-bit three phase single level CCD shift register with 2 micron separation between electrodes was sucessfully fabricated using the "shadow-mask" technique.

ACKNOWLEDGEMENTS

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REFERENCES

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