DESIGN OF A 4-BIT PMOS PARALLEL COMPARATOR A/D CONVERTER

Amel Gaddo
5th year Microelectronic Engineering Student
Rochester Institute of Technology

ABSTRACT

This project dealt with the design of a 4-bit PMOS parallel comparator analog-to-digital converter. Using a predesigned comparator circuit, the rest of the logic was completed. Circuit analysis was performed using SPICE simulation. Circuit layout was done using Integrated Circuit Editor (ICE). The PMOS process consists of four masking levels; diffusion, thin oxide, contact cuts, and metal.

INTRODUCTION

There are various circuits to accomplish A/D conversion, some of which are parallel-comparator, successive-approximation, digital ramp, and integrating A/D converters. The parallel or flash converter was chosen for this project since it is the simplest and fastest of all of the other types. The disadvantage of this type of converter is the complexity of the hardware. Since the number of comparators needed is 2EN - 1, where N is the desired number of bits, the number of comparators doubles for each added bit.[1]

Figure 1 shows the basic architecture of a 4-bit parallel A/D converter. The number of comparators and reference levels needed is 15 and 16 , respectively. The analog signal voltage, Va, is fed one input of each of the comparators simultaneously. The other input is connected to a reference voltage, Vref. The voltage reference is tiered down into equal steps through the resistor ladder. The output of the voltage comparators will be low for all those whose Vref is greater than Va, and high for those which is smaller than Va[2]. Figure 2 shows the output states of the voltage comparator.

The segment detection logic circuit, refer to Figure 1, is used to simplify the design of the encoder. It consists of fourteen 2-input NOR gates where one input is the output of one of the comparators, and the other is the inverted output of the comparator below it. The logic symbol, Boolean expression, truth table, and circuit design are shown in Figure 3.

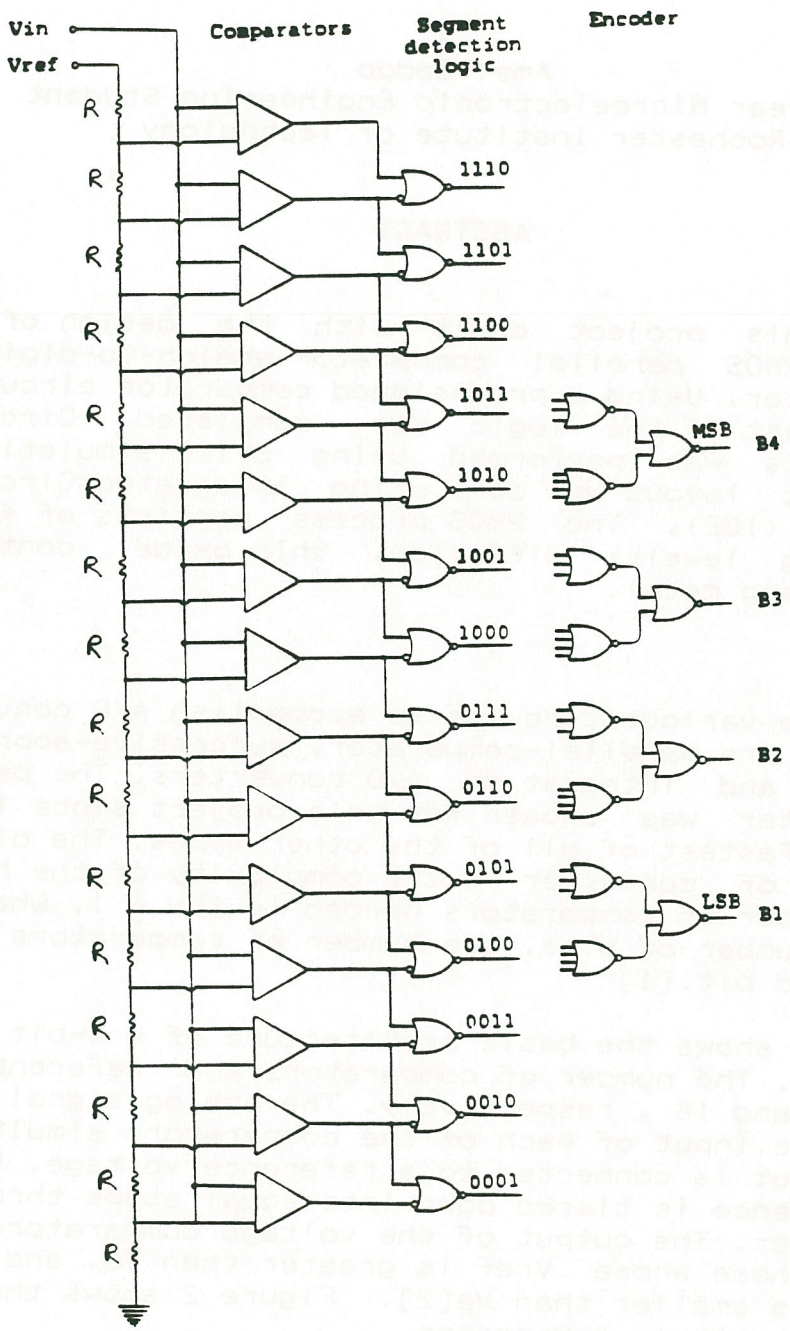


Figure 1. Basic Architecture of a 4-Bit A/D Converter

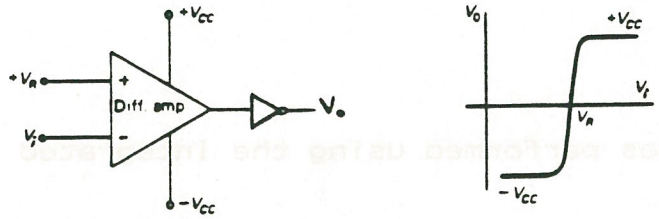
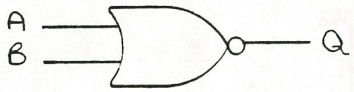


Figure 2. DIFF AMP comparator

THE advantage of the segment detection logic is that only one segment output will be high at a time since the output of the NOR gate is high only when both inputs are low. This in turn will make the design of the encoder easier.[1]

The encoder design consists of eight NOR gates where four of them have four inputs and the rest have three inputs. The outputs of each two adjacent 4-input and 3-inpt NORs are fed into another NOR gate whose output correspond to a certain bit. The digital output generated by the encoder corresponds to the highest comparator activated by the input voltage times the size of the voltage reference step. The input of each of the eight NOR gates is taken in the following manner : A binary code is assigned to the output of the segment detection logic from (0001 - 1110) where the left most number corresponds to MSB and the right most to LSB. If LSB is equal to 0, then the output is fed to the first and second NOR gates of the encoder, while if the MSB is equal to 0 then the output is fed to the seventh and eighth NOR gates.



Q = A + B

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

Figure 3. Logic symbol, Boolean expression, and Truth table of a NOR gate

EXPERIMENT

SPICE simulation was used to analyze the subcomponents of the A/D converter circuit. These include the comparator circuit and the NOR gates. The transistor model used in these simulations is the following:

Substrate doping	= 1.2e15 /CC
Oxide thickness	= 700 Angstroms
Channel Length Modulation	= 0.02 /V
Surface Mobility	= 200 sq-cm/V-S
Junction Depth	= 2 Microns
Surface State Density	= 8E11 /sq-cm
Source and Drain Resistance	= 100 OHMS
Gate to Source Capacitance	= 3.45 nF
Gate to Drain Capacitance	= 3.45 nF
Gate to Substrate Capacitance	= 1.38 nF
Junction Capacitance	= 98.6 uF

The circuit layout was performed using the Integrated Circuit Editor (ICE).

RESULTS/DISCUSSION

The PMOS circuit used in the comparator is basically a differential amplifier with the inverting input tied to the analog input. The differential amplifier is designed to use two inverters with the source of their drivers coupled and driven by a current source, as shown in Figure 4. The ratio of the pull-up to pull-down of the inverters is 400:1 for optimum gain. The current source was designed to supply 9.06 microamps and has an output impedance of 86 Kohms. SPICE simulation shows that the comparator circuit works for reference voltages from 0 to -10 volts and will convert an analog signal into a digital output with a resolution of 0.16 volts. The simulation of the NOR gates shows that the gates have a rise time of 24 nanoseconds. The ratio of the pull-up to the pull-down of the NOR used was 16:1. Figure 5 shows the schematic of a NOR gate with one inverted input.

The final chip design covers an area of 4700x3200 microns and the circuit uses 225 transistors.

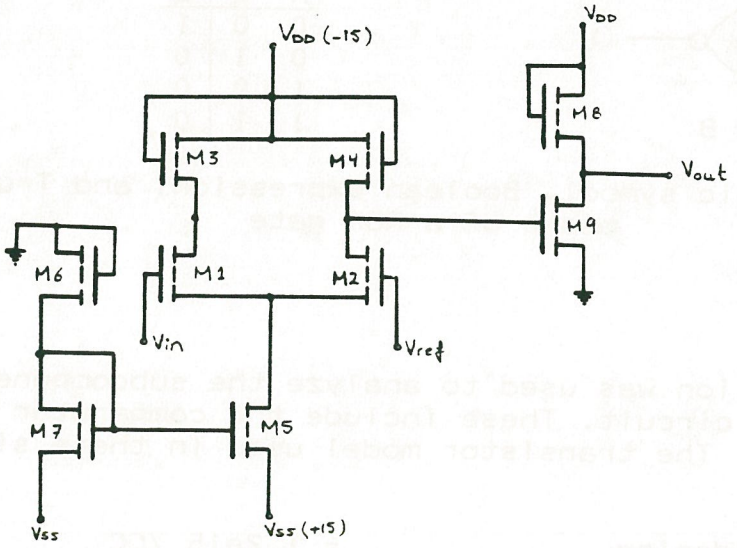


Figure 4. Voltage Comparator Circuit

CONCLUSION

A PMOS A/D converter was designed and laid out using 10 microns design rules. This design is fully compatible with RIT's present maskmaking and fabrication capabilities.

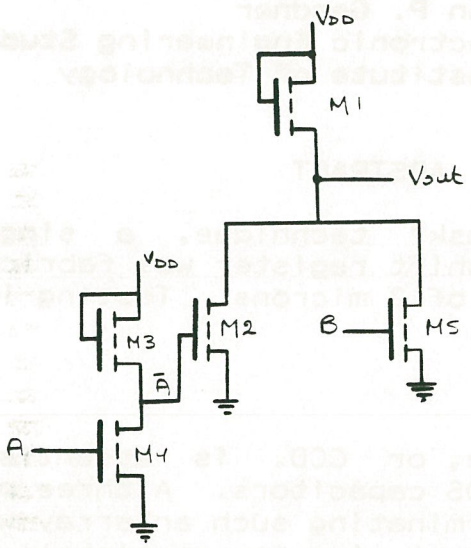


Figure 5. Schematic Representation of the 2-input NOR gate with one inverted input

REFERENCES:

[1] Alan B. Grebene, Bipolar and MOS Analog integrated circuit design. Data conversion circuits: analog to digital converters, pp. 825-827 & pp. 865-867.

[2] Jacob Millman, Microelectronics. Analog to digital converters, pp. 612-613.

[3] Michael M. Cirovic, Basic Electronics, second edition, Comparators, pp. 494-495.