

16 x 1 nMOS STATIC RANDOM ACCESS MEMORY DESIGN

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ABSTRACT

A Static Random Access Memory (SRAM) was designed using a 2 micron minimum geometry, nMOS fabrication process on an Apollo design station. In addition to the SRAM integrated circuit, test structures were included to help characterize the process and design. The chip contained over 200 transistors on a die size of 800 square microns. Simulation results predicted an access time of 50 nano-seconds. The pads were configured to fit a 20 pin probe card to facilitate automatic testing.

INTRODUCTION

The design of any complex integrated circuit needs to be reduced into its component parts. A hierarchical approach can be used in which circuits are built from the bottom up. Cells are made to represent the commonly used parts and combined to form the final circuit. *MentorGraphics is a design software company that has implemented this approach to VLSI design.

As shown in Figure 1, the first phase of any hierarchical design is the creation of the basic cells. These schematics are then entered into the computer through the NETED software package. NETED is a schematic capture program which converts circuit diagrams into nodelists. These nodelists, in conjunction with a transistor Models file, define the circuit, interconnections, and the device characteristics of the nMOS transistors.

Circuit simulations are performed with the MSIMON software package. This program is similar to SPICE but optimized for MOS devices. For each cell, input waveforms had to be determined in order to provide thorough simulation of all combinations of inputs. Results often indicate the need for changes to the circuits. After the cells operate correctly, they are combined and tested in larger groups.

After correct circuit simulation layout is performed. This is the transformation of the schematics into the various levels

* NETED, MSIMON, CHIPGRAPH and DRACULA are proprietary products of MentorGraphics Corporation.

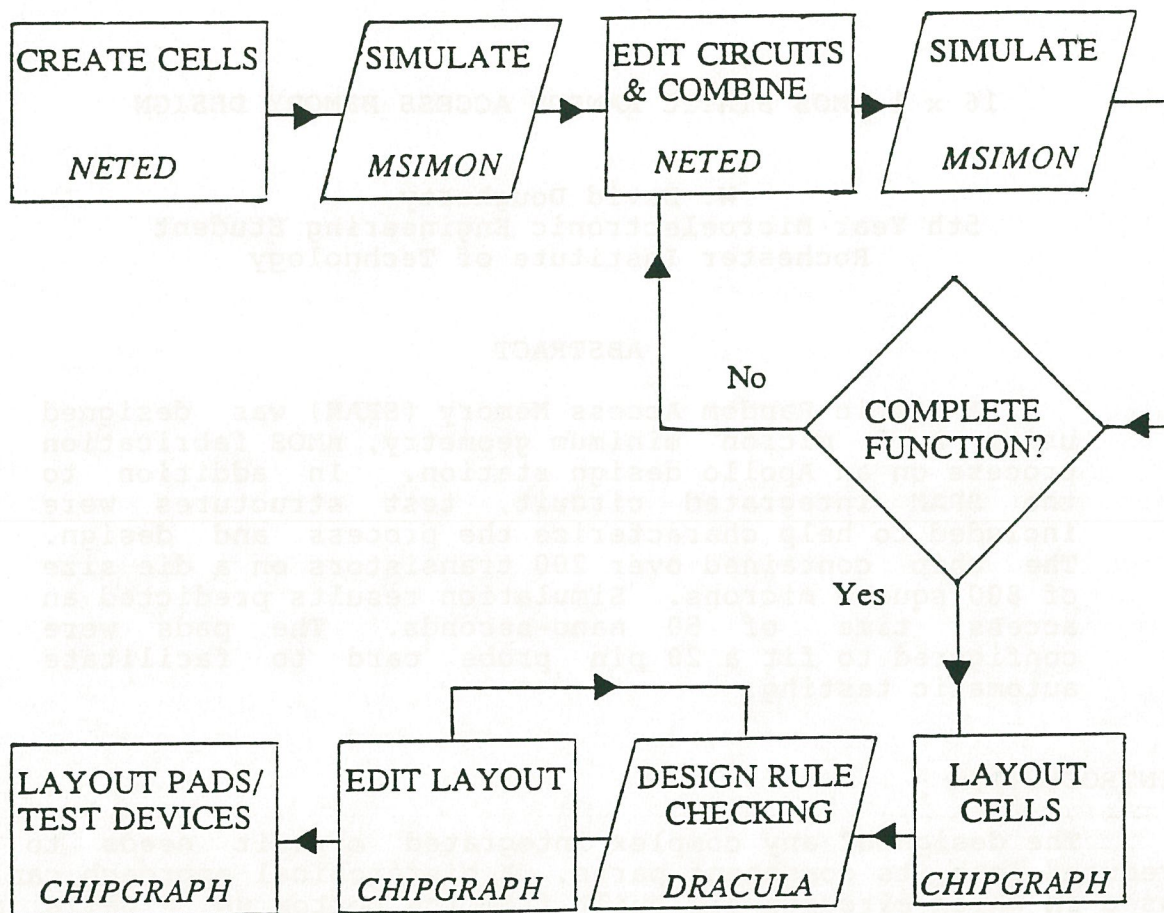


FIGURE 1: DESIGN FLOWCHART

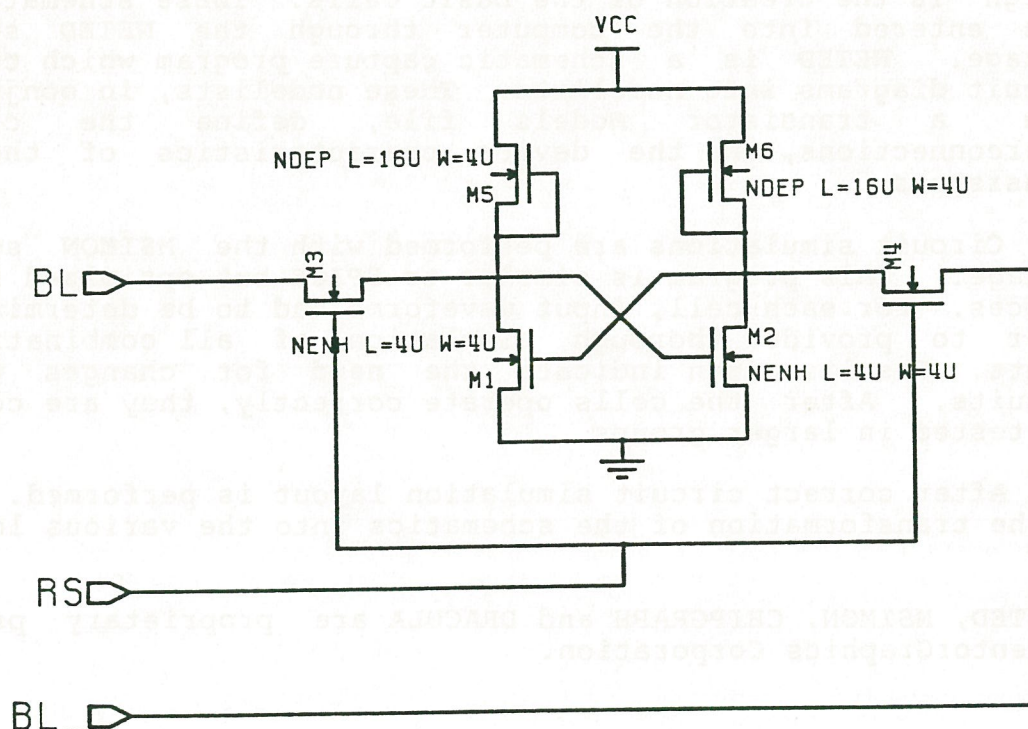


FIGURE 2: STATIC MEMORY CELL

of an integrated circuit. In the nMOS process the following layers were needed; n+ diffusion, n implant, poly-silicon, contact cuts and metal. The CHIPGRAPH program is used to graphically represent these layers. Standard cells for the more commonly used circuits are laid out first, then combined. The remainder of the circuits were added on to this array and created the actual SRAM chip. Input/Output pads were carefully placed for convenient automatic probing based on RIT's probe card configuration.

After layout each cell was verified using DRACULA, a design rule checker, configured to check the layout against Mead-Conway design rules. DRACULA catches the human errors associated with a large scale integrated design.

EXPERIMENT

The fundamental cell in the 16 x 1 SRAM was the memory cell, shown in Figure 2. This cell consists of two cross coupled inverters with depletion mode transistor loads and two pass transistors. This cell uses the bit lines BL and BL which contain the data signal, its complement, and the Row Select, (RS). When a memory cell is going to be accessed RS goes high, which biases the pass transistors and allows data to flow into or out of the cell.

The sense amplifier, shown in Figure 3, also uses two cross coupled inverters, however there is a pass transistor to ground controlled by the SENSE signal and no pass transistors on the bit lines. The sense amplifier's function is to boost the output signal during the read cycle and to be off during the write cycle and dormant states. This is important because the bit lines are run in poly-silicon and through pass transistors so losses are expected to occur between memory cell and outputs.

The SENSE and RS signals are provided through two line decoders, one of which is shown in Figure 4. This circuit provides a 2 to 4 decoder function. Using one as a row decoder and the other as a column decoder, all 16 memory cells can be individually addressed. The line decoder is a pass transistor network which only functions when the chip enable, (CE) line is high. A0-3 are the address lines.

These components were combined to provide a 4 x 1 memory element. This combined 4 memory cells, sense amp, and line decoder. Additional control logic for Write Enable, (WE), was added as a component of the SENSE signal and DATA was connected to the bit lines. The circuit was then simulated by providing force pulses which would write a '1', read a '1', write a '0', read a '0'.

Once these functions were performed successfully, this column was replicated four times to create a 16 x 1 memory array. This circuit was simulated, modified and the final circuit is shown in Figure 5, in which the actual circuits are represented

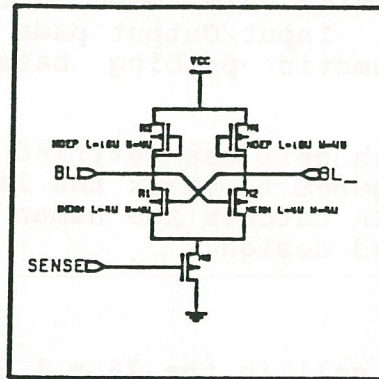


FIGURE 3: SENSE AMPLIFIER

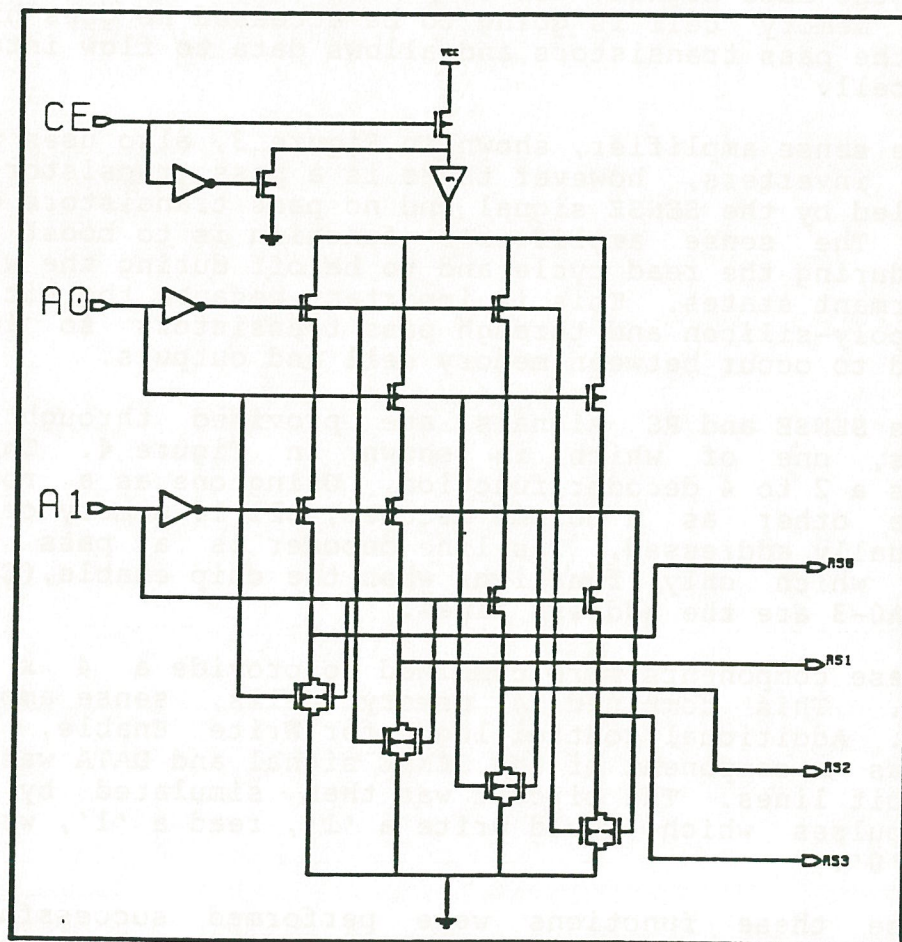


FIGURE 4: LINE DECODER

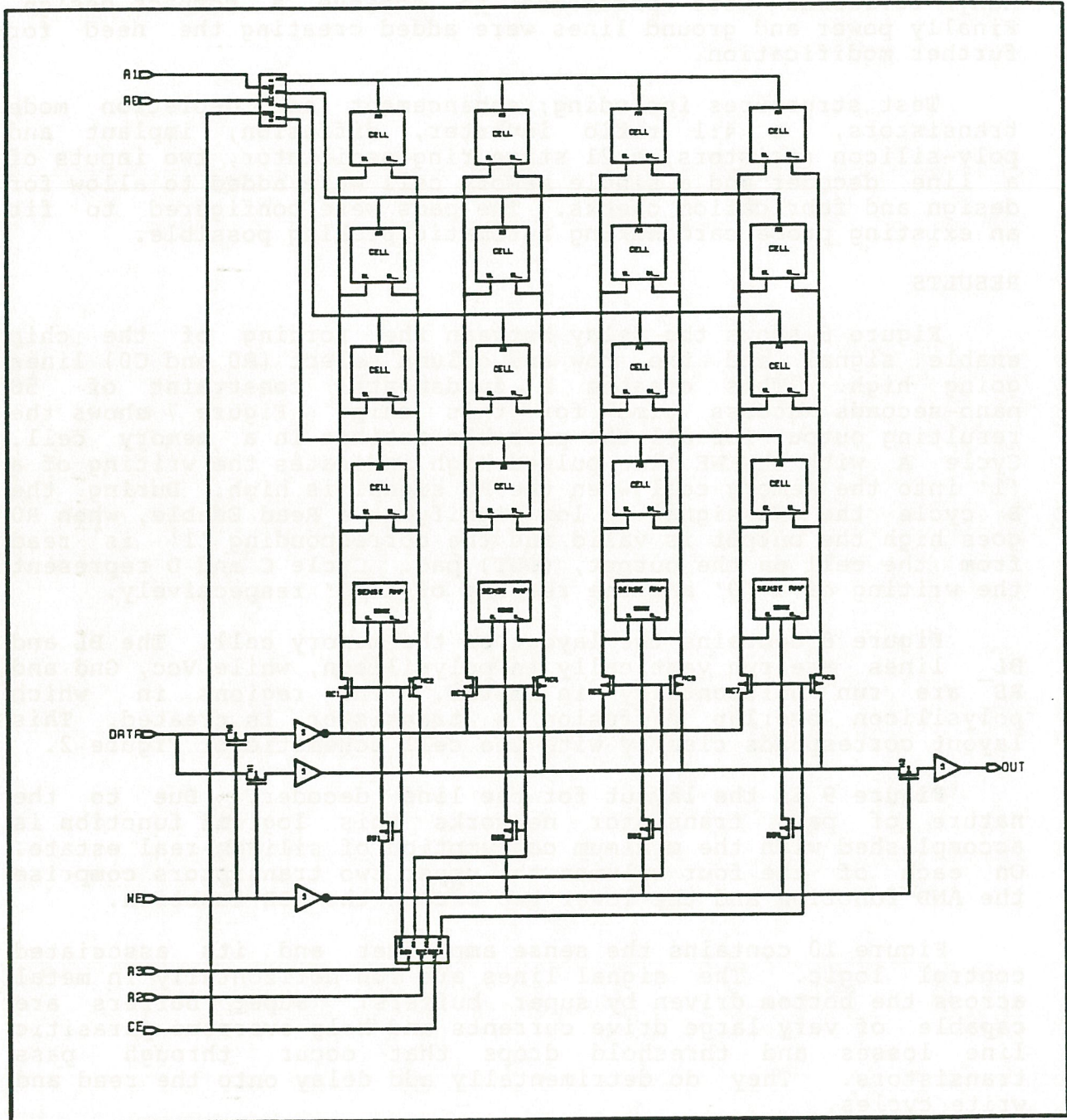


FIGURE 5: SRAM FUNCTIONAL DIAGRAM

symbolically in the various blocks labeled cell, sense amp and row decoder.

Layout followed a similar technique starting with the creation of basic cells. Special effort was made to have the SRAM cell and sense amp be the same size in order for the control lines to run together efficiently. The cells were then replicated and combined to form the correct functional groups. Many revisions were performed to achieve a compact design. Finally power and ground lines were added creating the need for further modification.

Test structures including; enhancement and depletion mode transistors, a 4:1 ratio inverter, diffusion, implant and poly-silicon resistors, a 21 stage ring oscillator, two inputs of a line decoder and a single memory cell were added to allow for design and fabrication checks. The pads were configured to fit an existing probe card making automatic probing possible.

RESULTS

Figure 6 shows the delay between the forcing of the chip enable signal and the row and column select (R0 and C0) lines going high. This creates a fundamental constraint of 50 nano-seconds access time for this chip. Figure 7 shows the resulting output for all the possible actions in a memory cell. Cycle A with the WE line pulsed high indicates the writing of a '1' into the memory cell when the R0 signal is high. During the B cycle the WE signal is low signifying a Read Enable, when R0 goes high the output is valid and the corresponding '1' is read from the cell on the output, (OUT) pad. Cycle C and D represent the writing of a '0' and the reading of a '0' respectively.

Figure 8 contains the layout of the memory cell. The BL and BL₋ lines are run vertically in polysilicon, while Vcc, Gnd and RS are run horizontally in metal. The regions in which polysilicon overlap diffusion a transistor is created. This layout corresponds clearly with the cell schematic of Figure 2.

Figure 9 is the layout for the line decoder. Due to the nature of pass transistor networks this logical function is accomplished with the minimum consumption of silicon real estate. On each of the four columns the upper two transistors comprise the AND function and the lower two create the NOR function.

Figure 10 contains the sense amplifier and its associated control logic. The signal lines are run horizontally in metal across the bottom driven by super buffers. Super buffers are capable of very large drive currents and help overcome parasitic line losses and threshold drops that occur through pass transistors. They do detrimentally add delay onto the read and write cycles.

U(R0)
U(CE)
U(C0)

ROW/COL SELECT US CE

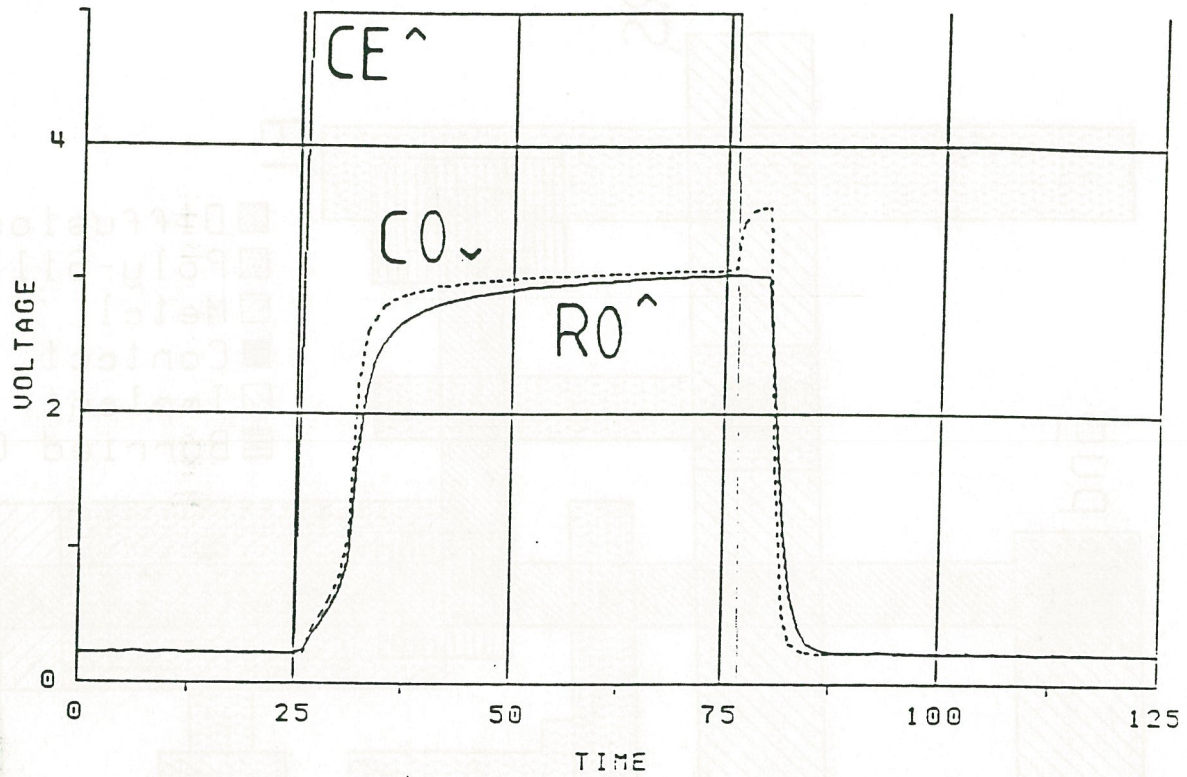


FIGURE 6

U(R0)
U(OUT)
U(WE)

READ/WRITE CYCLE

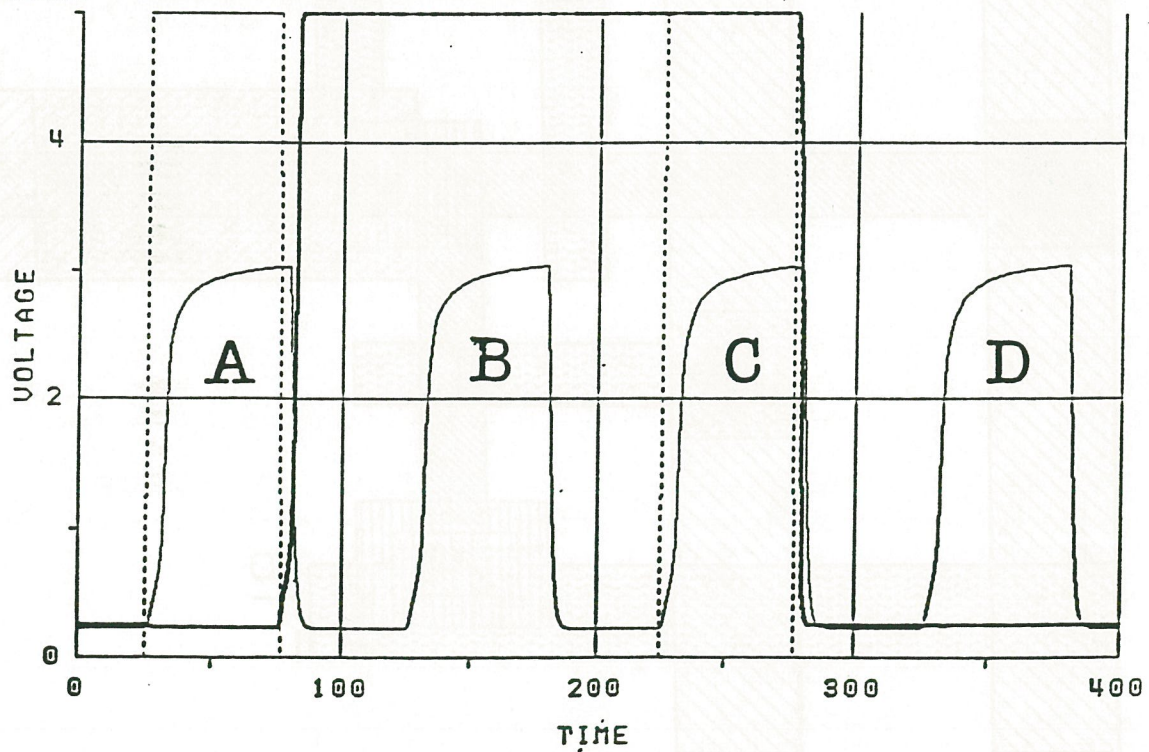


FIGURE 7

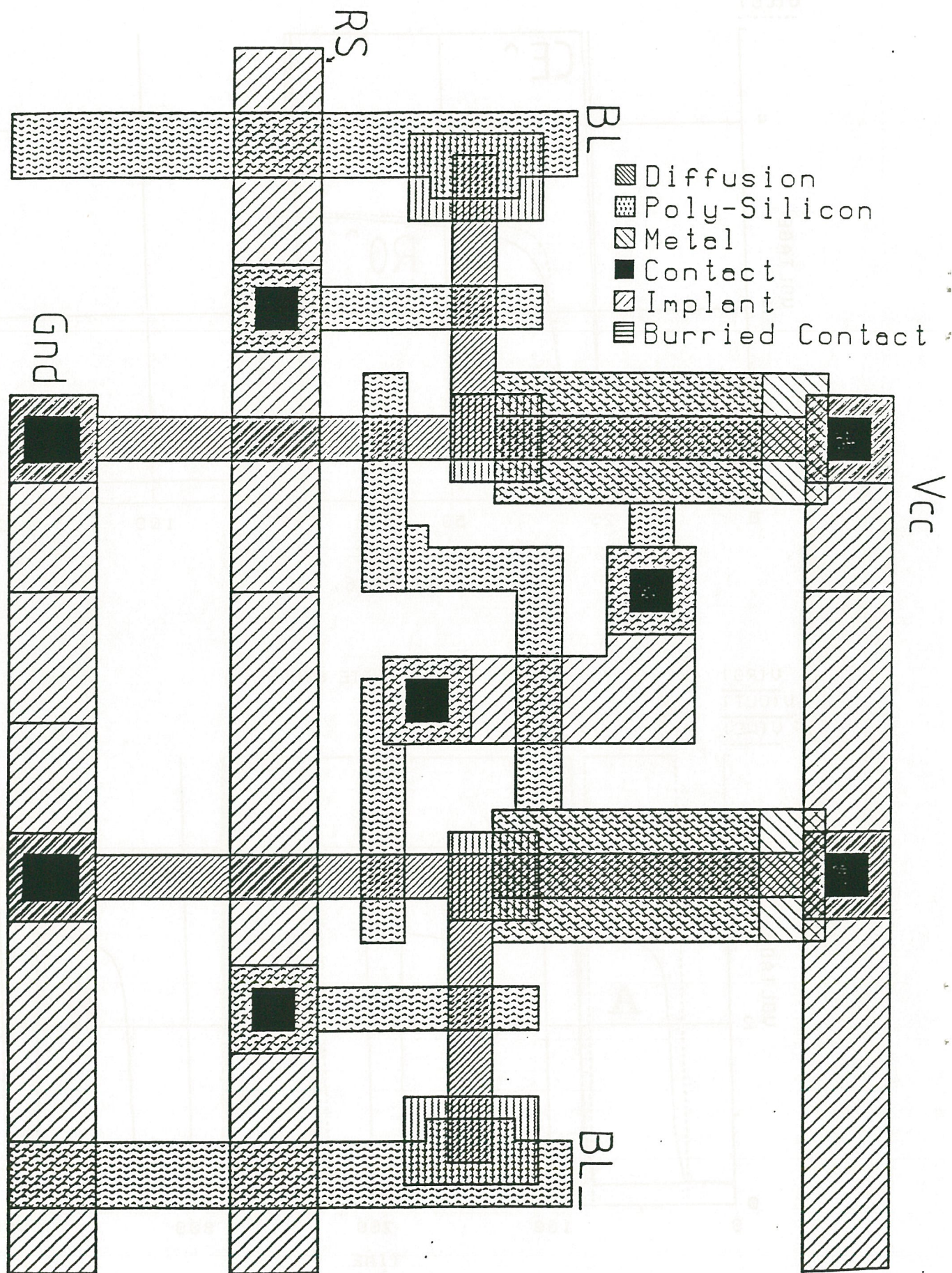


FIGURE 8: SRAM MEMORY CELL LAYOUT

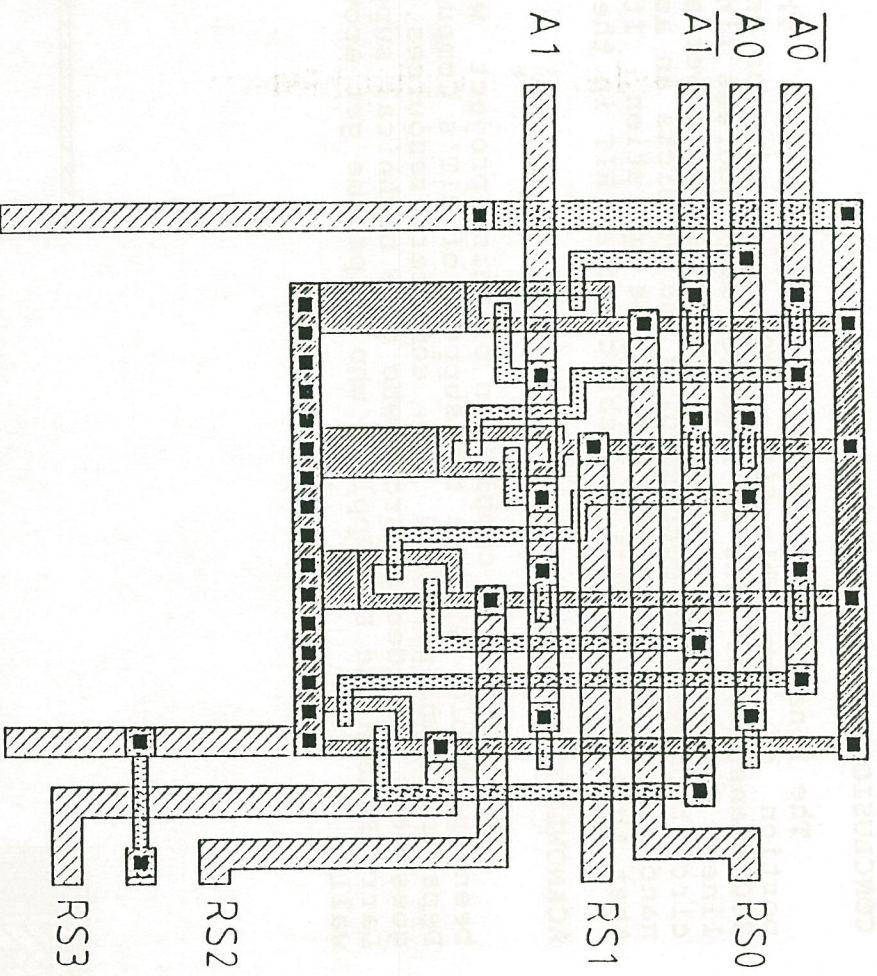


FIGURE 9: LINE DECODER LAYOUT

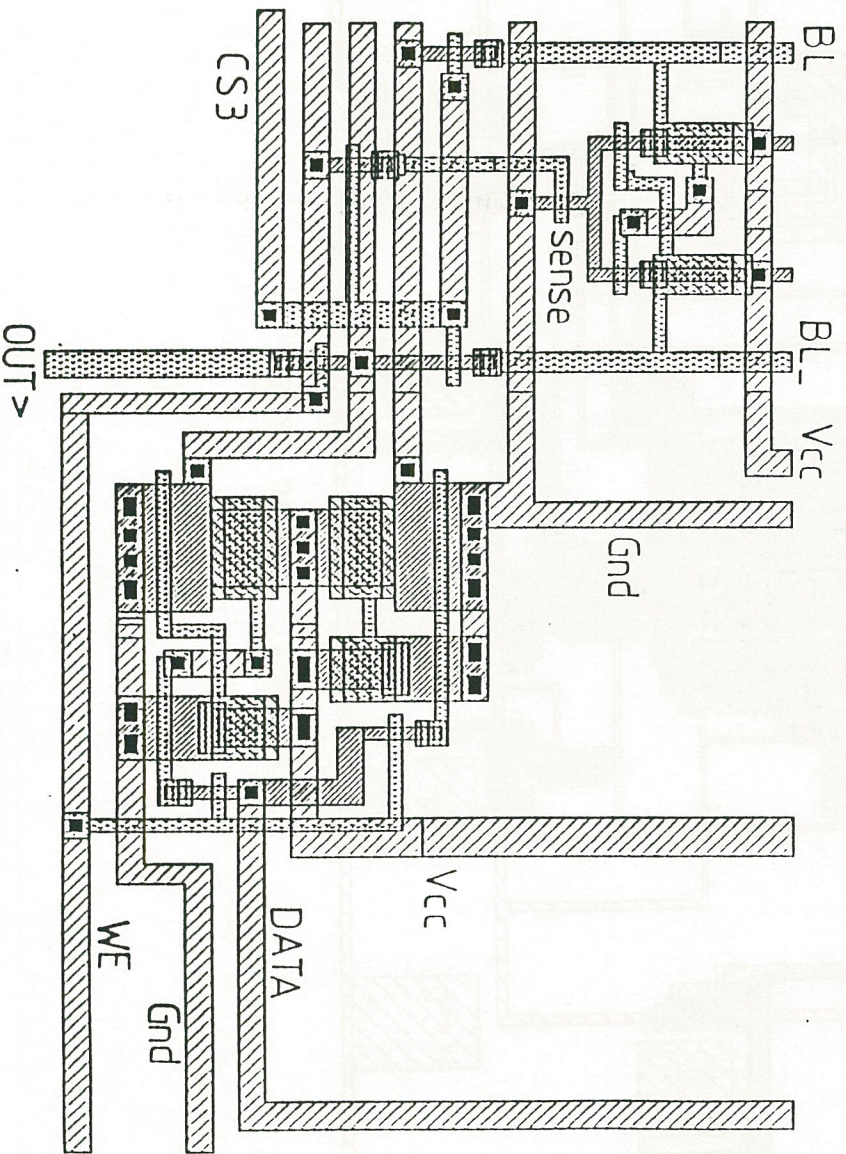


FIGURE 10: SENSE AMPLIFIER AND CONTROL LOGIC LAYOUT

CONCLUSION

The final chip is shown in Figure 11. The actual SRAM portion of the chip fills 800 square microns and contains over 200 transistors. The IC requires four address lines, 2 control lines, 2 Input/Output lines in addition to power and ground. The circuits simulated successfully and predicts an access time of 50 nano-seconds for a given Read/Write operation. It is anticipated that this project will be fabricated at RIT in the future.

ACKNOWLEDGEMENTS

The successful completion of this project would not have been possible without the support of RIT's Computer Engineering Department who provided the computer resources. Appreciation goes to Dr. George Brown who gave technical support along with Larry Reuben and Bob Appleby who helped me get around the brick walls.

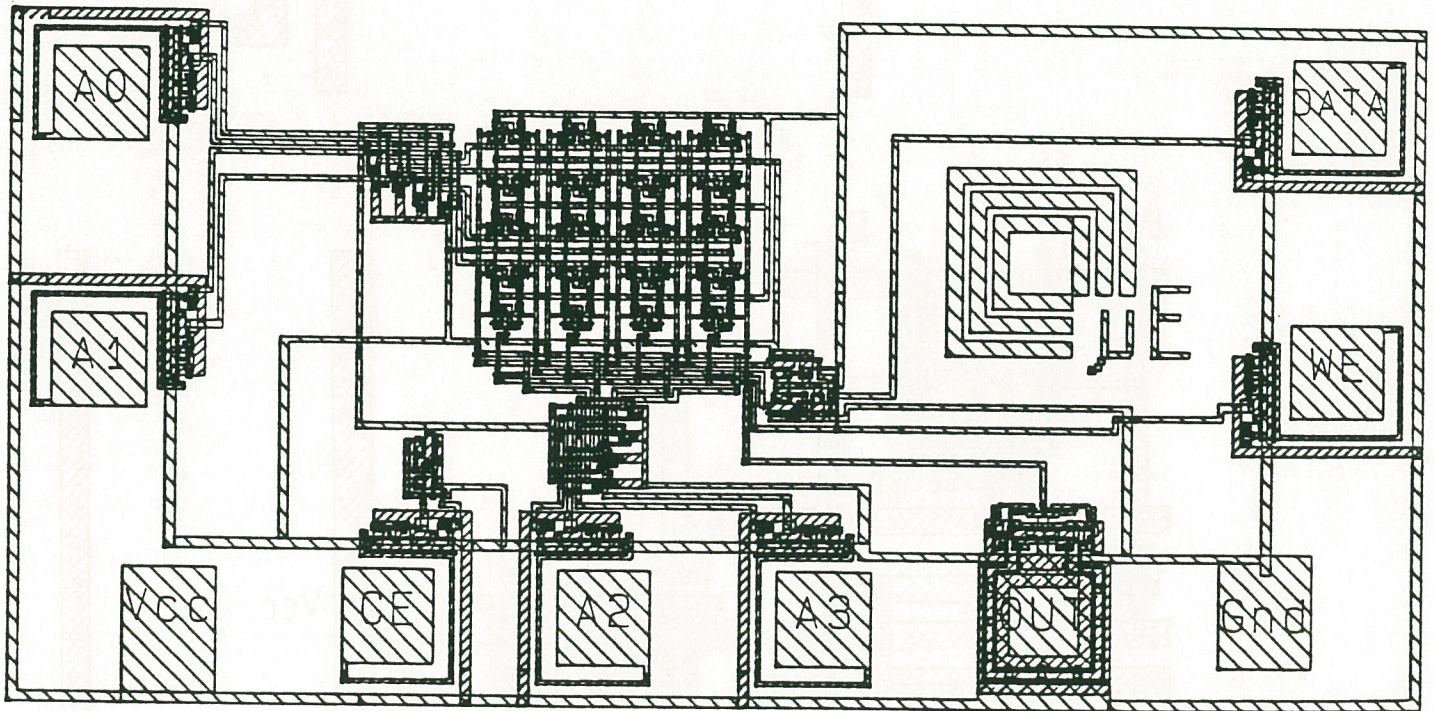


FIGURE 11: SRAM IC LAYOUT