

## Multilevel Metallization at RIT

Manuel N. Carneiro  
5th Year Microelectronic Engineering Student  
Rochester Institute of Technology

### ABSTRACT

This project was a preliminary study of an aluminum/dielectric/aluminum multilayer metallization scheme. Polyimide and spin on glass were compared using high frequency CV analysis on fabricated capacitors. The simple processing involved showed that good crack-free and adhesive films could be formed with both materials although the polyimide was the more ideal CV characteristics. Test masks were generated to measure via resistance and dielectric breakdown in a bi-level structure. The Spin on Glass processing was unsuccessful because of underetching of vias. The polyimide processing was successful displaying good breakdown characteristics but high via resistances.

### INTRODUCTION

The new VLSI (very large scale integration) era is requiring longer interconnect paths as the density and complexity of the circuits increase [1]. In circuits of several hundred transistors single level metallization becomes severely limiting.

The necessity for multilevel metallization is clear if we consider the circuit performance characteristics. The effect of this increase is best described by the equation [1]:

$$RC = (R_s \cdot L^2) \cdot E_{ox} / X_{ox} \quad (1)$$

where,  $R_s$  is the sheet resistivity of the connection,  $L$  is the length of the connection,  $E_{ox}$  is the permittivity of the dielectric and  $X_{ox}$  is the thickness of dielectric. It can be seen from the above equation that time delays are due to a square relation of the length of interconnects becoming an increasingly limiting factor in performance.

The traditional dielectric for the purposes previously stated has been some type of CVD oxide [2]. Recently, cost and reduced complexity in processing has prompted study of alternative dielectrics. It is the previous work of Robert Newcomb [3], Christopher Knaus [4] and Eric Westerhoff [5] that has shown that both polyimide and spin on glass can be used as an intermediate dielectric layer. This further research is intended to extend their work so that these methods may become workable and comparable. In the past incomplete via cleanout, cracking, and adhesion have been the limiting problems. A modified curing



method will be used to attempt to solve the cracking and adhesion problems. It shall also be necessary to determine the best method for via cleanout in the multilevel test scheme.

The comparison of the spin on glass and polyimide dielectrics can begin by determining the capacitor voltage characteristics of the dielectrics in a standard capacitor structure. In current process technology capacitance-voltage measurements are standard and required in determining dielectric properties [6]. The analysis to be performed can be utilized to determine oxide capacitance, threshold voltage and flatband voltage.

One of the important considerations of the multilevel process is the dielectric strength of the intermediate layer. Each layer must be able to simultaneously hold any necessary voltage with no fear of parasitic conduction through the dielectric. This can be accomplished by simply overlaying the two metal layers thereby forming a capacitor structure. Figure 1 is an example of this dielectric breakdown structure. The dielectric breakdown being measured by applying a voltage on one metal with respect to the other until a predetermined current density is measured.

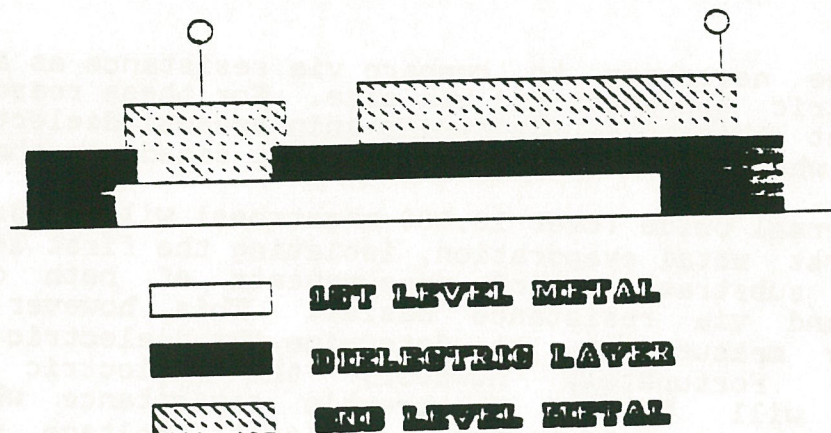


Figure 1: Cross section of breakdown structure [3].

The final test structures which are presented in Appendix A, the ICE (Integrated Circuit Editor) layout, contains six different area capacitors on a die where four wafers will be processed at four different dielectric thickness's.

Another equally important characteristic is the proper formation of vias. Geometric considerations cause via resistance to increase with decreasing via size. This via resistance can adversely effect the time delay of circuits. The expected low resistance of aluminum will necessitate the need for long via chains. This method simply involves dividing the measured resistance by the total number of vias to determine the individual via resistance. The basic structure of the via chains is presented in Figure 2.



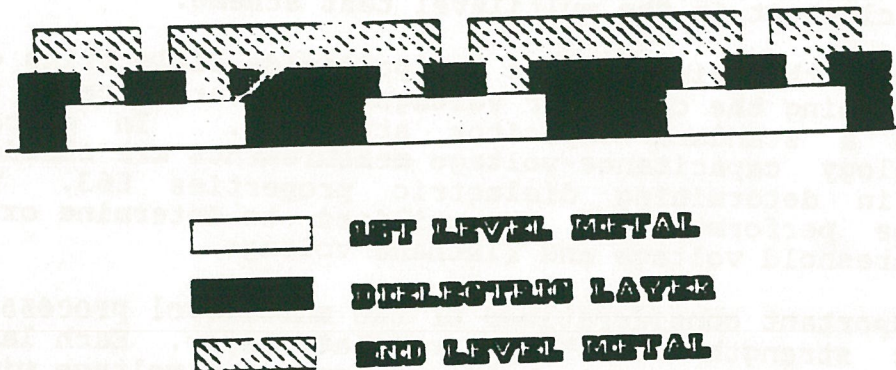


Figure 2: Cross section of via chain structure [3].

It shall be necessary to compare via resistance as a function of, dielectric thickness and via size. For these reasons wafers of different thickness (different spin speeds) dielectrics must be prepared where each contains the varying sized via chains.

A thick thermal oxide (over 10,000 angstroms) will be grown prior to the first metal evaporation, isolating the first level metal from the substrate making measurements of both dielectric breakdown and via resistance easier. This however will make ellipsometry measurement, to determine the dielectric thickness impossible. Fortunately however, the dielectric breakdown structures will have a measureable capacitance which when combined with the calculated capacitance voltage values of permittivity ( $\epsilon_{ox}$ ) will allow us to indirectly determine the thickness's of the test structures.

#### EXPERIMENTAL

The process sequence shall be presented in abbreviated form, where the full description is left for appendix B. This sequence was to first make capacitors to take CV measurements, it could then be seen if in a simply process, crack-free films with good adhesion dielectric properties were possible using these materials. The CV plots are presented in appendix C.

Using the generated test masks (Appendix A) both polyimide and spin on glass bi-level structures could be processed for varying thickness's of the dielectrics.



Four three inch polyimide coated wafers were processed at four different spin speeds given below in order to obtain four different thickness's of the dielectric:

Spin speeds (RPM's)	expected film thickness
1000	greater than 1.0 micrometers
3000	greater than 1.0 micrometers
5000	aprox. 1.0 micrometer
7000	less than 1.0 micrometers

Also processed were four, three inch, spin on glass wafers. Each received four different spin speeds, given below, in order to obtain four different thicknesses of the dielectric.

Spin speeds (RPM's)	expected film thickness (angstroms)
1000	2000
2000	1680
3000	1350
4000	1150

Please refer to references [7] and [8] for information regarding the choice of process cure times and temperatures.

The conclusion of this experimental portion was the measurement of the via resistance and dielectric breakdown characteristics of the materials. The HP-parameter analyser was used in both cases with the plots presented in appendix D.

## RESULTS

The CV plot results presented in appendix C show that the Spin on glass had extreme surface state problems prior to sinter. Ten minutes at 400 C seemed to improve the dielectric to aluminum contact sufficiently to alleviate this problem. The polyimide did not show the extreme pre-sinter surface states but seemed to also improve post-sinter. Both the polyimide and spin on glass CV curves are very positively flat band shifted. The dielectrics are clearly not ideal situations but demonstrated sufficiently good process and high frequency CV characteristics to warrant continuation of the experiment.

The final test structures were more successfully processed in the case of the polyimide dielectric compared to the spin on glass. The spin on glass was severely underetched during the HF via etch. The high temperature bake (400 C) intended to improve film quality (prevent cracking) caused an apparent densification of the film which increased expected etch rates in the HF. For this reason subsequent data of the bi-level metal structure is presented for the case of the polyimide only.

In both cases however it was not possible to measure the thickness of the dielectrics used in the capacitors with ellipsometry techniques. This would be necessary to determine the permittivity of the materials. The lack of these permittivity



values prevented the determination of thicknesses of the dielectrics in the test structures. This is the reason why subsequent data is presented with respect to spin speeds and not thickness's.

The breakdown voltages presented in Table 1 were determined by choosing a current density of  $16\text{nA}/\mu\text{m}^2$  where this value must be calculated from the relation of equation 4.

$$J = I/A \quad (4)$$

where: J=current density

I=current

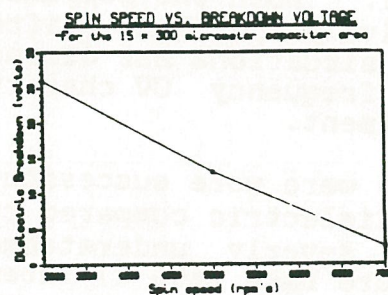
A=cross sectional area of capacitor

The I-V characteristics of the data for Table 2 is presented in appendix D.

TABLE 1

Capacitor area ( $\mu\text{m}^2$ )	Breakdown Voltages (Volts)		
	Spin speeds		
	3000	5000	7000
40*300	26.64	25.50	4.45
30*300	21.08	16.32	3.20
15*300	26.00	13.00	2.40

The data of Table 1 shows the expected trend of decreasing breakdown voltage for decreasing film thickness (increasing spin speeds). Graphs 1 of the  $15 \times 300 \mu\text{m}$  structure is representative of the relation discussed.



Graph 1: Breakdown voltage vs. dielectric spin speed

Table 2 contains measured resistances of selected areas of the four via chains for three different spin speeds.



TABLE 2

via dimension (um)	individual via resistance in ohms		
	spin speeds		
	3000	5000	7000
30	7.80e9	8.33e9	4.68e9
20	9.50e9	10.5e9	7.44e9
10	4.20e9	4.26e9	3.04e9
5	5.63e9	4.40e9	3.43e9

The 30 and 20 micrometer via resistance was measured using 12 of the 114 via chain (the resultant resistance plots presented in appendix B) and dividing the total measured resistance by 12. Similarly the 10 and 5 um via resistance was measured using 30 of the 600 via chain (the resultant resistance plots presented in appendix B) and dividing the total measured resistance by 30.

Table 2 demonstrates the expected trend for decreasing via size of increasing via resistance for each measured pair (5 compared to 10 um and 20 compared to 30 um). Added to this is the fact that no breakdown is apparent in the I-V characteristics from which the resistance was determined. Examining table 2 it is seen that although the vias appeared cleared when visually inspected during processing an aluminum oxide must have formed (prior to the evaporation of the second level metal) which resulted in the unduly high resistances.

It should be also noted that the working masks can only be aligned to certain die areas because of problems encountered with the GCA photo-repeater. The photo-repeater produced differing spaces between die. Therefore die were properly aligned must be searched for on the wafer.

## CONCLUSIONS

The CV plot data demonstrated the feasibility of both spin on glass and polyimide as dielectric materials. Subsequent processing of test structures demonstrated the polyimide as a viable bi-metal dielectric. When using properly dated materials, a sufficiently high curing method (such as to prevent cracking), and an adhesion promoter (VM651), both good adhesion and a crack-free surface was obtained. Further work using these materials should include:

- Examining etch rates of spin on glass to eliminate undercutting during the via etch.
- An HF etch prior to second level metal evaporation to remove a suspected oxide formed over the first level aluminum.
- Studying the thickness vs. spin speeds of both dielectrics discussed in this paper.



## ACKNOWLEDGEMENTS

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