8-30-2016

Engineering SiO2 Passivated Indium-Gallium-Zinc-Oxide TFTs for Improvement in Channel Control

Nicholas R. Edwards
nre4690@rit.edu

Engineering SiO_2 Passivated Indium-Gallium-Zinc-Oxide TFTs for Improvement in Channel Control

Nicholas R. Edwards

Engineering SiO_2 Passivated Indium-Gallium-Zinc-Oxide TFTs for Improvement in Channel Control

Nicholas R. Edwards
August 30, 2016

A Thesis Submitted
in Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in
Microelectronic Engineering

R·I·T | Kate Gleason *College of* ENGINEERING

Department of Electrical and Microelectronic Engineering

Engineering SiO_2 Passivated Indium-Gallium-Zinc-Oxide TFTs for Improvement in Channel Control

Nicholas R. Edwards

Committee Approval:

Dr. Karl Hirschman *Advisor* Professor	Date
Dr. Sean Rommel Gleason Professor	Date
Dr. Michael Pierce Assistant Professor	Date
Dr. Robert Pearson Program Director	Date

Acknowledgments

I would like to acknowledge and thank everyone whose guidance and support made this project possible. Firstly, my advisor Dr. Karl Hirschman, for his support and guidance throughout my time at RIT and throughout this project. My committee members, Dr. Sean Rommel and Dr. Michael Pierce, for the guidance that they likewise provided. I would also like to thank the members of the Team Eagle research group for their support and assistance in processing and data collection: Tarun Mudgal, Prashant Ganesh, Anish Bharadwaj, Patricia Meller, and the rest of Team Eagle. I would also like to thank the SMFL staff: Sean O'Brien, John Nash, Dave Yackoff, Rich Battaglia, Bruce Tollesen, Peter Morici, Scott Blondell and Tom Grimsley, for without their support this project would not have been possible.

Abstract

The performance of Indium Gallium Zinc Oxide (IGZO) Thin-Film Transistors (TFTs) has improved significantly in recent years; however, device stability still remains a significant issue. In bottom-gate TFTs a difficult challenge is the lack of gate control on the back-channel region, resulting in distortion in $I_D - V_{GS}$ characteristics. In this work a bottom-gate TFT process was established using SiO_2 as a back-channel passivation layer. The process was modified with options to implement TG (TG) and Double-Gate (DG) configurations. TFTs were fabricated utilizing a SiO_2 layer deposited shortly after the IGZO sputter process, followed by an oxidizing ambient anneal treatment. The process supports a low-defect IGZO interface, with TG and DG configurations demonstrating improvements in channel control compared to a traditional bottom-gate TFT. Electrical characteristics from each process treatment and gate configuration where then compared. A SPICE level 2 compatible IGZO TFT model was developed, with extracted parameter values providing a quantitative measure of device operation. Measured characteristics were also used to develop a refined material and device model for TCAD simulation.

Contents

List of Figures

List of Tables

List of Symbols

Term	Description	Units/Value
C'_{ox}	Oxide capacitance per unit area	$\mathrm{F/cm^2}$
E_g	Band gap energy	eV
E_{OV}	Energy of oxygen vacancies	eV
g_m	Transconductance	S
I_D	Drain current	A
L	Channel length	µm
N_F	Fixed charge	$\mathrm{cm^{-2}}$
N_{OV}	Energy density of oxygen vacancies	$\mathrm{cm^{-3}\,eV^{-1}}$
N_{TA}	Energy density of acceptor like tail-states	$\mathrm{cm^{-3}\,eV^{-1}}$
N_{TD}	Energy density of donor like tail-states	$\mathrm{cm^{-3}\,eV^{-1}}$
R_{SD}	Source/Drain series resistance	Ω
SS	Subthreshold swing	V/dec
V_{DS}	Drain–Source voltage	V
V_{GS}	Gate voltage	V
V_R	Series resistance voltage drop	V
V_T	Threshold voltage	V
W	Channel width	µm
W_{OV}	Width of oxygen vacancies (gaussian distribution)	eV
W_{TA}	Width of acceptor like tail-states (gaussian distribution)	eV
W_{TD}	Width of donor like tail-states (gaussian distribution)	eV
χ	Electron affinity	eV
ϵ_{IGZO}	Relative permittivity of IGZO	
ΔV_G	Sub-threshold separation	V
μ_0	Intrinsic electron mobility	$\mathrm{cm^2/Vs}$
μ_{eff}	Effective electron mobility	$\mathrm{cm^2/Vs}$
μ_{TH}	Threshold mobility	$\mathrm{cm^2/Vs}$
θ	Mobility modulation	$\mathrm{V^{-1}}$

Chapter 1

Literature Review

1.1 Background

Liquid crystal displays (LCDs), such as the one depicted in Fig. 1.1, are comprised of a backplane light source such as a Cold-Cathode Fluorescent Lamps (CCFLs), or more recently light-emitting diodes (LEDs). The light from these sources passes through a diffuser and polarizer. These are bonded to the glass substrate the thin-film electronics are fabricated on. The second half of the display is composed of a transparent common electrode, color filter and polarizer bonded to a second glass substrate. The liquid crystal is sandwiched between the two glass substrates where a voltage may be developed across the liquid crystal [1].

Prior to the development of active-matrix LCDs (AM-LCDs) the direct pixel addressing method known as the passive-matrix was the standard for LCDs. The main drawback of directly addressing a pixel is the presence of leakage paths which allow adjacent pixels to be partially turned on. Addressing the pixel through a transistor eliminated the leakage paths and allowed AM-LCDs to dominate the display industry. An example of a simple active-matrix circuit can be seen in Fig. 1.2 which consists of a switching Thin-Film Transistor (TFT), storage capacitor, and liquid crystal.

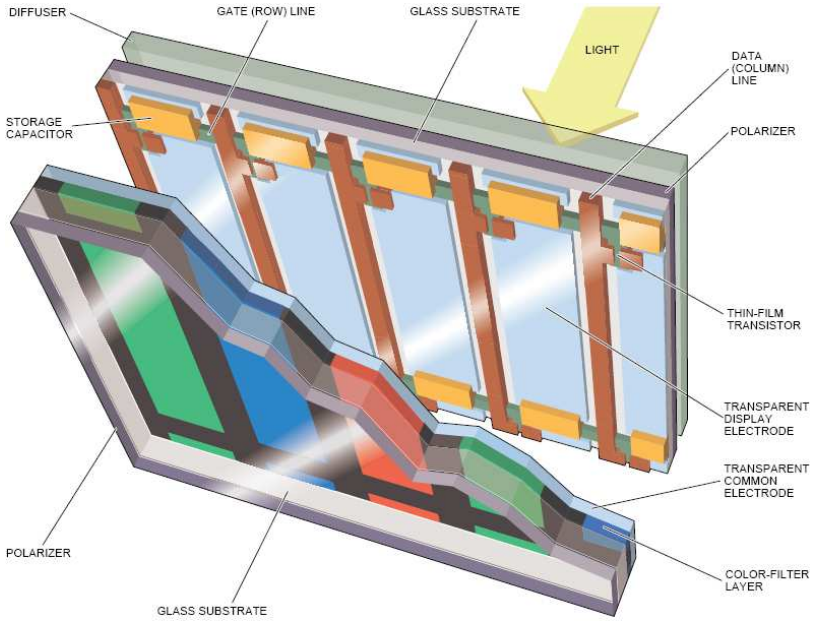

Figure 1.1: Structure of an LCD [1].

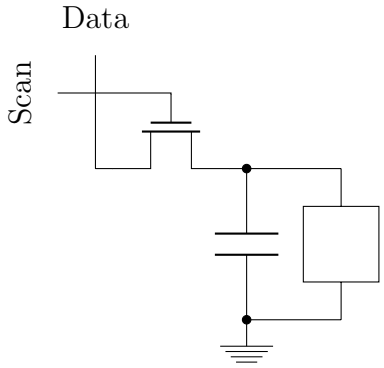

Figure 1.2: Equivalent circuit of active matrix display. A liquid crystal and storage capacitor are connected in parallel being driven by a TFT that is connected to the scan and data circuits.

For a pixel to be turned on, the liquid crystal must be uncoiled by applying a voltage to it. A pixel is turned on when there is an appropriate voltage applied to the data line and the pixel is being addressed through the scan line. A pixel is addressed until the storage capacitor is charged after which the TFT is turned off by disconnecting the scan line. Voltage is maintained across the liquid-crystal by the storage capacitor until the pixel is addressed again. By precisely controlling the voltage applied to the liquid crystal high contrast ratios may be achieved by allowing a precise amount of light through the display. For organic light-emitting diode (OLED) displays precise control of pixel illumination can be achieved by controlling current injected into the OLED.

With advancing technology more stringent manufacturing and performance requirements are necessary. Large area uniformity is a major concern as display technology advances to generation 10 (Gen 10) which uses a substrate that is roughly $3\,\mathrm{m} \times 3\,\mathrm{m}$. Electrical uniformity requirements are more demanding for OLED displays due to the high sensitivity of brightness on the drain current of the driving TFT. Another requirement is that the semiconductor material must be low-temperature compatible, as they are typically fabricated on glass substrates using process temperatures less than $600\,^{\circ}\mathrm{C}$. For flexible displays the temperature requirements are much lower than this. Another consideration is that high temperature processing may result in material changes (e.g. crystallization) which degrades large area electrical uniformity. Finally, with decreasing pixel to TFT aspect ratios in high pixel density displays it is advantageous for TFTs to be transparent to visible light.

1.2 Current Technology and Limitations

In the semiconductor industry, crystalline silicon is the undisputed leading technology platform. Historically, his was a result of favorable economics realized by the ability to grow a high quality dielectric and obtain a low defect density interface. As a

result silicon has been extensively studied over the past 60 years making it the most understood semiconducting material. Not surprisingly silicon became the dominant technology in the display industry. Rather than crystalline bulk silicon, thin-film Hydrogenated Amorphous Silicon (a-Si:H) is the primary channel material for TFTs.

The use of a-Si:H is attractive as it is low-temperature compatible and can be deposited with plasma-enhanced chemical-vapor deposition (PECVD) below 350 °C. It has good large area uniformity due to its amorphous structure and it is a well understood, low-cost material.

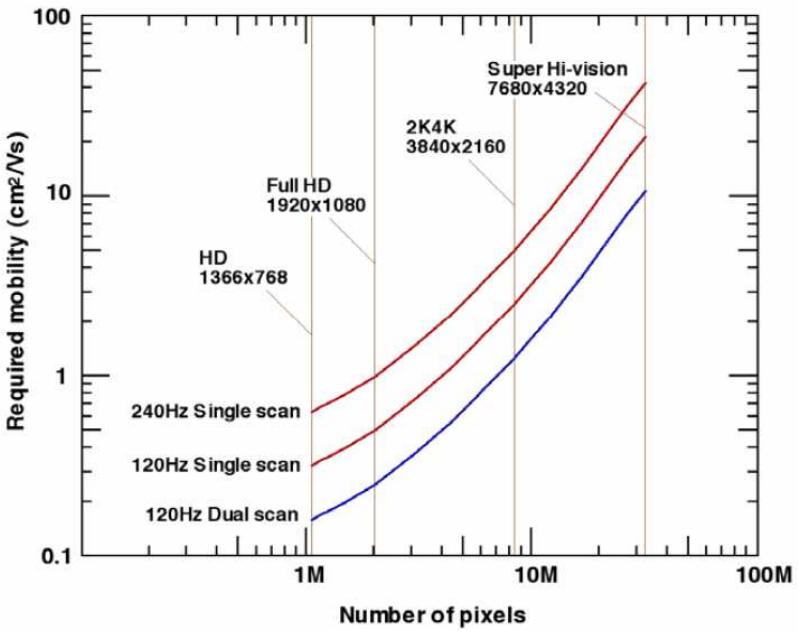

Figure 1.3: Mobility requirements for current and future displays [7].

Several challenges have emerged with the demanding requirements of next generation displays. These limitations are observable in high pixel density displays and fast switching speed applications. Both require a high mobility semiconductor for improved current drive to minimize delay times [5, 8]. A 50-inch AM-LCD with copper bus lines was assumed to determine the estimated mobility requirements shown in Fig. 1.3. These values roughly double when considering a 70-inch AM-LCD due to increased delay times [7]. Bias stress threshold voltage (V_T) instability is a major

drawback to using a-Si:H in OLED displays. A 20 % change in brightness can occur if the driving TFTs V_T shifts by 0.1 V [6]. Compensation circuits which cancel out V_T errors exist and make it possible to use a-Si:H as an OLED driver. One example of such a circuit can be seen in Fig. 1.4. The added complexity of these circuits reduces yield driving costs up.

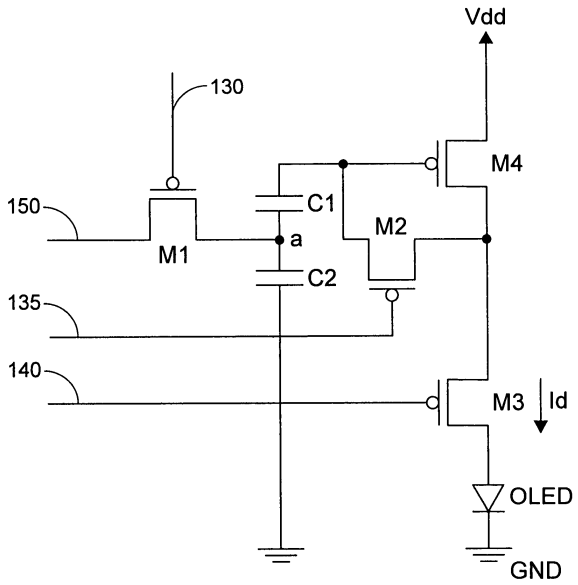

Figure 1.4: Active matrix V_T compensation circuit utilizing 4 TFTs and 2 storage capacitors [2].

1.3 Candidates to Replace a-Si:H

Several candidates to replace a-Si:H are being investigated, some represented in Table 1.1. Low-temperature polycrystalline silicon (LTPS) fulfills the mobility requirements and are at least an order of magnitude greater than its amorphous counterpart. The bias stress V_T stability is sufficient for driving OLED, and it is also possible to fabricate CMOS TFTs. LTPS is formed by depositing a-Si:H and then crystallizing the material by excimer laser annealing (ELA). This technique is appealing because of its ability to crystallize the a-Si:H without heating the substrate. Significant issues with this process is the high cost and process scaling limitations.

LTPS also has challenges with large scale electrical uniformity, which is a result of grain boundaries present in the film. Amorphous-oxide semiconductors are a contender to replace a-Si:H. This is due to their high electron mobility compared to a-Si:H. These materials can have a lower density of tail-states in the conduction band making them less sensitive to bias stress than a-Si:H [5]. They also don't suffer from electrical non-uniformities like LTPS due to their amorphous structure and are low-temperature compatible.

Table 1.1: Comparison of a-Si:H, Poly-Si, ZnO and a-IGZO as TFT channel materials [5, 6].

Semiconductor	Electron Mobility ($cm^2/V \cdot s$)	Bias Stress V_T Shift (V)	Large Scale Uniformity	Transistor Type
a-Si:H	< 1	> 10	Good	NMOS
LTPS	$30 - 100$	< 0.5	Poor	CMOS
ZnO	$10 - 30$	~ 25	Poor	NMOS
a-IGZO	$10 - 20$	< 1	Good	NMOS

1.4 Electron Conduction in Amorphous Semiconductors

Orbital drawings of a covalent and ionic-oxide semiconductor in a crystalline and amorphous structure are shown in Fig. 1.5. This illustrates the mobility degradation in a-Si:H from its crystalline state and why this is not observed in ionic bonded semiconductors.

1.4.1 Covalent Bonded Semiconductors

In covalent bonded semiconductors such as silicon sp^3 orbitals form the conduction paths. In a crystalline film, these orbitals are aligned allowing band conduction to occur and results in high carrier mobility. However, sp^3 orbitals are highly sensitive to spatial directivity. Degraded mobility in an amorphous structure is the result

of disordered bonds which limit electron transport to hopping conduction through band-tail states [9].

1.4.2 Ionic Oxide Semiconductors

The conduction path in ionic oxide semiconductors, such as AOS, are comprised of s orbitals contributed by heavy-metal cations. The large overlap between neighboring s orbitals makes them insensitive to bond distortion and allows band conduction to occur, even in an amorphous material [9].

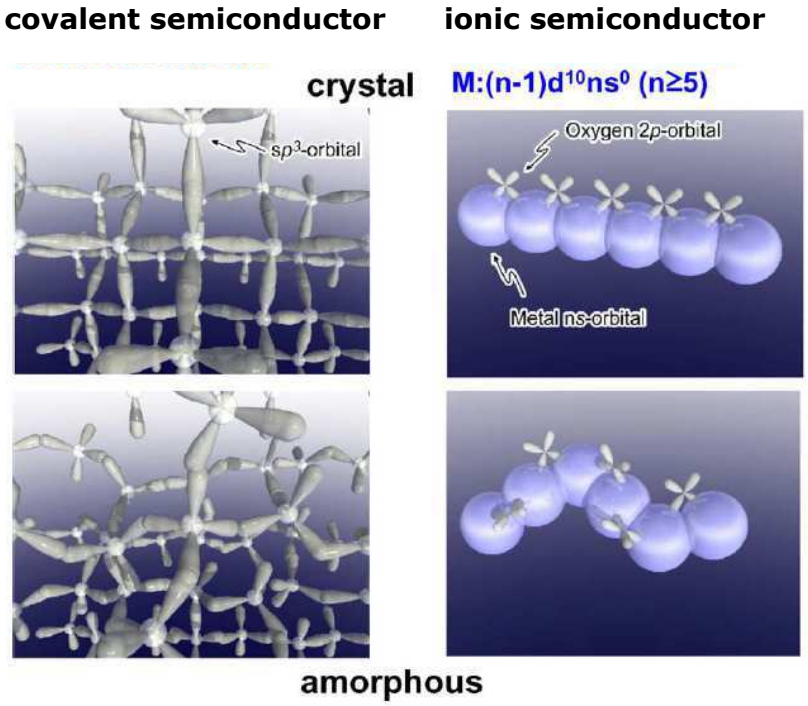

Figure 1.5: Illustration of orbitals of a covalent (left) and ionic (right) semiconductors in crystalline (top) and amorphous (bottom) structures [10].

1.5 Brief History of Oxide-Semiconductors

The first oxide-semiconductors came into fruition after the publication of a CdS TFT in 1962. Following this several binary TFTs were demonstrated including; In_2O_3 in 1964, ZnO in 1968 and SnO_2 in 1970. The first AM-LCD was demonstrated in

1973 using CdSe TFTs and following this a-Si:H took over the market. ZnO saw revitalized interest in 2003 when shortcomings of a-Si:H TFTs were first becoming apparent. Since then several new ternary and quaternary AOS have been developed to address electrical performance and stability challenges present in binary oxide-semiconductors [5].

1.6 Prospective of ZnO TFTs

ZnO is a promising candidate to replace a-Si:H. Its semiconducting properties were first reported in 1968. Renewed interest occurred during the early 2000s for potential integration into display technologies. This was due to its electron mobility being an order of magnitude greater than a-Si:H. For more uniform electrical properties an amorphous film is desirable. ZnO is typically sputter deposited which is both a low-temperature process and suitable for large area deposition. Like most binary semiconductors ZnO is easily crystallized into a polycrystalline structure resulting in grain boundaries that present significant challenges with electrical uniformity [5]. Compensation circuits may be used to overcome electrical non-uniformity at the cost of lower yield, higher fabrication costs and added complexity [6]. Many ternary and quaternary AOS have since been developed to combat electrical uniformity issues that ZnO suffers from. The additional elements serve to frustrate crystallization and tend to naturally form amorphous structures [9].

1.6.1 PE-ALD ZnO with Alumina Passivation

Plasma-Enhanced Atomic Layer Deposition (PE-ALD) of ZnO can achieve high performance TFTs as was demonstrated by D. A. Mourey et al. The device in Fig. 1.6 has a V_T of 4.5 V, μ_{sat} of $20 - 30$ cm^2/V $\cdot$ s and a sub-threshold swing of 200 mV/dec [11]. These results were achieved by minimizing process induced damage to the ZnO semiconductor. PE-ALD uses a remote plasma source minimizing any plasma induce

damage in the ZnO. PE-ALD allows for low-temperature deposition and has a high deposition rate, minimizing time spent in vacuum at elevated temperature. Most importantly hydrogen free precursors, CO_2 and N_2O are used. Hydrogen incorporation increases the number of free electrons in oxide semiconductors by bonding with oxygen forming OH^- bonds in which act as additional donors. This causes a left shift in V_T and degrades off-state current [12]. While this deposition method yields high performance TFTs, the process is not yet scalable to 8G/10G glass substrates and is currently unsuitable for high volume manufacturing.

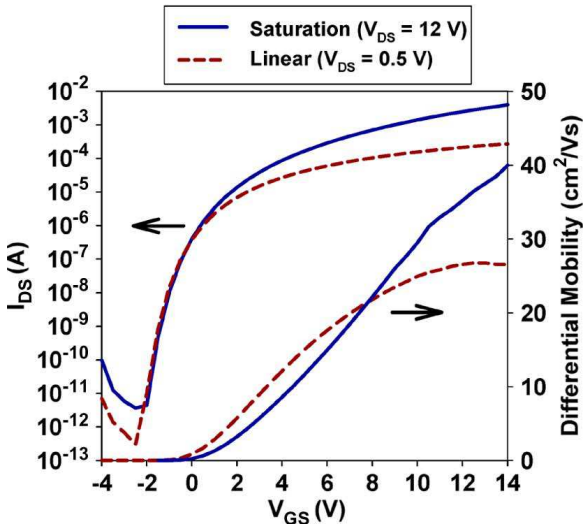

Figure 1.6: $I_D - V_{GS}$ measurements and differential mobility extraction of a PE-ALD deposited ZnO TFT [11].

1.7 Motivation For The Development of IGZO TFTs

Amorphous indium-gallium-zinc-oxide (a-IGZO) is a promising material that has gained interest in the FPD industry due to its high electron mobility, which is about an order of magnitude larger than a-Si:H and similar to that of ZnO. The 4 atom composition frustrates crystallization even under higher temperature annealing ($\leq$400 °C). This is in contrast to ZnO and as a result the film can achieve better large area uniformity while being deposited by sputtering. The $|V_T|$ of IGZO is also much lower than

ZnO it is hypothesized that this is due to gallium suppression of the free electrons [10]. IGZO is low-temperature deposition capability and high ON/OFF current ratios. [5, 6]. IGZO is also less sensitive to illumination induced instability than a-Si:H resulting in improved device reliability. Additionally its compatible with processing techniques currently used with a-Si:H ensuring a quick transition when integrating with high-volume manufacturing at a low cost [5, 8, 13]. AOS are typically more stable than a-Si:H with regard to temperature bias stress, and illumination bias stress testing. This is the result of a lower number of tail states near the conduction band [14].

Several challenges with a-IGZO must be overcome before it is widely adopted in the FPD industry. Storage ambient will cause the electrical properties of the film to change requiring a passivation material being deposited on the back-channel of a Staggered Bottom-Gate (BG_{stg}) TFT to ensure device stability. IGZO is not a chemically robust material requiring lift-off processing following the active area etch. Process induced damage is also a concern whenever plasma processes are considered as it may generate defects in the IGZO degrading $I_D - V_{GS}$ characteristics.

1.8 Summary of Literature Review

With more advanced display applications the incumbent technology, a-Si:H, becomes less economical for backplane switching circuits. This is in part due to the low electron mobility of the amorphous material. The bias-stress instability of the material is another shortcoming which can negatively impact the lifetime of a display. IGZO is one material currently being investigated which provides both higher electron mobility and lower bias-stress sensitivity than a-Si:H. The improved electron mobility is illustrated in Fig. 1.7 where, when normalized by device width the IGZO TFT current drive is approximately 1.5 times larger than the a-Si:H TFT despite being roughly 10 times longer in channel length. This allows for lower voltage operation

and can result in reduced power consumption. IGZO can be deposited via sputtering, is low-temperature compatible and does not have high-cost processing and large-scale uniformity issues associated with materials such as LTPS or ZnO. Challenges with device stability and passivation without degrading device performance need to be solved before IGZO can be widely adopted FPD industry. When comparing various TFT treatment combinations it is useful to look at the $I_D - V_{GS}$ transfer characteristics for a preliminary qualitative comparison. For a quantitative comparison parameter extraction from these measured transfer characteristics must be performed. Typically parameters such as V_T, μ and SS are used to evaluate the electrical performance of these devices. This becomes difficult when considering IGZO as it does not show normal field degradation that typical silicon devices exhibit. As a result the linear mode $I_D - V_{GS}$ transfer characteristics are concave up rather than concave down. This makes it impossible to extract V_T by finding the x-intercept from the maximum of the slope and attempts to perform this result in extracted parameters of questionable validity.

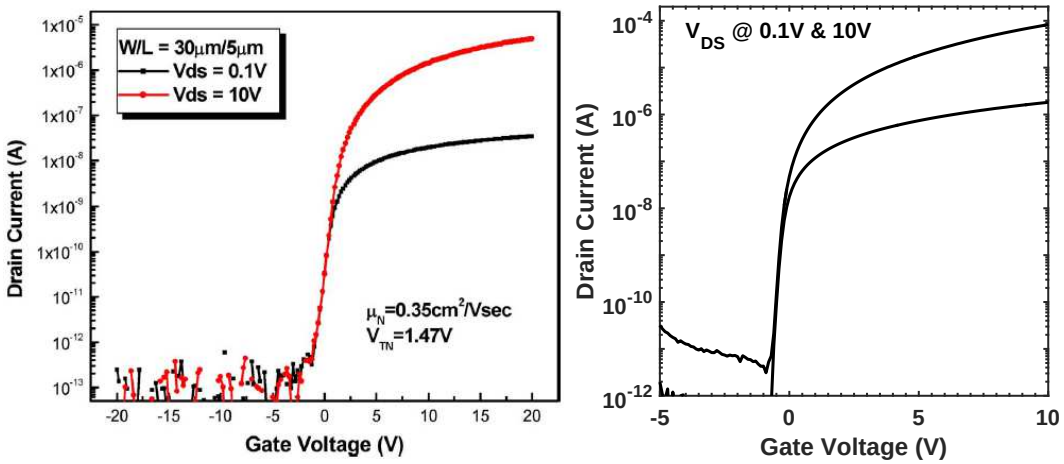

Figure 1.7: Comparison of a-Si:H and un-passivated IGZO TFT $I_D - V_{GS}$ transfer characteristics with dimensions of L/W = 5/30 µm and 48/100 µm, respectively [3, 4].

Chapter 2

Comprehensive Parameter Extraction Model

2.1 Motivation

The development of a consistent and reliable parameter extraction model is of paramount importance if a quantitative analysis and comparison of different treatments is required. It is important for this method to have minimum error so that any differences observed can be accounted for by processing factors. IGZO TFTs appear to have little influence by normal field degradation and series resistance when operated in linear mode, as silicon devices do as shown in Fig. 2.1. Thus, traditional methods used for silicon devices, such as extracting V_{GS} at the maximum transconductance for V_T do not work. An attempt to use this method will result in grossly overestimated V_T and subsequently the threshold and effective mobilities, μ_{TH} and μ_{eff}, respectively. Traditional methods used for IGZO TFTs calculate V_T at the maximum of the derivative of g_m. This method provides an acceptable, albeit conservative measurement of V_T; however, this is not a robust method. False peaks may occur in the off-state or on-state resulting in a V_T which is grossly incorrect. Data smoothing by taking a rolling 5 point average can be used to improve the reliability; however, there will invariably be some devices which cause this extraction to fail. A SPICE level-2 model which utilizes an effective channel mobility model would satisfy both of these issues.

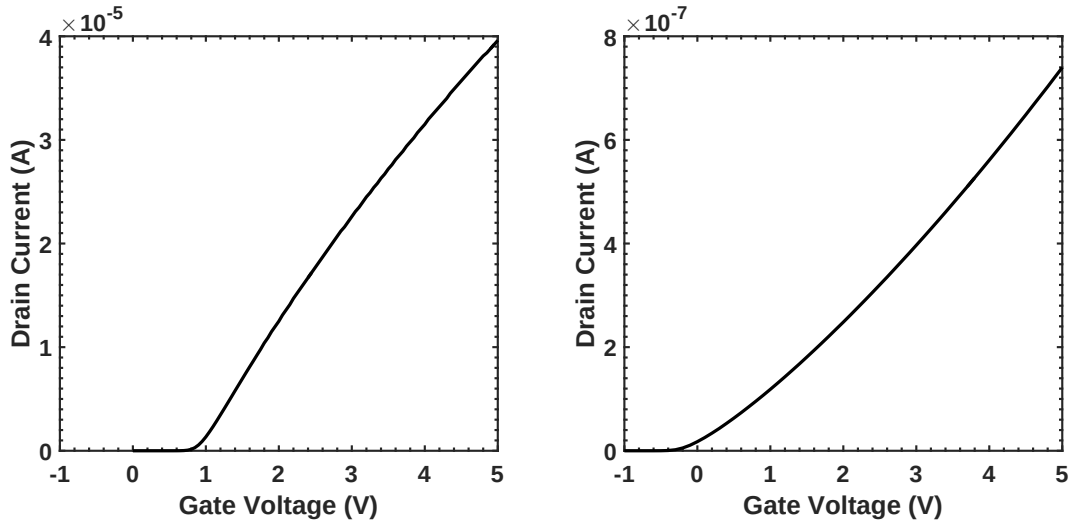

Figure 2.1: Linear I_D-V_{GS} measurements of Si (left) and IGZO (right) TFTs.

2.2 Derivation and Development of SPICE Level-2 Model

This method implements a SPICE level-2 model which uses an effective mobility model to account for the on-state mobility enhancement seen in IGZO TFTs. This model can also consider any R_{SD} and ΔL that may be present in these devices. This model was developed starting with the linear and saturation current equations given in (2.1).

$$I_{D_{lin}} = \frac{W}{L}\mu C_{ox}{}' \left(V_{GS} - V_T\right) V_{DS} \ ^1 \tag{2.1a}$$

$$I_{D_{sat}} = \frac{W}{L}\mu C_{ox}{}' \frac{\left(V_{GS} - V_T\right)^2}{2} \tag{2.1b}$$

Where an effective mobility model, shown in (2.2), is used to account for the normal field mobility enhancement seen in a-IGZO by allowing the fitting parameter, θ to be negative.

$$\mu = \mu_{eff} = \frac{\mu_{TH}}{1 + \left(V_{GS} - V_T\right)\theta} \tag{2.2}$$

[1]This equation assumes a negligibly small ${V_{DS}}^2/2$ term.

This substitution for mobility results in (2.3).

$$I_{D_{lin}} = \frac{W}{L}\left[\frac{\mu_{TH}}{1+(V_{GS}-V_T)\,\theta}\right] C_{ox}{}'\,(V_{GS}-V_T)\,V_{DS} \tag{2.3a}$$

$$I_{D_{sat}} = \frac{W}{L}\left[\frac{\mu_{TH}}{1+(V_{GS}-V_T)\,\theta}\right] C_{ox}{}'\frac{(V_{GS}-V_T)^2}{2} \tag{2.3b}$$

To make this model more flexible, parasitic source and drain series resistance (R_{SD}) and effective channel length (L_{eff}) will also be considered, these values may be extracted by Terada-Muta analysis. An equivalent circuit showing R_{SD} can be seen in Fig. 2.2, where the internal V_{GS} and V_{DS} from (2.1) and (2.2) are now defined as $\tilde{V_{GS}}$ and $\tilde{V_{DS}}$. When including R_{SD} and ΔL (2.3) must be rearranged to solve for V_{GS} with respect to I_D so that the equation is tractable, this results in (2.4).

$$\tilde{V_{GS}} = I_{D_{lin}}\left[\frac{W}{L}\mu_{TH}C_{ox}{}'\tilde{V_{DS}} - I_{D_{lin}}\theta\right]^{-1} + V_{T_{lin}} \tag{2.4a}$$

$$\tilde{V_{GS}} = \left[\theta + \sqrt{\theta^2 + 2\frac{W}{L}\mu_{TH}C_{ox}{}'{I_{D_{sat}}}^{-1}}\right] I_{D_{sat}}\left[\frac{W}{L}\mu_{TH}C_{ox}{}'\right]^{-1} + V_{T_{sat}} \tag{2.4b}$$

By rearranging the relationships defined in (2.5) the applied voltages may be substituted into (2.4) and results in (2.6).

$$V_{DS} = \tilde{V_{DS}} - V_R = \tilde{V_{DS}} - I_D R_{SD} \tag{2.5a}$$

$$V_{GS} = \tilde{V_{GS}} + V_R/2 = \tilde{V_{GS}} + I_D R_{SD}/2 \tag{2.5b}$$

$$V_{GS_{lin}} = I_{D_{lin}}\left[\frac{W}{L-\Delta L}\mu_{TH}C_{ox}{}'\,(V_{DS} - I_{D_{lin}}R_{SD}) - I_{D_{lin}}\theta\right]^{-1} + V_{T_{lin}} \tag{2.6a}$$

$$V_{GS_{sat}} = \left[\theta + \sqrt{\theta^2 + 2\frac{W}{L-\Delta L}\mu_{TH}C_{ox}{'}{I_{D_{sat}}}^{-1}}\right]\left[\frac{W}{L-\Delta L}\mu_{TH}C_{ox}{'}{I_{D_{sat}}}^{-1}\right] + V_{T_{sat}} + I_{D_{sat}}\frac{R_{SD}}{2} \quad (2.6b)$$

This model can accommodate ΔL or R_{SD}, however it is important to note that this method can not be used to extract these parameters, as the additional degrees of freedom causes these equations to be not uniquely solvable.

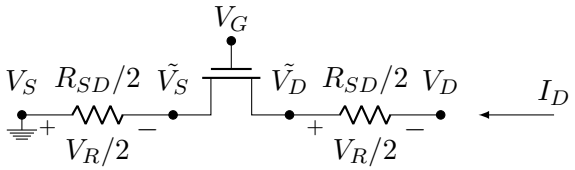

Figure 2.2: Circuit representation of TFT including parasitic series resistance.

2.3 Methodology

The parameters are extracted from the refined model by iterative numerical approximation where μ_{TH} and θ are directly coupled between linear and saturation operation while V_T is not coupled between these models. This allows for different extracted values linear and saturation threshold voltage, henceforth referred to as $V_{T_{lin}}$ and $V_{T_{sat}}$ respectively.

The routine utilizes boundary conditions from 2.7 to prevent the routine from ending at a local minimum.

$$1 \leq \mu_{TH} \leq 100 \quad (2.7a)$$

$$-10 \leq V_T \leq 10 \quad (2.7b)$$

$$-1 \leq \theta \leq 1 \quad (2.7c)$$

The routine's goal is set to minimize the error between linear and saturation mode

fit and measurement data.

$$RMSE = \sqrt{\frac{\sum_{i=1}^{n} (\hat{y}_i - y_i)^2}{n}} \tag{2.8}$$

$$NRMSE = \frac{RMSE}{y_{max} - y_{min}} \tag{2.9}$$

This is achieved by summing the Normalized Root-Mean-Square Error (NRMSE) to ensure each mode of operation is weighted equally. The routine uses an initial guess provided by the user then varies the fitting parameters until either the maximum number of iterations is reached, the function, or step tolerance is achieved. When the step size is smaller than the step tolerance the iterations are stopped. On the other hand when the change in NRMSE is less than the function tolerance the iterations stop. The maximum number of iterations is set to 600 while the step and function tolerances are set to 1×10^{-6}.

This minimization routine is run in a while loop which checks for $V_{GS} - V_T > 0$ for both linear and saturation operation. If these criteria are not achieved $V_{GS} < V_T$ is removed and the minimization routine is performed again using the extracted parameters as the initial guess. When performing the fit for the saturation model V_{GS} data above 5 V is not considered to ensure that the device remains operating in saturation mode. The measured and modeled I_D-V_{GS} transfer characteristics using the method described above is shown in Fig. 2.3. This example shows a low sum of normalized error of 2.1 %, indicating a good match between model and measured data.

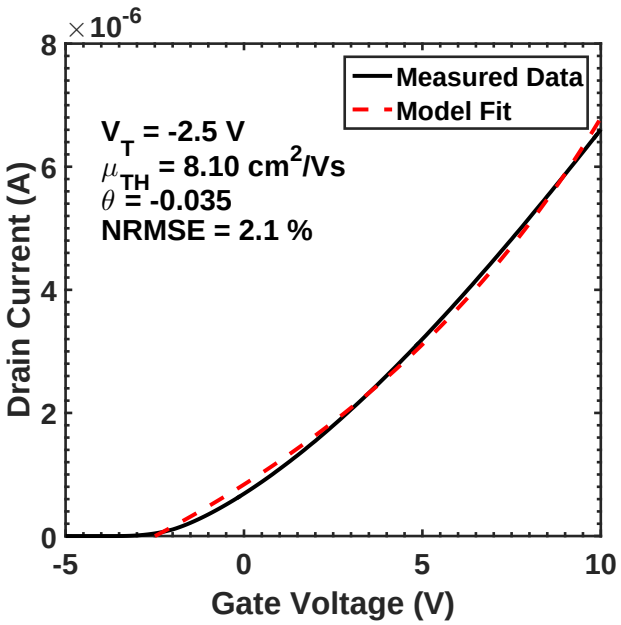

Figure 2.3: Measured and modeled I_D-V_{GS} transfer characteristics.

2.4 Additional Extracted Parameters

For quantitative comparison, μ_{eff} from 2.10 will be used to compare the mobility between treatments as V_T and the fitting parameter θ can compensate for a low μ_{TH}.

$$\mu_{eff}(V_{GS} = 10\,\mathrm{V}) = \frac{\mu_{TH}}{1 + (V_{GS} - V_T)\theta} \tag{2.10}$$

The sub-threshold separation in $I_D - V_{GS}$ transfer characteristics will be evaluated as shown in 2.11.

$$\Delta V_G = \left| V_{GS_{sat}}(I_{D_{sat}} = 10^{-10}\,\mathrm{A}) - V_{GS_{lin}}(I_{D_{lin}} = 10^{-10}\,\mathrm{A}) \right| \tag{2.11}$$

2.5 Summary of the Parameter Extraction Model

A SPICE level-2 model for parameter extraction has been successfully demonstrated. This model operates by performing nested iterative calculations of V_T, μ_{eff} and θ to arrive at a solution. When the nested iterative loop arrives at a minimum in

NRMSE between the modeled and measured data the solution is returned to the outer loop. If the condition $V_{GS} - V_T > 0$ is not satisfied the solution is rejected, data not conforming to this condition is removed and the nested iterative loop is called again. This method shows reliable performance with NRMSE on the order of $1 - 2\%$ and allows the user to account for ΔL and R_{SD} extracted by Terada-Muta analysis.

Chapter 3

Preliminary Research

This chapter will provide an overview of the preliminary research that was performed. This consists of a discussion of the baseline TFT configuration, fabrication and electrical characteristics. Various experiments evaluating the gate dielectric, passivation material, and integration of dry-etching for self-aligned structures will be discussed. Finally a process referred to as ripening, which involves passivated and un-passivated devices improving in electrical performance over the period of up to two weeks, will be discussed and a mechanism will be proposed.

3.1 Staggered Bottom-Gate TFT Fabrication Process

A 6-inch Si wafer is oxidized to simulate a glass substrate. The Mo gate is sputter deposited 10 nm thick and patterned by a subtractive wet etch. A 100 nm SiO_2 gate dielectric is deposited by plasma-enhanced chemical-vapor deposition (PECVD) using TEOS as the precursor. The SiO_2 is densified for 2 hours at 600 °C in nitrogen ambient. A 50 nm IGZO film is deposited by RF sputter from a target with an In:Ga:Zn:O atomic ratio of 1:1:1:4, then the IGZO mesa is patterned by subtractive etching in a dilute HCl mixture. The gate contact cuts are patterned and etched in 10:1 buffered HF. The source and drain metal is defined by lift-off processing, following which a Mo/Al bilayer is deposited by DC sputter. An optional AlO_x passivation layer is electron-beam evaporated, then defined by lift-off processing. Annealing is performed at 400 °C. Devices without a back-channel passivation material are annealed

in a furnace with an N_2 ambient soak followed by an air ramp-down. Passivated devices are annealed on a hotplate with room air ambient. A top-down micrograph and cross-sectional illustration of the resulting structure is shown by Fig. 3.1.

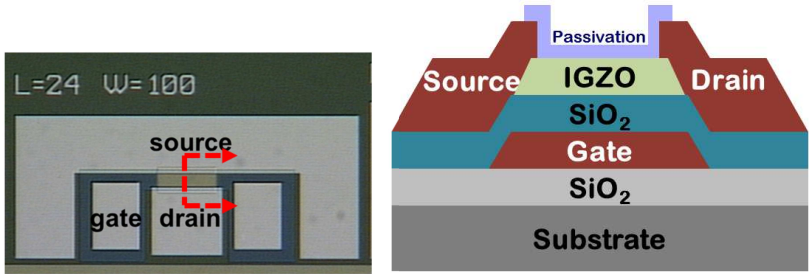

Figure 3.1: Top-down (left) and cross-sectional view (right) of a BG_{stg} TFT.

3.1.1 Test Chip Layout

The test chip layout can be seen in Fig. 3.2. This design includes a variety of test structures such as Interdigitated Capacitors (IDCs), Van der Pauw structures, inverters, a ring oscillator and various TFTs. Electrical parameter extraction is performed with measurements of both the IDCs and TFTs. The TFTs fabricated include two rows of devices with varying channel widths of; 6 µm, 12 µm, 24 µm, 36 µm and 48 µm with a constant width of 100 µm. Two additional TFTs are have dimensions of L/W = 24/200 µm.

3.2 Staggered Bottom-Gate TFTs

BG_{stg} TFTs are investigated as a baseline treatment for further studies, these devices are fabricated according to Section 3.1. The TFT structure and $I_D - V_{GS}$ transfer characteristics can be seen in Fig. 3.3. The V_T is $-0.25\,V$ with a μ_{eff} of 11.19 $cm^2/V \cdot s$ and a sub-threshold swing of 124 mV/dec [4]. This device was annealed in a nitrogen ambient at 400 °C for 30 min with an air ramp-down. This anneal is required to reduce conductivity of the IGZO film such that it is suitable for transistor operation.

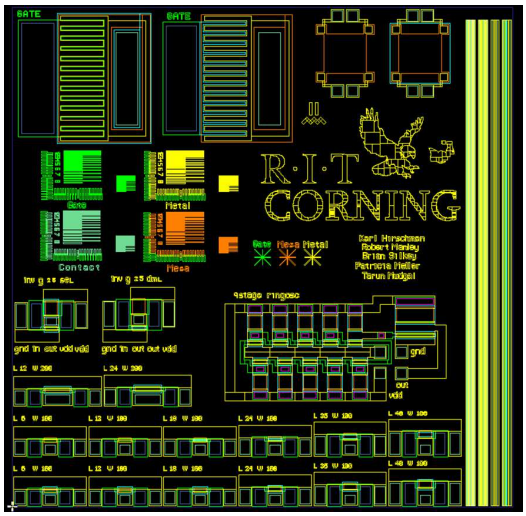

Figure 3.2: RIT TFT test chip layout.

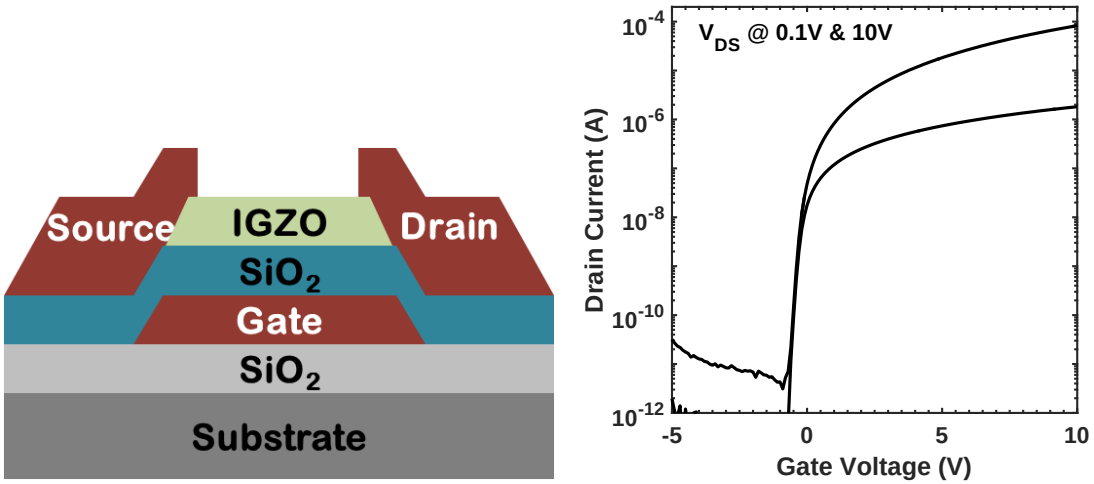

Figure 3.3: Structure of a BG_{stg} IGZO TFTs without a back-channel passivation material (left) and the $I_D - V_{GS}$ transfer characteristics of a L/W = 48/100 µm TFT with V_{DS} = 0.1 V and 10 V [4].

3.3 Gate Dielectric/IGZO Interface

An investigation to characterize the gate dielectric/IGZO interface was executed using the treatments in Table 3.1. The thermally grown Silicon Dioxide (SiO_2), while not compatible with a glass substrate, provides a best case interface to compare the other treatments with. The Si_3N_4 and re-oxidized Si_3N_4 were investigated due to the purported benefits with bias stress testing and are intended as proof of concept in this experiment [15]. Fig. 3.4 shows the $I_D - V_{GS}$ characteristics of each treatment. The SiO_2/IGZO interface treatments, despite deposition method, perform similarly. The Al_2O_3/IGZO interface also performed similarly to the SiO_2/IGZO. The Si_3N_4/IGZO interface produced significant distortion in the $I_D - V_{GS}$ characteristics. The lack of benefit over the standard PECVD SiO_2 and added complexity of ALD Al_2O_3 did not justify further process development. The re-oxidized Si3N_4 showed no benefit over PECVD SiO_2 in $I_D - V_{GS}$ characteristics. The promise of improved gate bias-stress stability makes the development of a low-temperature compatible process an interest in future investigations.

Table 3.1: Gate dielectric investigation treatments.

Gate Dielectric	Deposition Method
SiO_2	PECVD (TEOS)
	Thermally grown (substrate gate)
	Re-oxidized Si_3N_4
Si_3N_4	LPCVD
Al_2O_3	ALD

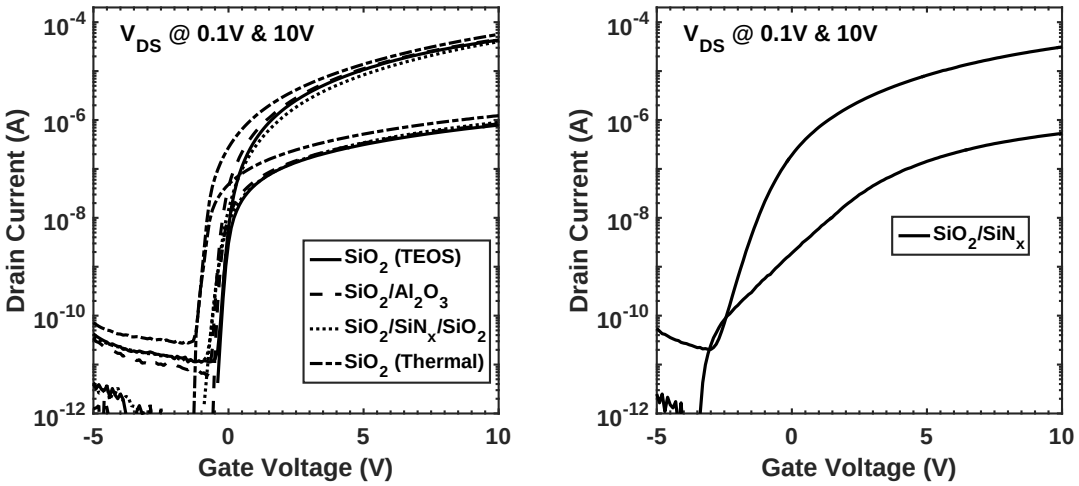

Figure 3.4: Overlay of PECVD and thermal SiO_2 and ALD Al_2O_3 transfer characteristics (left) and LPCVD Si_3N_4 transfer characteristics with L/W = 48/100 µm.

3.4 IGZO Ripening

It is well known that the back-channel of BG_{stg} IGZO TFTs needs a passivation material to prevent shifting of electrical characteristics. An interesting phenomenon referred to as ripening[1] recently shown is the improvement in electrical characteristics of IGZO TFTs for up to two weeks after annealing when stored in room ambient and is illustrated in Fig. 3.5.

To investigate this mechanism TFTs with 50 nm IGZO were fabricated in a BG_{stg} structure without depositing a back-channel passivation material. The TFTs were annealed in a nitrogen ambient at 400 °C for 30 min with air ramp-down, following initial device testing the IGZO was partially etched. The IGZO thickness was measured by profilometry to be 25 nm. Devices were tested immediately after the IGZO etch and stored in room ambient for 2 weeks after which devices were re-tested. Fig. 3.6 shows that the initial $I_D - V_{GS}$ transfer characteristics were degraded likely due to defects present at the back-channel after the wet etch. After a storage period of 2 weeks

[1]Note that the term ***ripening*** is simply an analogy to an evolutionary change. The actual mechanism is under investigation and may or may not relate to *Ostwald Ripening*

the $I_D - V_{GS}$ transfer characteristics recover fully indicating something is occurring at the back-channel. The working hypothesis being that oxygen from room air is incorporating itself with the etched surface where large defect densities were present.

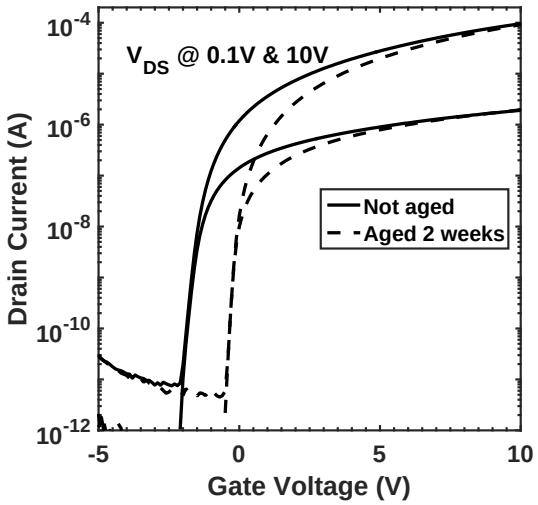

Figure 3.5: Transfer characteristics of an L/W = 24/100 µm TFT immediately after annealing and 2 weeks after annealing.

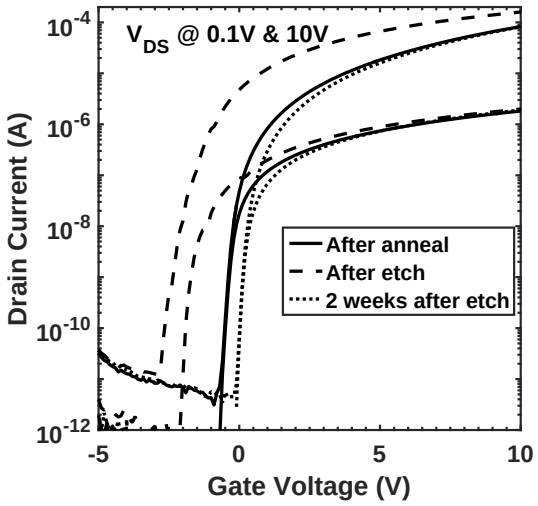

Figure 3.6: $I_D - V_{GS}$ transfer characteristics of an L/W = 24/100 µm TFT after; annealing, wet etching the IGZO channel and 2 weeks after etching.

3.5 E-Beam Alumina Passivation

The condition of the back-channel has a significant effect on the $I_D - V_{GS}$ transfer characteristics of IGZO TFTs. In an attempt to prevent age related degradation of the $I_D - V_{GS}$ characteristics various passivation materials and deposition methods have been investigated [16]. The most promising of which is evaporated AlO_x. Annealing is done on a hotplate in room air ambient. A more aggressive annealing ambient is required for TFTs with back-channel passivation. There is a slight increase in the subthreshold swing (SS) and a left shift in V_T when compared with an un-passivated TFT and can be seen in Table 3.2 and Fig. 3.7. This was shown to be a result of fixed charge and donor-like interface traps on the back-channel which are not present in un-passivated devices [4]. These devices also show ripening occurring for up to two weeks after annealing is performed. This time period has been observed to be channel length dependent with shorter devices requiring longer time after annealing before stabilizing and longer devices requiring minimal time before stabilizing.

Table 3.2: Extracted electrical parameters of L/W = 48/100 µm TFTs with and without a passivation material. Transfer characteristics are in Fig. 3.7.

Device Type	V_T (V)	μ_{eff} ($cm^2/V \cdot s$)	SS (mV/dec)
No passivation material	0.25	11.38	117
100 nm e-beam alumina	−0.2	11.12	194

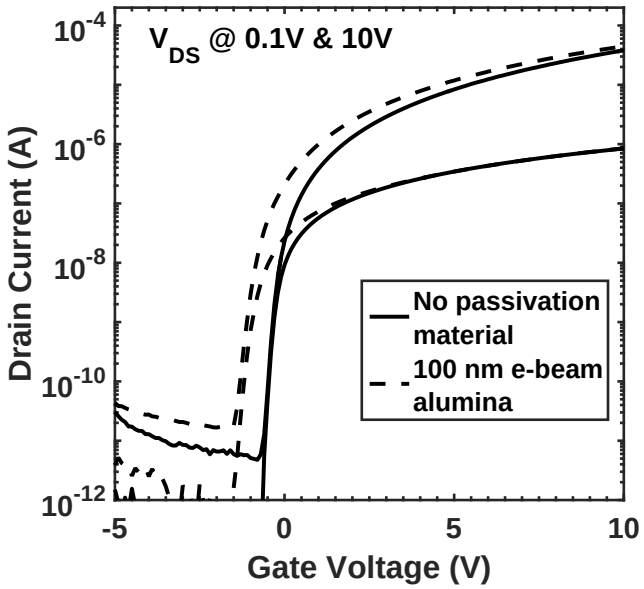

Figure 3.7: $I_D - V_{GS}$ transfer characteristics of L/W = 48/100 µm TFTs with and without 100 nm e-beam evaporated alumina passivation material.

3.6 Dry Etch Integration

In typical fabrication schemes deposition of the passivation material is the last step prior to annealing and testing. IGZO $I_D - V_{GS}$ characteristics has been shown to be dependent on ambient storage conditions when devices without a passivation material. It has also been shown that device fabrication time can have a strong effect on the $I_D - V_{GS}$ characteristics of TFTs. To avoid storage and process induced alteration of IGZO $I_D - V_{GS}$ characteristics a passivation scheme which involved depositing the passivation material immediately after IGZO sputter was developed. The mesa and source/drain contacts to the IGZO are patterned by subtractive dry etch using a LAM 4600 chlorine etcher. After this step they followed the standard process flow outlined in Section 3.1. The resulting $I_D - V_{GS}$ characteristics seen in Fig. 3.8 are severely distorted. It is speculated that this is due to the plasma damage in the source/drain contact regions preventing an ohmic contact to be formed between the IGZO/Mo

interface.

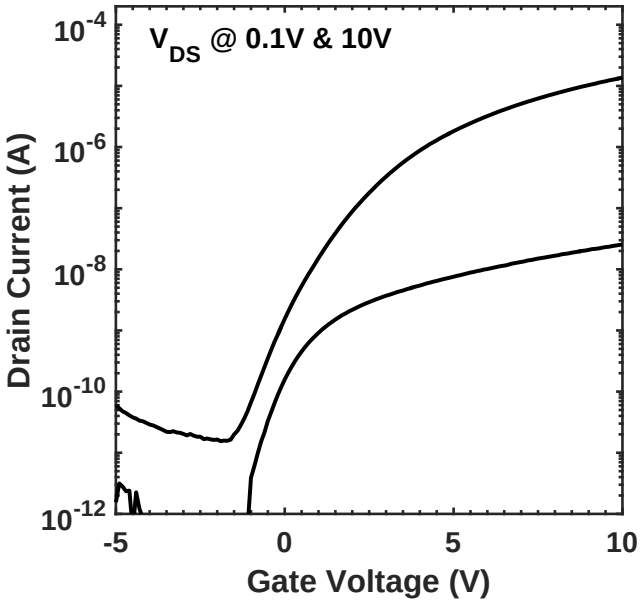

Figure 3.8: $I_D - V_{GS}$ transfer characteristics of TFT with a dry etched mesa.

3.7 Terada-Muta Analysis of IGZO TFTs

To make full use of the parameter extraction method previously described, Terada-Muta analysis was performed on IGZO TFTs to calculate ΔL and R_{SD}. The results of this analysis may be seen in Fig. 3.9. Specifically the enlarged image of the intersection point on the right shows that there are two separate locusts at 2.7 µm and 3 µm. By finding the minimum standard deviation ΔL and R_{SD} were determined to be 3 µm and 1.6 kΩ for a Ti/TiN contact metal, respectively. For a Mo/Al contact metal R_{SD} is close to 0 Ω.

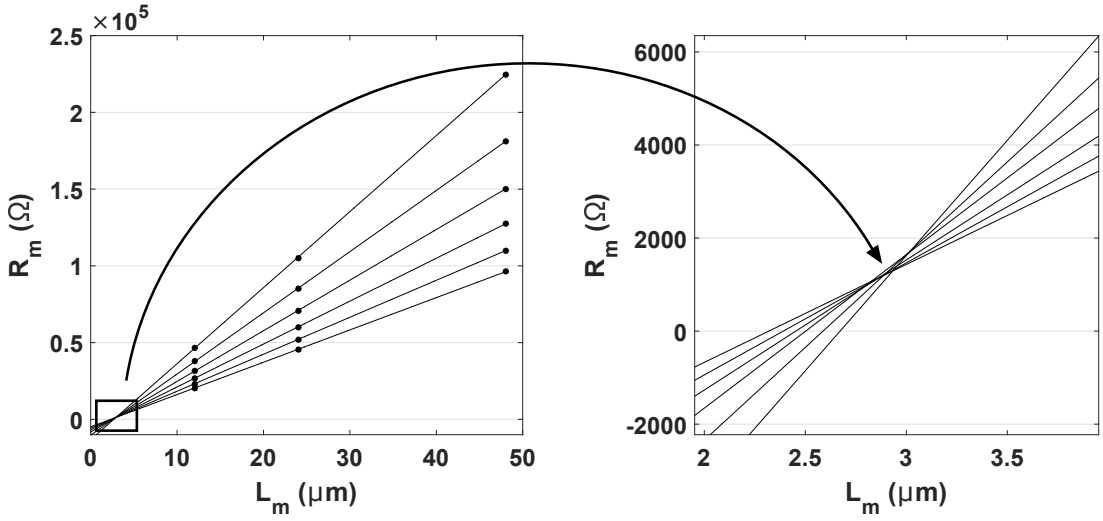

Figure 3.9: Terada-Muta analysis of IGZO TFTs.

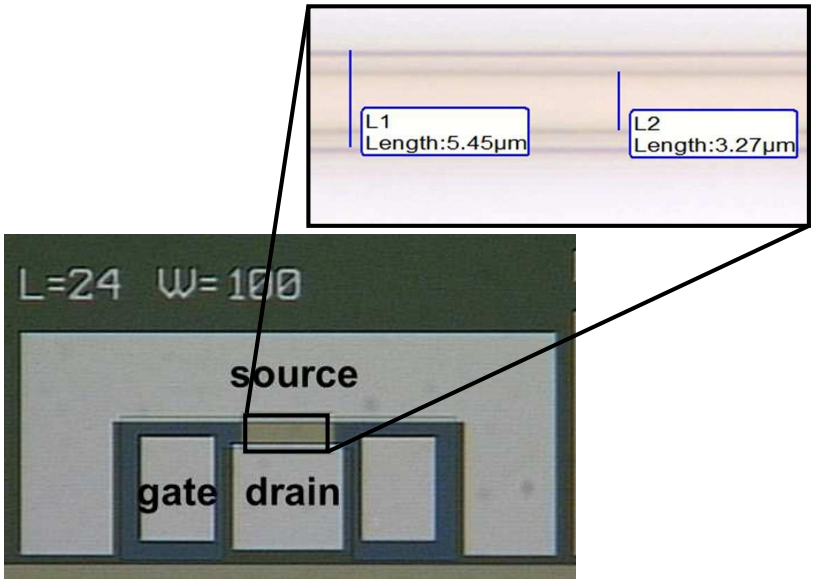

Figure 3.10: S/D lift-off lithography bias with a mask defined channel length of 6 µm.

The image of the TFT channel in Fig. 3.10 shows the S/D liftoff lithography bias present with a mask defined channel length of 6 µm. The photoresist in this image is L1 and the lift-off resist being L2. This is a result of the lift-off resist not being photosensitive and when developing the photoresist additional lift-off resist is removed, undercutting the photoresist. Fig. 3.10 shows an approximate ΔL of 2.18 µm, which shows good correlation with the Terada-Muta extracted ΔL. While the R_{SD} may change with the contact metal used, the ΔL should be consistent assuming the channel length is defined by lift-off lithography.

3.8 Summary of Preliminary Research

Through these experiments it has been established that, for the gate dielectric/IGZO interface of BG_{stg} TFTs no material showed clear benefit over SiO_2 in terms of electrical performance and processing simplicity. Additionally this showed that the densified PECVD SiO_2 compares well with thermally grown SiO_2, in terms of interface quality.

A ripening process was initially observed in un-passivated devices where their electrical properties improve over a period of two weeks. This was further confirmed by partially etching the IGZO of a device which already worked. The result was degraded $I_D - V_{GS}$ transfer characteristics which recovered after two weeks. This phenomenon is hypothesized to be the result of an interaction with air atmosphere and defects created at the back-channel, resulting in effective passivation.

An evaporated Alumina (AlO_x) passivation material was evaluated against un-passivated electrical performance. The results showed that there was slight degradation in SS and V_T was left shifted. Through simulation it was determined that these were the result of traps present at the IGZO/AlO_x interface and additional fixed charge. These devices were not immune to the ripening process observed in un-passivated devices suggesting that oxygen is able to penetrate the evaporated AlO_x at room temperature indicating a relatively porous film.

Integration of a dry-etch into the fabrication process was unsuccessful due to the large amount of plasma damage to the S/D regions. It was speculated that this damage prevented ohmic contact from being formed and was the cause of the distorted $I_D - V_{GS}$ transfer characteristics.

It is undesirable for this ripening process to occur naturally as this may be a large source of variability if left uncontrolled. To remedy this, alternative higher quality passivation materials are desirable. It has also been demonstrated that defects at the back-channel play a major role in the electrical operation of IGZO TFTs. It is reasonable to question how effective the bottom-gate is at controlling any defects present at the back-channel and consider alternative device configurations such as a Top-Gate (TG) electrode.

Terada-Muta analysis revealed $\Delta L = 3$ µm. This value correlated with the lift-off lithography process bias shown in Fig. 3.10. This value of ΔL along with an R_{SD} which was assumed to be negligible were used for all parameter extractions performed throughout this work.

Chapter 4

SiO_2 Passivated TFTs

To address the concerns regarding the quality of the passivation material, in this experiment arguably higher quality PECVD and LPCVD SiO_2 were investigated. Various annealing times were evaluated to determine the optimum for each deposition method. Four different TFT configurations: BG_{stg}, Coplanar Top-Gate (TG_{cop}), Staggered Top-Gate (TG_{stg}) and Double-Gate (DG) will be evaluated individually and comparatively to determine if electrode configuration plays a major role on the electrical performance of IGZO TFTs. The influence of ripening observed in un-passivated and AlO_x passivated TFT were also considered. Device stability was evaluated applying a voltage stress to the gate gate while the source and drain remain grounded. These investigations were evaluated by $I_D - V_{GS}$ transfer characteristics and the extracted electrical parameters.

4.1 Staggered Bottom-Gate Configuration

As a baseline comparison with un-passivated and evaporated alumina passivated devices, TFTs were fabricated in the standard BG_{stg} configuration with a SiO_2 passivation material. Preliminary results which utilized low-pressure CVD and plasma-enhanced CVD were not promising and resulted in poor I_D-V_{GS} transfer characteristics, or conductive IGZO which showed no gate modulation which can be seen in Fig. 4.1.

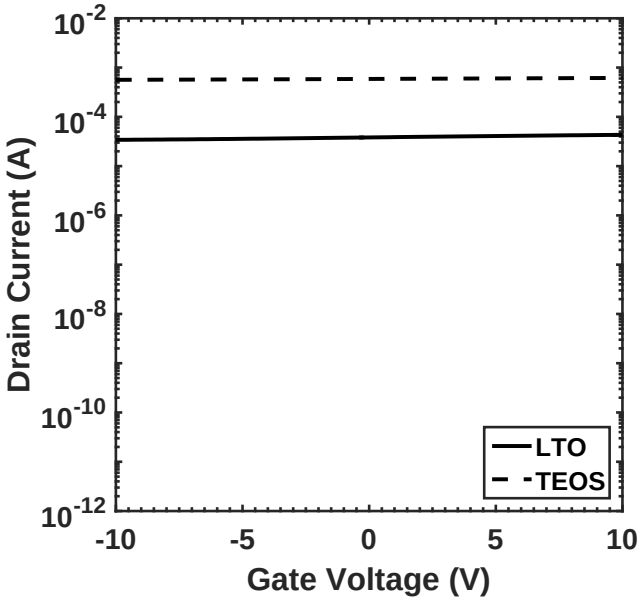

Figure 4.1: I_D-V_{GS} transfer characteristics of SiO_2 passivated TFTs, $V_{DS} = 10$ V.

4.1.1 Designed Experiment BG (bottom-gate)

This experiment follows the outlined process flow in Section 3.1. The passivation material was 140 nm and 100 nm of SiO_2 deposited by low-pressure CVD or plasma-enhanced CVD, respectively and may be seen in Table 4.1. Three different annealing conditions were also performed prior to the gate metal deposition at 400 °C with varying soak times of 2 h, 4 h and 8 h and a 6 h ramp-down, all in an O_2 ambient.

Table 4.1: BG_{stg} TFT experiment.

Wafer	Gate Dielectric	Passivation Material	Anneal
1	100 nm SiO_2 (TEOS)	140 nm SiO_2 (LTO)	A
2		100 nm SiO_2 (TEOS)	B
3		140 nm SiO_2 (LTO)	B
4		100 nm SiO_2 (TEOS)	C

- Anneal A: Soak time 2 h, O_2 ambient, 6 h ramp-down
- Anneal B: Soak time 4 h, O_2 ambient, 6 h ramp-down
- Anneal C: Soak time 8 h, O_2 ambient, 6 h ramp-down

4.1.2 Electrical Characteristics BG

The I_D-V_{GS} transfer characteristics of wafers $1-3$ outlined in Table 4.1 can be seen in Fig. 4.2. For LTO deposited SiO_2 the TFTs benefit from longer anneal times as the off-state performance improves after a 4 h anneal. Representative extracted parameters for the first 3 treatments can be seen in Table 4.2. This shows a clear improvement in sub-threshold separation ΔV, μ_{eff} and SS when LTO is annealed for a longer time. This may also indicates that LTO may benefit from even longer anneal times. Curiously, V_T shifted even further left for the 4 h anneal. Wafer 3 showed superior off-state performance and minimal ΔV while maintaining a reasonable μ_{eff}. For SiO_2 deposited by PECVD a longer, 8 h anneal time was performed. The result was degraded μ_{eff} and SS when compared with the 4 h anneal. This corresponds with an over oxidized state first observed in un-passivated devices and thus this treatment will not be considered further.

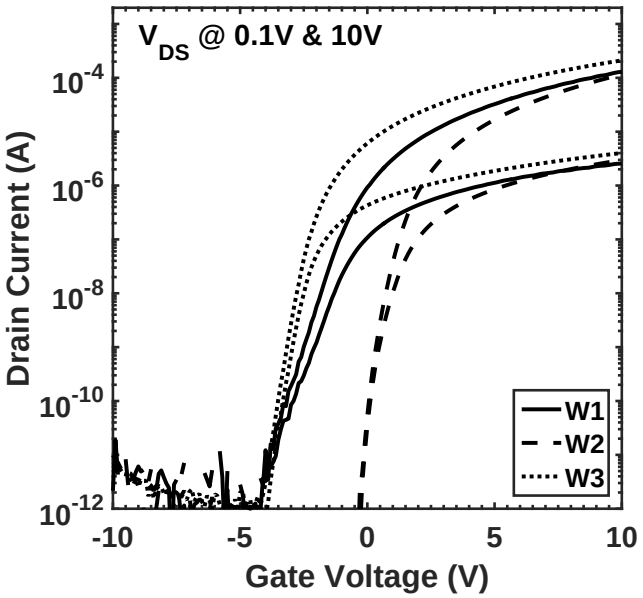

Figure 4.2: BG I_D-V_{GS} transfer characteristics of L/W = 12/100 µm SiO_2 passivated TFTs.

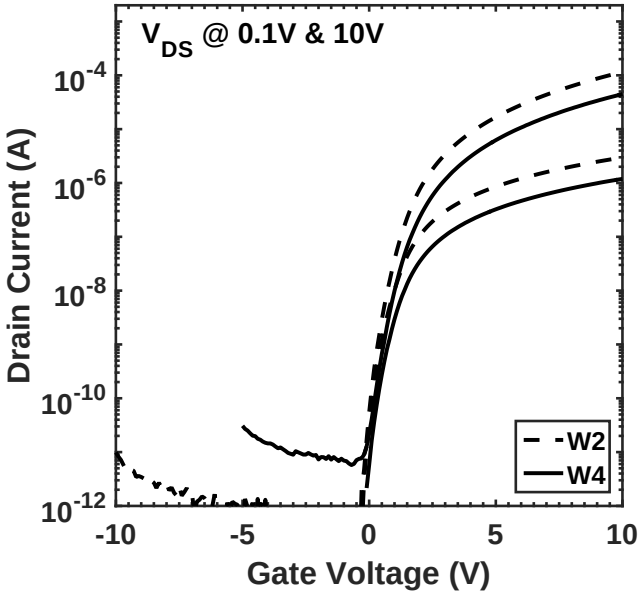

Figure 4.3: I_D-V_{GS} transfer characteristics of over-oxidized IGZO L/W = 12/100 µm SiO_2 passivated TFT.

Table 4.2: BG extracted electrical characteristics of L/W = 12/100 µm SiO_2 passivated BG_{stg} TFTs.

Wafer	V_T (V)	ΔV (V)	μ_{eff} ($cm^2/V \cdot s$)	SS (mV/dec)
1	-0.9	0.5	6.47	614
2	1.1	0.1	8.63	248
3	-2.1	0.3	8.38	396

To determine the behavior of the population of wafers $1-3$ a sample of 30 devices were measured from each wafer. Fig. 4.4 shows that there are clear difference in V_T, μ_{eff} and SS between each of these treatments. Each notch within the box plot indicates that when there is no overlap, the medians are different with a 95 % confidence level. When considering ΔV in terms of off-state performance, it is clear that wafer 2 is the superior treatment; however, wafer 3 is a close runner up in terms of SS.

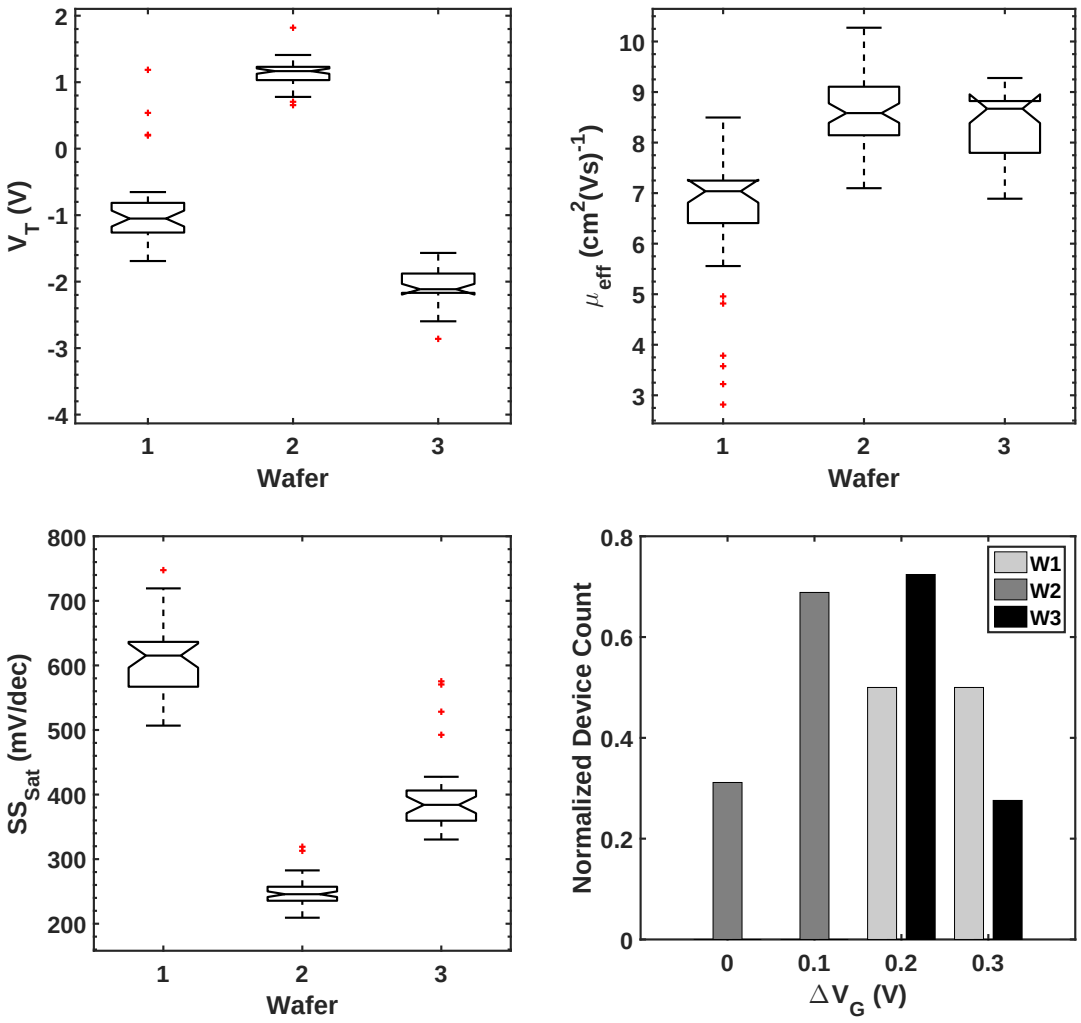

Figure 4.4: Box plots of extracted parameters for wafers BG_{stg} TFTs on $1-3$.

4.1.3 Summary of Results BG

LTO shows reasonable performance with up to 4 h anneal and may benefit from even longer anneal times. TEOS SiO_2 passivated devices show comparable μ_{eff} and superior SS; however, 8 h annealing times resulted in degraded SS from over oxidized IGZO. In contrast to un-passivated and evaporated alumina passivated IGZO, these devices show no signs of short term ripening. Measurements performed a week after initial device testing suggest that the ripening process is inoperative as no notable changes were observed in device performance.

4.2 Coplanar Top-Gate Configuration

4.2.1 Fabrication Process TG_{cop} (Coplanar Top-Gate)

Starting with a 6-inch silicon wafer with a thick oxide, to simulate a glass substrate, a 50 nm IGZO film is RF sputter deposited. The IGZO mesa is defined by etching in a dilute HCl mixture. The source and drain metal is defined by lift-off processing and a Mo/Al bilayer is DC sputter deposited. The gate dielectric is deposited, then annealing is performed. Contact cuts to the source/drain metal are defined by etching in 10:1 buffered HF. The gate metal is defined by lift-off processing and a 250 nm Al film is evaporated. The cross-sectional structures of a BG_{stg} staggered and TG_{cop} TFT structure may be compared in 4.5. This particular configuration is compatible with the BG_{stg} configuration and could be a potential path in developing a DG TFT for improved electrostatics.

4.2.2 Designed Experiment TG_{cop}

The treatment combinations listed in Table 4.3 have two different SiO_2 top-gate dielectrics; plasma-enhanced and low-pressure CVD using TEOS and SiH_4 precursors, respectively. Three different annealing treatments were also performed which include

a 2 h and 4 h oxygen soak followed by a 6 h ramp-down in oxygen. Wafer 2 was performed post gate-metal, on a hotplate, in room air ambient with no ramp-down.

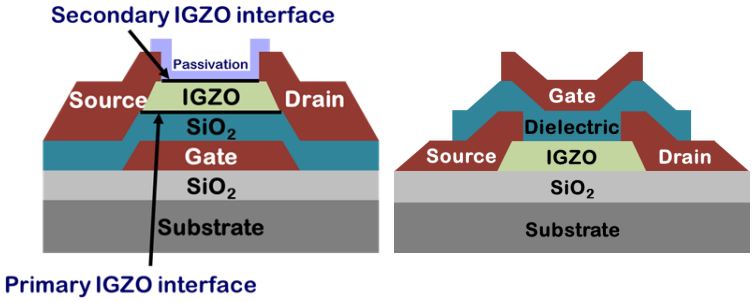

Figure 4.5: Cross-sectional image comparing BG_{stg} (left) and TG_{cop} (right) TFT structures.

Table 4.3: TG_{cop} TFT experiment.

Wafer	S/D Metal	Gate Dielectric	Gate Metal	Anneal
1	Mo/Al	SiO_2(TEOS)	Evaporated Al	A
2		SiO_2(LTO)		B
3		SiO_2(LTO)		C

- Anneal A: Soak time 4 h, O_2 ambient, 6 h ramp-down
- Anneal B: Various soak times, room-air ambient, no ramp-down, (post gate-metal)
- Anneal C: Soak time 2 h, O_2 ambient, 6 h ramp-down

4.2.3 Electrical Characteristics TG_{cop}

Wafers 1 and 3 show reasonable off-state performance followed by significant current challenges in the on-state. Wafer 2, which was annealed after gate metal deposition showed no current modulation. This likely a result of the gate metal effectively blocking any oxidant from reaching the IGZO channel.

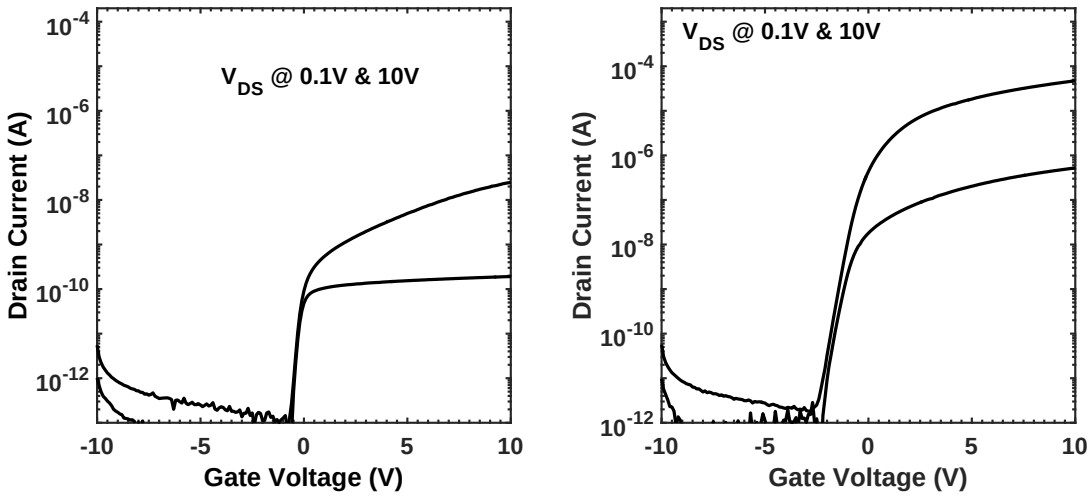

Figure 4.6: TG_{cop} I_D-V_{GS} transfer characteristics with L/W = 12/100 µm of wafer 1 (left) and wafer 3 (right).

4.2.4 Summary of Results TG_{cop}

Devices annealed after gate metal deposition show no current modulation; this indicates that a TG metal could also prevent any age induced degradation in I_D-V_{GS} transfer characteristics and may offer long-term stability. Every device fabricated in this configuration had distorted on-state performance. This is thought to be the result of thicker oxide near the edge of the channel due to the topology of the metal S/D regions. The lowered capacitance in these areas makes it difficult to control the channel in these areas. This manifests itself to appear as if the devices have S/D contact issues and/or significant series resistance.

4.3 Staggered Top-Gate Configuration

4.3.1 Fabrication Process TG_{stg} (Staggered Top-Gate)

Starting with a 6-inch silicon wafer with a thick oxide, to simulate a glass substrate, the source and drain metal is defined by lift-off processing and a Ti/TiN bilayer is DC sputter deposited. Next, a 50 nm IGZO film is RF sputter deposited. The IGZO

mesa is patterned by etching in a dilute HCl mixture. The SiO_2 gate dielectric is deposited, then annealing is performed. Contact cuts to the source/drain metal are defined by etching in 10:1 buffered HF. The gate metal is defined by lift-off processing and a 250 nm Al film is evaporated. The cross-sectional structures of a BG_{stg} and TG_{stg} TFT structure may be seen in Fig. 4.7 on the left and right, respectively.

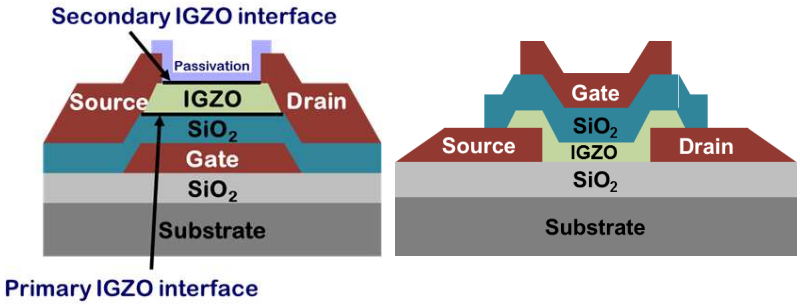

Figure 4.7: Cross-sectional image comparing BG_{stg} (left) and TG_{stg} (right) TFT structures.

4.3.2 Designed Experiment TG_{stg}

This experiment had the same treatment combinations as the coplanar configuration with the only differences being the electrode configuration and S/D metal. The IGZO was unintentionally sputtered with the chuck specified at room temperature rather than the 200 °C standard process.

Table 4.4: TG_{stg} TFT experiment.

Wafer	S/D Metal	Gate Dielectric	Gate Metal	Anneal
4		SiO_2(TEOS)		A
5	Ti/TiN	SiO_2(LTO)	Evaporated Al	B
6		SiO_2(LTO)		C

- Anneal A: Soak time 4 h, O_2 ambient, 6 h ramp-down
- Anneal B: Various soak times, room-air ambient, no ramp-down, (post gate-metal)
- Anneal C: Soak time 2 h, O_2 ambient, 6 h ramp-down

4.3.3 Electrical Characteristics TG_{stg}

As with the coplanar top-gate configuration, annealing after the gate metal has been deposited (wafer 5) resulted in no current modulation. The staggered configuration overcomes the on-state current issue seen in the coplanar configuration and shows improved off-state performance. The two treatments which yielded working TFTs perform near identically as shown in Fig. 4.8. Representative extracted parameters can be seen in Table 4.5 which shows the only discernible difference between wafer 4 and 6 to be a slight difference in μ_{eff}. Upon sampling 120 devices per wafer this relationship holds true and can be seen in Fig. 4.9, which confirms that μ_{eff} is different with a 95 % confidence level. Despite the larger spread of V_T in wafer 4 the other extracted parameters appear to be similar.

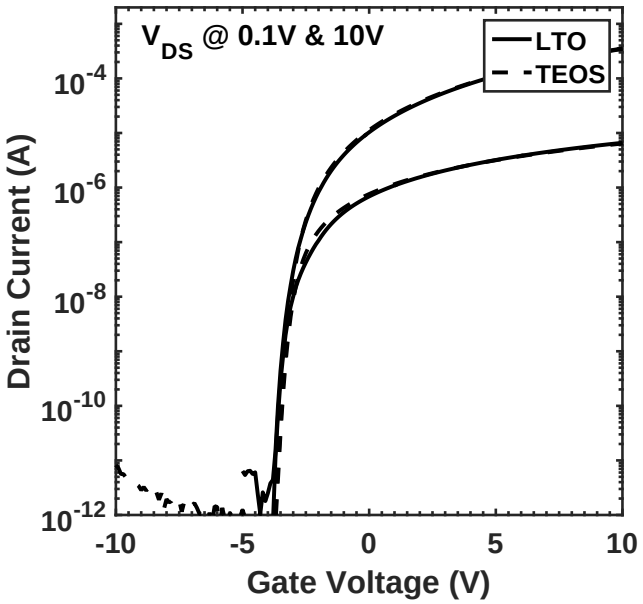

Figure 4.8: Transfer characteristics of TG_{stg} TFTs with dimensions of L/W = 12/100 µm.

Table 4.5: Parameter extractions for wafers 4 and 6.

Wafer	V_T (V)	ΔV (V)	μ_{eff} ($cm^2/V \cdot s$)	SS (mV/dec)
4	-2.5	0	12.53	161
6	-2.6	0.1	13.23	165

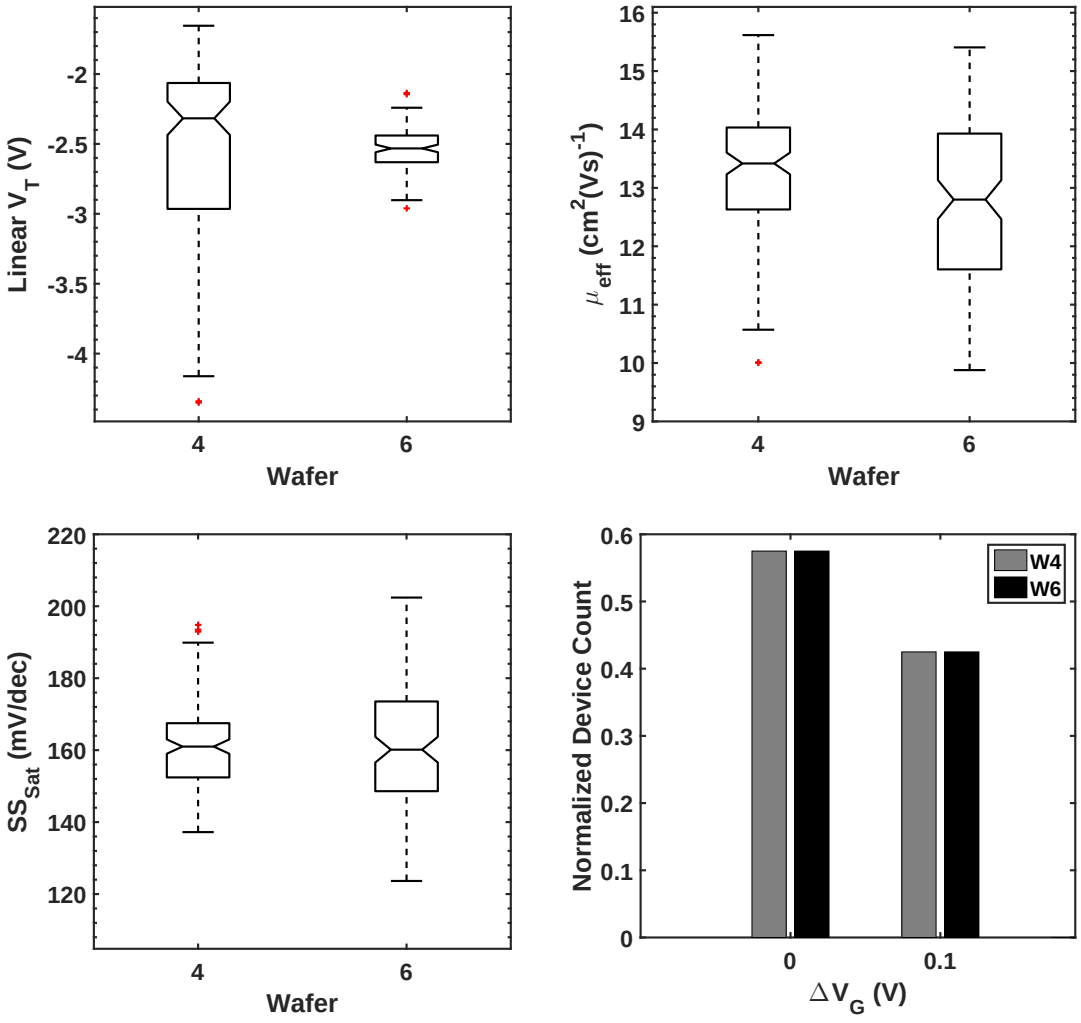

Figure 4.9: Box plots of extracted parameters for L/W = 12/100 µm TFTs.

4.3.4 Summary of Results TG_{stg}

The LTO and TEOS treatments on wafers 6 and 4, respectively were virtually identical. The treatments demonstrated comparable SS despite the LTO anneal being less aggressive. The performance improvement of TG_{stg} over a BG_{stg} configuration supports the hypothesis that a top-gate provides improved channel control due to its close proximity to the secondary interface. It is noted that the V_T is significantly left shifted compared with the BG_{stg} configuration, presumably due to the chuck temperature or perhaps oxide charge beneath the IGZO not operative on the BG_{stg} device.

4.4 Double-Gate Configuration

4.4.1 Fabrication Process DG (Double-Gate)

This device combines a BG_{stg} with TG_{cop}. A 6-inch Si wafer is oxidized to simulate a glass substrate. The Mo gate is sputter deposited 10 nm thick and patterned by a subtractive wet etch. A 100 nm SiO_2 gate dielectric is deposited by plasma-enhanced chemical-vapor deposition (PECVD). The SiO_2 is densified for 2 hours at 600 °C in nitrogen ambient. A 50 nm IGZO film is deposited by RF sputter from a target with an In:Ga:Zn:O atomic ratio of 1:1:1:4, then the IGZO mesa is patterned by subtractive etching in a dilute HCl mixture. The gate contact cuts are etched in 10:1 buffered HF. The source and drain metal is defined by lift-off processing, following which a Mo/Al bilayer is deposited by DC sputter. The SiO_2 gate dielectric is deposited, then annealing is performed. Contact cuts to the source/drain metal are defined by etching in 10:1 buffered HF. The gate metal is defined by lift-off processing and a 250 nm Al film is evaporated. The cross-sectional structures of a BG_{stg} and DG TFT structure may be seen in Fig. 4.10 on the left and right, respectively.

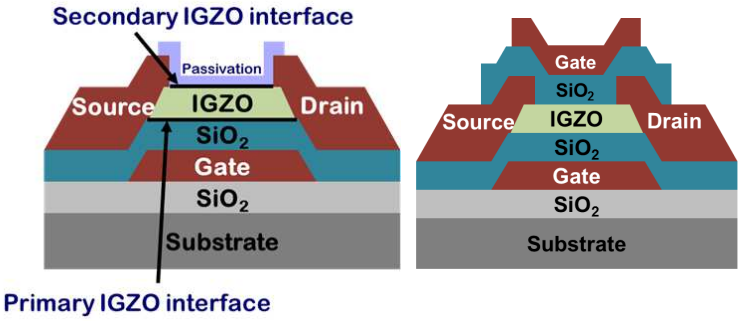

Figure 4.10: Cross-sectional image comparing BG_{stg} (left) and DG (right) TFT structures.

4.4.2 Designed Experiment DG

This configuration replicates the BG_{stg} device experiment with an added co-planar top-gate. The anneal times were 2 h and 4 h and the top-gate dielectric is SiO_2 deposited by PECVD and LPCVD.

Table 4.6: DG TFT experiment.

Wafer	BG_{stg} Dielectric	Top-gate Dielectric	Anneal
1		140 nm SiO_2 (LTO)	A
2	100 nm SiO_2 (TEOS)	100 nm SiO_2 (TEOS)	B
3		140 nm SiO_2 (LTO)	B

- Anneal A: Soak time 2 h, O_2 ambient, 6 h ramp-down
- Anneal B: Soak time 4 h, O_2 ambient, 6 h ramp-down

4.4.3 Electrical Characteristics DG

The I_D-V_{GS} transfer characteristics shown in Fig. 4.11 show clear improvements in off-state performance and μ_{eff} with longer anneal times for LPCVD deposited SiO_2. SiO_2 deposited by PECVD and annealed for 4 h showed further improvement in SS, comparable μ_{eff} and slightly right shifted V_T this may be seen in Fig. 4.11. Please note that μ_{eff} was calculated assuming the electrostatics of a single-gate. Representative extracted values can be seen in Table 4.7.

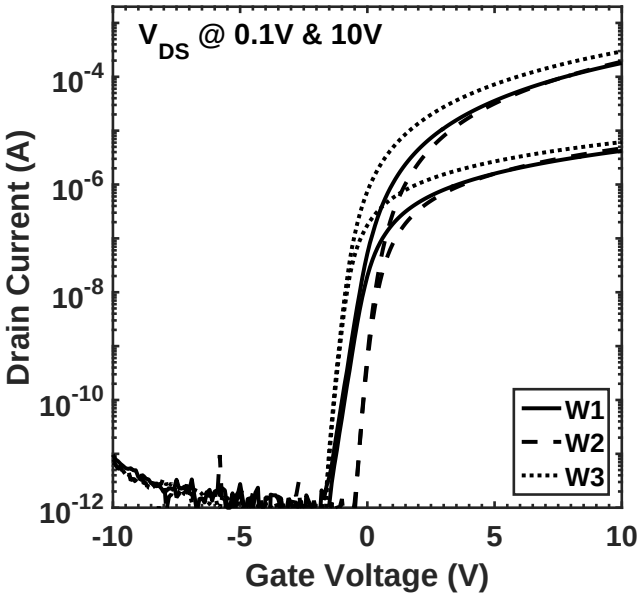

Figure 4.11: I_D-V_{GS} transfer characteristics of DG TFTs.

Table 4.7: Parameter extractions for DG configuration.

Wafer	V_T (V)	ΔV (V)	μ_{eff} ($cm^2/V \cdot s$)	SS (mV/dec)
1	0	0.1	11.82	302
2	0.6	0	14.6	184
3	-0.5	0.1	14.48	210

With a sample size of 30 devices per wafer, box plots which compare DG treatments can be seen in Fig. 4.12. The V_T 4 h anneal for LPCVD SiO_2 was slightly left shifted compared with the 2 h anneal. The μ_{eff} and SS were also improved with longer anneal times. The notches indicating 95 % confidence intervals show that the true medians do differ between these two treatments. The PECVD SiO_2 showed a right shifted V_T. Its SS was also improved over the LPCVD SiO_2 with a 4 h anneal; however, the μ_{eff} was identical.

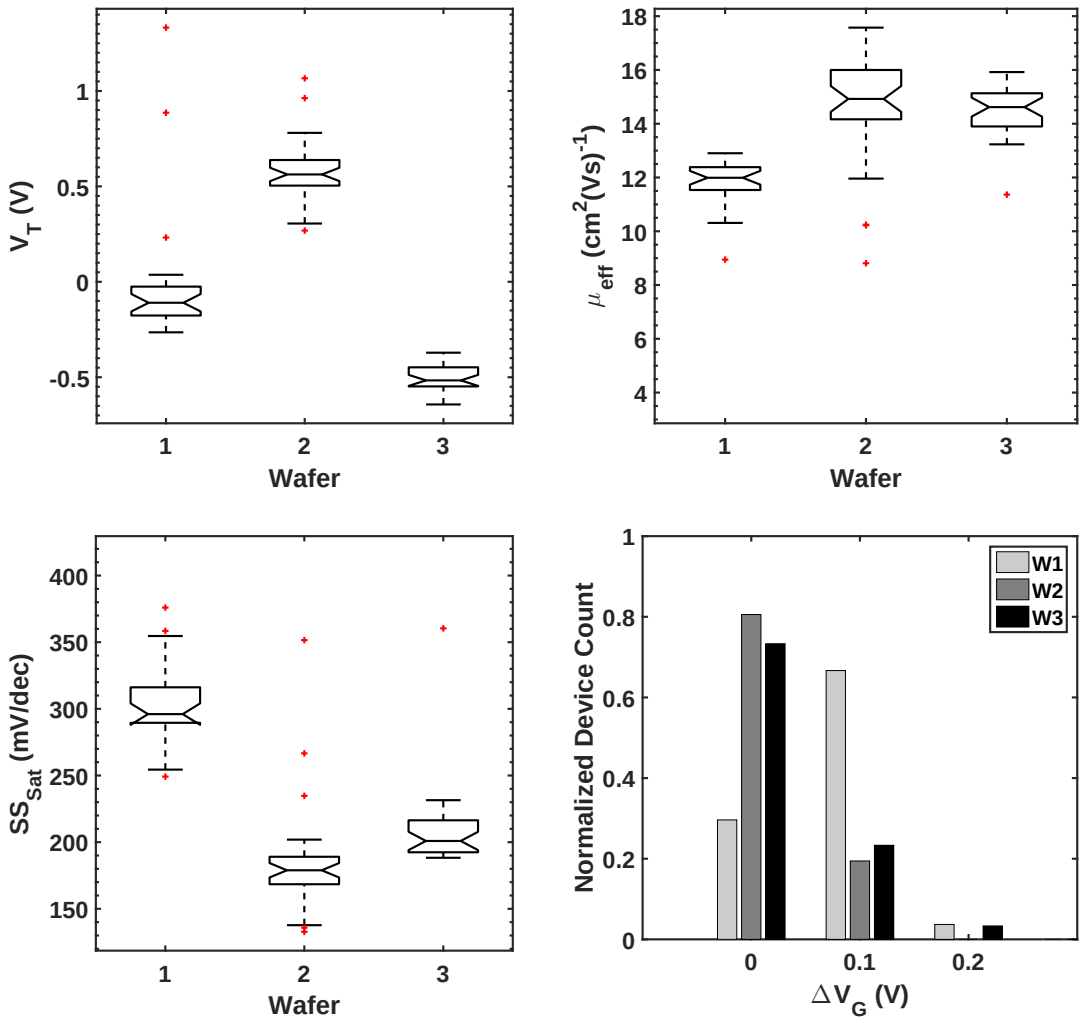

Figure 4.12: Box plots of extracted parameters for L/W = 12/100 µm DG configuration wafers $1-3$.

4.4.4 Summary of Results DG

The DG configuration enjoys improved μ_{eff} and SS. The trends reported for BG_{stg} configuration hold true, in that a 4 h anneal time shows improved μ_{eff} and SS for SiO_2 deposited by LPCVD. When PECVD SiO_2 is used, SS improves from 210 mV/dec to 184 mV/dec.

4.5 Evaluation of TFT Configurations

This section presents a quantitative analysis of BG_{stg}, TG_{stg} and DG configurations with a SiO_2 deposited by PECVD passivation/TG dielectric and 4 h oxygen anneal at 400 °C. An overlay of the I_D-V_{GS} characteristics may be seen in Fig. 4.13.

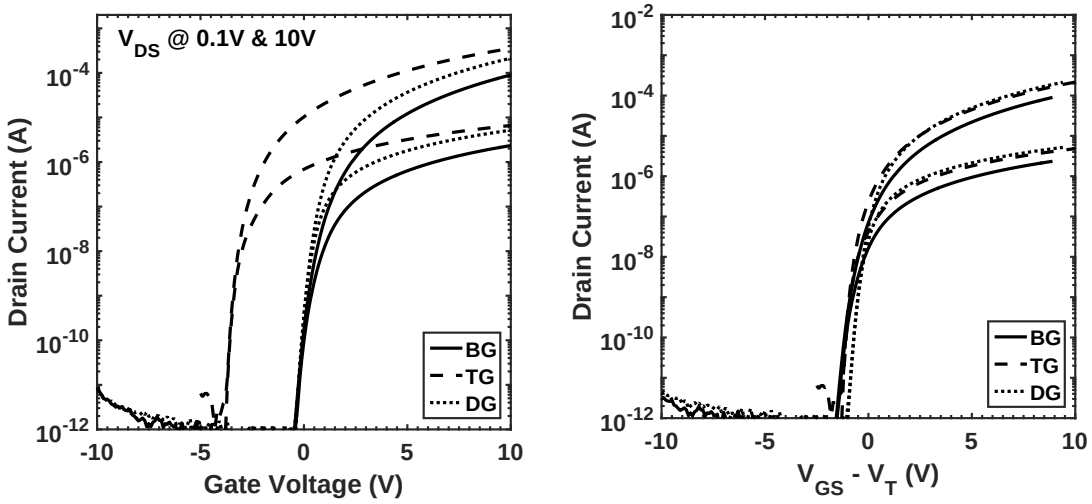

Figure 4.13: I_D-V_{GS} transfer characteristics of BG, TG_{stg} and DG configurations with dimensions of L/W = 12/100 µm as measured (left) and normalized x-axis (right).

To further quantify the difference in these configurations box plots were generated in Fig. 4.14, the sample size of the BG_{stg} and DG configurations was 30 while the sample size of the TG_{stg} configuration was 120. It is noted that the V_T of TG_{stg} is left-shifted by 3 V compared with BG_{stg} and DG configurations. This is may be due to either the chuck temperature being incorrectly set to room temperature rather than

200 °C during the IGZO sputter or oxide charge beneath the IGZO. TG_{stg} and DG configurations show the same trend in ΔV_G where the peak is at 0 V, whereas BG_{stg} shows its peak at 0.1 V. This could indicate performance improvements in both TG_{stg} and DG configurations; however, this measurement lacks significant resolution, as V_{GS} is incremented by 0.1 V. This could be further improved with a 2 part V_{GS} sweep with refined increments in the sub-threshold regime. There is a noted improvement in μ_{eff} when going from a BG_{stg} configuration to a TG_{stg} or DG configuration. For the DG configuration this is a result of μ_{eff} being calculated with a $C_{OX}{}'$ value consistent with a single-gate. The TG_{stg} configuration is likely seeing an enhancement in the μ_{eff} due to the devices being fabricated on a 70 nm thermal oxide[1], effectively making it a DG configuration with a TG_{stg} configuration. By leaving substrate connection floating there will be floating capacitance on the BG_{stg}; however, this may still enhance the electrostatics of the device compared to a true TG TFT on a glass substrate. The SS is also improved with a TG_{stg} and DG configuration. In this case the TG_{stg} configuration has a lower SS than the DG configuration, indicating that potentially the combination of a coplanar BG_{stg} and TG_{stg} may be the optimal configuration for IGZO TFTs.

[1]This does not represent a valid TFT configuration.

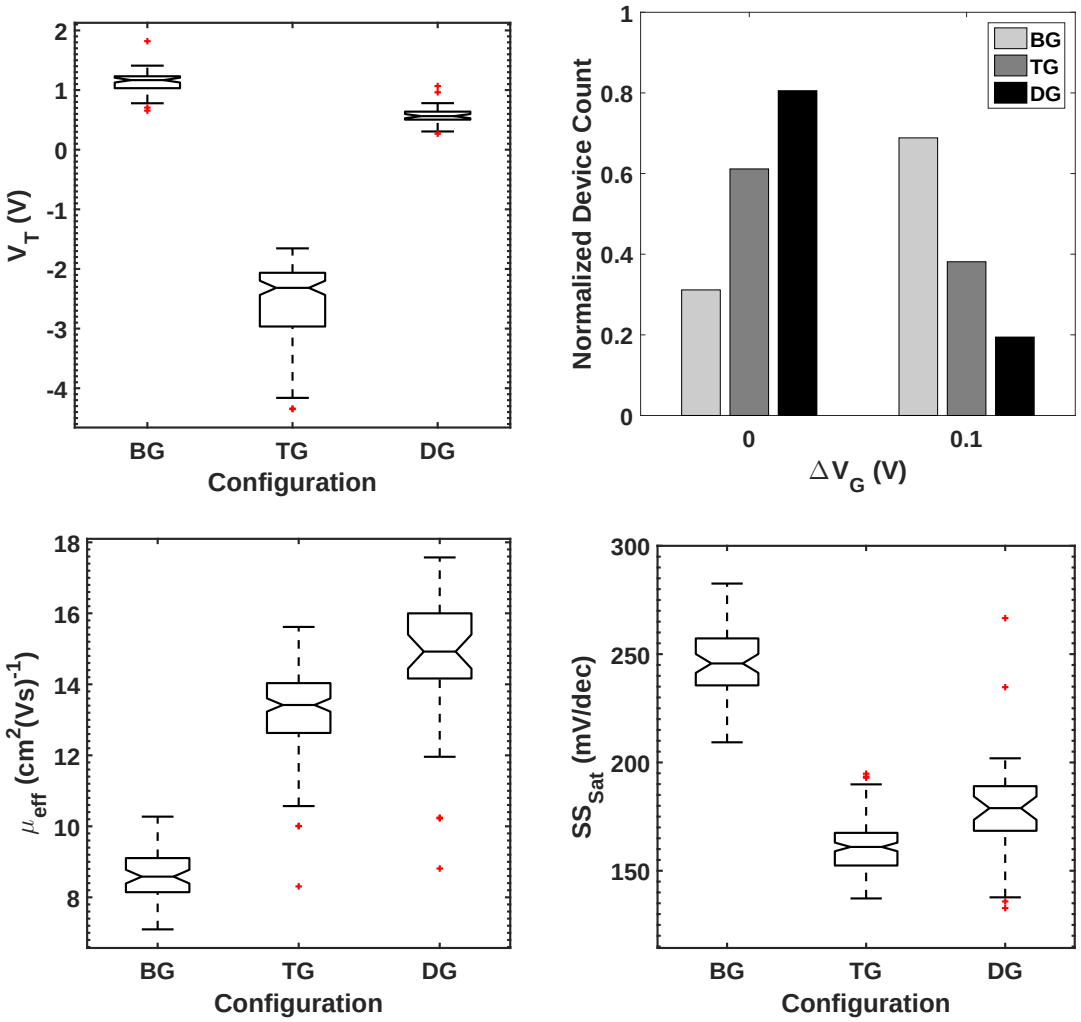

Figure 4.14: Extracted parameters from L/W = 12/100 µm devices with PECVD TG dielectric and 4 h anneals[2].

[2] μ_{eff} calculated for DG configuration assumes a single gate configuration.

4.5.1 Bias-Stress Stability

The bias-stress stability of TFTs is an important parameter when considering the lifetime a display. Over time bias-stress can lead to V_T shifts or degradation of SS which affect the display brightness and may eventually result in sub-pixels not turning on or off. To evaluate the stability of the SiO_2 passivated TFTs each device configuration was considered but only PECVD SiO_2 annealed for 4 h was evaluated. The TFT channel dimensions are L/W = 12/100 µm. An initial measurement was performed, then devices were put under stress according to the conditions listed in Table 4.8. Immediately following the applied stress the devices were measured again. The Positive-Bias Stress Test (PBST) and Negative-Bias Stress Test (NBST) represent normal ON-state and an overdriven OFF-state biases on the gate respectively with no V_{DS} bias. These I_D-V_{GS} transfer characteristics can be seen in Figs. 4.15–4.17. The parameters being evaluated for bias stress stability are ΔV_T, and SS before and after stress, which accounts for any lateral shifting and degradation in the I_D-V_{GS} transfer characteristics.

The BG_{stg} $I_D{-}V_{GS}$ transfer characteristics show significant instability after NBST. Most notably there is a moderate left shift in V_T and a severe degradation in SS. Stability was better with PBST with only a small right shift V_T. This device was not a prime candidate for stress testing due to the large ΔV_G present and may not accurately represent the population.

Table 4.8: Bias stress conditions.

Parameter	Value
V_G (V)	±10
V_{DS} (V)	0
V_S (V)	0
Stress Time (s)	100

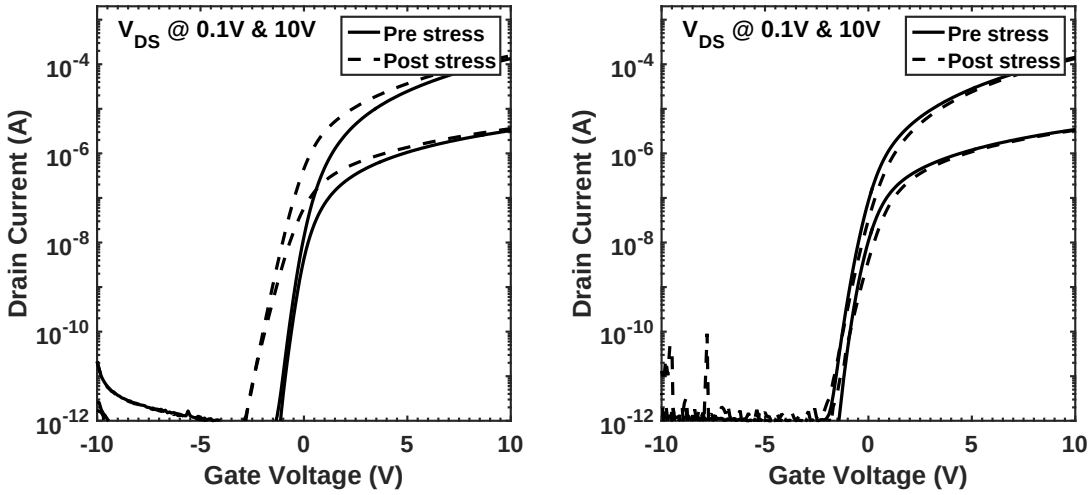

Figure 4.15: BG_{stg} NBST (left) and PBST (right).

The TG_{stg} configuration showed improved bias stress stability compared to the BG_{stg} configuration. After NBST there was a small left shift in V_T and minor increase in SS. Post PBST the opposite was observed, a small right shift in V_T and decrease in SS. Due to the lack of sampling it is impossible to conclude there is a real improvement in SS after PBST or if this is an anomaly due to the relatively large V_{GS} step size when measuring the $I_D - V_{GS}$ transfer characteristics.

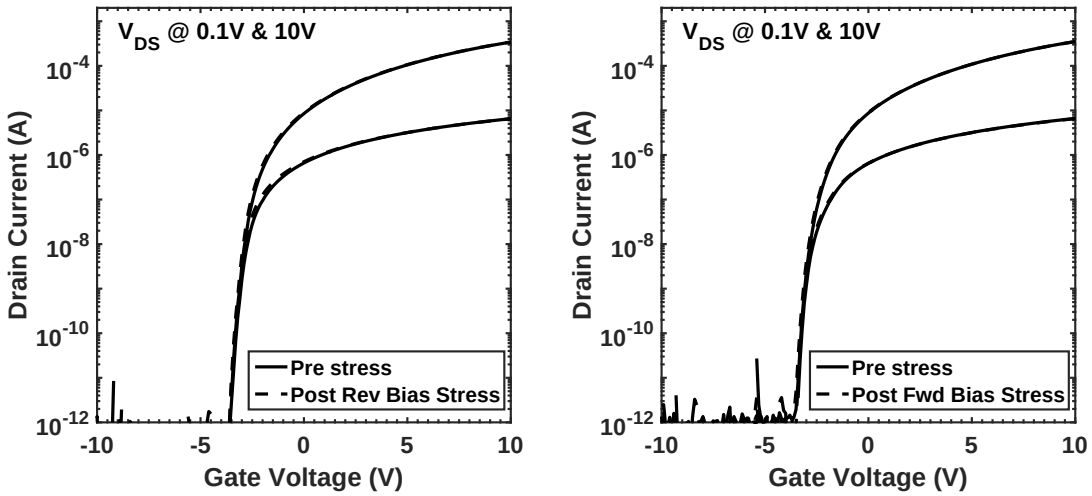

Figure 4.16: TG_{stg} NBST (left) and PBST (right).

The DG configuration showed negligible shift in $I_D - V_{GS}$ transfer characteristics after NBST. There was a moderate right shift in V_T and negligible degradation of SS after PBST. Table 4.9 contains a quantitative summary of the NBST and PBST.

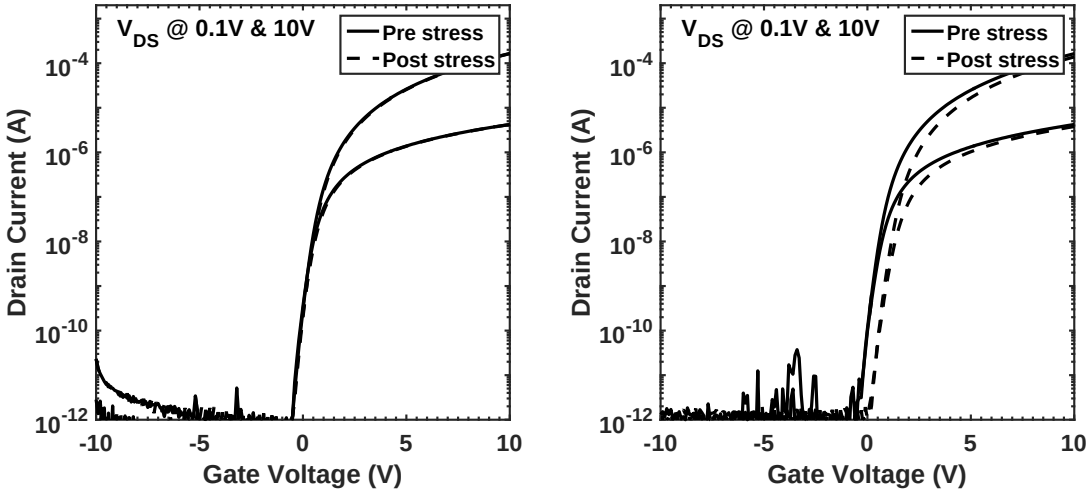

Figure 4.17: DG NBST (left) and PBST (right).

Table 4.9: Change in extracted parameters after bias stress testing.

Configuration	ΔV_T (V)	SS_{pre} (mV/dec)	SS_{post} (mV/dec)
NBST			
BG_{stg}	-0.7	295	445
TG_{stg}	-0.1	166	185
DG	0.1	237	247
PBST			
BG_{stg}	0.1	295	295
TG_{stg}	0.1	167	158
DG	0.2	244	252

The TG_{stg} configuration showed the most resilience to NBST and PBST with the DG configuration being a close second due to the shift in V_T after PBST. BG_{stg} showed the least stability in response to NBST and PBST. These results suggest that a TG is required for improved channel control and stability to voltage stress testing.

This lends credibility to the hypothesis that placing the gate closer to the secondary interface grants it improved control over any process induced defects that may be present at that interface. Additional sampling is required to determine if there truly is a statistical difference in bias stress stability between these configurations.

4.6 Summary of SiO_2 Passivated TFTs

Both TG_{stg} and DG configurations show promising improvements to μ_{eff} and SS over the BG_{stg} configuration. The TG_{stg} configuration was superior to the TG_{cop} which suffered from low current drive. This is likely a result of lack in gate control near the S/D contacts due to the topology present during the gate dielectric deposition. The TG_{stg} had slightly improved SS compared to DG suggesting that the optimum TFT configuration may be a DG which combines a coplanar BG_{stg} with a TG_{stg}. This investigation is currently in progress.

More lateral shifting and degradation in SS is observed in the BG_{stg} configuration whereas forward bias testing these changes are minimal. TG_{stg} and DG configurations show similar shifts for NBST and PBST which were improve over that of the BG_{stg} configuration. This indicates that the TG, whether independent or included with a BG, is important for both improved channel control and reduced sensitivity to bias stress. These results are promising and future work will include larger sampling and more aggressive bias stress testing. These results indicate that the condition of the secondary interface, which is exposed to processing after the IGZO sputter, is critical to the final electrical performance of IGZO TFTs. Further understanding of what is occurring at this interface is required to refine the scope of future research into IGZO TFTs. TCAD modeling can prove invaluable in this aspect but first an IGZO material model must be developed which considers each TFT configuration with the same bulk material model.

Chapter 5

TCAD TFT Simulation

A TCAD model can provide valuable insight into what changes IGZO undergoes during various treatments. Such a model must be able to consider different TFT configurations without modifying the bulk properties and instead introduce defect models to the IGZO interfaces. This level of consistency can be difficult to achieve and thus only BG_{stg} and TG_{stg} configurations were considered for this work. XPS spectra were measured and compared to determine an effective level of oxygen vacancies in the IGZO film before and after annealing, which are represented by doner states in the TCAD model.

5.1 Structure Definition

The TG_{stg} configuration was modeled using the structure shown in Fig. 5.1 which is simulating a 12 µm device with an L_{eff} of 9 µm. The gate is defined at the top of the structure and covers its entire width. Below is a 100 nm SiO_2 gate dielectric and 50 nm IGZO film. The S/D contacts are defined below the IGZO and extend 1 µm in from each side. The distance between these contacts defines the channel length. Below this is a SiO_2 film to simulate the substrate the actual devices are fabricated on. The default material model parameters in Table 5.1 were determined by [4] to be optimal for un-passivated TFTs and were used as the basis for additional model refinement.

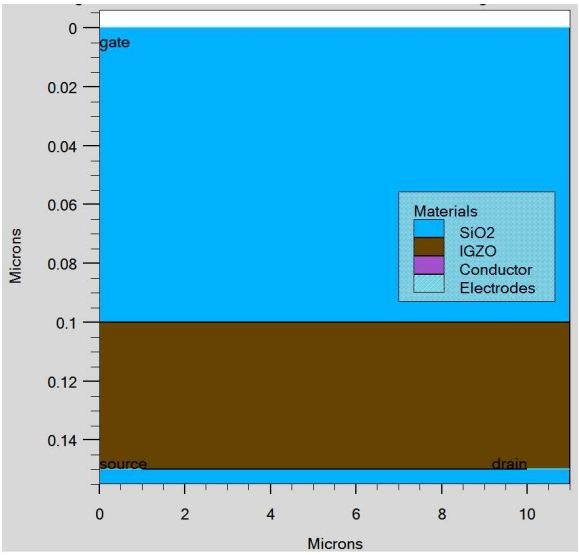

Figure 5.1: Simulated structure of a $\mathrm{TG_{stg}}$ TFT where $L_{eff} = 9$ µm.

Table 5.1: Bulk material model parameters [4].

Parameter	Value	Units
E_g	3.05	eV
χ	4.16	eV
ϵ_{IGZO}	10	
μ_0[1]	25	$\mathrm{cm^2/V \cdot s}$
N_{OV}	2×10^{16}	$\mathrm{cm^{-3}\,eV^{-1}}$
E_{OV}	2.9	eV
W_{OV}	0.1	eV
N_{TA}	1.55×10^{20}	$\mathrm{cm^{-3}\,eV^{-1}}$
W_{TA}	0.013	eV
N_{TD}	1.55×10^{20}	$\mathrm{cm^{-3}\,eV^{-1}}$
W_{TD}	0.12	eV

[1]Note that μ_0 was changed from 15 to 25 to match TG device operation.

The parameters listed in Table 5.1 include: band-gap (E_g), electron affinity (χ), relative permittivity of IGZO (ϵ_{IGZO}), the peak value, mean energy and energy standard deviation of the donor-like states are N_{OV}, E_{OV} and W_{OV}, respectively. The density of acceptor-like and donor-like states in the tail distribution of the conduction and valence band edges, respectively are N_{TA} and N_{TD}, respectively, while the characteristic decay energy of the conduction and valence band-tail states are W_{TA} and W_{TD}, respectively.

This structure was initially developed for and matched to the un-passivated BG_{stg} configuration. This device was fabricated according to the BG_{stg} process flow and annealed in a furnace at 400 °C for 30 min followed by a ramp-down in air for approximately 3 h. In this case the SiO_2 layer below the S/D regions was defined as vacuum and there is no defect statement defined for the gate oxide/IGZO interface. The modeled $I_D - V_{GS}$ transfer characteristics in Fig. 5.2 match very well with the measured data.

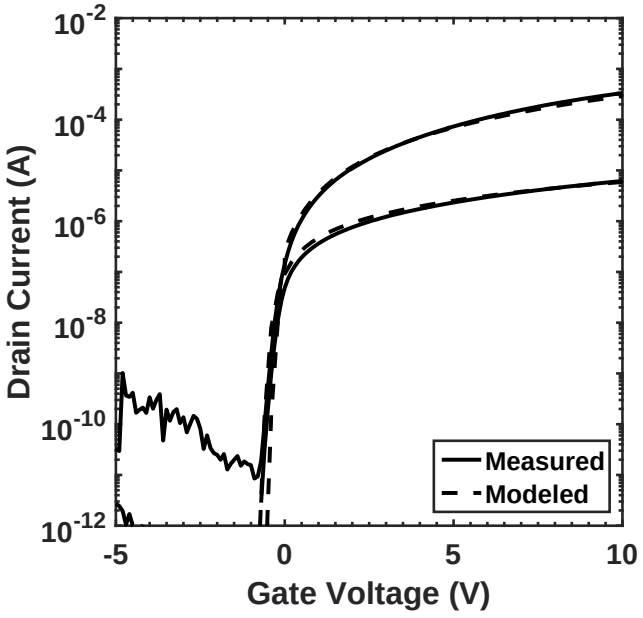

Figure 5.2: Overlay of measured data and TCAD model for an un-passivated TFT with L/W = 6/100 µm where L_{eff} = 3 µm [4].

5.2 IGZO Material Characterization by XPS

Oxygen vacancies play a critical role in the semiconducting properties of IGZO, thus it is important to establish the relationship between the relative number of vacancies and the electrical performance of the TFT. In this case, IGZO was deposited on a silicon wafer which had a thick thermal oxide. The IGZO was annealed in a furnace at 400 °C for 30 min under nitrogen ambient, the ramp-down was for 3 h under room air ambient. XPS spectras were taken before and after annealing with the data windowed to show the O^1s spectra. The oxygen vacancies and lattice oxygen are defined in Fig. 5.3 as O_V^{2-} and O_L^{2-}, respectively. These peaks are centered about 532.5 eV and 531 eV, which agrees well with literature [17]. This spectra lacked an additional Gaussian fit higher in energy than the O_V^{2-} which would correspond with weakly bound oxygen species at the films surface. By taking the integrals of O_V^{2-} and the sum of O_V^{2-} and O_L^{2-} then taking the ratio a quantitative comparison can be performed to characterize the ratios of vacancy and lattice oxygen present in the IGZO film before and after annealing.

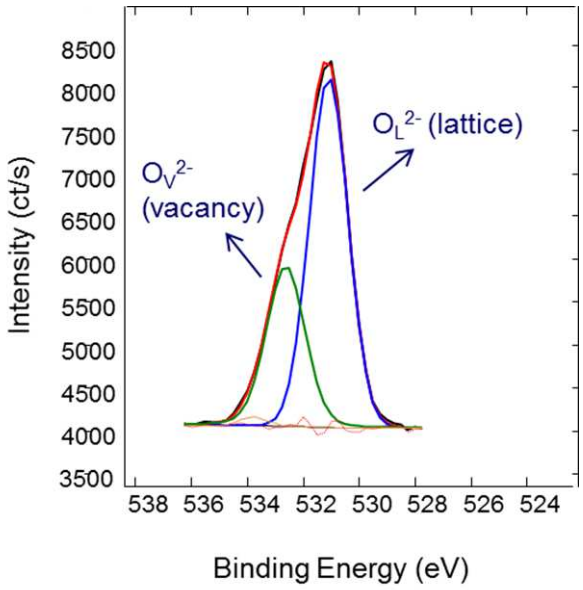

Figure 5.3: O^1s spectra of IGZO with the addition of two Gaussian fits indicating oxygen lattice and vacancy states.

Table 5.2: Ratios of O_V^{2-} in IGZO before and after furnace annealing in a N_2 ambient.

Sample	O_V^{2-}/total
As deposited	0.38
Annealed	0.21

The ratio of O_V^{2-} calculated in Table 5.2 shows nearly a 50 % decrease after annealing indicating a significant reduction in the number of vacancies following the annealing process. These values are much lower than those reported by [17], possibly explaining why the devices in [17] have a very left shifted V_T compared with the device used as a baseline for the TCAD model. A decrease in the N_{OV} parameter in the TCAD model is consistent with these results.

5.3 Model Refinement

The bulk material model was left unchanged initially to maintain consistency with the un-passivated BG_{stg} model. Later, μ_0 was increased to account the higher current of the TG_{stg} devices.Interface defects were added to the IGZO at the IGZO/SiO_2 gate dielectric interface. These represent any process induced damage present at this interface. After performing several preliminary simulations, the primary variables used to match the data were determined to be the peak value and energy of the donor-like interface traps, N_{IT} and E_{OV}, respectively. Fixed charge (N_F) was also added to the primary IGZO interface at $y = 0.15\,\mu m$ to account for the left shifted V_T seen with the TG_{stg} configuration. The default and modified values of these parameters can be found in Table 5.3. Reducing E_{OV} was required to degrade SS while N_{IT} was used to tune the current near V_T. An overlay of a measured device and the model can be seen in Fig. 5.4. This shows a reasonable fit in the off-state and on-state. There is a discrepancy near V_T where the model overestimates the current drive.

Table 5.3: Interface defect model parameters.

Parameter	Initial Value	Refined Value	Units
N_{IT}	0	3×10^{11}	$\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$
$E_{OV}{}^{2}$	2.9	2.8	eV
N_F	0	$+3.3 \times 10^{11}$	cm^{-2}

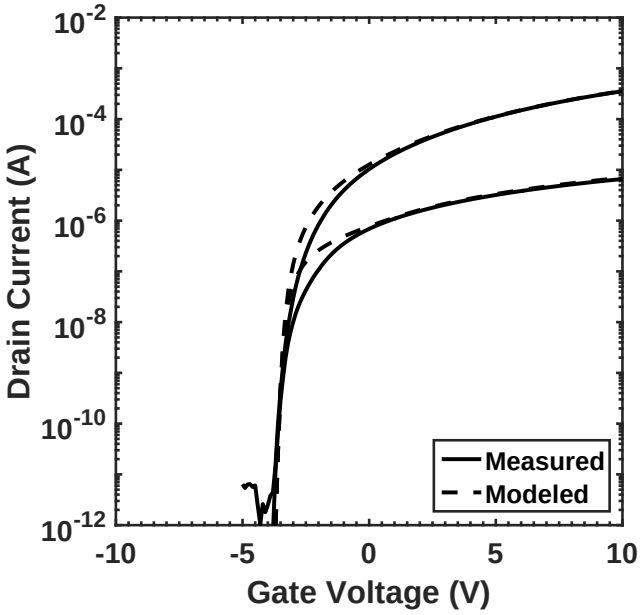

Figure 5.4: Measured and modeled I_D-V_{GS} transfer characteristics L/W = 12/100 µm and L_{eff} = 12 µm.

5.4 Summary of TCAD Simulations

A structure was created and the IGZO model was initially matched with an un-passivated TFT. Through minor modification of oxygen vacancy donors a good match was achieved between the model and measured data. The TG model is currently consistent with the bulk material model used for un-passivated TFT simulation with a minor change to μ_0 to account for current drive enhancement. The addition of interface defects at the secondary interface and fixed charge at the primary interface

[2]Referenced to valence band.

results in a reasonable fit to the experimental data with some overestimation of current in the model near V_T. Investigations are currently underway to determine which parameter in the interface defect may be used to further refine the model in this region.

Chapter 6

Final Remarks

6.1 Summary of Work

IGZO has been shown to be a strong contender for future display applications due its electrical characteristics being superior to a-Si:H, specifically higher electron mobility and lower operating voltage. Issues performing parameter extraction on IGZO TFTs makes a true quantitative comparison with published work impossible. Traditional methods developed for silicon are not applicable and can grossly overestimate V_T and consequently mobility. This issue was solved by developing a parameter extraction method based on a SPICE level-2 model. This uses an effective mobility model where the θ term changing sign to negative accounts for the concave up profile seen in linear mode. This model was then modified to be able to account for ΔL and R_{SD} that can be extracted via Terada-Muta analysis. The IGZO TFTs measured showed a ΔL term of 3 µm while R_{SD} was either 0 kΩ and 1.6 kΩ for Mo/Al and Ti/TiN_x S/D contacts, respectively. This value of ΔL corresponded well with an observed lift-off lithography bias and can be assumed to be valid for all devices whose S/D metal is patterned with this method. In practice this model provides a good fit to the data averaging between 1 % and 2 % NRMSE.

In the preliminary work, the PECVD SiO_2 gate dielectric was evaluated against thermally grown SiO_2, ALD AlO_x and SiN_x. The results showed that PECVD SiO_2,

when densified performs just as well as thermally grown SiO_2, while AlO_x showed no benefits and significant distortion was seen with SiN_x. A ripening process was first observed on un-passivated devices, where after annealing the electrical performance would improve for up to 2 weeks. This process was confirmed by wet etching a working IGZO TFT. The result was a severely distorted $I_D - V_{GS}$ transfer characteristic which then improved again and was fully restored after two weeks of sitting in room air. This process, while beneficial, reveals a potential issue with wafer-to-wafer and lot-to-lot consistency. It would be desirable to directly control this process through annealing or remove it completely. The first attempts at passivation of IGZO TFTs involved evaporated AlO_x. This degraded the SS and resulted in a slight left shift in V_T compared with an un-passivated device. While this degradation was minimal ripening was still observed in the passivated devies. The time for this process appeared to be inversely proportional to channel length. A recipe for dry-etching AlO_x selectively over IGZO was developed in an attempt to move away from lift-off processes and wet-etching. While recipe development was a success, when integrated into the process severe distortion in $I_D - V_{GS}$ transfer characteristics was observed. This was likely caused by plasma damage to the S/D regions not allowing ohmic contact from being formed.

Alternative TFT configurations and passivation materials were investigated to determine their affect on electrical performance, ripening and bias stress stability. In this experiment PECVD and LPCVD SiO_2 was used as a passivation material in the traditional BG_{stg} configuration. In TG and DG configurations the passivation material and gate dielectric were one in the same. The BG_{stg} configuration showed degraded SS compared to AlO_x passivated devices and the TG_{stg} and DG configurations. There was noticeable degradation in the on-state current for the TG_{cop} configuration and it is speculated that this is a result of the topology near the S/D

causing thicker regions of oxide and thus degraded gate control. The TG_{stg} configuration did not suffer from this issue and showed significantly improved $I_D - V_{GS}$ transfer characteristics. Equipment issues during the fabrication of the TG_{stg} devices resulted in the IGZO sputter being performed without appropriate chuck temperature. The left-shifted V_T seems to suggest that this resulted in more oxygen vacancies in the film. The devices were also fabricated on a thermal oxide that may have had significant bulk charge. The DG configuration offered a clear improvement in performance due to the improved electrostatics. The TG_{stg} had slightly lower SS compared to DG suggesting that the optimum TFT configuration may be a DG which combines a coplanar BG_{stg} with a TG_{stg}. This investigation is currently in progress. For each of these configurations PECVD SiO_2 performed better than LPCVD. The annealing experiments suggest for PECVD that 8 h is beyond the upper time limit for annealing. At this point $I_D - V_{GS}$ transfer characteristics begin to degrade. More lateral shifting and degradation in SS is observed in the BG_{stg} configuration after NBST whereas after PBST these changes are minimal. TG_{stg} and DG configurations show similar shifts for reverse and forward bias stress and were improve over that of the BG_{stg} configuration. This indicates that the TG, whether independent or included with a bottom-gate, is important for both improved channel control and reduced sensitivity to bias stress. These results are promising and future work will include larger sampling and more aggressive bias stress testing. These results indicate that the condition of the secondary interface, which is exposed to processing after the IGZO sputter, is critical to the final electrical performance of IGZO TFTs.

A TCAD structure was created and the IGZO model was initially matched with an un-passivated TFT. Through minor modification of oxygen donor states a good match was achieved between the model and measured data. The TG model is currently consistent with the bulk material model used for un-passivated TFT simulation with a change to μ_0 to account for current drive enhancement. The addition of interface

defects and fixed charge to the secondary and primary interfaces, respectively results in a reasonable fit to the experimental data with some overestimation of current in the model near V_T.

6.2 Future Work

Additional work will be performed to determine the effect annealing in alternative ambients have on IGZO $I_D - V_{GS}$ transfer characteristics. The fabrication of TFTs with BG_{stg}, TG_{stg} and the combination of BG_{cop} and TG_{stg} electrode configurations on a single glass wafer. This would eliminate wafer-to-wafer variation when comparing various electrode configurations. The purpose this experiment is to use the measured $I_D - V_{GS}$ transfer characteristics of each electrode configuration to develop a fully consistent TCAD model which considers each TFT electrode configuration. Development of a new testchip with smaller and more refined transistor lengths will allow for analysis of short-channel effects in smaller channel length devices. More aggressive bias-stress testing will be performed to determine comprehensively how resistance these configurations to bias-stress induced shifts in extracted parameters.

Bibliography

[1] S. Depp and W. Howard, "Flat-panel displays," *Scientific American*, vol. 266, no. 3, pp. 90–97, Mar. 1993.

[2] W. Hsueh, "Pixel driving circuit and method for use in active matrix OLED with threshold voltage compensation," US Patent 7 317 435, Jan., 2008.

[3] J.-S. Yoo, S.-H. Jung, Y.-C. Kim, S.-C. Byun, J.-M. Kim, N.-B. Choi, S.-Y. Yoon, C.-D. Kim, Y.-K. Hwang, and I.-J. Chung, "Highly Flexible AM-OLED Display With Integrated Gate Driver Using Amorphous Silicon TFT on Ultrathin Metal Foil," *Journal of Display Technology*, vol. 6, no. 11, pp. 565–570, Nov. 2010.

[4] T. Mudgal, N. Walsh, N. Edwards, R. G. Manley, and K. D. Hirschman, "Interpretation of defect states in sputtered IGZO devices using i-v and c-v analysis," vol. 64, no. 10, pp. 93–100, Aug. 2014.

[5] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In–Ga–Zn–O thin-film transistors," *Science and Technology of Advanced Materials*, vol. 11, no. 4, p. 044305, Aug. 2010.

[6] J. K. Jeong, "The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays," *Semiconductor Science and Technology*, vol. 26, no. 3, p. 034008, Mar. 2011.

[7] Y. Matsueda, "Required characteristics of TFTs for next generation flat panel display backplanes," *Digest of Int. Transistor Conf*, p. 314, 2010.

[8] Y. Kuo, "Thin film transistor technology-past, present and future," *The Electrochemical Society Interface*, vol. 22, no. 1, pp. 55–61, 2013.

[9] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO4," *Thin Solid Films*, vol. 486, no. 1, pp. 38–41, Aug. 2005.

[10] H. Hosono, "Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application," *Journal of Non-Crystalline Solids*, vol. 352, no. 9, pp. 851–858, Jun. 2006.

[11] D. A. Mourey, D. A. Zhao, J. Sun, and T. N. Jackson, "Fast PEALD ZnO thin-film transistor circuits," *IEEE Transactions on Electron Devices*, vol. 57, no. 2, pp. 530–534, Feb. 2010.

[12] T. Kamiya, K. Nomura, and H. Hosono, "Subgap states, doping and defect formation energies in amorphous oxide semiconductor a-ingazno4 studied by density functional theory," *physica status solidi (a)*, vol. 207, no. 7, pp. 1698–1703, 2010.

[13] J. Raja, K. Jang, C. P. T. Nguyen, J. Yi, N. Balaji, S. Q. Hussain, and S. Chatterjee, "Improvement of mobility in oxide-based thin film transistors: A brief review," *Transactions on Electrical and Electronic Materials*, vol. 16, no. 5, pp. 234–240, Oct. 2015.

[14] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono, "Trap densities in amorphous-InGaZnO[sub 4] thin-film transistors," *Applied Physics Letters*, vol. 92, no. 13, p. 133512, 2008.

[15] H.-H. Hsieh, C.-H. Wu, C.-W. Chien, C.-K. Chen, C.-S. Yang, and C.-C. Wu, "Influence of channel-deposition conditions and gate insulators on performance and stability of top-gate IGZO transparent thin-film transistors," *Journal of the Society for Information Display*, vol. 18, no. 10, p. 796, 2010.

[16] N. Walsh, "Passivation of Amorphous Indium-Gallium-Zinc Oxide (IGZO) Thin-Film Transistors," Master's thesis, Rochester Institute of Technology, 2014.

[17] T. T. T. Nguyen, O. Renault, B. Aventurier, G. Rodriguez, J. P. Barnes, and F. Templier, "Analysis of IGZO Thin-Film Transistors by XPS and Relation With Electrical Characteristics," *Journal of Display Technology*, vol. 9, no. 9, pp. 770–774, Sep. 2013.

Acronyms

AlO_x Alumina

a-Si:H Hydrogenated Amorphous Silicon

BG_{stg} Staggered Bottom-Gate

CCFL Cold-Cathode Fluorescent Lamp

DG Double-Gate

IDC Interdigitated Capacitor

IGZO Indium Gallium Zinc Oxide

LTO Low-Temperature Oxide

NBST Negative-Bias Stress Test

NRMSE Normalized Root-Mean-Square Error

PE-ALD Plasma-Enhanced Atomic Layer Deposition

PBST Positive-Bias Stress Test

SiO_2 Silicon Dioxide

TEOS tetraethyl orthosilicate

TFT Thin-Film Transistor

TG_{cop} Coplanar Top-Gate

TG_{stg} Staggered Top-Gate

Appendix A: Parameter Extraction Matlab Code

```
function [extract]=iv_fit_extraction(IV,l_chan,delL,Rsd)
%% Iterative model fit until Vgs-Vt is > 0
x1=IV(:,1);x2=x1;y1=IV(:,2);y2=IV(:,3);
indx=find(x2==5);
if x1(1)<x1(2)
%Removing Vg above 5V for saturation
x2(indx:length(x2))=[];y2(indx:length(y2),:)=[];
%Finding SS
indx=find(IV(:,3)<1e-10,1,'last')+1;
indx2=find(IV(:,2)<1e-10,1,'last')+1;
%Removing data below SS location
x1(1:indx-1)=[];y1(1:indx-1)=[];
x2(1:indx-1)=[];y2(1:indx-1)=[];
else
%Removing Vg above 5V for saturation
x2(1:indx)=[];y2(1:indx)=[];
%Finding SS
indx=find(IV(:,3)<1e-10,1,'first')-1;
indx2=find(IV(:,2)<1e-10,1,'first')-1;
%Removing data below SS location
x1(indx-1:length(x1))=[];y1(indx-1:length(y1))=[];
x2(indx-1:length(x2))=[];y2(indx-1:length(y2))=[];
end
SS_sat=(IV(indx+1,1)-IV(indx-1,1))/(log10(IV(indx+1,3))-log10(IV(indx
    -1,3)))*1e3;
vg_ss=IV(indx,1);
vg_lin=IV(indx2,1);
dvg=abs(vg_ss-vg_lin);
vt_lin=vg_lin; vt_sat=vg_ss;mu0=10;theta=-0.001;
logic=min(x1)-vt_lin>0 && min(x2)-vt_sat>0;
while logic==0
x1=round(x1,1);
```

```
x2=round(x2,1);
indx1=find(x1==round(vt_lin,1));
indx2=find(x2==round(vt_sat,1));
if x1(1)<x1(2)
x1(1:indx1)=[];y1(1:indx1)=[];
x2(1:indx2)=[];y2(1:indx2)=[];
else
x1(indx1:length(x1))=[];y1(indx1:length(y1),:)=[];
x2(indx2:length(x2))=[];y2(indx2:length(y2),:)=[];
end
[xfit,rmse]=minimize(x1,y1,x2,y2,l_chan,mu0,vt_lin,vt_sat,theta,delL,Rsd
    );
mu0=xfit(1);vt_lin=xfit(2);vt_sat=xfit(3);theta=xfit(4);
logic=min(x1)-vt_lin>0 && min(x2)-vt_sat>0;
end
if isempty(Rsd)==1
extract=[vt_lin,vt_sat,dvg,mu0,SS_sat,vg_ss,theta,rmse];
else
extract=[vt_lin,vt_sat,dvg,mu0,SS_sat,vg_ss,theta,Rsd,delL,rmse];
end
% fprintf('NRMSE=%d\n',rmse);
% fprintf('mu0=%d, vt_lin=%d, vt_sat=%d, theta=%d, SS=%d\n',mu0,vt_lin,
    vt_sat,theta,SS_sat)
end
function [xfit,rmse] = minimize(x1,y1,x2,y2,l_chan,mu0,vt_lin,vt_sat,
    theta,delL,Rsd)
%% Setup initial conditions and bounds
% x(1)=mu0, x(2)=vt_lin, x(3)=vt_sat, x(4)=theta,
%IGZO
x0=[mu0,vt_lin,vt_sat,theta];
lb=[1,-10,-10,-1];
ub=[100,10,10,1];
```

```
%Returns RMSE of linear and saturation current equations summed together
    .
%This assumes vt theta and mobility are the same in linear and
    saturation.
objective = @(x) myerrorfun(x,x1,x2,y1,y2,l_chan,delL,Rsd);
%% Modify options setting
options = optimoptions('fmincon');
options = optimoptions(options,'Display', 'off');
options = optimoptions(options,'TolFun', 1e-6);
options = optimoptions(options,'TolCon', 1e-6);
%% Performs the simultaneous non-linear regression
%xfit returns [mu0 vt theta]
xfit = fmincon(objective,x0,[],[],[],[],lb,ub,[],options);
%Gathering RMSE and each function for plotting,
% [rmse,~,~,~,~]=myerrorfun(xfit,x1,x2,y1,y2,l_chan,delL,Rsd);
[rmse,nrmsl,nrmss,f1,f2]=myerrorfun(xfit,x1,x2,y1,y2,l_chan,delL,Rsd);
end
function [rmse,nrmsl,nrmss,f1,f2] = myerrorfun(x,x1,x2,y1,y2,l_chan,delL
    ,Rsd)
% x(1)=mu0, x(2)=vt_lin, x(3)=vt_sat, x(4)=theta
f1=(y1./(((3.408e-6/(l_chan-delL))*x(1)).*(0.1-y1*Rsd)-y1*x(4)))+x(2);
f2=(x(4)+sqrt(x(4)^2+2*((3.408e-6/(l_chan-delL))*x(1))./y2)).*(y2
    /(((3.408e-6/(l_chan-delL))*x(1))))+x(3)+y2*Rsd/2;
indx1=isnan(f1)==1;
indx2=isnan(f2)==1;
f1(indx1)=0;
f2(indx2)=0;
nrmsl=sqrt(sum((f1-x1).^2)/length(x1))/abs(max(x1)-min(x1));
nrmss=sqrt(sum((f2-x2).^2)/length(x2))/abs(max(x2)-min(x2));
rmse=nrmsl+nrmss;
end
```

Appendix B: Silvaco TCAD Simulation Code

```
c

go atlas simflags="-P 8"
#==========Set Variables==================
#-------------------Save variable
#-----------thickness
set T=0.05
#---------Length
set L=9
#----------Number of Oxygen Vacancies (OV), donor type ngd
set nov=2e16
#-----------Average energy of OV , donor  egd
set eov=2.9
set ideov=2.8
#-----------Std Deviation of OV ,donor   wgd
set wov=0.15
set idwov=0.15
#----------Conduction band tail slope , acceptor type wta
set cbtw=0.013
set idcbtw=0.013
#---------- Valence band tail slope ,donor type  wtd
set vbtw=0.12
set idvbtw=0.12
#----------Capture cross-section
set sig=1e-15
set qf=3.3e11
set nit=3e11
#set ntd=5e17
#set idnta
#======================================= mesh outf statement required,
    otherwise wont run, specifies the format of output file
mesh width=100 master.out
```

```
x.m l=0 s=0.1
#x.m l=0.8 s=0.01
#x.m l=1.2 s=0.01
#x.m l=(2+$"L")/2 s=0.05
#x.m l=1+$"L"-0.2 s=0.01
#x.m l=1+$"L"+0.2 s=0.01
x.m l=2+$"L" s=0.1
y.m l=0 s=0.01
y.m l=0.1 s=0.001
y.m l=0.1+$"T" s=0.001
y.m l=0.105+$"T" s=0.005

eliminate rows x.min=0 x.max=16 y.max=0.06
#
#
#================Define IGZO=================
#region num=1 material=igzo y.min=0.005 y.max=0.005+$"T"
#============================================
#region num=2 material=sio2 y.min=0.005+$"T" y.max=0.105+$"T"
#region num=3 material=vacuum y.max=0.005

region num=1 material=sio2 y.max=0.1
region num=2 material=IGZO y.min=0.1 y.max=0.1+$"T"
region num=3 material=sio2 y.min=0.1+$"T" y.max=0.105+$"T"

elec num=1 name=gate top
elec num=2 name=source y.max=0.1+$"T" y.min=0.1+$"T" x.min=0.0 x.max
    =1.0
elec num=3 name=drain y.max=0.1+$"T" y.min=0.1+$"T" x.min=1+$"L" x.max
    =2+$"L"
#
#================Gate=================
```

```
contact num=1 workf=4.53
#============S/D Contacts============
contact num=2 workf=4.13
contact num=3 workf=4.13
#==========Set IGZO Parameters==========
material region=2 material=IGZO user.group=semiconductor user.default=
    silicon mun=25 mup=.1 nc300=5e18 nv300=5e18 eg300=3.05 affinity=4.16
     permittivity=10 mc=.34
#====================Defects=========================
################ Bulk defects
defects nta=1.55e20 ntd=1.55e20 wta=$"cbtw" wtd=$"vbtw" \
nga=0.0 ngd=$"nov" egd=$"eov" wgd=$"wov" \
sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
numa=128 numd=64 tfile=bulk_defects.dat
################ Fixed charge at the dielectric/IGZO interface presumably
    created during sputtering
interface       y.min=0.1+$"T" y.max=0.1+$"T" qf=$"qf"
############ For passivation use these defects at the back channel
intdefects y.min=0.1 y.max=0.1 x.min=0 x.max=2+$"L" nta=0 ntd=0 wta=$"
    idcbtw" wtd=$"idvbtw" \
nga=8e10 ngd=$"nit" egd=$"ideov" wgd=$"idwov" \
sigtae=$"sig" sigtah=$"sig" sigtde=$"sig" sigtdh=$"sig" \
siggae=$"sig" siggah=$"sig" siggde=$"sig" siggdh=$"sig" \
numa=128 numd=64 tfile=interface_defects.dat dfile=tftex10_don.dat afile
    =tftex10_acc.dat
#
models fermi print
#models bbt.std
#material d.tunnel=1e-6 me.tunnel=0.2
method climit=1e-4 maxtrap=4 carrier=1 electron
output con.band val.band u.trap
#========================= Id-Vg============================
```

```
solve init
save outfile=solveinit_nit$"nit"_nta0_ntd0_idcbtw$"idcbtw"_idvbtw$"
    idvbtw"_egd$"ideov"_idwov$"idwov"_L$"L".str
solve vgate=-0.1
solve vgate=-0.2
solve vgate=-1
solve vgate=-2
solve vgate=-3
solve vgate=-5
solve vdrain=0.1
save outfile=vg-5vd0.1_nit$"nit"_nta0_ntd0_idcbtw$"idcbtw"_idvbtw$"
    idvbtw"_egd$"ideov"_idwov$"idwov"_L$"L".str
log outf=6um_0.1V_1umOL_nit$"nit"_nta0_ntd0_idcbtw$"idcbtw"_idvbtw$"
    idvbtw"_egd$"ideov"_idwov$"idwov"_L$"L".log
solve vgate=-5 vstep=0.1 vfinal=10 name=gate
extract init inf="6um_0.1V_1umOL_nit$"nit"_nta0_ntd0_idcbtw$"idcbtw"
    _idvbtw$"idvbtw"_egd$"ideov"_idwov$"idwov"_L$"L".log"
extract name="vg1dibl" x.val from curve(abs(v."gate"),abs(i."drain"))
    where y.val=1e-8
log off

#High Drain
solve init
solve vgate=-0.1
solve vgate=-1
solve vgate=-3
solve vgate=-5
solve vdrain=0.1
solve vdrain=0.2
solve vdrain=1
solve vdrain=2
solve vdrain=3
```

```
solve vdrain=4
solve vdrain=5
solve vdrain=7
solve vdrain=10
save outfile=vg-5vd10_nit$"nit"_nta0_ntd0_idcbtw$"idcbtw"_idvbtw$"idvbtw
    "_egd$"ideov"_idwov$"idwov"_L$"L".str
log outf=6um_10V_1umOL_nit$"nit"_nta0_ntd0_idcbtw$"idcbtw"_idvbtw$"
    idvbtw"_egd$"ideov"_idwov$"idwov"_L$"L".log
solve vgate=-5 vstep=0.1 vfinal=10 name=gate
log off

extract init inf="6um_10V_1umOL_nit$"nit"_nta0_ntd0_idcbtw$"idcbtw"
    _idvbtw$"idvbtw"_egd$"ideov"_idwov$"idwov"_L$"L".log"
extract name="vg2dibl" x.val from curve(abs(v."gate"),abs(i."drain"))
    where y.val=1e-8
extract name="ndibl" abs($"vg1dibl"-$"vg2dibl")/(10.0-0.1)
extract name="vg1ss" x.val from curve(v."gate",i."drain") where y.val=1e
    -10
extract name="vg2ss" x.val from curve(v."gate",i."drain") where y.val=1e
    -12
extract name="SS_sat" ($"vg1ss"-$"vg2ss")/(log10(1e-10)-log10(1e-12))
    *1000

quit
```

Appendix C: Process Recipies

Table C.1: LAM 4600 BCl_3/Cl alumina etch recipe.

Parameters	Stabalization	Breakthrough	Etch	Purge
Power (W)	0	250	250	0
Gap (cm)	3	3	3	5.3
Pressure (mTorr)	100	100	100	0
N_2 (sccm)	13	13	20	25
BCl_3 (sccm)	50	50	25	0
Cl_2 (sccm)	10	10	30	0
$CHCl_3$ (sccm)	8	8	8	8
Time (s)	15	5	500	5

Table C.2: CVC 601 Sputter Recipes.

Material	Power (W)	Gas	Flow Rate (sccm)	Pressure (mTorr)	Deposition Rate ($Å\,min^{-1}$)
Al	1000	Ar	20	5	500
ITO[1]	180	Ar	20	5	40
Mo	1000	Ar	20	2.8	150
Ti	1000	Ar	20	6	322
TiN_x	500	Ar/N_2	20/22	4.8/1.2	31

[1]Pulsed DC sputter with 1600 ns pulse width at 250 kHz

Appendix D: BG Process Flow

#	Step	Process Parameters	Process Details	Record	Wafers
1	Create Lot Notebook	Obtain a cleanroom notebook, a previous notebook can be used Update and insert the file located in:	Tape into the notebook: Process Flow (this document) and lot split info Important Lot Processing Information Sheet		
2	Scribe	Tool: Diamond Tips Scrib Scribe monitor wafers with the lot number and M1, M3, M4. (these can be found in the monitor wafer box) Print out wafer box label and tape it on 6" or 4" polypropylene box	Also make sure all wafers are scribed correctly.		All Wafers
3	RCA Clean	Tool: RCA Bench			All Wafers
4a	Thick oxide growth	Tool: Bruce furnace Tube: Tube 1 Recipe: 350	Grow oxide on all silicon wafers	Verify Oxide thickness is 650nm	All Si wafers
4b	TEOS Oxide (glass wafers only)	Tool: P5000 Chamber: A Thickness: 1 kÅ Time:			
5	Mo Sputter	Tool: CVC 601 Target: 2 - Molybdenum Ar Flow: 20sccm Pressure: ∼2.7mTorr Power: 1000W Thickness: 500 Presputter: 300 sec (use shutter) Dep. Time: 200 seconds	Want a base pressure of 1.5E-6 before sputtering Mo Change the platen according to wafer size, Include glass slide for thickness measurement and monitor wafers for etch test/stress etc	Load Time: _____ Dep Time:_____ Base Pressure:_____ Torr Ar Flow: _____ sccm Dep Pressure:_____ sccm Power:_____ W	All Wafers
6	Measure Mo thickness	Tool: Tencor P2 Recipe: Ger		Thickness:_____ Å	Slide

7	Measure Mo Rs	Tool: CDE Resmap Recipe: 6", Rs 61 points			Etch Test Wafer
8	Measure Bow	Tool: Tencor P2 Recipe: 6_INCH_STRESS	Take Vertical and Horizontal measurements SAVE, SCAN, and COPY them to Lot Folder on morbo. Save Files as L**D*H or L**D*V	File Names:_____ _____ _____ _____ _____	Si Wafers
9	Gate Litho	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake		All Wafers
10	Gate Exposure Level 1	Tool: GCA Lithography Tool: SVG Program 1 or SSI - Develop.rcp Mask: RingFET reticle # 5 Job: IGZO1.6IN Pass: P1 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Verify stepper is in INTEGRATE & 6" Mode		All Wafers
11	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers
12	Gate Etch	Tool: Al etch bench Chemistry: Al etchant Time: Until all moly is removed (about 30 seconds)	Check that etchant is room temperature before processing	Etch Times:	All Wafers
13	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers
14	Resist Strip	Tool: Wet Bench Solvent: PRS2000 Temp: 90C Time: 5 min (each bath)			All Wafers

15a	TEOS First gate dielectric, check the designed experiment, may need to do other dielectric than TEOS	Tool: P5000 Chamber: A Recipe: LS1000A Thickness: 1,000Å Time: ∼ 12 sec for 1 kÅ ∼ 5 sec for 500 Å	SMFL low stress 1kA TEOS recipe Use bare Si monitor wafers for deposition rate	Time: _____ sec Thickness: _____ Å
15b	LTO First gate dielectric, can be utilized in place of TEOS	Tool: LPCVD Thickness: 1000Å of LTO Upper Tube Recipe: 425 LTO Time: Check most recent runs (about 9min for 6", 7min for 4")	425 LTO Use bare Si wafer to monitor deposition rate	Time: _____ sec Thickness: _____ Å
15c	SiNx Check experiment for dielectric thickness	Tool: P5000 Thickness: 500 Å Recipe: B6-1M NIT CON Time: 6 sec	Use bare Si monitor wafers for deposition rate	Time: _____ sec Thickness: _____ Å
16a	Densify TEOS/LTO Skip this step if the dielectric doesn't need to be densified e.g. LTO, SiN etc	Tool: BruceTube 5 Temperature: 600C Time: 2 hours Ramp Down: Standard (not long) Recipe: 535		
16b	Reoxidize SiNx	Tool: BruceTube 5 Temperature: 600C Time: Variable check experiment Ramp Down: Standard (not long) Recipe: 588	Turn the torch controller ON (Power then manual) and wait till it heats up to 800 C before starting recipe	

17	6” wafers: Send to Corning for IGZO			IGZO thickness: _____ Å	All Wafers or SPC wafers
18	MESA Litho	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake		All Wafers
19	MESA Exposure Level 2	Tool: GCA Lithography Tool: SVG Program 1 or SSI - Develop.rcp Mask: RingFET reticle # 5 Job: IGZO1.6IN Pass: P4 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6” Mode		All Wafers
20	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.	Verify alignment	All Wafers
21	IGZO Etch	Wetbench Etchant: DI + HCl, 6:1 by volume, etch-rate increases with HCl proportion. Use IGZO monitor wafer for etch-time. Also look for visual endpoint Time: Depends on thickness Use ZnO dedicated petridishes This could be a very fast etch!!!	Typically 15-20 seconds	Etch Time:	All Wafers
22	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers

23	Resist Strip	Use acetone + IPA on wet chemical bench Use ZnO dedicated petridishes or Tool: Wet Bench Solvent: PRS2000 Temp: 90C Time: 5 min (each bath)	First strip off resist using acetone and then before rinsing in DI water, rinse with IPA. Dont do DI water rinse right after acetone		All Wafers
24	Gate, via open litho	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake		All Wafers
25	Gate, via open exposure (Level 3)	Tool: GCA Lithography Tool: SVG Program 1 or SSI - Develop.rcp Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P1 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		All Wafers
26	Inspection	Tool: Leica Microsope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers
27a	Oxide etch	Tool: MOS grade 10:1 BOE verify etch rate first	$\sim$ 2.5 min for 1 kÅ TEOS oxide	Etch Time:	All Wafers
27b	SiNx etch	Tool: MOS grade 10:1 BOE Time: 2.5 min Tool: LAM 490 Recipe: Standard nitride etch Time: _____ Å	Must remove surface oxide before dry etching nitride		
28	Inspection	Tool: Leica Microsope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers

29	Resist Strip	Use acetone + IPA on wet chemical bench Use ZnO dedicated petridishes or Tool: Wet Bench Solvent: PRS2000 Temp: 90C Time: 5 min (each bath)	First strip off resist using acetone and then before rinsing in DI water, rinse with IPA. Dont do DI water rinse right after acetone.	All Wafers
30	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.	All Wafers with active etched
31	S/D, gate pad lift-off lithography	Use SVG for HMDS prime ONLY SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm) 1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime	HMDS prime, LOR 5A, 150C bake, HPR 504, 100C bake	All Wafers
32	S/D, gate pad lift-off exposure (level 4)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P2 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode No post develop bake	All Wafers
33	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.	All SPC Wafers

34	S/D, gate pad metal deposition	Tool: CVC 601 Target: 2 - Molybdenum Ar Flow: 20sccm Pressure: 2.6mTorr Power: 1000W Thickness: 500 Presputter: 300 sec (use shutter) Dep. Time: 200 seconds Tool: CVC 601 Target: 1 Al/Si Ar Flow: 20 sccm Pressure: 5mTorr Power: 1000 W Thickness: 2500 Presputter: 300 sec (use shutter) Dep. Time: 300 seconds Or Tool: CHA Flash evaporator Thickness: 2.5 kÅ	Sputter thin Mo then sputter Al Wait 5 min between sputter targets to allow wafers to cool If evaporating Al use the 100% Al wire	All SPC wafers
35	Metal lift-off	Tool: Ultrasonic Bench Perform tape liftoff then use ZnO dedicated petridish PG Remover about 20min per wafer	Dont do tape liftoff on glass wafers	All SPC wafers
36	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.	All SPC Wafers
37a	Passivation lift-off lithography Only perform if passivation deposition method is photoresist compatible	Use SVG for HMDS prime ONLY SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm) 1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime	HMDS prime, LOR 5A, 150C bake, HPR 504, 100C bake	

37b	Passivation lift-off exposure (level 5) Only perform if passivation deposition method is photoresist compatible	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P4 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode No post develop bake	
38a	Passivation layer	LTO, TEOS, Sputtered SiOx, Al2O3, SiF4 oxide- depending on the experiment		Thickness:
38b	Passivation layer/ Topgate dielectric	BCB Coat: SCS coater recipe #2, 3000rpm for 45 sec, bake 140C until Blue oven is at 140C Cure: With wafers in Blue oven ramp up to 250C in Nitrogen, once at temp cure for 60min	Coat adhesion promoter before coating BCB Time at 140C is not that critical Make sure that the wafers are in the oven during ramp up	
39a	G/S/D contact lithography Only perform if passivation cant be lifted off (TEOS, BCB)	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake	

39b	G/S/D contact exposure (level 5) Only perform if passivation cant be lifted off (TEOS, BCB)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P3 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		
40a	Passivation Liftoff	Tool: Ultrasonic Bench Perform tape liftoff then use ZnO dedicated petridish PG Remover about 20min per wafer	Dont do tape liftoff on glass wafers		
40b	G/S/D contact etch	HF MOS grade 10:1 or PAD etch Find etch rate first from monitor wafers			All SPC wafers
40c	G/S/D BCB contact etch	Tool: Drytek Quad- 25sccm CF4, 100sccm O2, 300mT time: 5min (need to figure this out)			All SPC wafers
41	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers
42	IGZO anneal	Tool: Bruce Furnace	Check experiment		All SPC wafers
43	Final Testing				All Wafers

Appendix E: TG_{cop} Process Flow

#	Step	Process Parameters	Process Details	Record	Wafers
1	Create Lot Notebook	Obtain a cleanroom notebook, a previous notebook can be used Update and insert the file located in:	Tape into the notebook: Process Flow (this document) and lot split info Important Lot Processing Information Sheet		
2	Scribe	Tool: Diamond Tips Scrib Scribe monitor wafers with the lot number and M1, M3, M4. (these can be found in the monitor wafer box) Print out wafer box label and tape it on 6" or 4" polypropylene box	Also make sure all wafers are scribed correctly.		All Wafers
3	RCA Clean	Tool: RCA Bench			All Wafers
4a	Thick oxide growth	Tool: Bruce furnace Tube: Tube 1 Recipe: 350	Grow oxide on all silicon wafers	Verify Oxide thickness is 650nm	All Si wafers
4b	TEOS Oxide (glass wafers only)	Tool: P5000 Chamber: A Thickness: 1 kÅ Time:			
5	6" wafers: Send to Corning for IGZO			IGZO thickness: _____ Å	All Wafers or SPC wafers
6	MESA Litho	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake		All Wafers

7	MESA Exposure Level 1	Tool: GCA Lithography Tool: SVG Program 1 or SSI - Develop.rcp Mask: RingFET reticle # 5 Job: IGZO1.6IN Pass: P4 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		All Wafers
8	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.	Verify alignment	All Wafers
9	IGZO Etch	Wetbench Etchant: DI + HCl, 6:1 by volume, etch-rate increases with HCl proportion. Use IGZO monitor wafer for etch-time. Also look for visual endpoint Time: Depends on thickness Use ZnO dedicated petridishes This could be a very fast etch!!!	Typically 15-20 seconds	Etch Time:	All Wafers
10	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers
11	Resist Strip	Use acetone + IPA on wet chemical bench Use ZnO dedicated petridishes or Tool: Wet Bench Solvent: PRS2000 Temp: 90C Time: 5 min (each bath)	First strip off resist using acetone and then before rinsing in DI water, rinse with IPA. Dont do DI water rinse right after acetone		All Wafers

12	S/D lift-off lithography	Use SVG for HMDS prime ONLY SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm) 1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime	HMDS prime, LOR 5A, 150C bake, HPR 504, 100C bake	All Wafers
13	S/D lift-off exposure (level 2)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P2 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode No post develop bake	All Wafers
14	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.	All SPC Wafers
15	S/D metal deposition	Tool: CVC 601 Target: 2 - Molybdenum Ar Flow: 20sccm Pressure: 2.6mTorr Power: 1000W Thickness: 500 Presputter: 300 sec (use shutter) Dep. Time: 200 seconds Tool: CVC 601 Target: 1 Al/Si Ar Flow: 20 sccm Pressure: 5mTorr Power: 1000 W Thickness: 2500 Presputter: 300 sec (use shutter) Dep. Time: 300 seconds Or Tool: CHA Flash evaporator Thickness: 2.5 kÅ	Sputter thin Mo then sputter Al Wait 5 min between sputter targets to allow wafers to cool If evaporating Al use the 100% Al wire	All SPC wafers

16	Metal lift-off	Tool: Ultrasonic Bench Perform tape liftoff then use ZnO dedicated petridish PG Remover about 20min per wafer	Dont do tape liftoff on glass wafers		All SPC wafers
17	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers
18	Top-gate dielectric	LTO, TEOS - depending on the experiment		Thickness:	
19	IGZO anneal	Tool: Bruce Furnace	Check experiment		All SPC wafers
20	S/D contact exposure (level 3)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 7 Job: IGZO1.6IN Pass: P3/P4 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		
21	S/D contact etch	HF MOS grade 10:1 or PAD etch Find etch rate first from monitor wafers			All SPC wafers
22	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers

23	Top-gate, S/D contact lift-off lithography	Use SVG for HMDS prime ONLY SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm) 1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime	HMDS prime, LOR 5A, 150C bake, HPR 504, 100C bake		All Wafers
24	Top-gate, S/D contact exposure (level 4)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P3 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		
25	Metal deposition	Tool: CHA Flash Evaporator Thickness: 2500 Å		Base Pressure:_____ Torr, Thickness :_____ Å	All Wafers
26	Metal lift-off	Tool: Ultrasonic Bench Perform tape liftoff then use ZnO dedicated petridish PG Remover about 20min per wafer	Dont do tape liftoff on glass wafers		All SPC wafers
27	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers
28	Final Testing				All Wafers

Appendix F: TG_{stg} Process Flow

#	Step	Process Parameters	Process Details	Record	Wafers
1	Create Lot Notebook	Obtain a cleanroom notebook, a previous notebook can be used Update and insert the file located in:	Tape into the notebook: Process Flow (this document) and lot split info Important Lot Processing Information Sheet		
2	Scribe	Tool: Diamond Tips Scrib Scribe monitor wafers with the lot number and M1, M3, M4. (these can be found in the monitor wafer box) Print out wafer box label and tape it on 6" or 4" polypropylene box	Also make sure all wafers are scribed correctly.		All Wafers
3	RCA Clean	Tool: RCA Bench			All Wafers
4a	Thick oxide growth	Tool: Bruce furnace Tube: Tube 1 Recipe: 350	Grow oxide on all silicon wafers	Verify Oxide thickness is 650nm	All Si wafers
4b	TEOS Oxide (glass wafers only)	Tool: P5000 Chamber: A Thickness: 1 kÅ Time:			
5	Densify TEOS/LTO Skip this step if the dielectric doesn't need to be densified e.g. LTO, SiN etc	Tool: BruceTube 5 Temperature: 600C Time: 2 hours Ramp Down: Standard (not long) Recipe: 535			

6	S/D lift-off lithography	Use SVG for HMDS prime ONLY SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm) 1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime	HMDS prime, LOR 5A, 150C bake, HPR 504, 100C bake	All Wafers
7	S/D, gate pad lift-off exposure (level 1)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 7 Job: IGZO1.6IN Pass: P1 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode No post develop bake	All Wafers
8	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.	All SPC Wafers
9	S/D, gate pad metal deposition	Tool: CVC 601 Target: 3 - Titanium Ar Flow: 20sccm Pressure: 6mTorr Power: 1000W Thickness: 500 Presputter: 300 sec (use shutter) Dep. Time: 300 seconds Tool: CVC 601 Target: 3 Titanium Ar Flow: 20 sccm Pressure: 4.8 mTorr N_2 Flow: 25 sccm Pressure: 1.2 mTorr Power: 500 W Thickness: 200 Presputter: 300 sec (use shutter) Dep. Time: 385 seconds	Sputter Ti then reactive sputter TiN	All SPC wafers

10	Metal lift-off	Tool: Ultrasonic Bench NO tape liftoff then use ZnO dedicated petridish PG Remover about 20min per wafer	Dont do tape liftoff on glass wafers		All SPC wafers
11	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers
12	6" wafers: Send to Corning for IGZO			IGZO thickness: _____ Å	All Wafers or SPC wafers
13	MESA Litho	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake		All Wafers
14	MESA Exposure (Level 2)	Tool: GCA Lithography Tool: SVG Program 1 or SSI - Develop.rcp Mask: RingFET reticle # 5 Job: IGZO1.6IN Pass: P4 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		All Wafers
15	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.	Verify alignment	All Wafers

16	IGZO Etch	Wetbench Etchant: DI + HCl, 6:1 by volume, etch-rate increases with HCl proportion. Use IGZO monitor wafer for etch-time. Also look for visual end-point Time: Depends on thickness Use ZnO dedicated petridishes	Typically 15-20 seconds	Etch Time:	All Wafers
17	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers
18	Resist Strip	Use acetone + IPA on wet chemical bench Use ZnO dedicated petridishes or Tool: Wet Bench Solvent: PRS2000 Temp: 90C Time: 5 min (each bath)	First strip off resist using acetone and then before rinsing in DI water, rinse with IPA. Dont do DI water rinse right after acetone		All Wafers
19	Top-gate dielectric	LTO, TEOS - depending on the experiment		Thickness:	
20	IGZO anneal	Tool: Bruce Furnace	Check experiment		All SPC wafers
21	S/D contact exposure (level 3)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 7 Job: IGZO1.6IN Pass: P3/P4 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		

22	S/D contact etch	HF MOS grade 10:1 or PAD etch Find etch rate first from monitor wafers			All SPC wafers
23	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers
24	Top-gate, S/D contact lift-off lithography	Use SVG for HMDS prime ONLY SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm) 1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime	HMDS prime, LOR 5A, 150C bake, HPR 504, 100C bake		All Wafers
25	Top-gate, S/D contact exposure (level 4)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P3 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		
26	Metal deposition	Tool: CHA Flash Evaporator Thickness: 2500 Å		Base Pressure:_____ Torr, Thickness :_____ Å	All Wafers
27	Metal lift-off	Tool: Ultrasonic Bench Perform tape liftoff then use ZnO dedicated petridish PG Remover about 20min per wafer	Dont do tape liftoff on glass wafers		All SPC wafers
28	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers
29	Final Testing				All Wafers

Appendix G: DG Process Flow

#	Step	Process Parameters	Process Details	Record	Wafers
1	Create Lot Notebook	Obtain a cleanroom notebook, a previous notebook can be used Update and insert the file located in:	Tape into the notebook: Process Flow (this document) and lot split info Important Lot Processing Information Sheet		
2	Scribe	Tool: Diamond Tips Scrib Scribe monitor wafers with the lot number and M1, M3, M4. (these can be found in the monitor wafer box) Print out wafer box label and tape it on 6" or 4" polypropylene box	Also make sure all wafers are scribed correctly.		All Wafers
3	RCA Clean	Tool: RCA Bench			All Wafers
4a	Thick oxide growth	Tool: Bruce furnace Tube: Tube 1 Recipe: 350	Grow oxide on all silicon wafers	Verify Oxide thickness is 650nm	All Si wafers
4b	TEOS Oxide (glass wafers only)	Tool: P5000 Chamber: A Thickness: 1 kÅ Time:			
5	Mo Sputter	Tool: CVC 601 Target: 2 - Molybdenum Ar Flow: 20sccm Pressure: ∼2.7mTorr Power: 1000W Thickness: 500 Presputter: 300 sec (use shutter) Dep. Time: 200 seconds	Want a base pressure of 1.5E-6 before sputtering Mo Change the platen according to wafer size, Include glass slide for thickness measurement and monitor wafers for etch test/stress etc	Load Time: _____ Dep Time:_____ Base Pressure:_____ Torr Ar Flow: _____ sccm Dep Pressure:_____ sccm Power:_____ W	All Wafers
6	Measure Mo thickness	Tool: Tencor P2 Recipe: Ger		Thickness:_____ Å	Slide

7	Measure Mo Rs	Tool: CDE Resmap Recipe: 6", Rs 61 points			Etch Test Wafer
8	Measure Bow	Tool: Tencor P2 Recipe: 6_INCH_STRESS	Take Vertical and Horizontal measurements SAVE, SCAN, and COPY them to Lot Folder on morbo. Save Files as L**D*H or L**D*V	File Names:_____ _____ _____ _____ _____	Si Wafers
9	Gate Litho	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake		All Wafers
10	Gate Exposure Level 1	Tool: GCA Lithography Tool: SVG Program 1 or SSI - Develop.rcp Mask: RingFET reticle # 5 Job: IGZO1.6IN Pass: P1 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Verify stepper is in INTEGRATE & 6" Mode		All Wafers
11	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers
12	Gate Etch	Tool: Al etch bench Chemistry: Al etchant Time: Until all moly is removed (about 30 seconds)	Check that etchant is room temperature before processing	Etch Times:	All Wafers
13	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers
14	Resist Strip	Tool: Wet Bench Solvent: PRS2000 Temp: 90C Time: 5 min (each bath)			All Wafers

15a	TEOS First gate dielectric, check the designed experiment, may need to do other dielectric than TEOS	Tool: P5000 Chamber: A Recipe: LS1000A Thickness: 1,000Å Time: ∼ 12 sec for 1 kÅ ∼ 5 sec for 500 Å	SMFL low stress 1kA TEOS recipe Use bare Si monitor wafers for deposition rate	Time: _____ sec Thickness: _____ Å
15b	LTO First gate dielectric, can be utilized in place of TEOS	Tool: LPCVD Thickness: 1000Å of LTO Upper Tube Recipe: 425 LTO Time: Check most recent runs (about 9min for 6", 7min for 4")	425 LTO Use bare Si wafer to monitor deposition rate	Time: _____ sec Thickness: _____ Å
15c	SiNx Check experiment for dielectric thickness	Tool: P5000 Thickness: 500 Å Recipe: B6-1M NIT CON Time: 6 sec	Use bare Si monitor wafers for deposition rate	Time: _____ sec Thickness: _____ Å
16a	Densify TEOS/LTO Skip this step if the dielectric doesn't need to be densified e.g. LTO, SiN etc	Tool: BruceTube 5 Temperature: 600C Time: 2 hours Ramp Down: Standard (not long) Recipe: 535		
16b	Reoxidize SiNx	Tool: BruceTube 5 Temperature: 600C Time: Variable check experiment Ramp Down: Standard (not long) Recipe: 588	Turn the torch controller ON (Power then manual) and wait till it heats up to 800 C before starting recipe	

17	6” wafers: Send to Corning for IGZO			IGZO thickness: _____ Å	All Wafers or SPC wafers
18	MESA Litho	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake		All Wafers
19	MESA Exposure Level 2	Tool: GCA Lithography Tool: SVG Program 1 or SSI - Develop.rcp Mask: RingFET reticle # 5 Job: IGZO1.6IN Pass: P4 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6” Mode		All Wafers
20	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.	Verify alignment	All Wafers
21	IGZO Etch	Wetbench Etchant: DI + HCl, 6:1 by volume, etch-rate increases with HCl proportion. Use IGZO monitor wafer for etch-time. Also look for visual endpoint Time: Depends on thickness Use ZnO dedicated petridishes This could be a very fast etch!!!	Typically 15-20 seconds	Etch Time:	All Wafers
22	Inspection	Tool: Leica Microscope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers

23	Resist Strip	Use acetone + IPA on wet chemical bench Use ZnO dedicated petridishes or Tool: Wet Bench Solvent: PRS2000 Temp: 90C Time: 5 min (each bath)	First strip off resist using acetone and then before rinsing in DI water, rinse with IPA. Dont do DI water rinse right after acetone		All Wafers
24	Gate, via open litho	SVG (program 1) or manual dispense SSI (nodispense recipe)	HMDS prime, 140C bake, HPR 504, 100C bake		All Wafers
25	Gate, via open exposure (Level 3)	Tool: GCA Lithography Tool: SVG Program 1 or SSI - Develop.rcp Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P1 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		All Wafers
26	Inspection	Tool: Leica Microsope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers
27a	Oxide etch	Tool: MOS grade 10:1 BOE verify etch rate first	$\sim$ 2.5 min for 1 kÅ TEOS oxide	Etch Time:	All Wafers
27b	SiNx etch	Tool: MOS grade 10:1 BOE Time: 2.5 min Tool: LAM 490 Recipe: Standard nitride etch Time: _____ Å	Must remove surface oxide before dry etching nitride		
28	Inspection	Tool: Leica Microsope	Take Pictures of devices on all wafers and transfer to morbo.		All Wafers

29	Resist Strip	Use acetone + IPA on wet chemical bench Use ZnO dedicated petridishes or Tool: Wet Bench Solvent: PRS2000 Temp: 90C Time: 5 min (each bath)	First strip off resist using acetone and then before rinsing in DI water, rinse with IPA. Dont do DI water rinse right after acetone.	All Wafers
30	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.	All Wafers with active etched
31	S/D, gate pad lift-off lithography	Use SVG for HMDS prime ONLY SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm) 1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime	HMDS prime, LOR 5A, 150C bake, HPR 504, 100C bake	All Wafers
32	S/D, gate pad lift-off exposure (level 4)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P2 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode No post develop bake	All Wafers
33	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.	All SPC Wafers

34	S/D, gate pad metal deposition	Tool: CVC 601 Target: 2 - Molybdenum Ar Flow: 20sccm Pressure: 2.6mTorr Power: 1000W Thickness: 500 Presputter: 300 sec (use shutter) Dep. Time: 200 seconds Tool: CVC 601 Target: 1 Al/Si Ar Flow: 20 sccm Pressure: 5mTorr Power: 1000 W Thickness: 2500 Presputter: 300 sec (use shutter) Dep. Time: 300 seconds Or Tool: CHA Flash evaporator Thickness: 2.5 kÅ	Sputter thin Mo then sputter Al Wait 5 min between sputter targets to allow wafers to cool If evaporating Al use the 100% Al wire		All SPC wafers
35	Metal lift-off	Tool: Ultrasonic Bench Perform tape liftoff then use ZnO dedicated petridish PG Remover about 20min per wafer	Dont do tape liftoff on glass wafers		All SPC wafers
36	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers
37	Passivation layer/ Topgate dielectric	LTO, TEOS, Sputtered SiOx, Al2O3, SiF4 oxide- depending on the experiment		Thickness:	

38	G/S/D contact exposure (level 5)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 7 Job: IGZO1.6IN Pass: P3/P4 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		
39	G/S/D contact etch	HF MOS grade 10:1 or PAD etch Find etch rate first from monitor wafers			All SPC wafers
40	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.		All SPC Wafers
41	Top-gate gate pad liftoff lithography	Use SVG for HMDS prime ONLY SCS spinner for LOR coat (LOR 5A 35sec @ 2k rpm) 1 min 150C hot-plate bake Coat HPR 504 on SVG track. No HMDS prime	HMDS prime, LOR 5A, 150C bake, HPR 504, 100C bake		All Wafers
42	Top-gate liftoff exposure (level 6)	Tool: GCA Lithography Tool: SVG Program 1 or SSI Mask: RingFET reticle # 8 Job: IGZO1.6IN Pass: P3 Time: 2.8 sec (integrate mode) Focus: 0 Alignment Marks: N	Adjust alignment as necessary Verify stepper is in INTEGRATE & 6" Mode		
43	Metal deposition	Tool: CHA Flash Evaporator Thickness: 2500 Å	Base Pressure:_____ Torr, Thickness:_____ Å	All Wafers	

44	Metal lift-off	Tool: Ultrasonic Bench Perform tape liftoff then use ZnO dedicated petridish PG Remover about 20min per wafer	Dont do tape liftoff on glass wafers	All SPC wafers
45	Inspection	Tool: Leica Microsope	Take Pictures of devices on all SPC wafers and transfer to morbo.	All SPC Wafers
46	Final Testing			All Wafers