CMOS PLA LAYOUT GENERATION

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ABSTRACT

A dynamic AND - dynamic OR type of PLA was designed using a CMOS process and the layout was done on a CALMA system using 1.5um design rules. A PLA with 200 transistors was completed and can be used to perform desired logic functions.

INTRODUCTION

Programmable Logic Arrays have been used for many years as a means of customizing logic design. PLA's, as they are known, provide a flexible and efficient way of synthesizing arbitrary combinational functions in a regular structure. The circuit is based on a representation of Boolean functions as a set of sum-of-products terms. The AND plane produces the distinct product terms in the expressions; the OR plane collects these terms to produce the desired outputs. PLA's can be fabricated in either bipolar, using ECL gates or CMOS using both P and N type gates. For certain types of logic networks, large CMOS arrays can achieve overall system speeds that compare favorably with ECL devices, yet don't have the problems associated with those devices. CMOS arrays are achieving a great deal of attention due to their short path delays that are possible with high circuit density (1).

There are three distinct types of PLA's that can be implemented and used for different designs, depending on the size of the PLA, the desired speed, and the timing sequence. They are the dynamic-dynamic, the dynamic-static, and the static-dynamic. The two terms are descriptive of the two separate planes, AND-OR, that provide the logic AND function or the logic OR function. Dynamic means that the plane is always performing some type of function while static means it performs a function only on specified clock pulses.

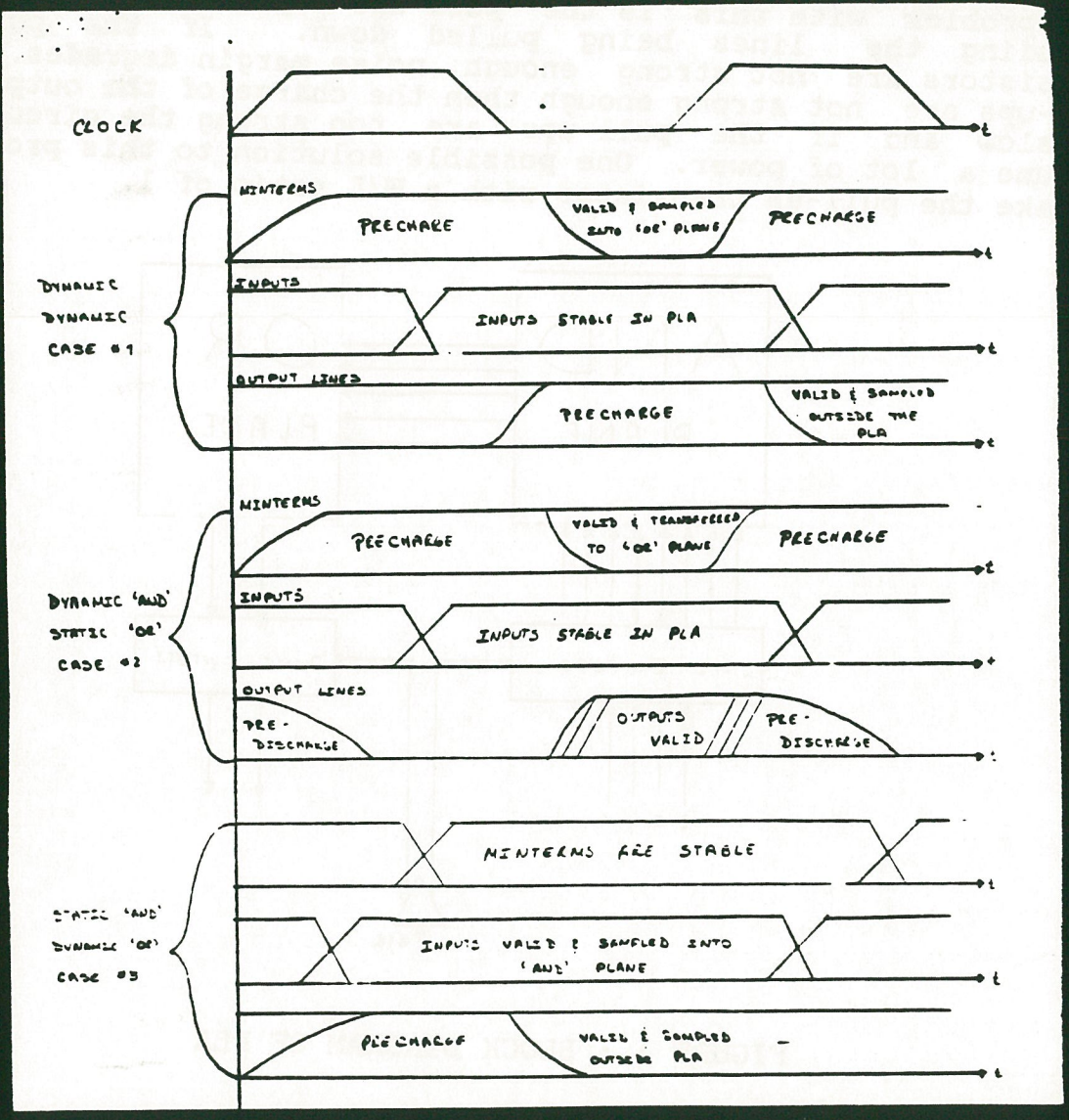
Figure 1 shows the block diagram for a typical PLA. The chart on the next page shows some typical uses, timing, sizes and current consumption comparison of the three types of PLA's. The timing diagrams are shown in Figure 2 (2). As can be seen the uses of the PLA would be according to the design specifications for the outputs being valid or the inputs being stable.

The main concept of a static plane is that the inputs/outputs are sampled while the pull-up transistors are

Comparison Description	Dynamic 'AND' Dynamic 'OR'	Dynamic 'AND' STATIC 'OR'	Static 'AND' Dynamic 'OR'
USES	Sample inputs at one clock phase produce outputs in same phase after clock cycle	Sample input @ one clock phase, produce outputs in the following phase	Sample input @ one clock phase, produce outputs in the following phase
WHEN PLANES ARE OPERATING	'AND' plane works on one phase, 'OR' on the other phase.	Both planes are working at the evaluation phase.	During 1st. phase, where inputs sampled, minterms must be valid, 2nd. phase only 'OR' operating
Size of PLA.	Many minterms, inputs and outputs	Limits max. number of minterms, inputs, outputs	Many minterms & demands inputs valid early during sampling phase.
Current Consumption	Low, due to no static plane	High due to static operation of 'OR'	High due to static operation of 'AND'
Buffers b/t Planes	Clocked buffers, sampling	NONE	Two Inverters
Output Buffers	Same as b/t planes	Clocked CMOS structure	same as D.D.
Stretching of 'OR' plane.	Increase length of outputs (metal line)	Increase width of source diffusion	Identical to D.S
Placement of precharge for Dynamic plane.	Between planes with input buffers to 'OR'	OUTSIDE of 'OR' plane	Lower side of 'OR'

TABLE I : COMPARISON OF THREE PLA's

FIGURE 2 : TIMING DIAGRAM OF THREE PLA'S



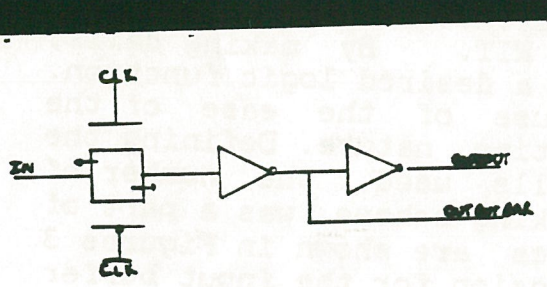


FIGURE 3 : INPUT BUFFER EXPLOSION

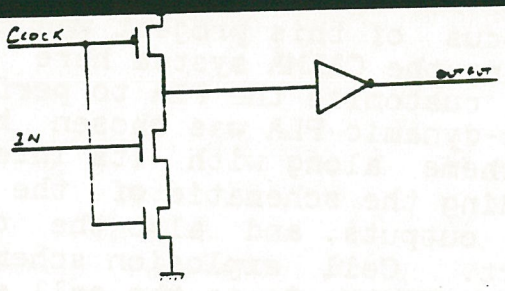


FIGURE 4 : OUTPUT BUFFER EXPLOSION

disconnected. This means that every line that is a logic "1" discharges and every line that is a logic "0" is floating. The main problem with this is the pull-ups try to charge all lines, including the lines being pulled down. If the pull-down transistors are not strong enough, noise margin degrades. If the pull-ups are not strong enough then the charge of the output line is slow and if the pull-ups are too strong the circuit will consume a lot of power. One possible solution to this problem is to make the pull-up transistor with a W/L ratio of 1.

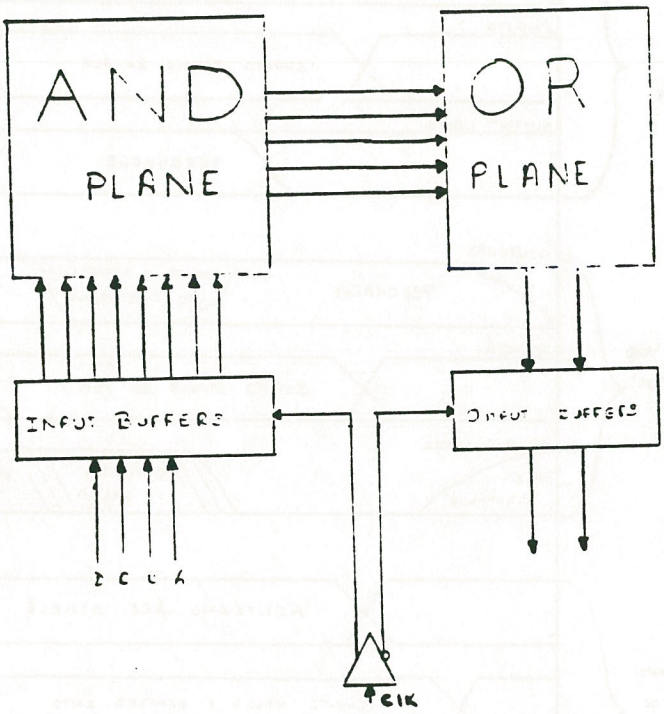


FIGURE 1 : BLOCK DIAGRAM OF PLA

The focus of this project was on layout of the cells for the PLA utilizing the CALMA system here at RIT. By making cells, others can customize the PLA to perform a desired logic function. The dynamic-dynamic PLA was chosen because of the ease of the clocking scheme along with its interesting nature. Defining the PLA, including the schematic of the cells used, the number of inputs and outputs, and also the clocking scheme was a part of this project. Cell explosion schematics are shown in Figures 3 and 4 (3). Figure 3 is the cell explosion for the input buffer and Figure 4 is the output buffer.

The PLA designed was for a CMOS double-metal process using the refractory-polysilicon techniques. The refractory-poly process uses metal placed on top of the polysilicon to reduce the resistance. This also insures that the double-metal process is

used. The double-level metal was used because of its low power consumption and short path delays.

The first step in the design process is developing the device at the schematic level. The majority of schematic capture tools available today require a designer to start with at least a behavioral description of the circuit. The PLA description for this design was arbitrary and was for demonstration purposes only. This is true because the purpose of this project was to create the standard cells necessary to help others redesign the PLA for a specific function. Assuming the device to be fully custom, the next step is to layout the physical geometries for each masking level associated with the transistors in the schematic. Here is where the CMOS, double level metal, polysilicon gate process was chosen.

DESIGN

PLA's are essentially uncommitted logic gates where the user determines the final logic configuration of the device. The basic programmable array is the AND-OR logic in the familiar sum-of-products (SOP) representation. A conventional schematic representation is shown in Figure 5. Its programmable logic equivalent is shown in Figure 6 (4).

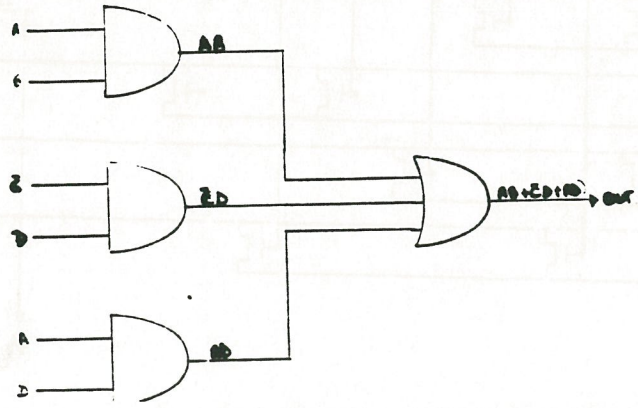


FIGURE 5 : PLA SCHEMATIC REPRESENTATION

One reason for using the SOP expressions is their straightforward conversion to very simple logic gates. In their purest and simplest form they go into two level networks which are networks for which the longest path through which a signal must pass is two gates long (5).

Today programmable logic typically implements from 4 to 20 SSI and MSI logic devices. This allows a reduction of size for a system as well as an increase in logic power. Also with the use of programmable logic, the designer is not limited to standard off the shelf parts and, therefore, can use non-standard structures. Another reason for its use is that designers can compress multiple levels of logic into a two level AND-OR structure, thus simplifying the design and in many cases obtaining speed and/or power advantages (6).

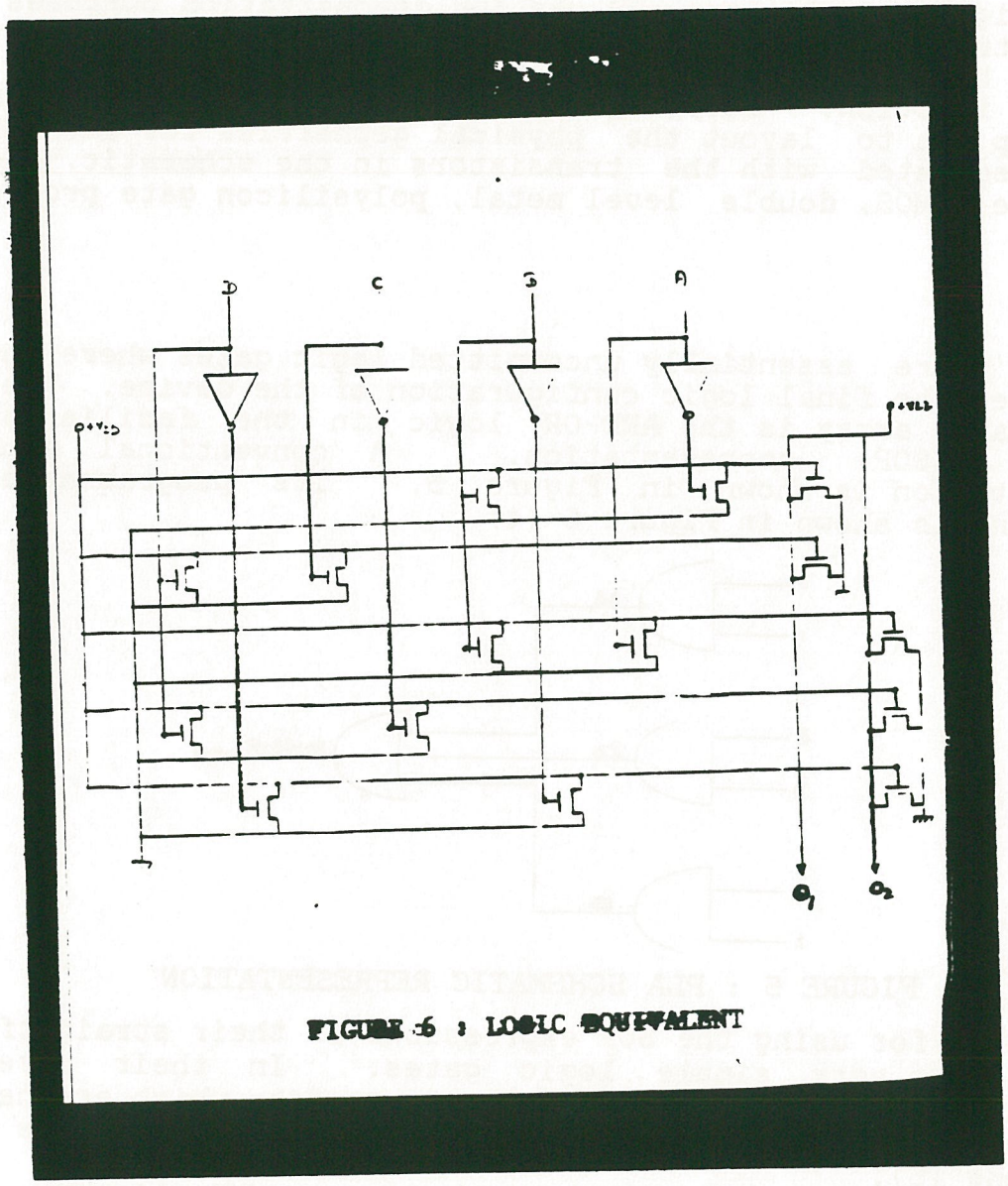


FIGURE 6 : LOGIC EQUIVALENT

The PLA for this project, was designed for the CMOS double level metal process. The design rules used are for the 1.5um polysilicon lines, and the masking steps for the process are listed below in Table II. A cross section of the process can be seen in Figure 7 (7). The reason for using double level metal is because if the PLA gets very large, to cut down on the resistance of the poly gates, metal two can be tapped into the poly and it is like having two resistors in parallel.

Table II Masking Steps for Double Level Cmos

(1) N-well
(2) Field Oxide
(3) N-well protection
(4) Polysilicon
(5) N+ regions
(6) P+ regions
(7) Contact cuts
(8) Metal One
(9) Via Cuts
(10) Metal Two

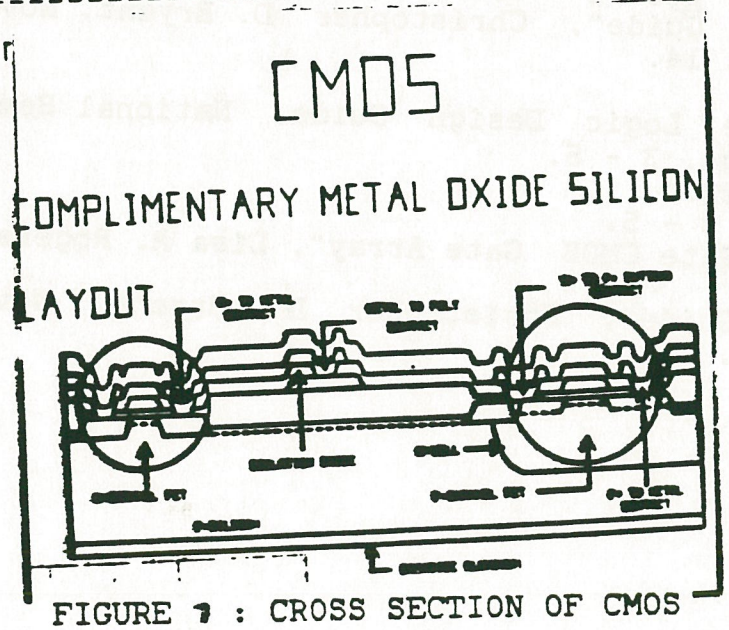


FIGURE 7 : CROSS SECTION OF CMOS

RESULTS

The schematics, shown in Figures 5 and 6, were drawn by hand since logic simulation had been done already in November 1987 while on co-op at National Semiconductor in Santa Clara, the program used for simulation was SPLA (8). The reason for simulation was part of the work that was being done in studying PLA's in general. The next step in the design was layout. This was done on the CALMA system in the CAD/CAM lab in the microelectronics building at RIT. The library name used for this project and where the cells can be found is called CMOSCDB.

All cells have been drawn, schematics have been constructed and connections to form the PLA has been completed. The PLA is drawn such that it is rectangular. The pad arrangement has not been set because of the way the PLA can be rotated to provide extra space. The number of transistors is approximately 200.

CONCLUSIONS

A dynamic - dynamic PLA has been done and the layout is completed. It can now be programed to do any logic function that is desired. The cells used can be modified to provide the best implementation for that desired function.

REFERENCES

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