DESIGN OF A FOUR-BIT MICROPROCESSOR A.L.U. USING PMOS 10-um METAL GATE TECHNOLOGY

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ABSTRACT

A four-bit ALU chip based on a metal gate PMOS process and 10-um minimum geometries was designed. The operations performed by the ALU included ADD w/carry, SUBTRACT(2's complement),INCREMENT,DECREMENT,and the logic functions AND, OR, XOR, and COMPLEMENT. Due to space limitations no data or shift registers were included on the chip. PMOS NOR gates and inverters were used in the hardware implementation of the logic design. The ALU chip was laid out by using the ICE (Integrated Circuit Editor) design tool.

INTRODUCTION

The Arithmetic and Logic Unit (ALU) of a microprocessor consists of a combinational digital system that can perform basic mathematical and logical functions in parallel on each corresponding bit of data taken from an accumulator register and one other register, with the result fed back to the accumulator.This project consisted of the design of a 4-bit ALU chip using the existing RIT PMOS process, with 10-um design rules and four masking levels (p-type diffusion, oxide, contact cuts, and metal gate). The Integrated Circuit Editor (ICE) was used to lay out the chip design. The chip size used was 5000um X 5000um. The hardware implementation of the ALU consisted of only PMOS NOR gates and inverters, with their combinations acting as universal logic gates representing the OR, AND, XOR, and COMPLEMENT functions of the logic design of the system. The ideal length to width ratios for the NOR gates and inverters were determined based on the SPICE analyses of Jim Taylor of RIT, who designed an RIT PMOS standard cell library[1].

Due to space limitations no data or shift registers were included in the chip design. This ALU was a strictly combinational circuit, with no clock signal used. All the data and previously decoded operation instructions must be input to the ALU pads. The connections to the outside world are power and ground, four data lines each for the two inputs, four lines for the resulting output, Cin and Cout (carry-in and carry-out) pads, and three 'select' lines carrying the specific instruction to be performed by the ALU. The Arithmetic and Logic Unit's functions include ADD, ADD w/carry, SUBTRACT (2's complement), INCREMENT, DECREMENT, and logic functions AND, OR, XOR, and COMPLEMENT. Major functional blocks included in the design were full adders, 2-1 and 4-1 line multiplexers, and a combinational circuit that expanded the capabilities of a full adder to include SUBTRACT, INCREMENT, and DECREMENT operations.

Figure 1 shows the pinout of the ALU designed in this project. It has four lines each for the data input by the accumulator (A) and one other register (B), and four lines for the output (F). The Cin line and the SELECT lines combine to specify the instruction set shown in Table 1. Line S2 is the 'mode select' that differentiates between the logic block and the arithmetic block of the circuit by using a 2-1 multiplexer for each bit in the circuit.

FIGURE 1: PINOUT OF THE ALU

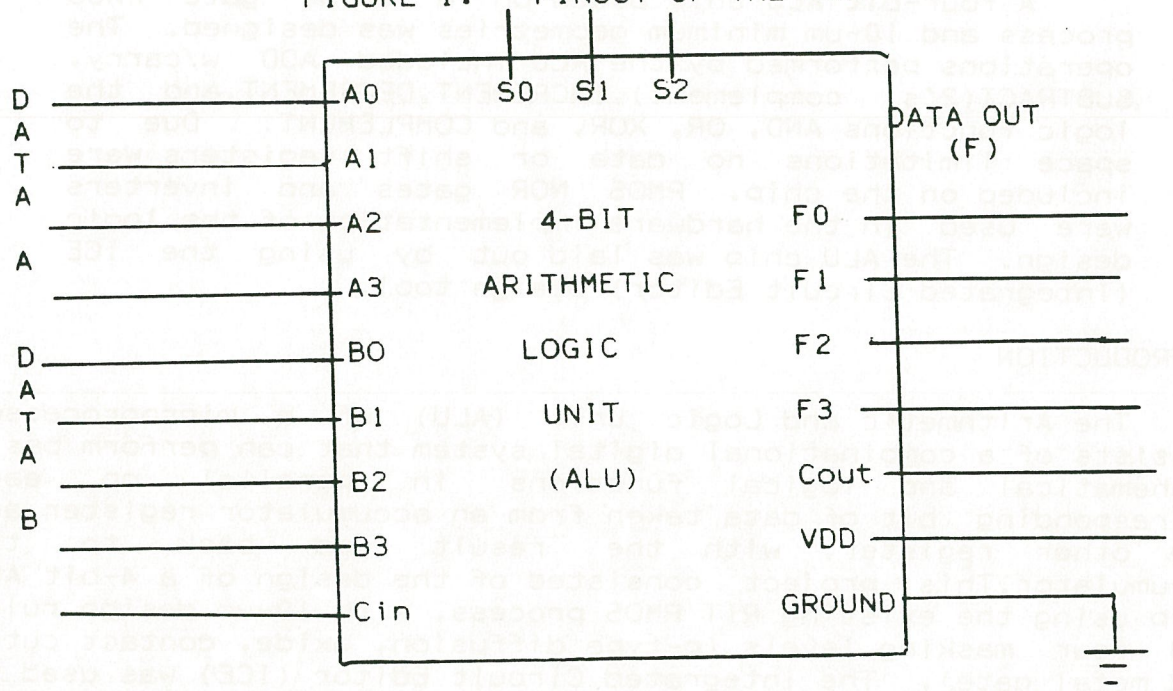
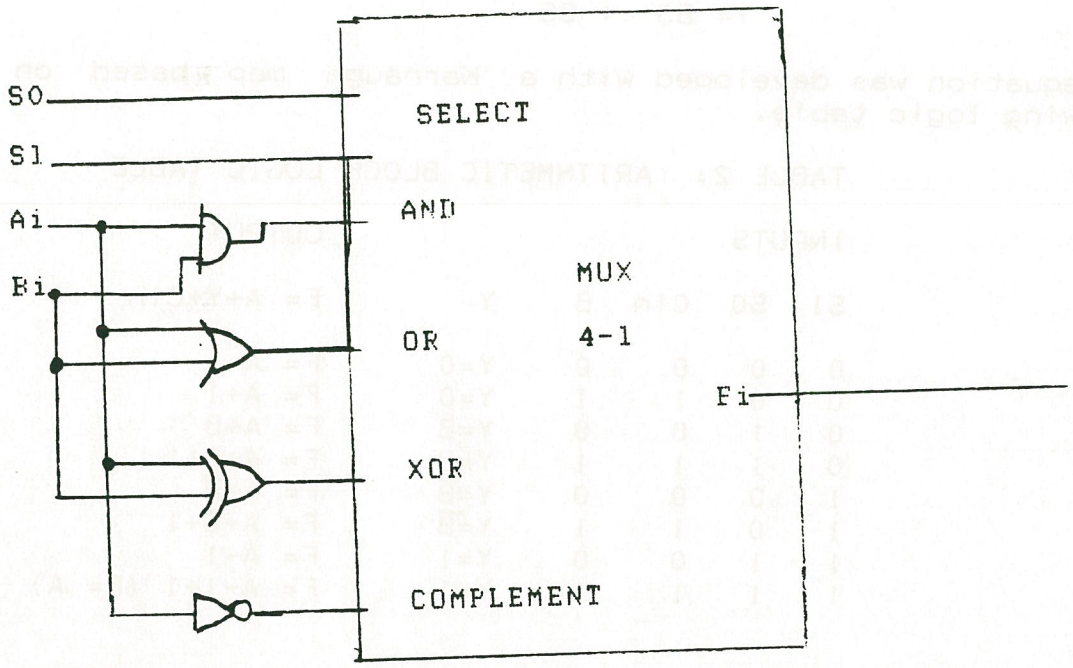


TABLE 1: INSTRUCTION SET

OPERATION SELECT				OPERATION	FUNCTION
S2	S1	S0	Cin		
0	0	0	0	F= A	TRANSFER A
0	0	0	1	F= A+1	INCREMENT
0	0	1	0	F= A+B	ADD
0	0	1	1	F= A+B+1	ADD w/carry
0	1	0	0	F= A+$\overline{B}$	
0	1	0	1	F= A-B	SUBTRACT
0	1	1	0	F= A-1	DECREMENT
0	1	1	1	F= A	TRANSFER A
1	0	0	0	F= A$\wedge$B	AND
1	0	1	0	F= A$\vee$B	OR
1	1	0	0	F= A$\oplus$B	EXCLUSIVE OR
1	1	1	0	F= $\overline{A}$	COMPLEMENT

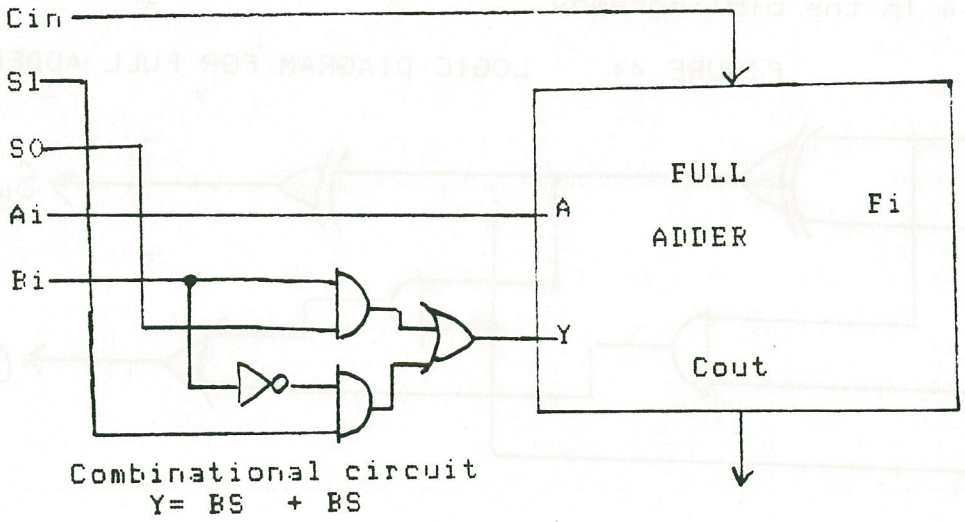
One of the four bits of the logic block is shown in Figure 2. The four logic functions are performed in parallel. Next the desired operation is selected by the 4-1 line multiplexer according to the S0 and S1 instructions as was shown in Table 1.

FIGURE 2: LOGIC BLOCK (ONE BIT)



One bit of the arithmetic block is shown in Figure 3. As with the logic block, the other three bits are identical. With the full adder, the Cout of one bit becomes the Cin of the next higher order bit. The full adder is used for parallel addition with carry. The combinational circuit placed in front of the full adder was designed to expand the full adder's capabilities to include the INCREMENT,DECREMENT, and SUBTRACT operations.

FIGURE 3: ARITHMETIC BLOCK



As shown in Figure 3, the inputs to the arithmetic block are Ai and Bi. The accumulator input (Ai) gets fed straight to the full adder. The Bi input gets manipulated prior to its entry to the full adder by the combinational circuit according to the logic table in Table 2. Conversion from B into Y follows the logic equation

$$Y = BS + B\overline{S}$$

This equation was developed with a Karnaugh map based on the following logic table.

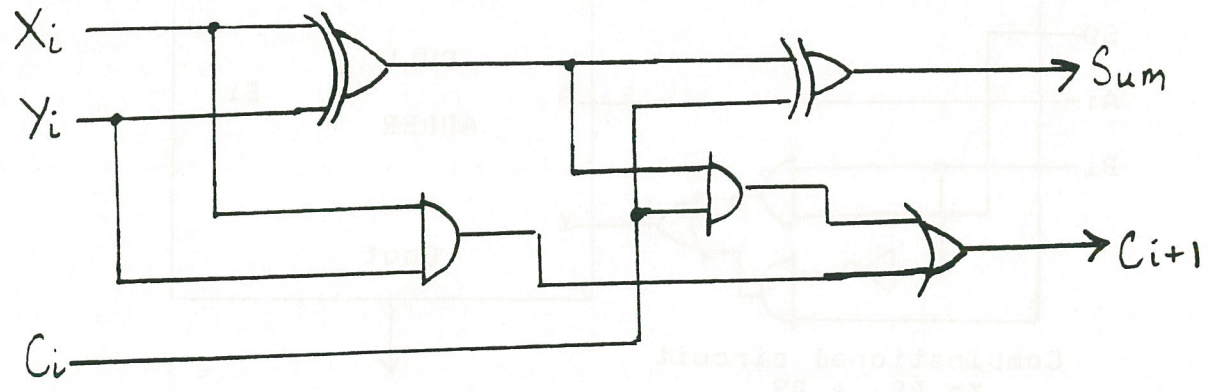
TABLE 2: ARITHMETIC BLOCK LOGIC TABLE

INPUTS					OUTPUT
S1	S0	Cin	B	Y	F= A+Y+Cin
0	0	0	0	Y=0	F= A
0	0	1	1	Y=0	F= A+1
0	1	0	0	Y=B	F= A+B
0	1	1	1	Y=B	F= A+B+1
1	0	0	0	$Y=\overline{B}$	F= A+$\overline{B}$
1	0	1	1	$Y=\overline{B}$	F= A+$\overline{B}$+1
1	1	0	0	Y=1	F= A-1
1	1	1	1	Y=1	F= A-1+1 (F= A)

If Y=0, the output is either F=A or F=A+1, depending on the set value of Cin. If the combinational circuit leaves B unchanged, the regular full adder operation of ADD or ADD w/carry is the output. If Y becomes the complement of B and Cin is set to 1, 2's complement subtraction is the result. If Cin=0 and all four bits of the second register are set to equal 1, the decrement operation results because (1111) is equal to the 2's complement of (0001) .

The logic design of a full adder is shown in Figure 4. This is a standard circuit found in several textbooks, such as Ref.3 and Ref.4 in the bibliography.

FIGURE 4: LOGIC DIAGRAM FOR FULL ADDER



In the actual Integrated Circuit Editor (ICE) layout of the chip, only PMOS NOR gates and inverters were employed. Figure 5 shows how the OR, AND, and XOR gates of the logic design were implemented in hardware. An OR gate was made by inverting the output of a NOR gate. An AND gate was made by inverting both inputs of a NOR gate. Whenever two inverters occurred in series, they were cancelled out, as was done in the hardware representation of the exclusive-or gate in Figure 5.

FIGURE 5: LOGIC IMPLEMENTATION: NOR GATES AND INVERTERS

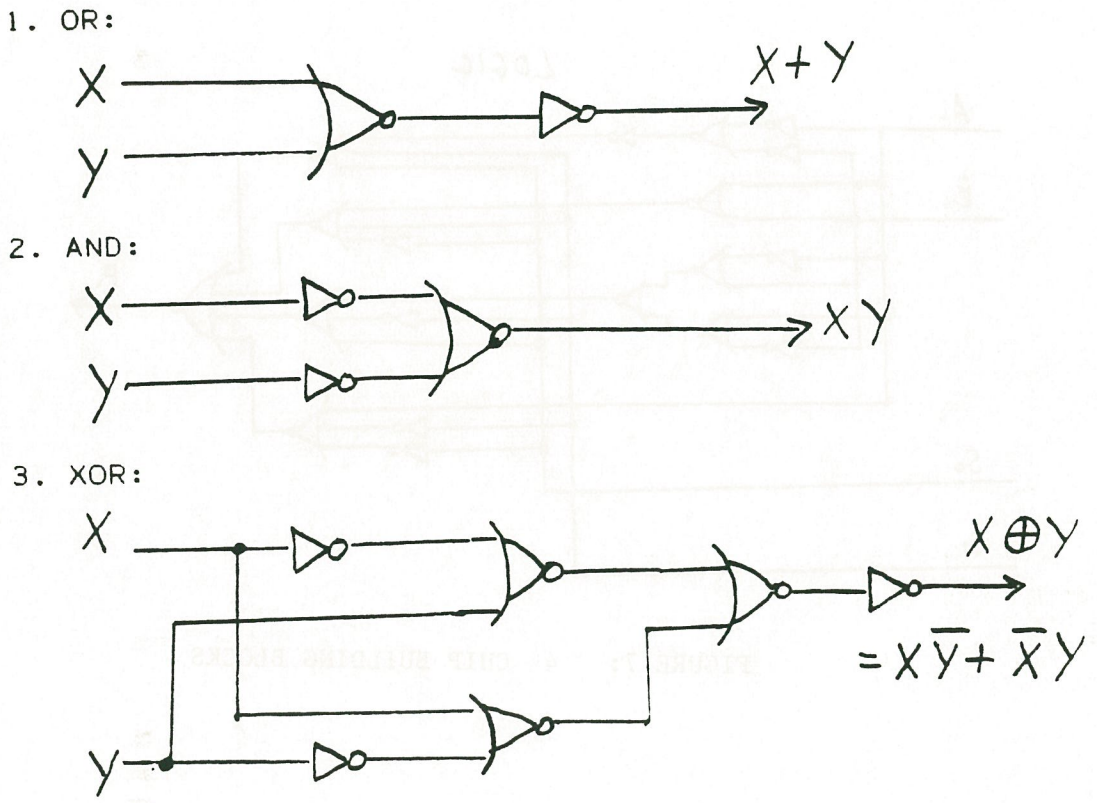


Figure 6 shows the hardware implementation of one bit of the ALU design. The arithmetic block shows the combinational circuit and the full adder, with sum S and Cout as outputs. The logic block shows the four logic functions that are fed to the 4-1 multiplexer, with an output of F. The S and F outputs along with mode select S2 would next go to a 2-1 line multiplexer not shown in Figure 6, and the final output would result.

FIGURE 6: ONE BIT OF THE ALU

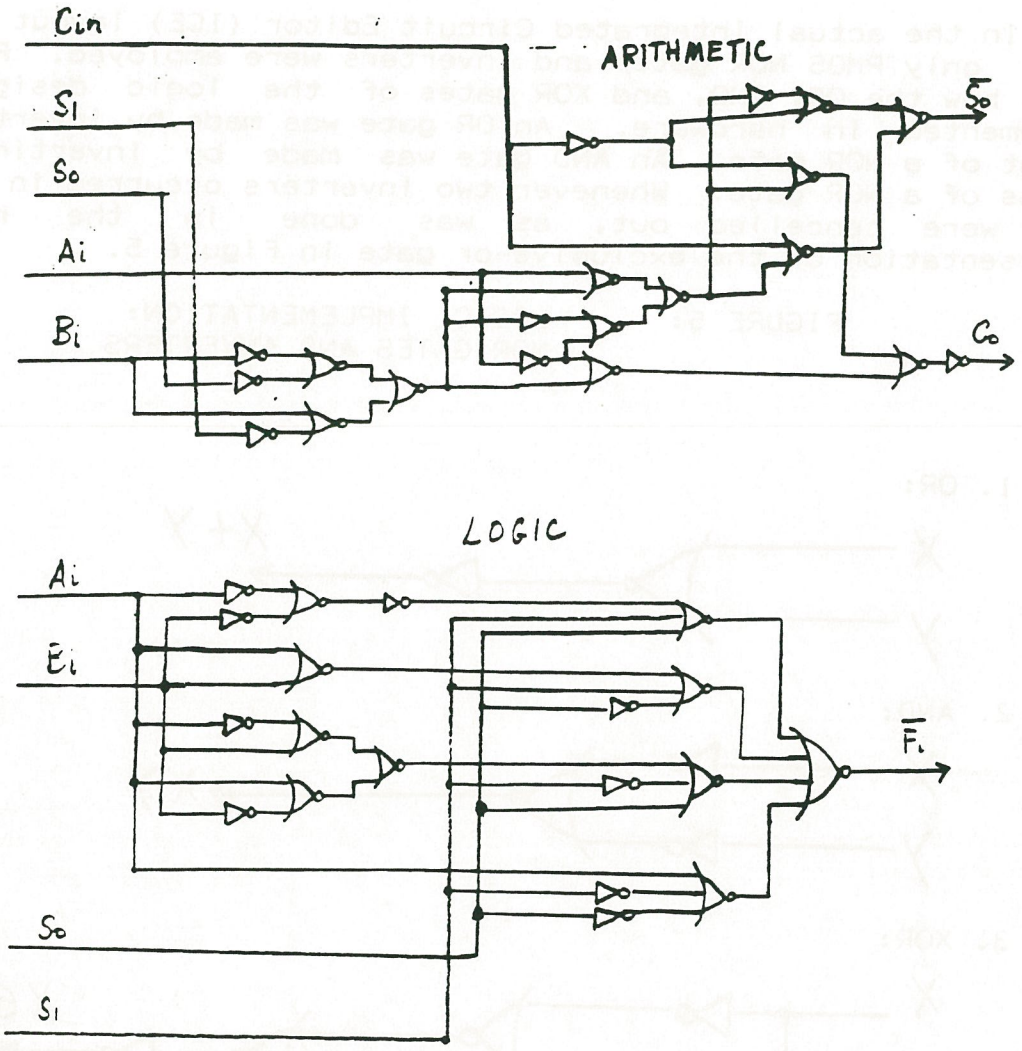
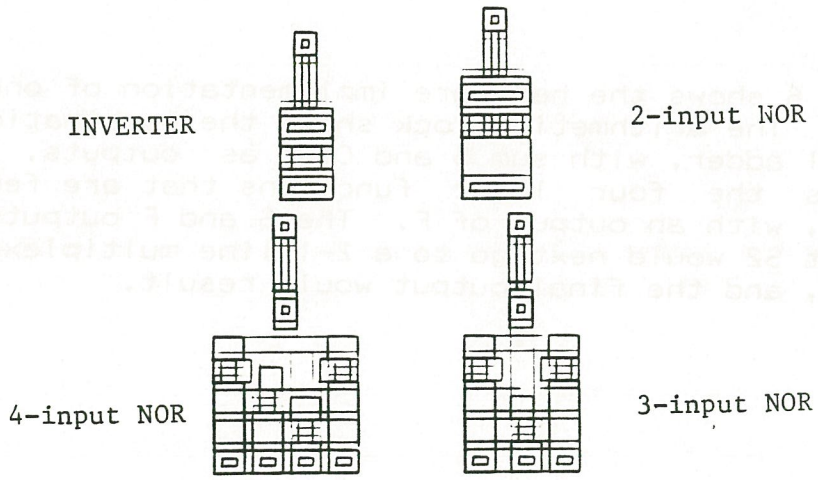


FIGURE 7: 4 CHIP BUILDING BLOCKS



RESULTS

Figure 7 shows the four types of gates used in the ICE layout: inverters and 2, 3, and 4- input NOR gates. The design was based on 10-um design rules and incorporated four mask levels: diffusion, oxide, contact cuts, and metal. All of the gates used PMOS enhancement drivers with active load transistors. The optimum length to width ratios for each gate were based on the SPICE analyses of Jim Taylor of RIT(2). These L/W ratios are listed below.

	LOAD		DRIVER	
INVERTER	L=50um	W=10um	L=10um	W=40um
2 input NOR	L=40um	W=10um	L=10um	W=20um
3 input NOR	L=50um	W=10um	L=10um	W=20um
4 input NOR	L=50um	W=10um	L=10um	W=20um

The exact ICE layout of the hardware design of Figure 6 is shown in Figure 8. This ICE plot shows the arithmetic and logic function blocks of one bit of the ALU. The dimensions of the one bit in Figure 8 are 1300um by 2400um. The four identical bits, one in each corner of the 5000um by 5000um chip, were brought together in the finished design found in the appendix. The pads were located in the center of the chip so that they would fit an automatic probe card arrangement for testing the logic of the chip after it was fabricated.

CONCLUSION

The design of the four bit ALU was completed. Built into the logic design was the capability to add on two shift registers to the arithmetic block. The design conforms to the current fabrication capabilities at RIT, including maskmaking, wafer processing, and testing.

REFERENCES

[1] Jim Taylor, RIT, "PMOS Standard Cell Library", 1987.

[2] Jim Taylor, RIT, SPICE Analyses on PMOS NOR Gates and Inverters, 1987.

[3] E.R.Salem, Course Notes on Digital Systems (EE 240), RIT,1988.

[4] M. Morris Mano, "Computer Engineering- Hardware Design", (Prentice-Hall Inc.,Englewood Cliffs, N.J.,1988), pp.28-115 and pp.240-245.

[5] Herbert Taub, "Digital Circuits and Microprocessors", (McGraw-Hill Inc., New York,1982), pp.43-223.

FIGURE *8* ONE BIT OF THE ALU