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R.I.T

Comprehensive Mapping and Benchmarking of Esaki

Diode Performance

by

David John Pawlik

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctorate of Philosophy in Microsystems Engineering

Microsystems Engineering Program
Kate Gleason College of Engineering

Rochester Institute of Technology
Rochester, New York
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Comprehensive Mapping and Benchmarking of Esaki Diode Performance
by
David Pawlik

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ABSTRACT

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The tunneling-FET (TFET) has been identified as a prospective MOSFET replacement technology with the potential to extend geometric and electrostatic scaling of digital integrated circuits. However, experimental demonstrations of the TFET have yet to reliably achieve drive currents necessary to power large scale integrated circuits. Consequentially, much effort has gone into optimizing the band-to-band tunneling (BTBT) efficiency of the TFET. In this work, the Esaki tunnel diode (ETD) is used as a short loop element to map and optimize BTBT performance for a large design space. The experimental results and tools developed for this work may be used to (1) map additional and more complicated ETD structures, (2) guide development of improved TFET structures and BTBT devices, (3) design ETDs targeted BTBT characteristics, and (4) calibrate BTBT models. The first objective was to verify the quality of monolithically integrated III-V based ETDs on Si substrates (the industry standard). Five separate GaAs/InGaAs ETDs were fabricated on GaAs-virtual substrates via aspect ratio trapping, along with two companion ETDs grown on Si and GaAs bulk substrates. The quality of the virtual substrates and BTBT were verified with (i) very large peak-valley current ratios (up to 56), (ii) temperature measurements, and (iii) deep sub-micron scaling. The second objective mapped the BTBT characteristics of the $\text{In}_{1-x}\text{Ga}_x\text{As}$ ternary system by (1) standardizing the ETD structure, (2) limiting experimental work to unstrained (i) GaAs, (ii) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and (iii) InAs homojunctions, and (3) systematically varying doping concentrations. Characteristic BTBT trendlines were determined for each material system, ranging from ultra-low to ultra-high peak current densities (J_p) of $11 \mu\text{A}/\text{cm}^2$ to $975 \text{ kA}/\text{cm}^2$ for GaAs and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, respectively. Furthermore, the BTBT mapping results establishes that BTBT current densities can only be improved by ~ 2 - 3 times the current record, by increasing doping concentration and In content up to $\sim 75\%$. The E. O. Kane BTBT model has been shown to accurately predict the tunneling characteristics for the entire design space. Furthermore, it was used to help guide the development of a new universal BTBT model, which is a closed form exponential using 2 fitting parameters, material constants, and doping concentrations. With it, J_p can quickly be predicted over the entire design space of this work.

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
ART	Aspect Ratio Trapping
BCB	Bis-benzocyclobutene
BGN	Band Gap nNarrowing
BTBT	Band-to-Band Tunneling
CFS/GFS	Constant/Generalized Field Scaling
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Planarization
CNT	Carbon Nano-Tube
CVD	Chemical Vapor Deposition
MOCVD	Metal-Organic CVD
RPCVD	Reduced Pressure CVD
UHVCVD	Ultra High Vacuum CVD
DC	Direct Current
DOS	Density of States
E-Beam	Electron Beam
EDX	Energy Dispersive X-ray
ETD	Esaki Tunnel Diode
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor FET
TFET	Tunneling FET
GUI	Graphical User Interface
IC	Integrated Circuit

ILD	Inter-Layer Dielectric
ITRS	International Technology Roadmap for Semiconductors
KMP	Kane Model Program
MBE	Molecular Beam Epitaxy
MOMBE	Metal-Organic MBE
NDR	Negative Differential Resistance
NPGS	Nano-Pattern Generation System
PC	Personal Computer
PIVET	Peak Including Valley Extraction Tool
PR	Photoresist
PVCR	Peak to Valley Current Ratio
RTA	Rapid Thermal Anneal
RTP	Rapid Thermal Processor
SEM	Scanning Electron Microscope
SIMS	Secondary Ion Mass Spectroscopy
SOG	Spin-on-Glass
SOI	Silicon-on-Insulator
SS	Sub-threshold Slope
TCAD	Technology Computer-Aided Design
TDD	Threading Dislocation Density
TEM	Transmission Electron Microscope
TLM	Transfer Length Modulation
UBM	Universal BTBT Model
WKB	Wentzel-Kramers-Brillouin approximation
XRD	X-Ray Diffraction

LIST OF SYMBOLS

I_p/I_v	Peak/Valley Current
J_p/J_v	Peak/Valley Current Density
e^-, h^+	electrons, holes
n, p	Electron/Hole carrier concentration
N_A, N_D, N^*	Acceptor & Donor concentrations, reduced average doping concentration
q	Magnitude of the charge on an electron
\hbar	Reduced Plank's constant
kT	Thermal energy (Boltzmann's constant & temperature)
ϵ_s, ϵ_r	Dielectric constant, Relative dielectric constant
E_G	Bandgap
m^*	Effective mass
$m_r, m_{r,n}, m_{r,p}, m_{r,BTBT}$	Relative effective mass, electrons, holes, average for BTBT
$m_{r,light}, m_{r,heavy}$	Relative effective mass for light and heavy holes
$E_F, E_{F,n}, E_{F,p}$	Fermi energy, n-side of junction, p-side of junction
$\Delta E_{F,n}, \Delta E_{F,p}$	$E_{F,n} - E_{C,n}$ and $E_{V,p} - E_{F,p}$
$E_C, E_{C,n}, E_{C,p}$	Conduction band, n-side of junction, p-side of junction
$E_V, E_{V,n}, E_{V,p}$	Valence band, n-side of junction, p-side of junction
N_C, N_V	Density of states (DOS) constants for the conduction & valence band
g_C, g_V	DOS energy distributions for conduction & valence bands
$f(E), f_n(E), f_p(E)$	Fermi-Dirac distribution, n-side, p-side
w_d, w_n, w_p	Depletion width, n-side, p-side
ξ	Electric field
V_{bi}	Built-in voltage

V_A	Applied bias
V_P, V_V	Peak, valley voltage
$D, D'(E)$	Overlap integral, integrand of D (differential with respect to energy)
T_{Kane}, T_{WKB}	BTBT probability from E. O. Kane [], using WKB approximation []

CHAPTER 1

Introduction and Motivation

1.1. Introduction

The success of the microelectronics industry is the result of continued MOSFET scaling to progressively smaller dimensions. Consequently, the number of transistors and functions per unit area has doubled approximately every two years, in accordance with Moore's Law [1-4]. Additionally, with proper scaling (Table 1.1), the transistors can operate at faster switching speeds [2-5]. The final results are computer chips with greater processing power with a cheaper price per function.

In 1974, Dennard, *et al.*, developed “constant field scaling” (CFS) wherein dimensions, voltages, and dopings are methodically reduced at the same rate (Table 1.1: CFS column) [5]. However, limitations in the scalability of subthreshold slopes (SS) for MOSFETs necessitated a “generalized field scaling” (GFS) method, wherein voltages are decreased at a slower rate than the physical dimensions [6]. In this fashion, circuit density and speed may be increased at the same rate as the CFS scheme. **The tradeoff is an increased power density.** Even with new channel materials, voltages can be scaled only so much before I_{On}/I_{Off} , I_{Leak} , and power densities rise to unacceptable levels. Therefore, a new type of switch will be needed for continued scaling.

“Eventually, toward the end of the Roadmap or beyond, scaling of MOSFETs is likely to become ineffective and/or very costly, and advanced non-CMOS solutions will need to be implemented to continue to improve performance, power, density, etc. ...”

“... Alternate channel materials and/or devices such as tunnel field-effect transistor can provide some relief in this area by potentially allowing more aggressive V_{dd} scaling or/and steeper subthreshold slope.”

The 2009 International Technology for Semiconductors (ITRS) [7] clearly identifies the tunneling-FET (TFET) as a replacement technology with the potential to alleviate some of the scaling challenges that look to be insurmountable in the future. TFETs have the potential to exceed the limited SS scalability of MOSFETs [8-20].

1.2. Importance of Subthreshold Slope

Ideally, the drain current (I_D) versus gate voltage (V_G) characteristics for a switch would be a perfect square function as shown in Fig. 1.1a. Specifically, I_D would be 0 A for all V_G less than the threshold voltage (V_t). For V_G greater than or equal to V_t , I_D instantaneously jumps to a target on current (I_{on}). Assuming V_t can be scaled, the minimum operating bias (V_{DD}) would approach 0 V as $V_t \rightarrow 0$ V.

Table 1.1: “Constant field scaling” (CFS) and “general field scaling” (GFS) schemes

<u>Parameter</u>	<u>Scaling Factors</u>	
	<u>CFS</u>	<u>GFS</u>
Physical Dimensions L, W, T_{OX} , wire pitch	$1/\lambda$	$1/\lambda$
Voltage	$1/\lambda$	$1/\alpha$
Body Doping	λ	λ^2/α
Circuit Density	$1/\lambda^2$	$1/\lambda^2$
Electric Fields	1	λ/α
Current Density	1	λ^2/α^2
Current	$1/\lambda$	λ/α^2
Power/Energy per circuit	$1/\lambda^2$	λ/α^3
Power Density	1	λ^3/α
Capacitance per circuit	$1/\lambda$	$1/\lambda$
Circuit speed	λ	λ (goal)

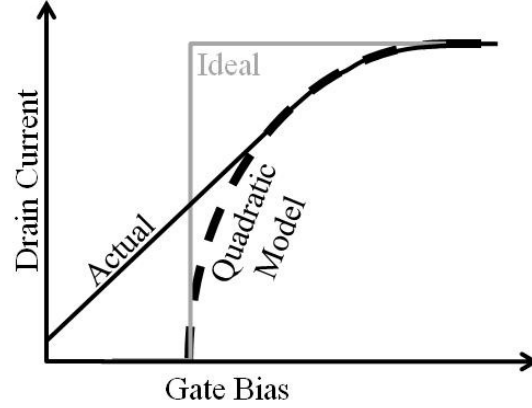


Fig. 1.1: Generic I_{DS} - V_{GS} characteristics for an (a) ideal switch, (b) quadratic MOSFET model, and (c) actual subthreshold characteristics.

However, the standard switches in modern digital integrated circuits (ICs) use MOSFETs. The basic quadratic MOSFET model, (1.1) and (1.2), describes half of an ideal switch seen in Fig. 1.1. Specifically, there is no current flow ($I_D = 0V$) when V_G is less than or equal to V_t . Once V_G is greater than V_t , the transistor will suddenly turn on, providing a non-zero I_D . However, I_D does not immediately increase to I_{ON} . Instead, it increases at the rate of $(V_G - V_t)^2$, as seen in (1.2), which makes the reasonable assumption that the channel is fully saturated. To achieve I_{ON} , V_G must increase to V_t plus an additional amount “ ΔV_G ”. Therefore, the minimum V_{DD} is ΔV_G , assuming that V_t can be engineered down to 0 V.

$$I_{DS} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right], \quad V_{DS} < V_{GS} - V_t \quad (1.1)$$

$$I_{DS} = \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_t)^2}{2}, \quad V_{DS} > V_{GS} - V_t \quad (1.2)$$

As one may expect, the quadratic model is incomplete and does not accurately capture the MOSFETs subthreshold characteristics. In reality, there is a non-zero leakage current (I_{off}) at V_G of 0 V, which increases exponentially in the subthreshold region, Fig. 1.1c. The SS is proportional to the inverse exponential slope, quantitatively describing how fast a MOSFET turns on. For a given SS there is a minimum threshold voltage, $V_{t,min}$, for which I_{off} and I_{on} remain at

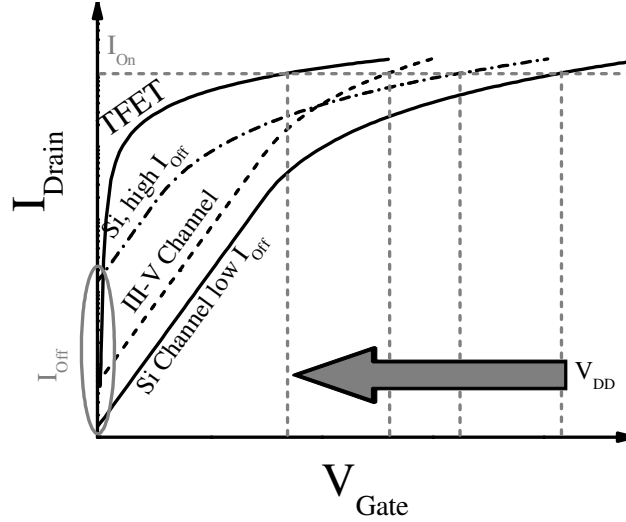


Fig. 1.2: Generic I_{DS} - V_{GS} characteristics showing the V_{DD} scaling for a (i) Si channel MOSFET with low I_{Off} , (ii), Si channel MOSFET with large I_{Off} , (iii) high mobility III-V channel MOSFET, and (iv) TFET.

their target values. In order for $V_{t,min}$ to decrease while keeping I_{Off} and I_{On} constant, the SS would have to decrease (an increased slope). Therefore, the minimum V_{DD} is roughly equal to $V_{t,min} + \Delta V_G$.

The main challenge regarding the scaling of MOSFET electrostatics pertains to a fundamental limitation in the scalability of SS; regardless of material type or device structure [11]. This situation is depicted in Fig. 1.2. For instance, assume that the “Si channel device with low I_{Off} ” is the current technology generation to be scaled. If the device is scaled without any dramatic changes (“Si, high I_{Off} ”), V_{DD} can be reduced a significant amount. However, a large sacrifice is made by drastically increasing I_{Off} . Eventually, the I_{On}/I_{Off} ratio would become too small, killing noise margins.

Replacing channel materials to a semiconductor with higher mobility and smaller effective mass can be a great help. As seen in Fig. 1.2, the “III-V channel device” has the same SS. However, all else being equal, the higher mobility and smaller effective mass results in a higher current density. As a result, there is a substantial reduction in V_{DD} with a minimal increase in I_{Off} , compared to the original Si device. In other words, by using various methods and materials to increase carrier mobilities, V_{DD} can still be aggressively scaled with only a small

reduction in I_{ON}/I_{Off} ratios. This can only be maintained as long as methods to increasing carrier mobilities are feasible.

Recall that the 2009 ITRS [7] states that methods to maintain the scalability of MOSFETs are “likely to become ineffective and/or very costly”. To overcome this issue, it is desirable to have a switch with an SS below the MOSFET limit such as the TFET [8-20]. As seen in Fig. 1.2, such a switch could enable continued scaling of power supplies and maintain the desired I_{ON}/I_{Off} targets.

1.3. Subthreshold Limit of MOSFETs

As a direct consequence of Fermi-Dirac statistics, MOSFETs have a minimum SS of 60 mV/dec. The origins of this limit are easily understood as the result of carrier diffusion over the source/body barrier formed by the forbidden bandgap. Fig. 1.3 shows the conduction band (E_C) of an n -channel MOSFET biased in the sub- V_i regime. Those carriers with energy greater than E_C in the body region ($E_C(B)$) will diffuse across the junction, creating a sub-threshold current.

As a direct result of Fermi-Dirac statistic, the distribution of carriers above E_C quickly becomes a decaying exponential of the form $A \times \exp[-qV/kT]$; where “ qV ” is any energy a few kT above E_C and E_f . Recall that current is proportional to the number of carriers taking part in the

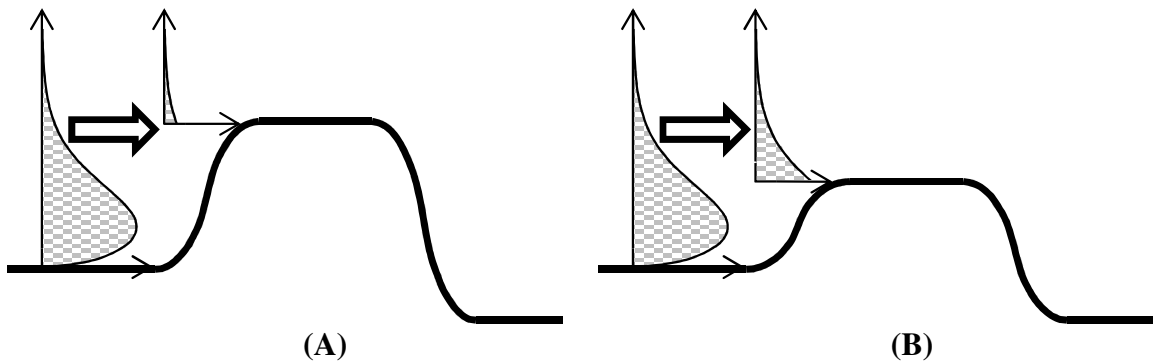


Fig. 1.3: The conduction band portion of the source, body, drain (left to right) regions of a MOSFET; including electron carrier concentration.

conduction. Therefore, I_D in the sub-threshold regime is,

$$I_{DS} = \int_{V_{bi}-V_G/n}^{\infty} A \exp\left[-\frac{q}{kT}V\right] dV \quad (1.3)$$

Where A is a constant, k is Boltzmann's constant, T is the temperature, and “ n ” is a measure of how effectively the gate can modulate the barrier ($E_C(B)$). The built in potential, V_{bi} , is equal to the barrier height when $V_G = 0$ V. Performing the integration, and grouping all constants into I_0 , the subthreshold current clearly becomes an exponential controlled by V_G .

$$I_{DS} = I_0 \exp\left[\frac{q}{nkT}V_G\right]; \quad V_G < V_T \quad (1.4)$$

The leakage current, I_0 , is dependent on material properties, device design, and V_{DS} . From (1.4), the SS of a MOSFET can be calculated as,

$$SS = \frac{dV_G}{d \log(I_{DS})} = n \frac{kT}{q} \ln(10) \quad (1.5)$$

Under optimal conditions the gate has perfect control of $E_C(B)$. Therefore the minimum value for “ n ” is one, resulting in a minimum SS of 60mV/dec at room temperature (300 K). From this analysis it can be seen that the SS limit cannot be overcome for MOSFET structures, regardless of the device structure or materials used.

The above conclusion is true unless one of the assumptions used for this derivation is violated. For all typical MOSFET structures this would be very difficult to do. It has recently been proposed that the application of magnetic materials to the gate oxide would result in an effective negative dielectric constant. The gate would then modulate $E_C(B)$ faster than V_G is changed, effectively reducing “ n ” below one and proportionately reducing the minimum achievable SS. This method has only recently been researched, and much work has yet to be done before it can be determined if it is a practical method to reduce SS.

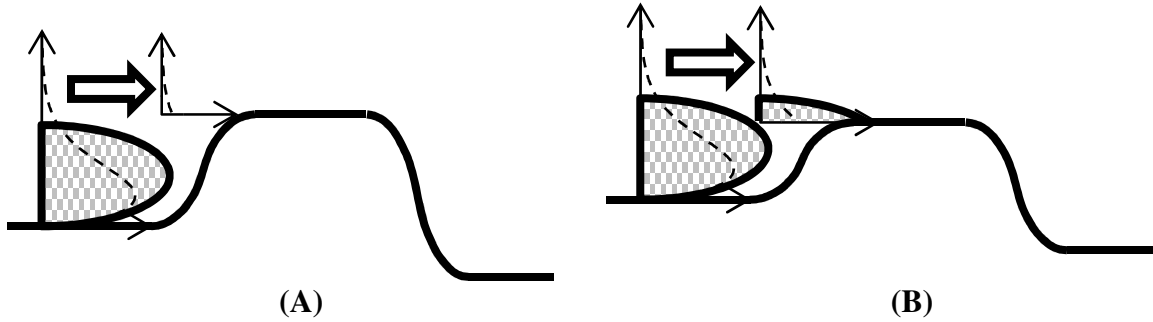


Fig. 1.4: The conduction band portion of the source, body, drain (left to right) regions of a MOSFET with engineered electron distribution.

Another potential way of reducing SS in a MOSFET is by engineering the carrier distribution to decay at a rate faster than the standard Fermi-Dirac statistics dictate (Fig. 1.4). Most semiconductors cannot deviate from that exponential rate because their density of states (DOS) predictably increase as you move away from the band edge and Fermi-Dirac statistics are fundamental physics. However, using a material whose DOS decreases after a few kT above E_C would result in a carrier distribution that falls off at a rate faster than q/kT , thereby reducing SS. Regardless, finding a suitable material or way to provide the necessary changes in dielectric constant or carrier distribution is beyond the scope of this proposal.

1.4. Objective, Implementation, and Application of Work

The over-all objectives of this work are geared towards improving the potential for integrating BTBT devices in commercial production settings. Towards this end, there are two main thrusts. The first is an investigation into the integration of III-V based ETDs onto Si substrates, which will likely remain the industry standard. Afterwards, BTBT characteristics will be systematically characterized and mapped over a large design space. This will provide an experimental baseline for future BTBT device development and advancement.

Si will remain a popular substrate of choice for production fabrication for a variety of reasons. Si is mechanically strong, with a long established history of use in industry. Furthermore, it is a commonly available element which can be purified and shaped into the

necessary the desired forms at low cost. However, the material properties of III-V semiconductors can provide superior device characteristics needed for continued scaling of CMOS. Unfortunately, III-V semiconductors are much more expensive and relatively weak or brittle, thereby limiting substrates to smaller dimensions (usually less than four inch diameters). Therefore, much effort has gone into integrating III-V virtual-substrates onto bulk Si wafers in order to obtain the benefits of both systems and minimize the drawbacks.

It is important to understand that none of the hetero-integration methods are perfect, and the density and electrical effects of the threading dislocations must be characterized. Typically these defects negatively impact carrier lifetimes, and provide deep level traps within the forbidden bandgap. This will typically increase leakage currents and decrease desirable current control. In an ETD, J_V will be increased and the PVCR will decrease. ETD structures designed to exhibit large PVCR will be more sensitive to these defects, making them a prime candidate for determining the electrical quality of virtual substrates. Specifically, this work will utilize a relatively new hetero-integration method known as aspect ratio trapping (ART) to generate GE and GaAs virtual-substrates on Si. Primarily, a series of high PVCR GaAs/InGaAs ETDs will be fabricated and tested, along with companion samples grown directly on Si and GaAs bulk substrates. Comparing the results of these structures will verify the quality of the virtual substrates. Additionally, low and high temperature measurements of the ETDs be used to gain addition insight into the quality of the semiconductor.

After verifying that high quality ETDs and virtual substrates can be integrated on Si, work will proceed with the second thrust. Even though there is a long history of literature reports on ETDs, most papers present fairly novel structure designs which cannot easily be compared with each other. Furthermore, the lack of calibrated BTBT models for a large design space makes it difficult, at best, to quantitatively predict BTBT behavior. This has been a large difficulty concerning the development of TFETs, which generally have suffered from limited on-state currents. Even though the gate stack is one dimension of the problem, BTBT efficiency from the

source to body region play a very large role for maximizing I_{on} . This work is geared towards determining a systematic way of engineering the source/body junction in order to optimize BTBT efficiency for maximum I_{on} . Additionally, without mapped BTBT behavior or adequate models, the main guide to targeting desired BTBT characteristics is past experience. In other words, it is difficult to design an ETD structure that meets desired specification, unless a previously fabricated structure already meets those criteria.

In this work, methods will be developed that will enable the efficient mapping of BTBT characteristics over a large design space. Experimental results from this mapping technique will provide the basis for (i) BTBT model calibration, (ii) determination of BTBT limitations, (iii) paths towards improved BTBT characteristics, and (iv) BTBT trendlines for quantitative relationship between ETD structure and BTBT characteristics. Furthermore, with a large database of self-consistent structure designs, a universal (or series of semi-universal) BTBT model may be developed. Such a model would add concrete relationships between material parameters and BTBT current density.

A basic ETD structure template will be developed for the mapping effort. To help eliminate and simplify the variables, the ETDs will be designed with unstrained, direct bandgap semiconductors with well known material parameters. Furthermore, layer thicknesses will be standardized and SIMS analysis used to determine final doping concentrations. Three material systems from the $\text{In}_{1-x}\text{Ga}_x\text{As}$ ternary system will be chosen; (i) GaAs, (ii) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and (iii) InAs. The N_A and N_D doping concentrations will be systematically varied, generating characteristic trendline for each material system. Interpolation can be used for In mole fractions between the chosen materials. The final results will be a mapping of the BTBT characteristics for the entire $\text{In}_{1-x}\text{Ga}_x\text{As}$ ternary system. Completion of this objective requires the development of (i) a modular fabrication process, (ii) formalized electrical testing procedure, and (iii) universal analysis and organization methods. Once proven, the tools developed for this mapping scheme can be applied to additional material systems, including complicated heterjunctions which do not

conform to the structure template used here. In other words, the developed tools and methods are just as useful as the results reported on in Chapters 4, 5, and 6.

Finally, the modeling effort in this work will be limited to a single physics based, analytical model. It is preferable to have a model which most clearly displays the relationship between material parameters, ETD operation, and BTBT current density. The model is to be calibrated to the mapped ETD design space, and compared with the experimental J-V measurements. One of the results will be the ability to predict BTBT characteristics for basic ETD structures, given a material system and the doping concentrations or J_p . Secondly, the model will be used as the basis for the development of a universal BTBT model or trend. Ideally, the model would accurately predict J_p for a wide range of material parameters and doping concentrations.

The methods, modeling, and experimental results provided in this work will be the basis for further BTBT development and model calibration. Device engineers can utilize the experimental results and characteristic trendlines to target desired BTBT current densities. The experimental results can be used to calibrate TCAD models over a large design space, enabling accurate modeling of complicated BTBT structures, beyond basic ETDs. Additionally, the mapping effort will provide clear direction on improving BTBT characteristics. Furthermore, the methods developed here will enable the consistent and efficient characterization of innumerable material systems.

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CHAPTER 2

Theory of Quantum Tunneling Devices

2.1. Esaki Tunnel Diodes

In the 1950's, intensive investigation into the internal field emission of p-n junctions in the semiconductor materials was being performed. Of great interest was the relationship between the I-V characteristics and doping concentration of p-n junctions. Chynoweth, and other research groups, systematically increased the doping concentration in p-n junctions, looking at breakdown voltages. With large enough concentrations, the breakdown was shifted to below one volt. These diodes would start to conduct a greater current density in reverse bias than in forward bias, earning them the name of *Backward Diodes*. Once the doping levels became highly degenerate for both terminals, Esaki [1] began to notice a breakdown of zero volts in reverse bias. The forward bias characteristic would initially rise to a peak current (I_p), then exhibit NDR and fall to a valley current (I_v), and then rise again in the traditional thermal current. This typical “N” shape characteristic was the first direct observation of quantum mechanical tunneling, earning Esaki the Nobel prize in Physics in 1973. The device structure of an Esaki tunnel diode (ETD) is a degenerately doped p-n junction, sometimes with the inclusion of a thin (< 10 nm) *i*-layer in the middle, as shown in Fig. 2.1.

Without any applied bias, Fig. 2.2c, E_f is flat and above E_C on the n-type side ($E_C(n)$), and below E_V on the p-type side ($E_V(p)$). Qualitative carrier density versus energy curves are provided for electrons and holes. In reverse bias, Fig. 2.2b, Zener tunneling occurs immediately, allowing

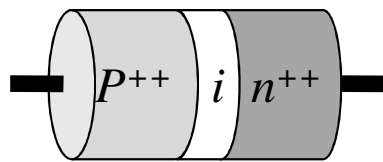


Fig. 2.1: ETD device structure.

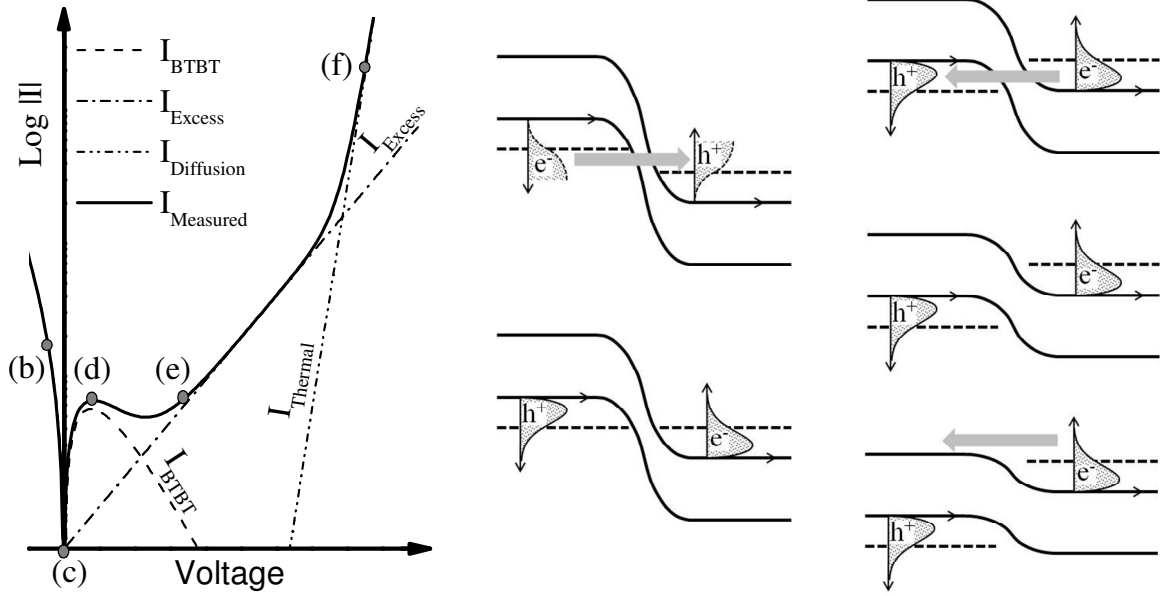


Fig. 2.2: (a) I-V characteristic, and schematic band diagram for (b) reverse bias, (c) equilibrium, (d) peak tunneling current, (e) minimum direct tunneling current, and (f) diffusion current for a generic ETD.

for large amounts of current to flow. With a small amount of forward bias, electrons occupying states below E_f in the n-side can begin tunneling to unoccupied states (holes) above E_f on the p-side, Fig. 2.2d. Eventually, E_C on the n-side is shifted above E_V on the p-side, which stops direct tunneling, Fig. 2.2e. However, the current does not drop down to 0 A; instead, carriers tunnel via indirect paths resulting in an excess current. Finally, after a large enough bias is applied, the p-n junction starts to behave like a standard diode, and a diffusion current begins to flow, Fig. 2.2f.

There have been many experimental reports of ETDs of various material systems, structures, current densities, and peak-to-valley current ratios (PVCR) over the last five decades. Depending on the application, the PVCR may be more important (Ex. Tunneling SRAM) or the current density (Ex. TFET). It is therefore useful to plot J_p vs. PVCR, Fig. 2.3. It quickly becomes evident that to achieve greater J_p , a trade-off in PVCR is made. Direct bandgap materials typically have been used to improve PVCR with respect to Si ETDs. However, very high current densities have been achieved for Si, InGaAs, staggered gap, and broken gap material systems. These structures are also prime candidates for the fabrication of TFETs with large I_{On} .

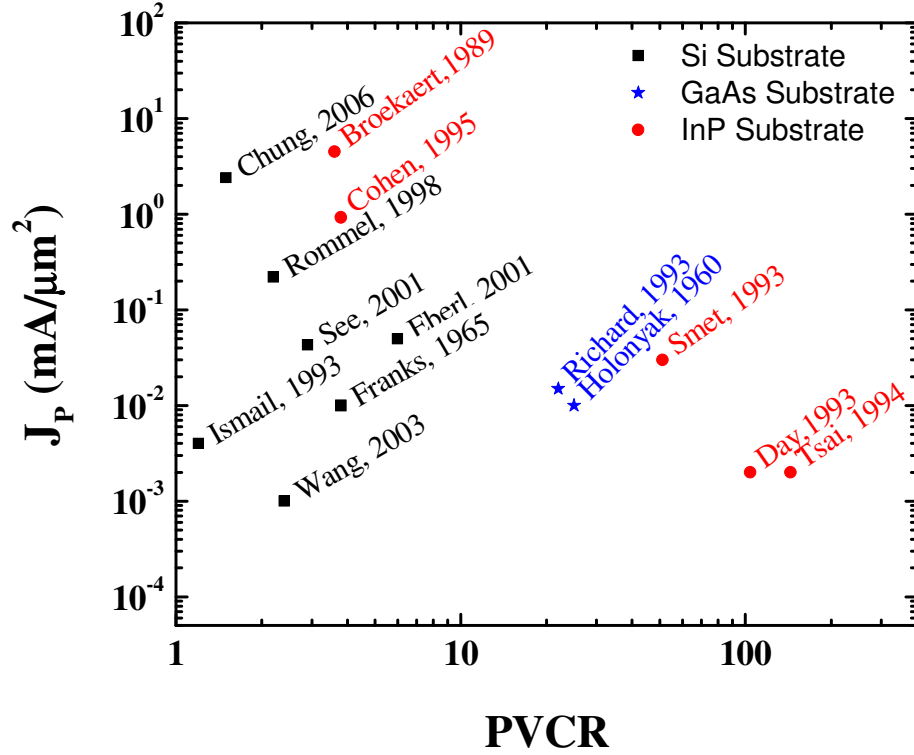


Fig. 2.3: J_P versus PVCR for key ETD structures of various material systems. InP substrate refers to lattice matched InGaAs ETD.

However, there is currently no way to predict the maximum I_{ON} or minimum subthreshold slopes (SS) that area achievable.

2.2. Analytical Band-to-Band Tunneling Models

Numerically based TCAD tools, such as SynopsysTM Sentaurus or Silvaco's Atlas, have the potential for accurate simulation of simple and complex BTBT structures. However, such methods lack the insight that analytical models quickly and easily provide; For instance, constant field scaling is easily understandable in conjunction with the MOSFET quadratic model. Therefore, this research will concentrate on physics based analytical models. The first such model to be fully derived and published was by E. O. Kane in 1961 [2]. Afterwards, many of the new BTBT models, such as Hurkx [3] and Milovanovic [4], have been derived from Kane's original model. Even though the new models are simplified, they typically only satisfy a subset of BTBT which does not include high current density ETDS and BTBT in forward bias. Other

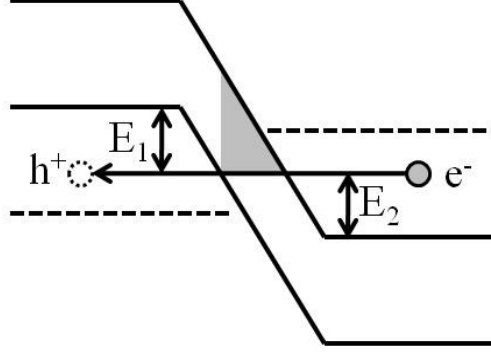


Fig. 2.4: Simplified band diagram used for Kane's BTBT model [2].

models from Schenk [5] and Solomon [6] are much more complex, and are not easily applicable fabricated structures.

The primary focus of this proposal will begin with the Kane model [2], which is described below. In the area of the tunnel junction, the electric field (ξ) is assumed to be constant, resulting in a triangular tunneling barrier as denoted by the shaded region in Fig. 2.4. Kane's original BTBT model for Esaki diodes is shown in (2.1). Where " D ", (2.2), is referred to as the "overlap integral". This factor looks at the probability of an e^- occupying an energy state above $E_C(n)$ minus the probability of occupancy below $E_V(p)$. The factor E_S is defined as the smaller value of $E_V(p) - E_{particle}$ or $E_{particle} - E_C(n)$. Notice that the overlap integral cannot be explicitly solved without any approximations.

$$J_{BTBT} = \frac{q^2 \xi}{36\pi\hbar^2} \sqrt{\frac{2m^*}{E_g}} \cdot D \cdot \exp\left(-\frac{\pi\sqrt{m^*} E_g^{3/2}}{2\sqrt{2}\hbar\xi}\right) \quad (2.1)$$

$$D \equiv \int_{E_C(n)}^{E_V(p)} [F_C(E) - F_V(E)] \left[1 - \exp\left(-\frac{2E_S}{E}\right)\right] dE \quad (2.2)$$

$$\bar{E} = \xi \sqrt{\frac{2\hbar^2}{\pi^2 m^* E_g}} \quad (2.3)$$

The constant electric field, (2.4), is calculated from the built in voltage (ψ_{bi}) minus applied bias (V_{app}) divided by the entire depletion width (w_d) as calculated from the full depletion

approximation typically used for p-n junctions. The term N^* is a form of reduced averaged doping on the p- and n-side of the junction calculated from (2.5). Given the exponential relationship between BTBT probability and tunnel barrier width, N^* will be used as the control variable for constructing characteristic J_p trendlines.

$$\xi = \frac{(\psi_{bi} - V)}{\omega_d} = \sqrt{\frac{q(\psi_{bi} - V)}{2\epsilon_s}} N^* \quad (2.4)$$

$$N^* = \frac{N_A N_D}{N_A + N_D} \quad (2.5)$$

Also, the effective mass (m^*) is an average of the conductivity effective masses for holes and electrons. Typically, (2.6) is used to calculate this average.

$$m^* = \left[\frac{1}{m_h} + \frac{1}{m_e} \right]^{-1} \quad (2.6)$$

Recall that momentum must be conserved, even for BTBT. As formulated above, the Kane model assumes that the momentum associated with the electron wave vector does not change during BTBT. Therefore, (2.1) is only valid for direct bandgap. Additionally, only two bands are treated in this model. The model will begin to breakdown if multiple valence and conduction bands are populated as a result of material and doping conditions.

In literature, the Kane model has been applied to Ge ETDs [7-10] with good agreement. Since both Si and Ge are indirect bandgap materials, phonon interactions were included in order to provide the momentum shift necessary for BTBT. This was accomplished by changing E_g to

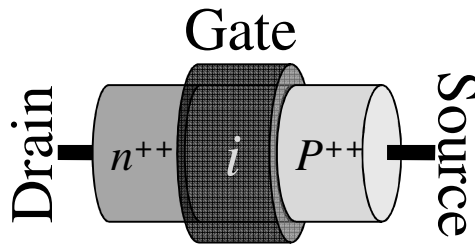


Fig. 2.5: TFET Device structure.

$(E_g + E_p)$ in the argument of the exponential. For this work phonon interactions are not included and all BTBT transitions are assumed to be direct (no momentum shifts needed). This is an appropriate approximation for all of the ETDs modeled in this work, whose primary bandgaps are located in the Γ -valley.

2.3. Tunneling FET

In a TFET, the primary current mechanism is BTBT, which does not suffer from the same SS limitations as MOSFETs [9, 11-21]. The typical structure of a TFET takes the form of a gated p^{++} - i - n^{++} diode, as shown in Fig. 2.5. The Source and Drain wells are degenerately doped, with sharp profiles near the gated body region, which is intrinsic or moderately doped (i -layer). For the best gate control and SS, a wrap around or multi-gate structure is often assumed. Currently the best doping profiles, and tunnel junctions, are grown epitaxially. Therefore, TFETs are often represented as vertical structures.

Fig. 2.6a shows the equilibrium band structure for the TFET. As drawn in the figure, to the left is the Source, in the middle is the body region, and the drain is at the end. The electron (“e⁻”) distribution below the valence band (E_V) and hole (“h⁺”) distribution in the conduction band are shown for the source and body region, respectively. These are the primary carriers contributing to current conduction in the TFET. Notice that the shape of the distribution of the electrons largely follows Fermi-Dirac statistics, which is scaled by the DOS. Conversely, due to the low E_f in the body region the distribution of holes are directly limited by the DOS in the conduction band.

The application of the positive drain bias ($V_{DS} > 0$) shifts the drain and body region down, as shown in Fig. 2.6b. For this discussion it is assumed that nearly all of the electric fields are confined to the p - i and i - n junctions. Without an applied V_G , the full thickness of the i -layer prevents BTBT from occurring, thereby reducing I_{DS} to a leakage current similar to a standard p - i - n diode.

A positive bias to the gate will lower the body region ($E_C(B)$ and $E_V(B)$), shown in Fig. 2.6c. With a large enough bias, $E_C(B)$ will be shifted below the E_V in the source region ($E_V(S)$), thus reducing the tunneling barrier thickness from the entire body region to less than the depletion width. Electrons in the source region are then free to tunnel through the barrier formed by the forbidden bandgap and into a vacant state in the conduction band of the body. The i - n junction will then sweep the carriers into the drain, forming a gate controlled BTBT current (I_{BTBT}). Further increases in V_G will increase the number of electrons available for tunneling and slightly reduce the tunneling barrier thickness. Recall that tunneling probabilities are exponentially dependent upon the barrier thickness. Therefore, the modulations in the barrier thickness caused by V_G will result in significant tunneling probably increases.

2.4. TFET Subthreshold Slope

Presented here are two ways to show that sub-60 mV/dec SS are achievable with TFETs. The first method presented looks at the electron distributions ($n(E)$) and assumes that tunneling probabilities (T) are approximately constant for all energies between $E_V(S)$ and $E_C(B)$. For the quantitative analysis we will also assume that there is always a hole ($h(E)$) or vacancy for electrons to tunnel into. In other words, it is assumed that $h_B(E) \gg n_S(E)$ for energies bounded by $E_V(S)$ and $E_C(B)$. Therefore, the number of carriers taking part in I_{BTBT} can be written as,

$$I_{BTBT} \propto n_{BTBT} = T \cdot \int_{E_C(B)}^{E_V(S)} n(E) dE \quad (2.7)$$

Where $n(E)$, given by (2.8), is the distribution of electrons below $E_V(S)$, and $n_C(E)$ is calculated as the density of states ($g_V(E)$) times the Fermi-Dirac statistics for electrons ($F_e(E)$). Note that $F_e(E)$ can be approximated as an exponential as long as the energy (E) is greater than a few kT above E_f in the source region, similar to the approximation used for the MOSFET.

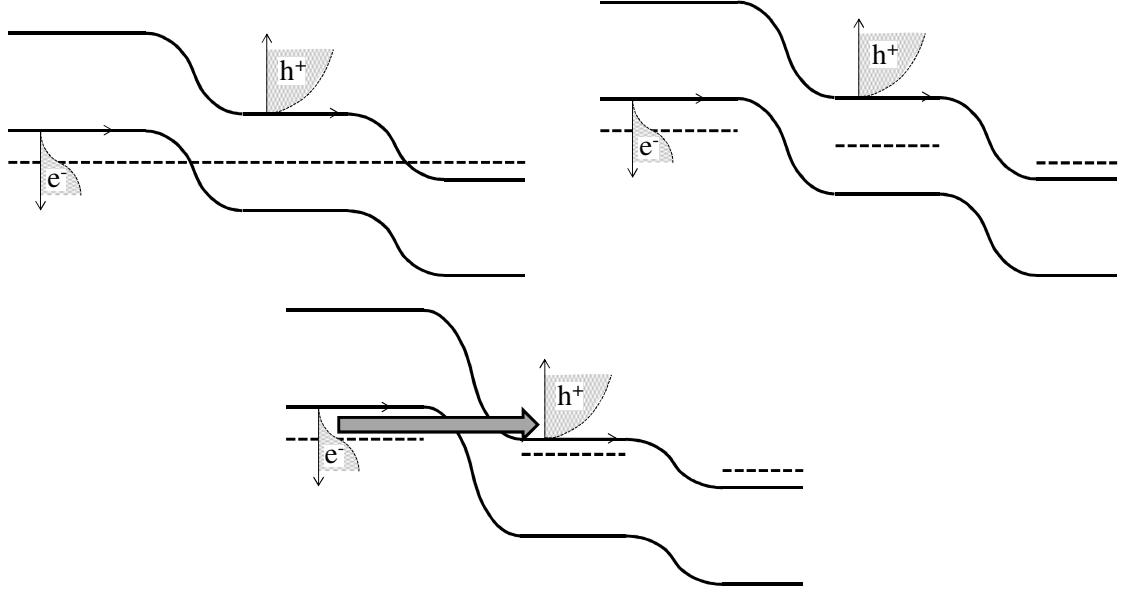


Fig. 2.6: Band diagrams showing the operation of the TFET: (a) at equilibrium, (b) with an applied V_{DS} , and (c) V_g turned on.

$$n(E) = g_v(E) \times F_e(E) = A \sqrt{E_v - E} \exp\left(\frac{E_f - E}{kT}\right) \quad (2.8)$$

Where “A” is the collection of material constants normally associated with DOS calculations. For this calculation the constant “A” does not affect the final result. The integral used to calculate n_{BTBT} results in an imaginary error function (“erfi”). It will be assumed that $E_v(B)$ drops below $E_c(S)$ as soon as V_G is increased above 0 V. Ideally, V_G will have perfect control over $E_c(B)$ as well. The final integration will look as follows, where B is a collection of constants.

$$n_{BTBT} = B \left[-\frac{1}{4} \sqrt{\pi (kT)^3} \operatorname{erfi}\left(\sqrt{\frac{V_G}{kT}}\right) + \frac{kT}{2} \sqrt{V_G} \exp\left(\frac{V_G}{kT}\right) \right] \quad (2.9)^1$$

At small V_G , the first term will reduce the rate at which n_{BTBT} increases, thereby reducing SS. However, the erfi function increases in magnitude at a slower rate than the exponential term.

¹ $\operatorname{erfi}(x) = -i \times \operatorname{erf}(ix) = -i \frac{2}{\sqrt{\pi}} \int_0^{ix} \exp(-t^2) dt = \frac{2}{\sqrt{\pi}} \int_0^x \exp(k^2) dk$

Therefore, for larger applied biases, the first term becomes negligible. As a result, the erfi function may be ignored as a first order approximation. The natural log of I_{BTBT} then becomes,

$$\ln(I_{BTBT}) \approx \ln\left(\frac{kT}{2}\right) + \frac{1}{2}\ln(V_G) + \left(\frac{V_G}{kT}\right) \quad (2.10)$$

The SS is then calculated as;

$$SS \approx \left[\frac{1}{2V_G} + \frac{1}{kT} \right]^{-1} \ln(10) \quad (2.11)$$

From (2.11), the gate will have direct control of the SS for small V_G . Once “ $2V_G$ ” becomes $\sim 1/10$ of kT , the gate will no longer directly control the SS. This is advantageous since the SS will approach $\ln(10)/kT$, which is the classical MOSFET limit as shown in (1.5). This means that the average achievable SS is less than 60 mV/dec at room temperature.

The above analysis is only valid when $E_C(B)$ remains a couple kT above $E_f(S)$. For greater accuracy the full Fermi-Dirac statistics is needed, which makes closed form approximations difficult. Numerical solutions are easily achieved. In Fig. 2.7 (dotted line), an example calculation is given where $E_f(S)$ of 0.3 eV is assumed. The SS approaches 60 mV/dec. up to a V_G of ~ 250 mV, at which point $E_C(B)$ is no more than a few kT above $E_f(S)$ and (2.11) breaks down. At greater V_G the SS rapidly increases, which does not matter as long as the power supplies are scaled small enough.

Another approach to calculating achievable SS is through the use of a BTBT Zener current model [4, 9, 16, 17, 22], approximated from the following version of the E.O. Kane Esaki diode model [2, 23], which will be discussed in greater detail later.

$$\begin{aligned}
I_{BTBT} &= aV_{eff}\xi \exp\left(-\frac{b}{\xi}\right) \\
a &= \frac{q^3 \sqrt{2m^* / E_g}}{4\pi^2 \hbar^2} \\
b &= \frac{4\sqrt{m^* E_g^{3/2}}}{3q\hbar}
\end{aligned} \tag{2.12}$$

Where ξ is the electric field at the tunnel junction, m^* is the averaged effect mass of electrons and holes, and V_{eff} is the tunnel junction bias. Taking the derivative of (2.12), the SS can be calculated as,

$$SS = \left[\frac{1}{V_{eff}} \frac{dV_{eff}}{dV_G} + \left(\frac{\xi + b}{\xi^2} \right) \frac{d\xi}{dV_G} \right]^{-1} \ln(10) \tag{2.13}$$

As usual, it is assumed that the gate would have perfect control of $E_C(B)$, therefore dV_{eff}/dV_G equals one. The second term is more complicated, but can be simplified by assuming that the junction width, w_d , does not change much with respect to V_G or V_{DS} . Assuming that the tunnel junction is roughly triangular; $\xi = (V_G + V_{bi})/w_d$, therefore $d\xi/dV_G = 1/w_d$. The above SS equation can then be rewritten as,

$$SS \approx \left[\frac{1}{V_G} + \frac{(\xi + b)}{(w_d \xi^2)} \right]^{-1} \ln(10) \tag{2.14}$$

As can be seen, there are two terms similar to (2.11). The first term can be seen as extrinsic, since it is only affected by the external application of V_G . The second term involves intrinsic characteristics such as material parameters and device structure/design as well as V_G . Looking at just the extrinsic portion, we can gain a “worst case” scenario where $SS = V_G \times \ln(10)$, shown in Fig. 2.7 (dash dot dot). The SS starts at 0 mV/dec, and rises linearly with a slope of $\ln(10)$. At V_G of 26.06 mV the SS becomes 60 mV/dec; the MOSFET limit. However, when the second term is included in the calculation, (2.14), the SS rises slower and significantly increases

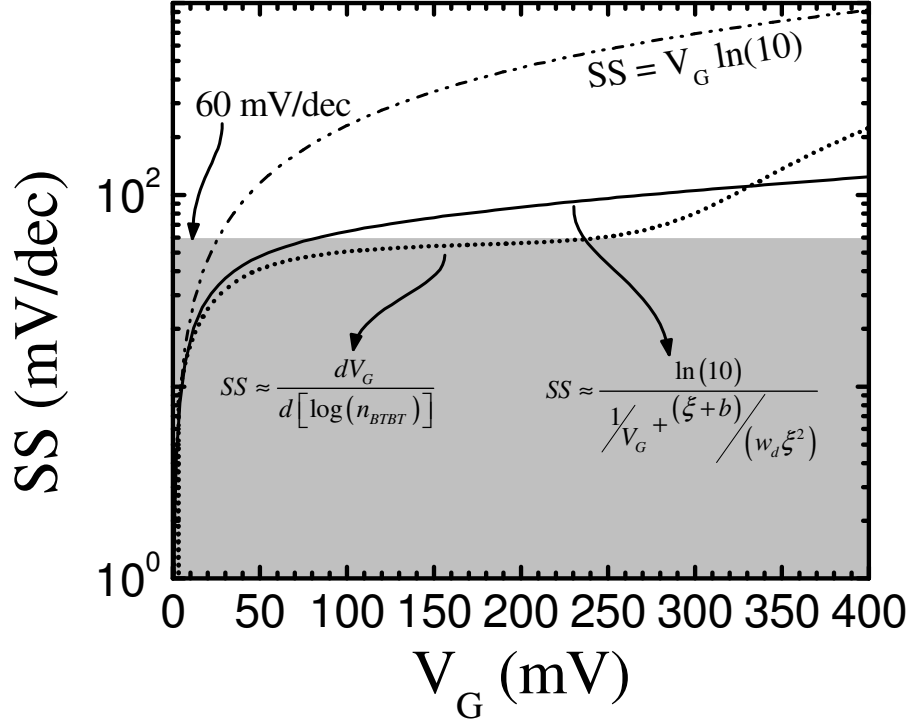


Fig. 2.7: Calculated SS limits of TFETs.

the range of sub-60 mV/dec SS operation, Fig. 2.7 (solid line). The exact change depends on material parameters and device structure (such as doping).

The two different methods presented here are to show that TFETs can achieve SS smaller than MOSFETs. In fact, to achieve sub-60 mV/dec SS, V_G should be minimized for TFETs. Since the goal is to reduce supply voltages, this makes TFETs look very promising for continued scaling. Additionally, it should be noted that the SS calculated here are instantaneous numbers. Meaning, they are valid only at one specific V_G . Of greater importance is the average $SS = (V_{on} - V_{off})/\log(I_{on}/I_{off})$, which will extend the usable V_G for a TFET even further.

There have been many reports of various TFET structures. Typically, experimental reports of TFETs have had poor SS, I_{ON} , I_{OFF} , and/or I_{ON}/I_{OFF} ratios. Table 2.1 lists a handful of experimental TFET results, which have been fabricated in CNT [19], Ge [14], Si [11, 12, 24], and InGaAs [25, 26] materials. However, they all have had small I_{ON} . Some structures have been able to dramatically improve drive currents by increasing V_{DD} above one volt, which is much

Table 2.1: Experimental Reports of TFETs

Study	Year	Material	Best SS			Best I _{ON}			Lg (nm)	Dielec./thickness
			V _{DS} (V)	SS (mV/dec)	I _{on} (μA/μm)	V _{DD} (V)	SS (mV/dec)	I _{on} (μA/μm)		
Appenzeller	2004	CNT	<0.5	40	0.1				200	Al ₂ O ₃ /4 nm
Krishnamohan	2008	Ge	0.5	50	~1	3	~250	300	1,000	SiO ₂ /NA nm
Gandhi	2011	Si	0.1	30	<0.01	1.2	50	~0.1	170	SiO ₂ /4.5 nm
Jeon	2010	Si	-1	46	2.5	-1.5		4.2	20,000	HfO ₂ /0.9 nm
Loh	2010	Si		80		-1	~200	109	56	"highK"/1.1 nm
Mookerjee	2009	InGaAs	0.05	200	0.5	0.75	~300	20	100	Al ₂ O ₃ /10 nm
Zhoa	2010	InGaAs	0.05	86	2	1.05	93	50	100	HfO ₂ /1.2 nm
Mohata	2011	Hetero*				0.75	~750	190	150	Al ₂ O ₃ /HfO ₂ 1/3.5
Dewey	2010	InGaAs	0.05	<60	4.7				150	TaSiO _x /4 nm

greater than target supply voltages (< 0.5 V) for deeply scaled devices. There has not been a reported TFET with a high I_{ON} , low I_{OFF} , and sub-60 mV/dec. SS.

Recall that TFETs can achieve low SS because I_D is dominated by BTBT as the Source/Body junction. The band diagram for that junction (See Fig. 2.6) is similar to that of an ETD (discussed below, Fig. 2.3). With some amount of V_{DD} , an increase in V_G corresponds to a reverse biased ETD with greater n-type doping. Therefore, ETDs are simple structures that can be used to investigate BTBT, calibrate models, and predict TFET characteristics.

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CHAPTER 3

Tunnel Diode Modeling

This chapter discusses the modeling of BTBT characteristics for ETD structures. First, an appropriate BTBT model is chosen after a brief discussion on the merits of several prominent models are examined. As the criteria for selection, the chosen model should be (i) a simplified analytical expression with the (ii) fewest fitting parameters, (iii) forward and reverse bias modeling capabilities, and (iv) applicable to multiple material systems (primarily direct bandgap systems). The chosen model will then be calibrated to experimental results (Chapters 4, 5, and 6), and used for gaining a greater understanding of ETDs. Specifically, identifying quantifiable relationships between J_{BTBT} and material/structural device parameters and determining optimal device structures.

The Kane model [1] will be chosen as the best option, since it most closely satisfies the previously stated criteria. Regardless, the Kane model is still sufficiently rigorous for calculating full BTBT characteristics, and therefore has only been compared to Ge and Si ETD experimental results in a few studies. First, the assumptions, approximations, and general form of the Kane model will be discussed. This is then followed by detailed qualitative and quantitative analysis of each component. Of particular interest is a comparison between the original BTBT probability by Kane and the more common WKB approximation, detailed by Sze, *et al.* [2]. This section concludes with an extensive discussion detailing the calculation and behavior of the overlap integral.

Following the discussions specific to the Kane model, the equations and methods used to accurately calculate degenerate Fermi energies (E_F) is detailed. Accurate E_F values are calculated using a numerical integration technique specifically developed for this work. Results are compared with non-degenerate and super-degenerate approximations, which are used as initial

guesses when determining E_F . Following this discussion, the type of effective mass, and formulas used to average various effective masses together is discussed.

Finally, the chapter discusses the Kane Model Program (KMP) developed for this work. First, the operation and organization of the graphical user interface (GUI) of the program is discussed. Then, the different types of analysis types available are explained, as well as the operation flow that the program uses to perform the calculations.

List of Variables:

e^-, h^+	electrons, holes
q	Magnitude of the charge on an electron
\hbar	Reduced Plank's constant
kT	Thermal energy (Boltzmann's constant & temperature)
ϵ_s, ϵ_r	Dielectric constant, Relative dielectric constant
E_G	Bandgap
m^*	Effective mass
$m_r, m_{r,n}, m_{r,p}, m_{r,BTBT}$	Relative effective mass, electrons, holes, average for BTBT
$m_{r,light}, m_{r,heavy}$	Relative effective mass for light and heavy holes
$E_F, E_{F,n}, E_{F,p}$	Fermi energy, n-side of junction, p-side of junction
$\Delta E_{F,n}, \Delta E_{F,p}$	$E_{F,n} - E_{C,n}$ and $E_{V,p} - E_{F,p}$
$E_C, E_{C,n}, E_{C,p}$	Conduction band, n-side of junction, p-side of junction
$E_V, E_{V,n}, E_{V,p}$	Valence band, n-side of junction, p-side of junction
N_A, N_D, N^*	Acceptor & Donor concentrations, reduced average doping concentration
N_C, N_V	Density of states (DOS) constants for the conduction & valence band
g_C, g_V	DOS energy distributions for conduction & valence bands
$f(E), f_n(E), f_p(E)$	Fermi-Dirac distribution, n-side, p-side

w_d, w_n, w_p	Depletion width, n-side, p-side
ξ	Electric field
V_{bi}	Built-in voltage
V_A	Applied bias
$D, D'(E)$	Overlap integral, integrand of D (differential with respect to energy)
T_{Kane}, T_{WKB}	BTBT probability from E. O. Kane [1], using WKB approximation [2]

3.1. General Discussion on BTBT Models

For the theoretical analysis in this work, an analytical, physics based, expression is desired. It is recognized that TCAD simulations using finite element numerical methods have the potential of providing far more accurate predictions for a much larger range of device structures. However, such models require much greater effort to calibrate with experimental results. On the other hand, closed form analytical expressions are great for (i) quick calculations, (ii) revealing underlying physics and relationships, and (iii) indentifying paths to optimizing and scaling device structure. *Additionally, it is desirable for the model to work with multiple material systems without altering generic fitting parameters, as that mitigates the previous two benefits.* Therefore, models that are relatively complex, or material specific such as those developed for Si and Si/SiGe interband tunnel diodes [3], will not be chosen for this work.

The E. O. Kane model [1], was developed to be a physics based analytical expression for the BTBT behavior of ETDs. It is appropriate for both the forward and reverse bias BTBT characteristics. As with any analytical model, there are a number of reasonable approximations and simplifications made (see Section 3.2). There exists one term, named the overlap integral, which has no closed form solution. However, a detailed qualitative and quantitative analysis simplifies its behavior into three generic forms. With this model, only basic physical and material constants, as well as doping concentrations, are needed to obtain a full direct BTBT J-V

characteristic. Even though it is one of the earliest BTBT models developed, it is the most appropriate for this work for it best fits the previously mentioned criteria.

Another original model was developed by Bergner and Kircher [4]. The author's in [4] were able to achieve excellent agreement between their model and experimental results for low and high electric fields. However, the model is built primarily for determining gate induced BTBT and is comprised of a double integral. Furthermore, within the paper a series of fitted parameters and parabolic fit to the tight binding calculation of the complex band structure for Si were key to the models accuracy. Once again, this model is not appropriate for this work due to the large use of various fitted parameters, which likely change with material systems.

Hurkx, *et al.* [5] and Milovanović, *et al.* [6] based their models directly off of Kane's [1]. In Hurkx, some of the constants (numeric, physical, and material) were combined into generalized constants which need to be determine for each material. Of greater importance is the simplification of the complex overlap integral, described in Section 3.2.3, as V_A . This is a limited approximation, and is not valid beyond very small forward V_A , and sometimes not even for small reverse V_A . As a result, the model will not capture the forward bias characteristics, including J_p and NDR. Milovanović improves the overlap integral approximation to work up to $V_A = 0$ V in most cases. However, the model was not designed, and therefore will not capture J_p and NDR.

Schenk, *et al.* [7] developed a rigorous model primarily for comparing direct BTBT, indirect phonon assisted BTBT, and trap assisted tunneling in Si. The final model form is reported as a tunnel rate function, which is presented as more appropriate for device simulation purposes, and was simplified specifically implementing the complex band structure of Si. Therefore, the J_{BTBT} function presented is still fairly generalized, with over a dozen terms, directional effective masses, wave vector functions, and multidimensional summations. However, the final complex J_{BTBT} formulation was developed out of a direct (zero-phonon) BTBT formulas which the authors admit as agreeing with a form of Kane's model [1]. Given that the

final model is specifically for Si, and the intermediate model is similar to Kane, Schenk's model is inappropriate for the goal's of this work.

In 2004, Solomon, *et al.* [8] reported on a method for determining universal tunneling behavior. The work was specifically geared towards, and analyzed experimental data from Si based structures. However, the method presented could easily be adopted for additional material systems. Each material system would exhibit its own "universal" tunneling behavior. The model simply relates $J_{\text{BTBT}}(V_A)$ to the tunnel barrier width for that V_A . For large doping concentrations and/or fields, an exponential relationship was observed. The additional of a band curvature correction factor improved the exponential relationship over eight orders of magnitude in J_{BTBT} . The model is quite reasonable, and was even used to extract an effective tunnel mass. However, in its present form the model would not capture J_P or NDR, thereby predicting J_{Zener} , and potentially J_{Forward} for very small V_A depending on the device structure and doping concentrations. Therefore, Solomon's model will not be used for calculating BTBT characteristics. It may become useful for developing a more generalized method of extracting material parameters, or even the development of a true universal BTBT model.

An interesting model by Jandiery, *et al.* [9] was developed to look at the ability of controlled mid-bandgap states enhancing the BTBT current density of an ETD. This may be a useful way to improve TFET drive currents, similar to intermediate band [10] and Quantum dot [11, 12] solar cells. However, it may also turn out that a TFET implementing midgap states would have unmanageable I_{Off} . In this work, ideally the tunnel junctions are formed with high quality epitaxy, with a negligible density of midgap states. Therefore, the model will not be pursued in this work.

3.2. Kane Model: Assumptions, Approximations, and Form

The E. O. Kane model, as described in [1], is the main physics based method for predicting the BTBT current densities of ETDs in this work. The model was developed shortly after the initial discovery of the ETD by Esaki in 1957 [14]. However, over the years the model has rarely been matched with experimental data, and typically only J_p . Furthermore, application of the model has been obscured by gross approximation of one of the major terms in the model [5, 6, 15] and inaccurate reproduction of the BTBT probability term [2, 15], both of which are discussed in sections 3.2.3 and 3.2.2, respectively.

As with any analytical model, several assumptions and approximations were made in its development. There have been many attempts to generalize the model [5-7, 16], potentially increasing its accuracy over a larger design space. This work concentrates on the most basic form, discussed in Section 3.2.1 (Eq. (3.1)). In this version, the E-k band valleys and maximums are assumed to be perfectly parabolic resulting in a constant m_r DOS.

The 2nd order derivative, and therefore m_r , does change as one moves away from the band

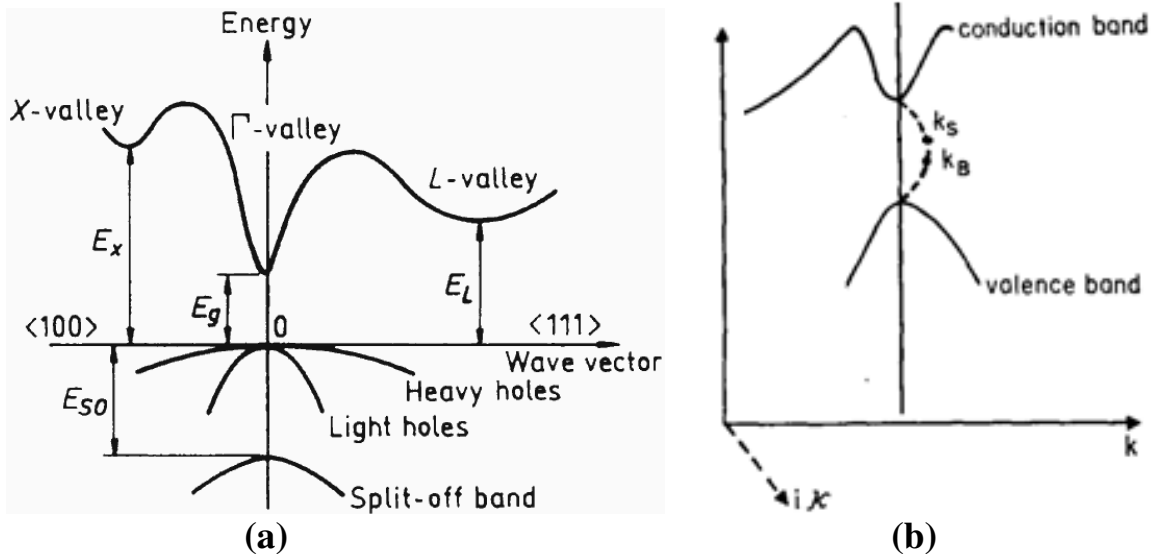


Fig. 3.1: Left (a), Generic E-k diagram indicating direct bandgap (Γ -valley), indirect bandgaps (L- and X-valleys), and light-, heavy-, and split-off holes (adopted from [13]). Right (b), generic E-k diagram showing parabolic tunneling path through imaginary k -space that carriers travel when through the forbidden bandgap (adopted from [1]).

minimums and maximums. However, generally the changes are fairly minor until one moves far from these points. Additionally, with very large doping the L- and X-valleys (shown in Fig. 3.1a) begin filling with e^- , limiting further increases $E_{F,n}$.

As indicated above, the material systems used are assumed to have a direct bandgap (Γ -valley), similar to Fig. 3.1a. Additionally, the vast majority of BTBT current is generated at the direct bandgap. Specifically, BTBT occurs between the Γ -valley and maximum in the conduction and valence bands of the n- and p-sides of the p-n junction, respectively. This is known as the “2-bands” approximation. Furthermore, the tunneling path through the forbidden bandgap is approximated as parabolic in shape, along the imaginary k-space as shown in Fig. 3.1b.

If additionally band are occupied (L- and X-valleys), typically their m_r and E_G are much larger than the direct gap. Combined with the need for a momentum shift in k-space, usually through phonon or photon interactions, the BTBT probabilities between these extra bands are generally negligible. Therefore, the $m_{r,BTBT}$ is an average of the conductivity $m_{r,e}$ and $m_{r,h}$ along $k(\Gamma)$.

The doping profiles are assumed to be perfectly square, fully activated, adjacent to each other, and fully-depleted. However, as a simplification of the BTBT probability, the tunnel barrier formed by the forbidden bandgap (Fig. 3.2) is assumed to be triangular as determined with a height of E_G and slope of ξ . Where ξ (average electric field) is the built in bias scaled by the applied bias, linearly dropped over the entire depletion width. In other words, it is the average electric field over the entire depletion width of the p-n junction.

3.2.1. Kane Model Equation

The Kane model, (3.1), can be separated into three terms. The pre-factor (first term) is a function of physical and material constants as well as ξ in (3.2), whose magnitude changes with

V_A and the reduced average doping (N^*) as defined by (3.4). As previously mentioned, ξ is approximated as a constant and defined by the magnitude of $(V_{bi}-V_A)/w_d$, which is represented in the band diagram in Fig. 3.2. Equation (3.3) is the depletion width calculated using the full depletion approximation of two square doping profiles with no i -layer in the middle of the p-n junction. This term is always positive, but it does attenuate the BTBT current density in forward bias and enhances it in reverse bias (Fig. 3.3a left y-axis).

$$J_{BTBT} = \frac{q\xi}{36\pi\hbar^2} \sqrt{\frac{2m^*}{E_G}} \times D \times \exp\left(-\frac{\pi\sqrt{m^*} E_G^{3/2}}{2\sqrt{2}\hbar\xi}\right) \quad (3.1)$$

$$\xi = \frac{V_{bi}-V_A}{w_d} = \sqrt{\frac{q(V_{bi}-V_A)}{2\epsilon_s} N^*} \quad (3.2)$$

$$w_d = \sqrt{\frac{2\epsilon_s(V_{bi}-V_A)}{qN^*}} \quad (3.3)$$

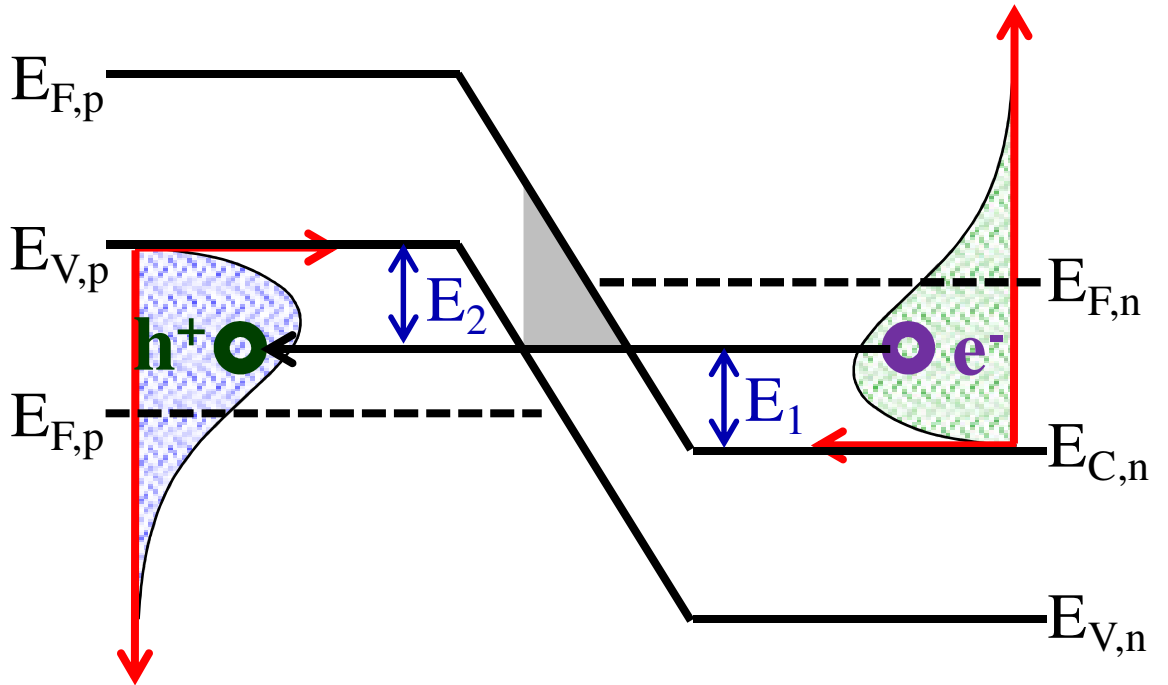


Fig. 3.2: Sketch of ETD band diagram with simplified, triangular depletion region. This is the idealized shape of the bands used in the Kane model.

$$N^* = \frac{N_A N_D}{N_A + N_D} \quad (3.4)$$

The second term is the overlap integral (D) and accounts for the degree of overlapping carrier distributions, which provides the actual current flow. Fig. 3.2 shows the generic band diagram of an ETD biased just prior to V_p . Due to the forward bias, there are a large number of electrons in the conduction band (right hand side) whose energy aligns with a similarly large quantity of holes (empty states) in the valence band (left hand side). This overlap of carrier distributions has provided an imbalance of electrons, which are free to tunnel through the bandgap (approximated as triangular) and into an empty states (holes) on the other side of the junction. As such, a BTBT current is generated. For the situation shown in Fig. 3.2, the current flows from right to left. However, in the Zener direction electrons in the valence band on the p-side will tunnel into hole states in the conduction band of the n-side, this reversing the current flow. Therefore, D handles the availability of carriers (electrons and holes) for BTBT and

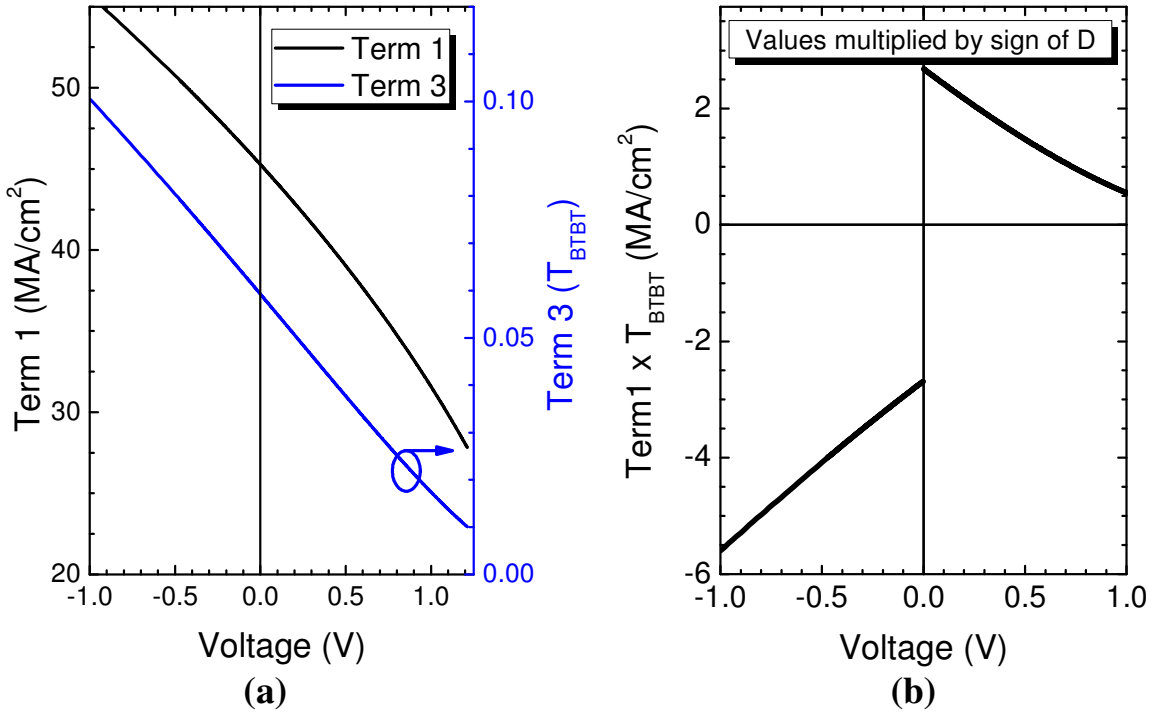


Fig. 3.3: Left (a), plot of the pre-factor on the left axis and T_{Kane} on the right axis. Right (b), pre-factor and T_{Kane} multiplied together as well as the sign of D to account for the direction of current flow.

dictates the direction of current flow. The complexity of D is symbolically and quantitatively discussed in sections 3.2.3 and 3.2.3.1.

The final term (the exponential) represents the BTBT probability associated with carriers tunneling through the forbidden bandgap. Similar to the pre-factor, the exponential is a function of physical and material constants, as well as ξ . As before, decreasing N^* or increasing V_A decreases BTBT current density (Fig. 3.3a right y-axis). However, J_{Kane} is naturally more strongly related with the exponential (BTBT probability), and therefore will tend to change exponentially with N^* and N_A . Furthermore, the pre-factor and exponential continually decreases with $\sqrt{V_{bi} - V_A}$ which, by themselves, would turn the entire forward J-V characteristics into NDR (Fig. 3.3b). Therefore, it is the behavior of D that causes J_{Kane} to initial increase, form a peak, and then decreasing (NDR) as V_A in forward bias. In other words, it is the overlap of carrier distributions on either side of the tunnel junction that is primarily responsible for the ETDs unique “N” shape characteristic in forward bias. The other terms are shaped by material parameters and biasing conditions, which primarily manipulate the magnitude of the various regions of the ETD J-V characteristic.

3.2.2. Common BTBT Probability Error

It has become common to calculate T_{BTBT} directly from the WKB approximation [1, 15] as in (3.5). Just like Kane’s original formulation, the ξ is assumed to be constant and triangular over the full depletion width. As per WKB, the absolute value of the wave vector ($k(x)$) is integrated over the classical turning points $x = 0$ to E_C/ξ (the tunnel barrier width). The tunnel barrier potential is the shaded triangular region in Fig. 3.2, with a slope of ξ , and y-intercept of E_e . (same as the tunnel electron). Therefore, the waver vector for the electron is (3.6). Performing the integral provides (3.7), which is similar the exponential term in (3.1).

$$T_{WKB} \approx \exp \left(-2 \int_0^{E_G/\xi} |k(x)| dx \right) \quad (3.5)$$

$$k(x) = i \sqrt{\frac{2m^*}{\hbar^2} [U(x) - E_{e^-}]}; \quad U(x) = \xi x + E_{e^-} \quad (3.6)$$

$$T_{WKB} \approx \exp \left(-\frac{4\sqrt{2m^*} E_G^{3/2}}{3\hbar\xi} \right) \quad (3.7)$$

The only differences between Kane's model and the WKB approximation end up in T_{WKB} and T_{Kane} , as shown in (3.8). Specifically, the numerical constants in T_{WKB} turn out to be ~70% larger than T_{Kane} , (3.9). Since this difference resides within an exponential, there can be very large discrepancies between the two models. For instance T_{Kane}/T_{WKB} for GaAs with an E_G on 1.42 eV, m_r of 0.54, and an ξ as low as 1.13×10^8 V/m ($N^* = 1 \times 10^{19}$ /cm³) would be ~18,000x. As the Current density increases, by increasing N^* to 2.5×10^{19} /cm³, the ratio decreases to ~250x. Moving towards a material system (InSb) with a smaller bandgap (0.18 eV) and m_r (0.019) reduces the ratio to 1.4x and 1.2x for the same doping concentrations. *In other words, the WKB approximation version of the model can substantially underestimate J_{BTBT} with respect to the original Kane model.* If one version of the model is more accurate than the other, it will become very apparent at low BTBT current densities, even if they both match well for very large current densities.

$$T_{Kane} = \exp \left(-\frac{\pi\sqrt{m^*} E_g^{3/2}}{2\sqrt{2}\hbar\xi} \right) \neq \exp \left(-\frac{4\sqrt{2m^*} E_g^{3/2}}{3\hbar\xi} \right) = T_{WKB} \quad (3.8)$$

$$\frac{\pi}{2\sqrt{2}} \approx 1.1107 \neq 1.8856 \approx \frac{4\sqrt{2}}{3} \quad (3.9)$$

3.2.3. Overlap Integral

The overlap integral, D in (3.10), accounts for the degree of overlapping carriers which provides the actual current flow. This takes place in the energy space above $E_{C,n}$ and below $E_{V,p}$, primarily between $E_{F,n}$ and $E_{F,p}$, which is depicted in Fig. 3.2. As dictated by Fermi-Dirac statistics, within this region most of the conduction band states are filled with electrons, which are free to tunnel through the bandgap into the largely empty states on of the p-side of the junction. Above $E_{F,n}$ and $E_{F,p}$, the majority of states are empty (filled with holes) on both sides of the junction and therefore there are few electrons available for tunneling. Conversely, below $E_{F,n}$ and $E_{F,p}$ there are very few states for readily available electrons to tunnel into.

$$D = \int_{E_{C,n}}^{E_{V,p}} [f_n(E) - f_p(E)] \left[1 - \exp\left(-\frac{2E_s}{E}\right) \right] dE \quad (3.10)$$

The overlap integral,(3.10), is the product of two separate terms. The first term is the difference between the Fermi-Dirac distributions, as defined in (3.11), on the n- and p-sides of the junction. This is the term that specifically accounts for the distribution of electrons and holes (empty states). The greatest imbalance between $f_n(E)$ and $f_p(E)$ occurs between $E_{F,n}$ and $E_{F,p}$, with a maximum value of one reached within a few kT of $E_{F,n/p}$. Outside of this region, the first term reduces to ~ 0 after a few kT . After a small reverse bias, the integral of the first term will increase at the same rate as V_A . In forward bias there will be an initial rise in D , until $E_{C,n}$ is less than $E_{F,p}$ when $\Delta E_{F,p} \gg \Delta E_{F,n}$, or $E_{V,p}$ is greater than $E_{F,n}$ when $\Delta E_{F,n} \gg \Delta E_{F,p}$. When one of the previous conditions are met, the integral of $f_n(E) - f_p(E)$ becomes pegged at a constant value by the smaller of $\Delta E_{F,p}$ or $\Delta E_{F,n}$, causing D to flatten out into a mesa type shape (discussed in 3.2.3.1, Fig. 3.4). When a very large V_A is applied, eventually $E_{F,n}$ will begin to drop below $E_{V,n}$ and $E_{F,n}$ will starts to rise above $E_{C,n}$. In this regime, the bounds of the integral directly impact the sum of $f_n(E) - f_p(E)$ between $E_{C,n}$ and $E_{V,p}$, thereby decreasing the output of D to 0 eV when $E_{C,n}$ equals $E_{V,p}$. In forward bias, $E_{F,n}$ is greater than $E_{F,p}$, allowing for electrons to tunnel from right to left and

providing positive current flow. In reverse bias, $E_{F,p}$ is greater than $E_{F,n}$, causing electrons to tunnel for left to right and providing a negative current flow.

$$f_{n/p}(E) = \frac{1}{1 + \exp\left(\frac{E - E_{f,n/p}}{kT}\right)} \quad (3.11)$$

$$\bar{E} = \frac{\sqrt{2}\hbar\xi}{\pi\sqrt{m^*E_G}} \quad (3.12)$$

The second term is an attenuation factor, where E_S is the smaller of E_1 and E_2 and always positive, as defined in Fig. 3.2. Additionally, \bar{E} is always positive and decreases as V_A increases due to its relation with ξ as shown in (3.12). Consequentially, the second term ranges between zero and one (unitless), depending on material parameters and biasing condition. The maximum value of E_S increases with doping and is linearly related to $-V_A$, whereas \bar{E} is related to $(V_{bi} - V_A)^{1/2}$. Therefore, E_S has a faster effect on the second term. Since E_S has a larger influence than \bar{E} , the second term will quickly approach a value of one in reverse bias. Consequentially, for large reverse bias and sometimes for small forward/reverse biases, both terms approach unity at energies between $E_{F,n}$ and $E_{F,p}$. Therefore, D increases at the same rate as the first term, which will increase the same as V_A ($D \approx V_A$). At forward V_A , E_S does not increase as large or fast with respect to \bar{E} , thereby attenuating the first term.

$$D(V_A) \approx \Delta E \sum_{n=0}^N \left[f_n(E_n) - f_p(E_n) \right] \left[1 - \exp\left(-\frac{2E_S(E_n)}{\bar{E}(E_n)}\right) \right] \quad (3.13)$$

$$E_n = n \times \Delta E = n \times \frac{V_{bi} - V_A - E_G}{N} \quad (3.14)$$

As previously mentioned, the overlap integral does not have a closed form solution. Therefore, D is calculated using rectangular numerical integration as defined in (3.13). The energy range of interest ($E_{C,n} \rightarrow E_{V,p}$) is divided into 500 (N) equal step sizes (ΔE) as defined in (3.14). Furthermore, D must be calculated for all V_A of interest.

3.2.3.1. Detailed Behavior of Overlap Integral

There are three basic shapes that D may exhibit, shown in Fig. 3.4; (i) simple cone, (ii) Simple mesa or trapezoidal, and (iii) complex mesa. The final shape obtained depends on the ratio of $E_{F,n}; E_{F,p}$. To simplify the analysis, the examples in this section assume $m_{r,e} = m_{r,p} = 0.1$, with a tunneling m_r of 0.065. Consequentially, the electron and hole DOS are the same at $7.94 \times 10^{17} / \text{cm}^3$. Therefore, with this fictitious material system, changes in N_A and N_D affect $E_{F,p}$ and $E_{F,n}$ to the same degree. E_G and ϵ_r were taken as the average of several common III-V compound semiconductors; (i) 0.67 eV and (ii) 15.14, respectively.

The simplest shape is cone-like, which occurs when $E_{F,n} \approx E_{F,p}$ ($N_D = N_A$ in Fig. 3.4). The dashed line is the ideal shape of D when the 2nd term in (3.10) is approximated as one. For V_A less than the peak value ($\sim V_{bi} - E_G$), D is approximately equal to V_A for both cases. As expected, the ideal case (dashed line) peaks at $(V_{bi} - E_G)/2$, then drops off to zero at $(V_{bi} - V_A)$ with a slope of -1. The rounded top is purely due to thermal spread in the Fermi-Dirac statistics. For the real

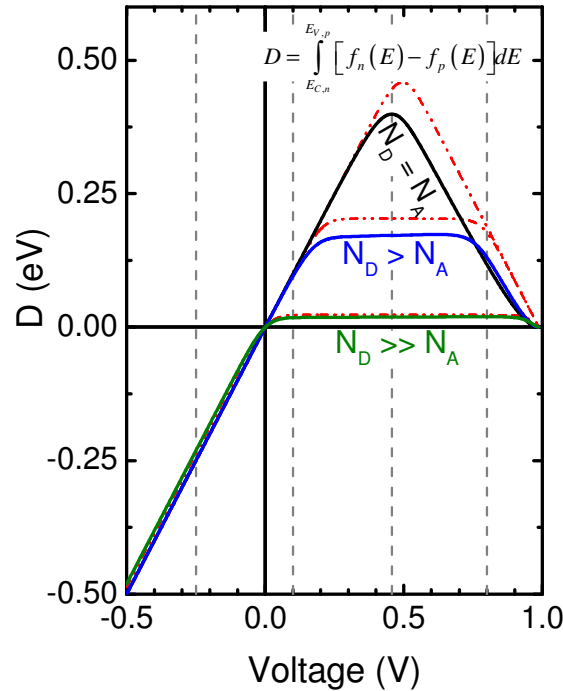


Fig. 3.4: Overlap integral for three different situations; (i) cone, (ii) simple mesa, and (iii) complex mesa shapes. The dash-dot-dot lines are idealized D characteristics.

D (solid line) characteristic, the 2nd term begins to significantly dampen the final values shortly before the peak. This has the effect of reducing the maximum peak, and shifting it slightly to the left. The post peak slope is still -1 until shortly before D reaches zero.

In Fig. 3.5, the 1st and 2nd terms comprising D are plotted for V_A of (a, e) -0.25 V, (b, f) 0.1 V, (c, g) 0.457 V, and (d, h) 0.8 V. The left hand portion of each plot constructs the 1st term involving f_{np} . The right hand portion plots the 1st and 2nd terms (solid lines) as well as the combined value ($D'(E)$) which is designed by the “*” symbols. *The area of the shaded region, bounded by $D'(E)$, is the final value of D for the given V_A .* To the right of each plot are representative band diagram sketches with appropriately scaled carrier distributions.

For V_A of -0.25 V (Fig. 3.5a, e), the BTBT current is generated symmetrically between $E_{V,p}$ and $E_{C,n}$. The first term reaches its maximum (~ 1) exactly in the middle of the bands, which corresponds to an equal match in e^- and h^+ concentrations. The entire 1st term fits within the region of the 2nd term that is ~ 1 , and therefore does not play a significant role in D . Consequentially, the actual D value is equivalent to the ideal case. Additionally, it is the e^- distribution in the p-side and the h^+ distribution in the n-side that provide the BTBT currents. This is opposite to the standard orientation expected in forward bias.

At a small forward bias of 0.1 V (Fig. 3.5b, f) there is only a small region of energies that provide BTBT. Additionally, within energy range the carrier distributions do not reach full occupancy of available states due to f_{np} . However, the 1st term still fully resides within the 2nd term, and therefore D continues to increase with V_A . This trend continues until near the peak (Fig. 3.5c, g), at which time the 2nd term begins to restrict $D'(E)$, and attenuate the final value. As $E_{F,np}$ approach the bandgap edges (according to kT and f_{np}), the 2nd term begins to “cut-off” the Fermi distribution tails. Notice that the maximum carrier distributions are not fully aligned. After $E_{F,np}$ are a few kT beyond the bandgap edges the carriers will fully occupy the available states, 1st will equal one, and $D'(E)$ will become fully defined by the 2nd term, as shown in Fig. 3.5d, h.

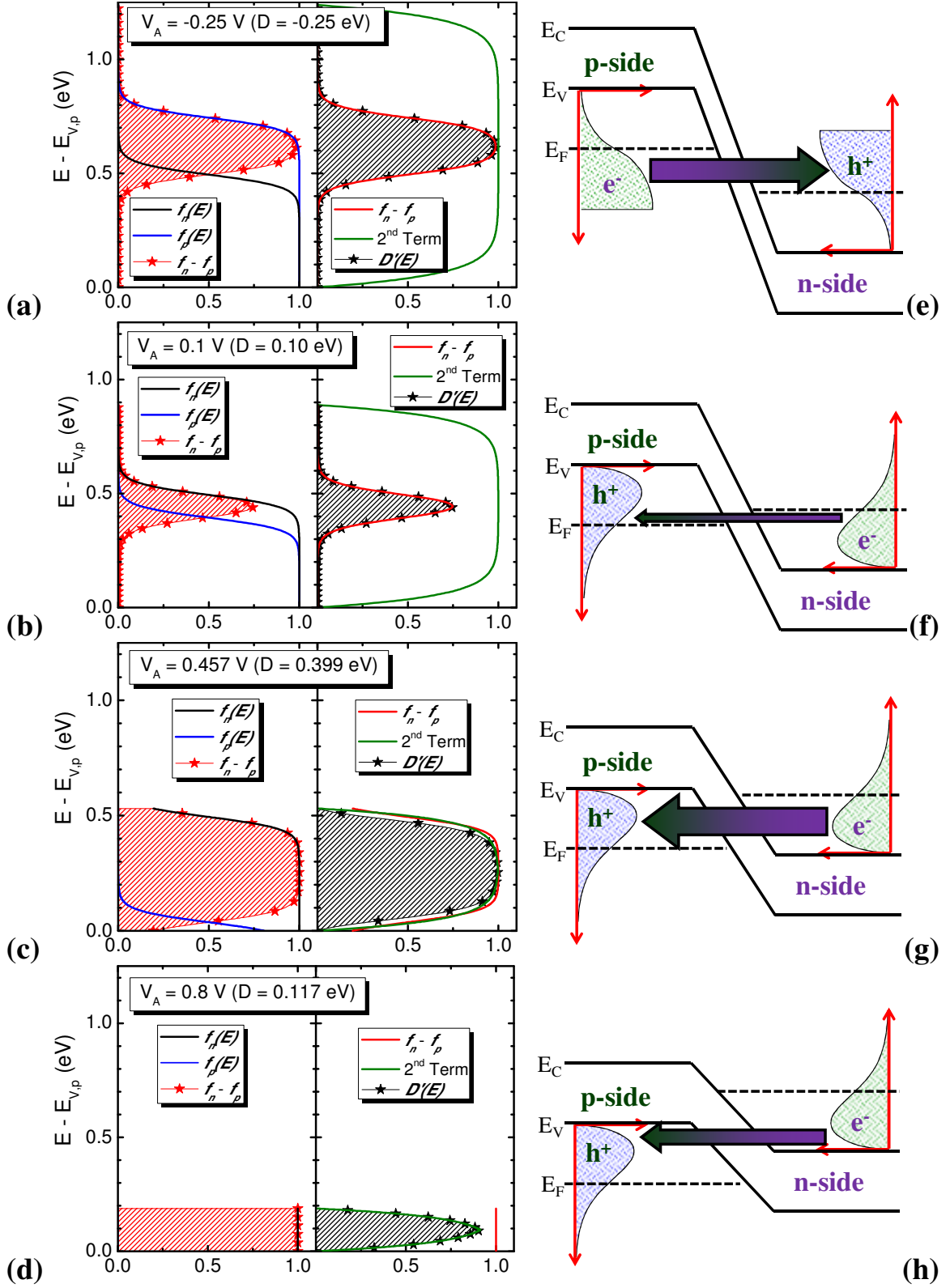


Fig. 3.5: Graphical representation of overlap integral calculations for $N_D = N_A$ ($E_{F,n} = E_{F,p}$) for V_A of (a) -0.25 V, (b) 0.1 V, (c) 0.457 V, and (d) 0.8 V. (e-h) Respective band diagram sketches for each biasing conditions shown to the right.

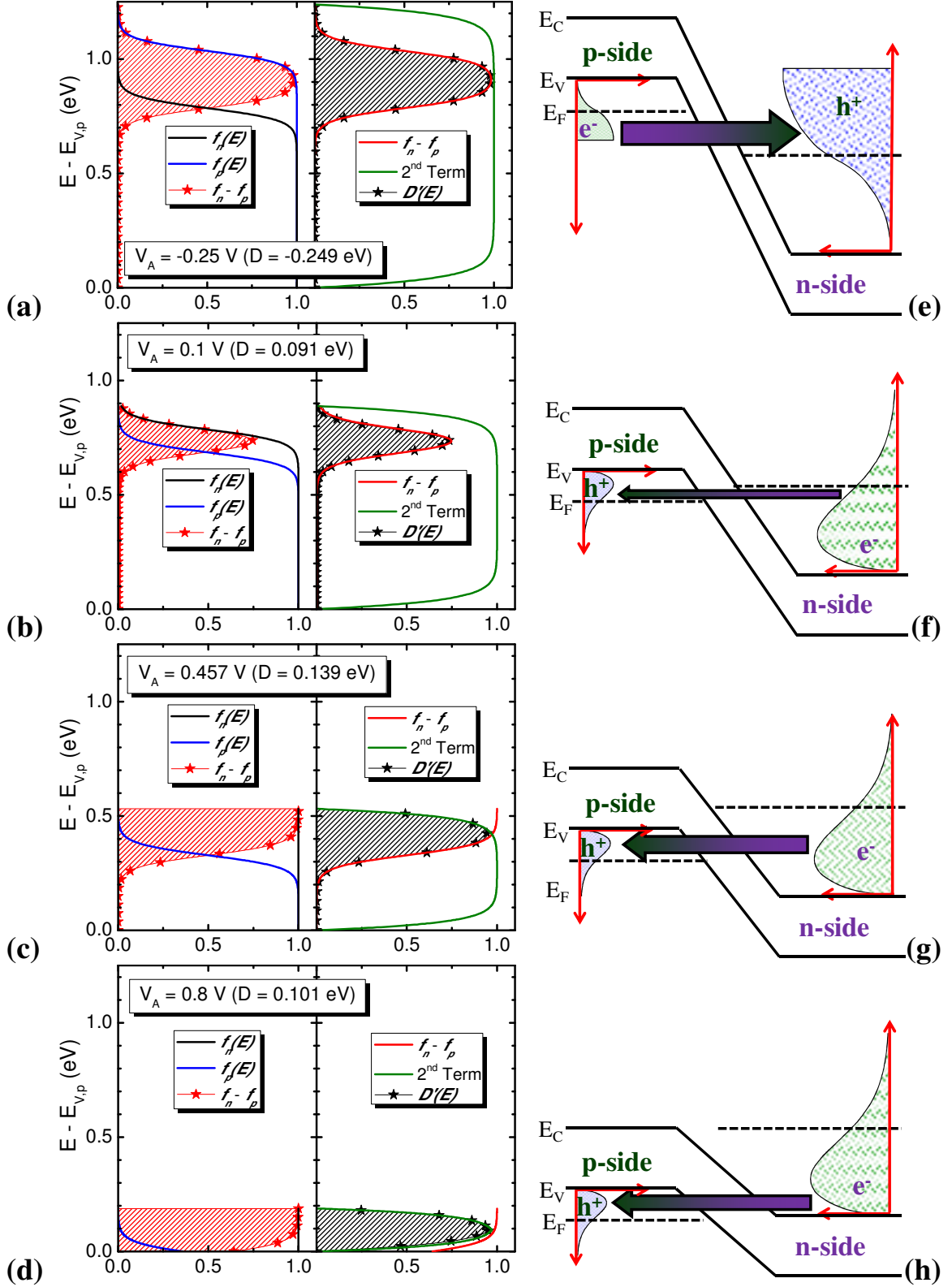


Fig. 3.6: Graphical representation of overlap integral calculations for $N_D > N_A$ ($E_{F,n} > E_{F,p}$) for V_A of (a) -0.25 V, (b) 0.1 V, (c) 0.457 V, and (d) 0.8 V. (e-h) Respective band diagram sketches for each biasing conditions shown to the right.

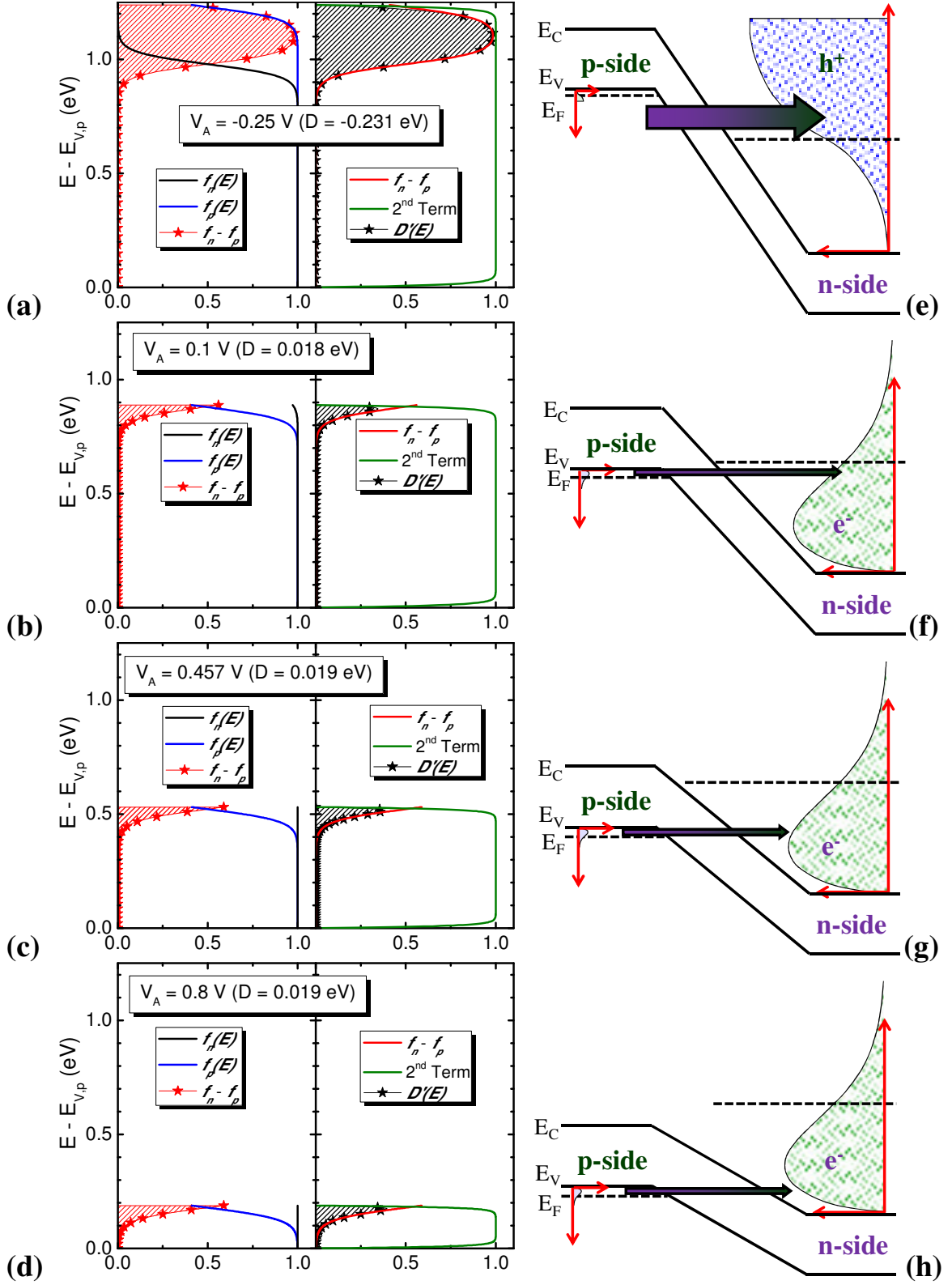


Fig. 3.7: Graphical representation of overlap integral calculations for $N_D \gg N_A$ ($E_{F,n} \gg E_{F,p}$) for V_A of (a) -0.25 V, (b) 0.1 V, (c) 0.457 V, and (d) 0.8 V. (e-h) Respective band diagram sketches for each biasing conditions shown to the right.

The second basic shape in Fig. 3.4, a simple mesa or trapezoidal, occurs when $E_{F,p}$ is significantly smaller than $E_{F,n}$ ($N_D > N_A$). Note, that this behavior is fully reversible between the $E_{F,n}$ and $E_{F,p}$. Before D flattens out, it is approximately equal to V_A , similar to the previous case studied. Shortly before V_A reaches the value of $E_{F,p}$, D begins to deviate from the previous trend. After a little further, the ideal D (dashed line) reaches its maximum value a flat mesa). As with the previous case, introducing the 2nd term attenuates that maximum value. Additionally, the mesa has a slight, positive slope. Eventually D begins to decrease with a slope of -1, and is approximately the same value and shape as the previous case. Notice the mesa portion of D is roughly symmetrical around the peak biasing condition of the cone shape.

As with the cone shape, Fig. 3.6 shows plots detailing the structure of $D'(E)$, along with their respective band diagram sketches for the same biasing conditions as before. In the band diagrams, notice that the shift in $E_{F,p}$ towards $E_{V,p}$ moves the 1st term closer to the band edge. For the first biasing condition in Fig. 3.6a, e, the 1st term is far enough away from the band edge such that the 2nd term does not affect it. As a result, the reverse bias characteristic looks the same the previous case.

For small forward bias (Fig. 3.6b, f), the 1st term is still confined within the 2nd. However, once $E_{F,n}$ is close to $E_{V,p}$, the 2nd term will begin to “clip” the 1st term’s composite Fermi distribution, limiting further increases in D . This is evident in Fig. 3.6c, g. Looking at the band diagram, one can clearly identify that the BTBT current is limited by the region between $E_{V,p}$ and $E_{F,p}$. Further increases in V_A shift the p-side down, but do not increase the region of BTBT. However, this BTBT region becomes align with larger e^- concentrations, providing a small boost in D . Eventually V_A is large enough that $E_{F,p}$ shifts below $E_{C,n}$, and the BTBT region is once again bounded by both band edges (Fig. 3.6d, h). Quickly, $D'(E)$ is dominated by the 2nd term, and behaves similarly to the previous case.

The final shape is being called a complex mesa. In this case, $E_{F,p}$ is much smaller than $E_{F,n}$ ($N_D \gg N_A$), shown in Fig. 3.4. At first glance, it looks the same as the simple mesa shape,

Table 3.1: Doping parameters, Fermi energies, and calculated D values used for detailed analysis considering (i) cone, (ii) mesa, and (iii) complex mesa shapes using fictitious mater parameters.

	Constant V_{bi} for all conditions (1.66 V)								
	N_D ($\times 10^{19} \text{ cm}^{-3}$)	N_A ($\times 10^{19} \text{ cm}^{-3}$)	$\Delta E_{F,n}$ (eV)	$\Delta E_{F,p}$ (eV)	$D(V_P)$ (eV)	$D(-0.25 \text{ V})$ (eV)	$D(0.1 \text{ V})$ (eV)	$D(0.46 \text{ V})$ (eV)	$D(0.8 \text{ V})$ (eV)
Cone	5	5	1.16	0.494	0.373	-0.250	0.100	0.399	0.117
Mesa	10	1.34	1.45	0.203	0.158	-0.249	0.0957	0.172	0.130
Complex Mesa	13.91	0.08	1.650	0.0093	0.0157	-0.231	0.0178	0.0188	0.0194

only with a smaller maximum value due to its smaller N_A ($E_{V,p} - E_{F,p}$). However, after a small amount of reverse bias, D becomes equal to $V_A - \Delta eV$ (~ 0.02 eV for this example). The cause of this deviation from the previous cases is visible in Fig. 3.7. $E_{F,p}$ is close enough to its own band edge ($E_{V,p}$), such that f_p is permanently clipped by the band edge. Therefore, no matter how large the reverse bias gets (Fig. 3.7a, e), D will always be missing that portion of the 1st term. As a result, D will increase with a slope of ~ 1 , but will be shift by an amount roughly equal to that portion of the 1st term clipped by $E_{V,p}$. The forward bias characteristics behave similarly to the basic mesa condition. The mesa width is still roughly centered around the cone peak, and is much wider and smaller in height due to the large disparity between $\Delta E_{F,p}$ and $\Delta E_{F,n}$.

The doping concentrations used, Fermi energies, and calculated D values for the previous examples are summarized in Table 3.1. For the complex cone, the ΔeV shift in the reverse bias D characteristics is simply calculated as $V_A - D(V_A)$. Doping concentrations were varied such that V_{bi} and $\Delta E_{F,n} + \Delta E_{F,p}$ remained constant to help elucidate the previously discussed properties. Given that the negative slope of the exponential and its 1st coefficient in the Kane model (3.1) (Fig. 3.3b) is fairly shallow, V_P is close to the V_A at which D has mostly leveled off. For the cone shape, this occurs just before the peak. For both mesa shapes, this typically occurs within a few kT of the smaller of $\Delta E_{F,p}$ and $\Delta E_{F,n}$.

3.3. Fermi Energy Calculations

Since ETDs require degenerate levels of doping E_F must be calculated in a rigorous manner for accurate results. Traditionally, the total carrier concentration (3.15) is calculated from the integration of $g_C(E)$, (3.16), and $f(E)$, (3.17), product. The dimensions of the ETDs considered in this work will not quantum mechanically confine the transport carriers. Therefore, it is appropriate to use the 3D density of states distribution function shown in (3.16). The following discussion is specifically written for electrons (n). However, the equations can be made equally valid for holes by substituting (i) m_e with m_h , (ii) E with $-E$, (iii) E_C with $-E_V$, (iv) E_F with $-E_F$, and (v) integrate from $-\infty$ to E_V .

$$n = \int_{E_C}^{\infty} g_C(E) \times f(E) dE \quad (3.15)$$

$$g_C(E) = \frac{8\pi\sqrt{2}m_e^{3/2}}{h^3} \sqrt{E - E_C} \quad (3.16)$$

$$f(E) = \frac{1}{1 + \exp\left[\frac{E - E_F}{kT}\right]} \quad (3.17)$$

By introducing three substitutions, (3.15) can be generalized over all material systems and temperatures; where (i) x is defined by (3.18), (ii) β is defined by (3.19), and (iii) y is defined by (3.20). Wherein N_C is the standard DOS, defined in (3.21).

$$x = \frac{E_C - E_F}{kT} \quad (3.18)$$

$$\beta^2 = \frac{E - E_C}{kT} \quad (3.19)$$

$$y = \frac{\sqrt{\pi n}}{4N_C} \quad (3.20)$$

$$N_C = 2 \left(\frac{2\pi \times kT \times m_e^*}{h^2} \right)^{3/2} \quad (3.21)$$

In the new form, (3.22), relates the material parameters (y) to the integral of a new function (F) with parameters x and β . As before, this new form still has no closed form solution. Therefore, it can only be solved numerically for with limited approximations. However, a table of numerical solutions can be generated without knowledge of material parameters or temperature. This is accomplished by assuming a value for x and then numerically integrating $F(x,\beta)$ to determine the corresponding value for y . Afterwards, with a given material system and doping concentration, y is easily computed then looked up in the pre-generated table for the corresponding x value. Finally, using the desired temperature and (3.18), E_F is easily calculated. For improved accuracy, linear interpolation was used in the table lookup process.

$$y = \int_0^{\infty} F(x, \beta) d\beta = \int_0^{\infty} \frac{\beta^2}{1 + \exp[x + \beta^2]} d\beta \quad (3.22)$$

Simpsons rule was used to numerically integrate $F(x, \beta)$, as shown in (3.23). Where N is the total number of discrete integration steps, and $\Delta\beta$ is the step size as defined by (3.24). β_{Max} is the maximum value of β needed to accurately capture the entire integral. Above β_{Max} , the contribution of $F(x, \beta)$ is assumed to be negligible. For this work, β_{Max} was set to 10 and 500 steps were used. In other words, $E-E_C$ up to 100 eV was calculated at 2 meV steps. For rare occurrences when x is less than -90, β_{Max} was doubled to 20. These parameters yield reliable and accurate results.

$$y \approx \frac{\Delta\beta}{6} \sum_{n=1}^N F[x, 2(n-1)\Delta\beta] + 4F[x, (2n-1)\Delta\beta] + F[x, (2n)\Delta\beta] \quad (3.23)$$

$$\Delta\beta = \frac{\beta_{Max}}{N} \quad (3.24)$$

When there is non-degenerate levels of doping, $(E_C-E_F)/kT$ is less than three, $f(E)$ can be approximated as a simple exponential. Consequently, y can be approximated as (3.25), which has a familiar closed form solution. A value for x , and therefore E_F , can be directly computed from

(3.26). For $E_C - E_F = 3kT$ ($x = 3$), the approximated E_F is 0.58% less than the actual value. For added accuracy this work uses the approximation at $E_C - E_F = 6kT$ ($x = 6$), which has an error of less than 0.015%.

$$y \approx \int_0^{\infty} \beta^2 \exp(-x - \beta^2) d\beta \quad (3.25)$$

$$x = -\ln \left[\left(\frac{4}{\sqrt{\pi}} \right) y \right] \quad (3.26)$$

A separate approximation can be made with extremely large levels of doping, which will be designated as super-degenerate. In this situation, the rate in change of $g_C(E)$ near E_F is very slow (almost flat). Consequentially, the number of electrons above E_F is approximately equal to

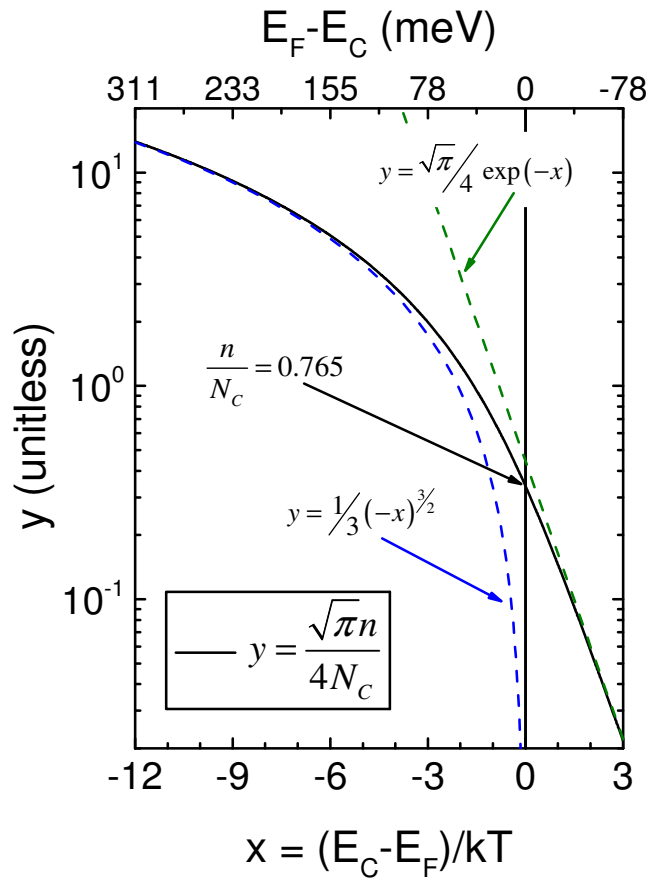


Fig. 3.8: Plot of y vs. x used to determine E_F from a given doping density and DOS. The solid line is from numerical evaluation of the carrier-energy distribution function. Dashed lines are approximations of non-degeneracy (right) and super-degeneracy (left).

the number of empty states below E_F (i.e. not filled due to Fermi-Dirac statistics). Another way to look at it is, the range needed for $f(E)$ to transition from ~ 1 to ~ 0 is negligible. Therefore, only $g_C(E)$ needs to be integrated from E_C to E_F , similar to the case at absolute zero ($T = 0$ K). The integral becomes (3.27), with closed form solution of (3.28). Super-degeneracy occurs at $E_C - E_F \approx -12kT$ ($x = -12$), with a 0.57% over-estimate of E_F . For this work, super-degeneracy was only used as an initial guess when looking up values in the pre-generated table.

$$y \approx \int_0^{\sqrt{-x}} \beta^2 d\beta \quad (3.27)$$

$$y = \left(\frac{1}{3}\right)(-x)^{3/2} \quad (3.28)$$

The solid line in Fig. 3.8 is a plot of y versus x as calculated numerically using (3.23), for the region of low to medium degeneracy. Also shown are the super degeneracy (dashed line on the left) and non-degeneracy (dashed line on the right) approximations. As can be seen, the solid line approaches the approximations for both the left and right hand extremes. The greatest error occurs for x between negative six and one, which covers a large range of doping conditions for ETDs. Additionally, E_F will equal E_C when N_D equals 76.5% of N_C , or approximately 3/4. With the methods and equations described above, accurate degenerate E_F values can be calculated, which is necessary for the Kane model and accurate band diagram calculations.

3.4. Relative Effective Mass Parameters

It is important that appropriate effective mass values are used when calculating the various parameters needed for the Kane model. For all E_F calculations, the DOS m^* is used. Typically these values are taken from measured values in literature [13]. Since there are generally two (light and heavy holes) valance band maximums centered at 0 eV in the Γ direction, they are typically averaged together using (3.29). Given the type of average used, the DOS for h^+ will be dominated by $m_{r,heavy}$, as one would expect. The split-off valance maximum is

ignored in this work. However, the split-off band may significantly impact $E_{F,p}$ with large enough N_A , but tunneling to that band will be negligible due to the large tunnel barrier height experienced by the carriers.

$$m_{r,h} = \left(m_{r,light}^{3/2} + m_{r,heavy}^{3/2} \right)^{2/3} \quad (3.29)$$

Given the presence of the electric field, conductivity effective masses are used in the Kane model itself. For direct bandgap semiconductors, the $m_{r,e}$ is taken to be the same as the DOS m_r . Equation (3.30) is used to average the light and heavy $m_{r,h}$ values. This average accounts for the larger number of heavy holes present, but the higher mobility and tunneling probability of the light holes. Finally, the model equation uses an average $m_{r,BTBT}$ as defined in (3.31), which follows the same form as resistors in parallel. That is because the Kane model presumes that e^- and h^+ tunnel into the bandgap in imaginary k-space, where they meet and recombine. Lighter carriers tunnel more easily through the bandgap/barrier, and therefore travel further than their heavier counter parts.

$$m_{r,h} = \frac{\left(m_{r,light}^{3/2} + m_{r,heavy}^{3/2} \right)}{\left(m_{r,light}^{1/2} + m_{r,heavy}^{1/2} \right)} \quad (3.30)$$

$$m_{r,BTBT} = \left(m_{r,e}^{-1} + m_{r,h}^{-1} \right)^{-1} \quad (3.31)$$

3.5. Kane Model Program

The Kane Model Program (KMP) was developed using VB.net to efficiently and accurately compute ETD characteristics for a wide variety of material systems and parameters. The graphical user interface (GUI), shown in Fig. 3.9a, is easy to operate and quickly generates desired information. The “Run” button initializes computation for desired analysis type. “ E_F Only” will calculate $E_{F,n/p}$ and the DOS for e^-/h^+ (N_C/N_V), then display the results in the top right table. “ N^* Sweep” generates a standard list of N_A and N_D concentrations for a doping sweep

analysis. The “Ef2” checkbox includes L- and X-valleys for added $E_{F,n}$ accuracy, but is only valid for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ material system. The “BNG” checkbox adds bandgap narrowing effects for the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ material system. The top right text box is used to notify the user of simulation progress.

The drop-down box is used to select the desired material system from a pre-defined list (Fig. 3.9b), which may be easily amended by the user. The known material systems are stored in “ETD_Calculations.xlsx”, which is created during initial installation of KMP. The room temperature values for the pre-loaded group-4, and binary III-V material systems are listed in Table 3.2. The Ternary systems use linear interpolation to estimate most material parameters. Within the data file, there are six spreadsheets used for (i) listing available material systems, (ii) storing/calculating effective masses, (iii) relative dielectric constants, and (iv) bandgaps. In each of those sheets the first column contains the name of the material system. The second column contains the value for the parameter of interest to be used. The third column designates the composition of a generic ternary system ($\text{In}_{1-x}\text{Ga}_x\text{As}$). The rest of the worksheet may be used for

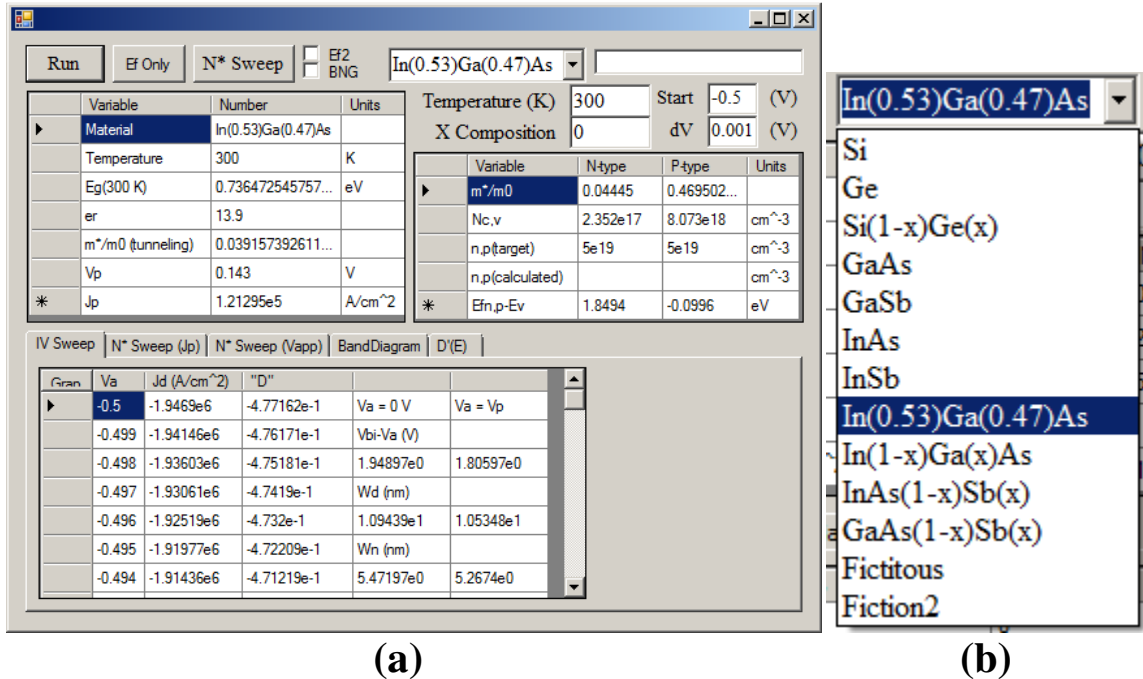


Fig. 3.9: GUI interface (a) for the Kane Model program. The drop-down box (b) can be used to select from a multitude of material systems.

Table 3.2: Material parameters stored in the Excel file used by KMP.

	E_G	ϵ_r	$m_{r,e}$		$m_{r,h}$				$m_{r,BTBT}$	N_C (10^{18} cm^{-3})	N_V (10^{18} cm^{-3})
	(eV)		DOS	Cond.	DOS	Cond.	light	heavy			
Si	1.12	11.68	1.08	0.26	0.81	0.39	0.16	0.49	0.16	28.2	18.3
Ge	0.66	16	0.56	0.12	0.29	0.21	0.044	0.28	0.076	10.5	3.92
GaAs	1.42	12.91	0.063	0.063	0.53	0.39	0.082	0.51	0.054	0.397	9.73
GaSb	0.73	15.7	0.041	0.041	0.41	0.31	0.050	0.40	0.036	0.208	6.63
InAs	0.35	15.15	0.028	0.028	0.41	0.33	0.026	0.41	0.026	0.118	6.69
InSb	0.18	16.8	0.02	0.02	0.43	0.36	0.015	0.43	0.019	0.0710	7.12

basic formulas and references used to calculate the final desired values. At startup, KMP reads the list of material systems and makes them available in the drop-down box. In this fashion, a user can easily add and edit material systems without modification to the program code.

When calculating Fermi energies, the same Excel workbook is used. The Fermi_Integral worksheet contains the lookup table of “x” (Column one) and “y” (column two) values used in (3.22). If “y” exceeds the pre-calculated values, the program will automatically increment “x”, and numerically calculate the corresponding “y” value using (3.23), until an appropriate value is achieved. For improved accuracy, the final “x” value used is linearly interpolated from the two nearest points listed in the table.

In the top left table the current material system and temperature are selected. When a new material system is selected, E_G , ϵ_r , $m_{r,tunnel}$ are updated from the Excel file. The user may modify these parameters in the table without affecting the stored values. This way, the user can easily investigate the effects of a single parameter on the output without changing any of the other values. Finally, when a J-V calculation is performed, J_P and V_P are reported at the bottom of this table.

The four text boxes directly above the right hand table may be modified by the user to designate a new (i) temperature, (ii) material composition, (iii) starting V_A , and (iv) voltage step (dV). The program will automatically update all dependent parameters when any of the previously mentioned values are changed. The table directly below is updated with the $m_{r,e/h}$ for

the desired material system. As before, the user may change the value within the table instead of modifying the Excel workbook. The user must enter n- and p-type doping concentrations before any analysis can be performed, except for the N^* sweeps. N_{CV} are calculated at the start of every analysis, then reported here. The calculated $\Delta E_{F,np}$ are reported at the bottom. The calculated n/p concentrations, 4th row, is no longer used.

The Tabs at the bottom of the window are used to select the desired analysis. Each tab is a separate analysis type, and may require additional input parameters. When the “Run” button is executed, the analysis for the selected tab will run.

3.5.1. KMP Flow & Operation

The flow diagram determining the operation of KMP is straight forward (Fig. 3.10). The user must first input some general parameters used by all analysis types. This includes the material system, composition, temperature, starting V_A , and voltage steps (dV). This is also the

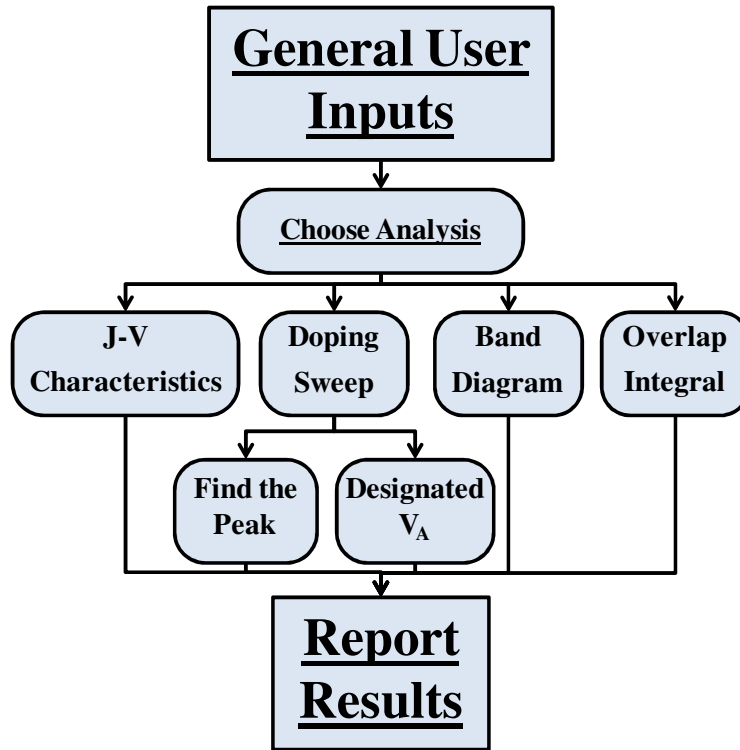


Fig. 3.10: Flow diagram for operation of KMP.

optimal point to alter any material parameters that the user wishes. Then the analysis type is chosen. The first choice is to calculate the full J-V characteristics, which require the additional input of N_A and N_D in the top right table. After “Run” is selected, N_C , N_V , $E_{F,n}$ and $E_{F,p}$ are immediately calculated. Then, for each biasing condition (i) the average ξ , (ii) D , and (iii) Kane model is calculated.

In the table for the selected tab at the bottom of the GUI, the calculated J_{BTBT} and D values are recorded for each V_A . Also in the same table the following parameters are recorded which may be used to reproduce any part, or the whole of the Kane model; (i) V_{bi} , (ii) w_d , (iii) $w_{n/p}$, (iv) average ξ (v) exponent pre-factor, (vi) argument inside the exponential, (vii) $E_{F,n/p}$, (viii) $N_{D,A}$, (ix) V_p , (x) J_p , and (xi) $D(V_p)$. Many of the parameters are reported at V_A of 0 V and V_p .

After the J-V results are reported, there is the additional option of generating plots of the various parameters involved (Fig. 3.11). The y1-axis (left) and y2-axis (right) can be linear or logarithmic using the check boxes on the side. The axis ranges can be adjusted using the top

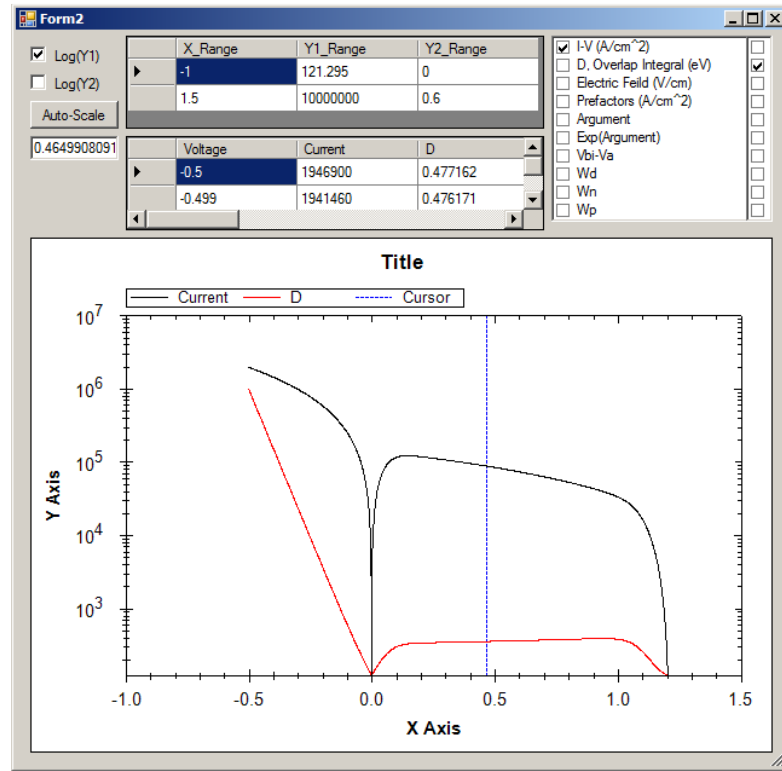


Fig. 3.11: Plotting functionality for J-V analysis.

table, or by clicking the “Auto Scale” button. The bottom table lists all values that change with V_A for the entire sweep range. The text box to the left displays the position of the vertical blue line, which moves with the cursor. The parameters shown in the plot are determined by the check box lists on the right. Checking to the left of the parameter plots it on the y1 axis. The left hand side is for the y2 axis. This function is for quick reference only.

One of the large portions of the experimental work to be discussed in this work is mapping the behavior of ETD characteristics over a large design. The most common and appropriate approach to this will be looking at J_{BTBT} , usually J_p , versus $N^{*-1/2}$ in order to generate trendlines for each material system. To facilitate modeling these trendlines, there are two separate N^* sweep options. For both methods, a list of N_A and N_D are supplied to the table within the appropriate tabs in the main GUI. There is the option of finding the values of interest at the peak, or a specified V_A .

When calculating band diagrams, an optional intrinsic layer may be inserted between the p- and n- sides. The layers are assumed to be perfectly abrupt, with full dopant activation. Full depletion approximation is used to not only calculate the depletion widths in (3.32) and (3.33), but also the curvature of the band bending near the p-i-n junction (3.34). In the following equations, the x-axis is centered in the middle of the i -layer. E_V is simply calculated as $E_C - E_G$. Additionally, the results use $E_{F,n}$ is used as the reference energy. Finally, $D'(E)$ and its individual elements are calculated in the final tab/analysis option. Only the material system, doping concentrations, and V_A need to be supplied.

$$w_d = \sqrt{i^2 + \frac{2\epsilon_s \times (V_{bi} - V_A)}{qN^*}} - i \quad (3.32)$$

$$w_n = w_d \left(\frac{N_A}{N_A + N_D} \right); \quad w_d = w_n + w_p \quad (3.33)$$

$$E_C(x) = \begin{cases} \frac{qN_D}{2\epsilon_s} \left(x + w_p + \frac{i}{2}\right)^2 - E_{F,n}; & -w_n - \frac{i}{2} \leq x \leq -\frac{i}{2} \\ \frac{qN_D}{2\epsilon_s} w_n \left(2x + w_n + \frac{i}{2}\right) - E_{F,n}; & -\frac{i}{2} \leq x \leq \frac{i}{2} \\ (V_{bi} - V_A) - \frac{qNA}{2\epsilon_s} \left(x - w_p - \frac{i}{2}\right)^2 - E_{F,n}; & \frac{i}{2} \leq x \leq w_p + \frac{i}{2} \end{cases} \quad (3.34)$$

3.6. Conclusions

The Kane model for predicting ETD characteristics has been discussed, beginning with the assumptions and approximations in the model. In particular, only direct bandgap BTBT (Γ -direction) is considered. Many material systems have a direct bandgaps that is much smaller than the L- and X-valleys, resulting in a much larger BTBT probability for the Γ -valley. The assuming a constant average ξ and m^* significantly simplify the calculations, without adding large error to the calculations.

The Kane model itself was broken up into three parts; (i) a pre-factor/coefficient, the (ii) overlap integral (D), and (iii) BTBT probability exponential. The BTBT probability (exponential term) has often been calculated using the WKB approximation, which can underestimate what the original model predicts by $\sim 20\%$ to $\sim 18,000x$ depending on material parameters and doping concentrations. This work proceeds with the original formulation []. Qualitative analysis of the pre-factor and exponential terms indicates that they are always positive, with a fairly shallow, negative logarithmic slope.

The overlap integral is solely responsible for indicating the direction of BTBT current flow, and providing positive differential resistance for V_A less than V_p . This is reasonable, given that D accounts for the overlap of e^- and h^+ distributions available for BTBT. Detailed analysis of “ D ”, which needs to be calculated numerically, shows that there are three basic shapes that it may take which depend on the ratio of $E_{F,n}$ to $E_{F,p}$; (i) simple cone, (ii) simple mesa, and (iii) complex mesa. For the 1st two shapes, D is equivalent to V_A in reverse bias, which is a common

approximation. However, for the complex mesa the approximation must be modified by a constant (ΔeV), and is generally invalid for small V_A .

The degenerate levels of doping concentrations needed for ETD structures requires full Fermi-Dirac statistics when determining E_F . As with D , there is no closed form solution to the Fermi-Direc/DOS integral, and must be solved numerically. Additionally, the dependent variable (E_F) is within the integral and the output is the known, independent variable (doping concentration). A simple variable substitution removed all material parameters from the integral, enabling the generation of a lookup table of values which is generic to all material systems and conditions. This greatly enhances the speed and accuracy of determining E_F .

Finally, the structure and operation of a GUI based program, KMP, was discussed in

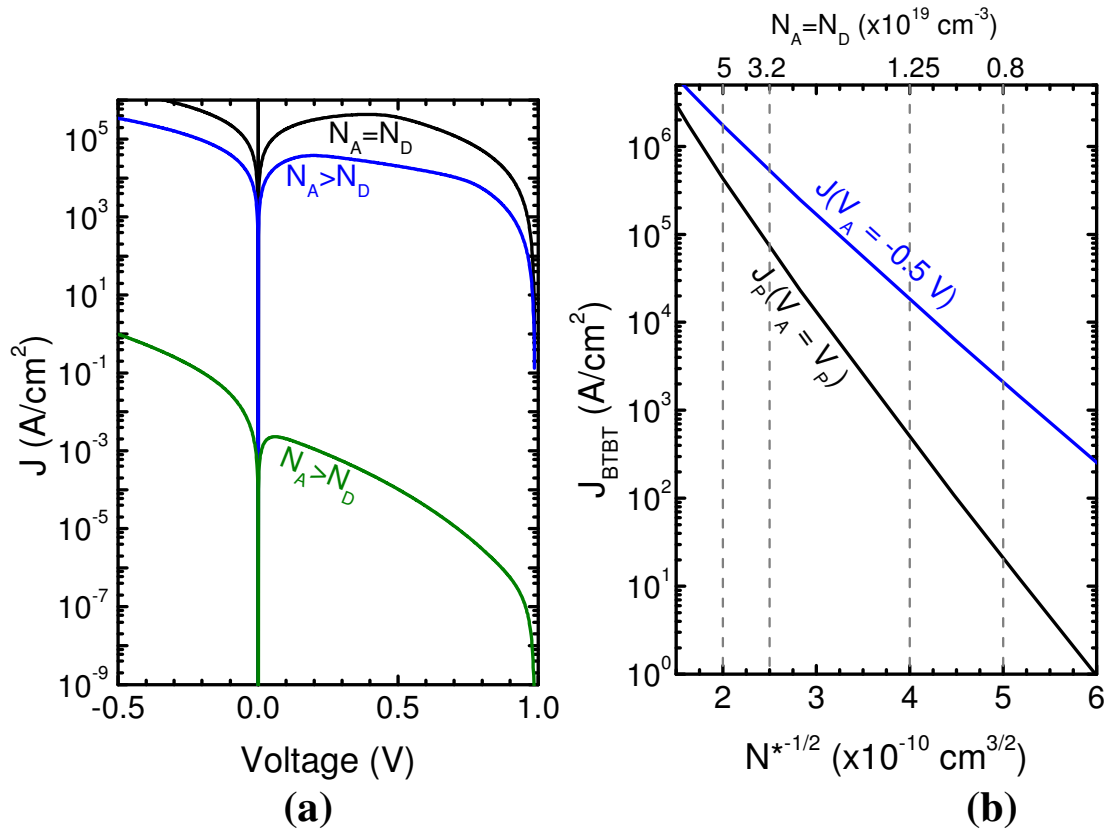


Fig. 3.12: Left (a), fully calculated BTBT J-V characteristics calculated using with KMP. Material and doping parameters are the same as those used for the detailed discussion on “D” (Section 3.2.3.1). Right (b), characteristic trendlines for the same fictitious material system. The doping sweep analysis was performed for J_P and $V_A = -0.5$ V.

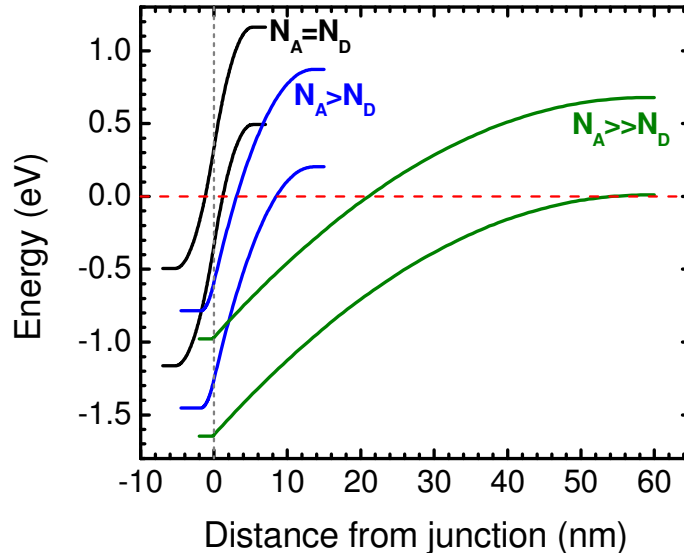


Fig. 3.13: Calculated band diagrams for the (i) cone, (ii) mesa, and (iii) complex mesa examples used in Section 3.2.3.1.

detail. This program was developed specifically for the work discussed in chapters 4, 5, and 6, using VB.net language and development environment. The KMP code can be found in Appendix A. Many material system parameters are stored within an Excel Workbook, as well as the E_F lookup table, and is directly used by the program. Materials can easily be modified and added by the user without modifying any code. In addition to (i) BTBT J-V characteristics, KMP can calculate (ii) doping sweeps for characteristic trendlines, (iii) basic band diagrams, and (iv) detailed $D'(E)$ analysis.

Using the same fictitious material parameters and doping concentrations in Section 3.2.3.1 (detailed analysis of D), KMP was used to generate J-V curves (Fig. 3.12a) and trendlines (Fig. 3.12b). As will be seen in the following chapters, the modeled J-V characteristics have similar shapes to experimental measurements. J_p increases with N^* . V_p also increases however; this is mostly due to the shape of D (at what bias it begins to level off). There is clearly an exponential characteristic trendline (J_p vs. $N^{*-1/2}$). The ratio of zener current density to J_p decreases as N^* and J_p increases. The calculated band diagrams (Fig. 3.13) clearly shows the large increases in w_d , and hence BTBT barrier width, for each case. This increase in w_d is the

primary reason for the very large reduction in BTBT current density from (i) cone to (ii) mesa to (iii) complex mesa cases.

With the developed algorithms and KMP, the Kane model can be quickly and easily compared to experimental results. This includes full J-V characteristics, which previously has not been accomplished. Previously, only characteristic trendlines have been compared with the Kane model, and typically at low temperature in order to minimize phonon interactions [17]. If proven accurate, KMP can be easily distributed and used to provide useful insights into the operation of ETD structures. Additionally, the Kane model would be very useful for designing ETD structures with J_{BTBT} matched to the circuit specifications without many separate epitaxial growths and fabrications.

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CHAPTER 4

Ge and III-V Tunnel Diodes on Si

In this chapter, a series of Ge and GaAs/InGaAs ETDs will be fabricated [1-4] and benchmarked against results from literature [5-18] to assess the quality non-traditional semiconductors on Si. This is a departure from traditional development performed by industry in order to meet the increasing demands of consumer electronics. To help satisfy the required continual improvement of integrated electronics, much effort has gone into the development of novel material systems [19], as well as alternate device structures [20-25]. Since its introduction as the main semiconductor, Si has remained the primary channel material. However, most other aspects of integrated circuits have been engineered with new materials; (i) high- k dielectrics, (ii) metal gates, (iii) Ge Source/Drains, (iv) straining liners, (v) low- k dielectrics, and (vi) refractory and low resistivity metals. This does not include dopant species and processing materials. Some of the modifications have modified the strain [26-29] and geometry of the Si channel [19, 30, 31] in order to improve mobility and gate control. However, the channel is still fundamentally limited by Si, which may be surpassed with new materials [19, 32-34]. The bulk of non-Si research is performed on substrates that are much more expensive and fragile than Si, and therefore unsuitable for mass manufacturing.

Previously, the majority of heterointegration of virtual substrates on Si involve thick graded buffers [35-37] or a surface transfer process [38-40]. While both of these processes have enabled limited research into the ability to fabricate non-traditional material systems on Si substrates, they are still viewed as non-manufacturable on a large scale. Therefore, the aspect ratio trapping (ART) [41-45] method discussed in Section 4.1.3, appears to provide high quality virtual substrates in a manufacturing friendly process. However, prior to this work there was no experimental result indicating the electrostatic properties of the ART virtual substrates [1-4].

This chapter investigates defect enabled leakage currents via high PVCR ETDs, which are known to be sensitive to such defects and require high quality crystalline semiconductors [46-51]. After verifying the electrostatic quality of ART substrates, the bulk of research and device optimization can proceed on standard III-V substrates. Optimized structures can be integrated on the still scarce heterointegrated virtual substrates to verify that minimal changes occur between substrate.

In this chapter, basic materials analysis techniques will be used to investigate the quality of the virtual substrate [41-44]. Quickly, the work will move towards verifying the electrical quality of the virtual substrate by investigating ETDs fabricated using an alloy junction process [1] and CVD based epitaxy [2-4]. Ge alloy junctions were fabricated and characterized as an initial study [1].

Afterwards, a series of five GaAs/InGaAs ETDs were grown on the Ge virtual substrates [1, 2]. Two companion GaAs/InGaAs ETDs were grown directly on Si and GaAs substrates, each. This investigated ETDs grown on the ART substrates, versus replicas grown directly on Si and GaAs substrates as nominally worst and best case scenarios. Furthermore, methodical changes to the baseline ETD structure looked at the effect of In concentration, In placement, graded In junctions, and *i*-layer thickness on ETD characteristics. A new fabrication process was developed, and served as the baseline process for all of the following device fabrication runs.

ETDs are also characterized over a large temperature range [3], to further elucidate the crystal quality. Finally, a new deep submicron process is developed from the original basic process [4]. As part of the process, a new e-beam lithography procedure is discussed.

4.1. Ge/III-V on Si Integration Methods

There are three basic issues regarding the integration of crystalline Ge and III-V semiconductors on Si substrates. The first is the large lattice constant difference between the various material systems. Ge and GaAs are the closest to Si, with a lattice mismatch (strain) of 4.1%. For thin epitaxial films, the mismatched layer will strain its lattice in order to conform to

the substrates dimensions. When the film exceeds a critical thickness the stress will become too large, and the film will relax by generating one dimensional misfit dislocations along the hetero-interface in [110] directions. Misfit dislocation must terminate at free surfaces (Eg. Sample edges or non-crystalline surfaces) or move away from the hetero-interface along (111) directions and form one dimensional threading dislocations. The threading dislocations act as non-radiative recombination centers and deep traps [52], increasing leakage currents (increasing J_V and decreasing PVCR). For Ge grown directly on Si a large threading dislocations density (TDD) of $\sim 1.25 \times 10^9 / \text{cm}^2$ is generated.

The Second integration issue are thermal expansion differences. Typically, epitaxial growths are performed at elevated temperatures ($\sim 400^\circ\text{C}$ up to $\sim 800^\circ\text{C}$). Thermal energy is necessary to form regular crystalline lattice arrangements. As a result, crystal relaxation due to lattice mismatch occurs at these elevated temperatures. Further strain and relaxation may occur due to differences in thermal expansion rates as the samples cooled to room temperature. This is typically much smaller effects, no more than 0.26% for GaAs on Si.

Finally, fundamental differences in the crystalline structure may give rise to anti-phase domains. This is an issue of the ionic bonding in III-V semiconductors, which require an ideal cation-anion bonding arrangement. However, Si and Ge are covalently bonded, thereby lacking a portion of the growth template needed by compound semiconductors. A mis-alignment of the bonding phases may occur between two regions of growth, forming anion-anion and cation-cation bonds. These sites reduce minority carrier lifetimes and increase majority carrier scattering, but have not been shown to act as trap states [52]. Therefore, the effects of antiphase domains on BTBT may be small, especially compared to TDD.

Methods of minimizing, or even eliminating anti-phase domains have previously been developed and implemented by others [53, 54]. The effects of thermal expansion mismatch can be minimized by reducing growth temperatures. The main issue remaining is the formation of threading dislocations. Previously, heteroepitaxy of non-lattice matched substrates has utilized

relaxed graded buffers or substrate transfer processes. This work was among the first utilize aspect ratio trapping [1-4][41-45].

4.1.1. Relaxed, Compositionally Graded Buffers

In this method, the composition of the epitaxial growth is stepped in order to incrementally increase/decrease the lattice constant [35-37]. For instance, Ge virtual substrates on Si can be achieved by grading the $\text{Si}_{1-x}\text{Ge}_x$ content from 0% to 100% with 10 or more steps. At each step, the grow is performed in a way to allow the layer to relax. However, when done correctly, threading dislocations will be recycled at each step and move towards the sample edge, instead of generating new dislocations (Fig. 4.1a). Furthermore, the interface between compositional stepped layers help to suppress and terminate threading dislocations. This is clearly seen in Fig. 4.1b, where a defect free GaAs-virtual substrate is integrated on a Si substrate. First, $\text{Si}_{1-x}\text{Ge}_x$ is compositionally graded from $x = 0$ to 100% (shown at the bottom of the figure).

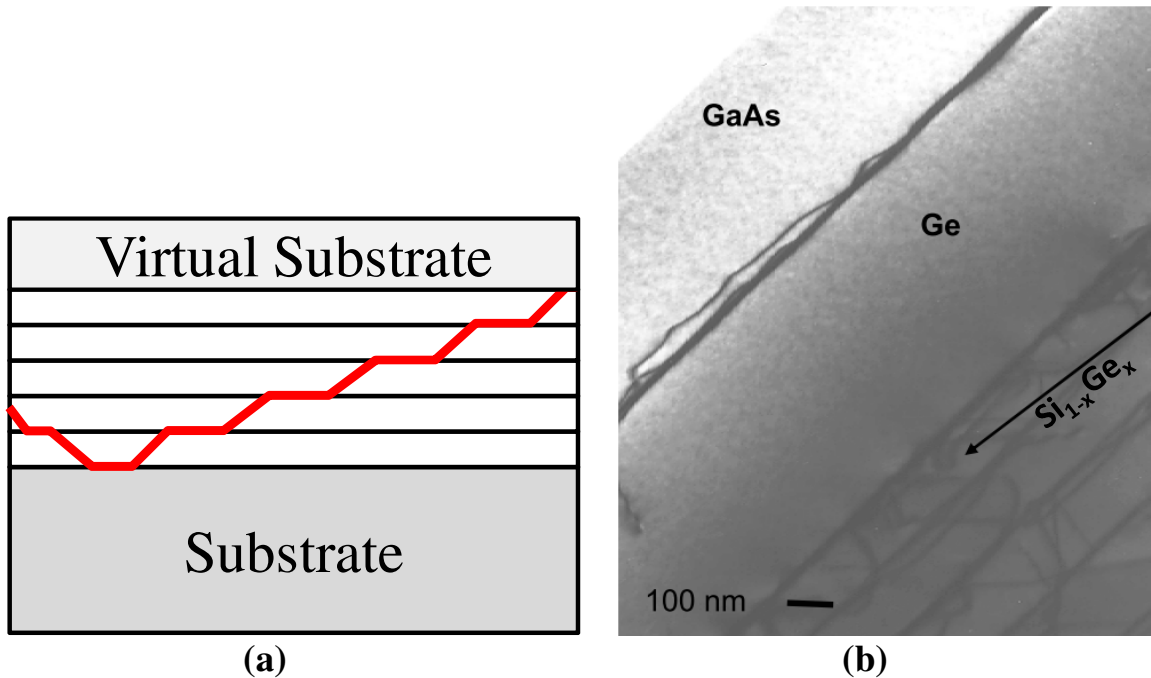


Fig. 4.1: Left (a), schematic diagram of graded buffer. Solid line shows a threading dislocation moving through the layers without generating new dislocations and terminating below the virtual-Ge substrate. Right (b) is a TEM of a $\text{Si}_{1-x}\text{Ge}_x$ graded buffer with defect free GaAs-on-Ge-virtual substrate integrated on a Si substrate (adopted from [36]).

Notice that each compositional step is clearly as dislocations are shunted horizontally. The final result is a defect free virtual-Ge substrate (middle of the image). On top of the Ge, GaAs is grown. Since there is only a 0.04% lattice mismatch between GaAs and Ge, no additional buffers are needed.

This method has produced virtual Ge substrates with TDD below $10^6 /\text{cm}^3$. Furthermore, this method can be employed to generate virtual substrates on large Si wafers (depending on the epitaxial reactor). Additionally, a large variety of non-traditional electronics material systems and devices have been integrated on Si [35-37]. However, due to the complexity and expense of the epitaxial growth, this method has not been expanded to productions. Furthermore, the relaxed graded buffers needed are very thick (usually greater than $\sim 1 \mu\text{m}$), requiring extended growth times, thereby elevating the cost of this method.

4.1.2. Substrate Transfer Process

For this technique, desired epitaxial layers are prepared on an ideal, temporary substrate. Then, the temporary substrate is flipped upside down onto a Si substrate and chemically bonded to each other. Finally, the desired layers are released from the temporary substrate, leaving behind a high quality virtual substrate on Si. There are several ways to accomplish the previous steps. One method utilizes similar steps as the SmartCuttm process [38] used for silicon-on-insulator (Fig. 4.2). First (a), the desired film stack is grown, starting with sacrificial InGaAs/InP layers. Then (b), H^+ implantation is done to desired depth (dashed line). Afterwards, (c) the epitaxial layers are bonded to a thin thermal oxide on top of a Si substrate. A (d) thermal step releases the temporary layer. Finally (e), the sacrificial InGaAs/InP layers are selectively etched, leaving behind a high quality III-V on insulator substrate.

Similar methods have been done without the H^+ implant. Instead, a selective etch to a sacrificial AlAs layer at the bottom of the structure (adjacent to the temporary substrate) is used to release the virtual substrate [39, 40]. Additionally, bonding has been done with metals (Mo,

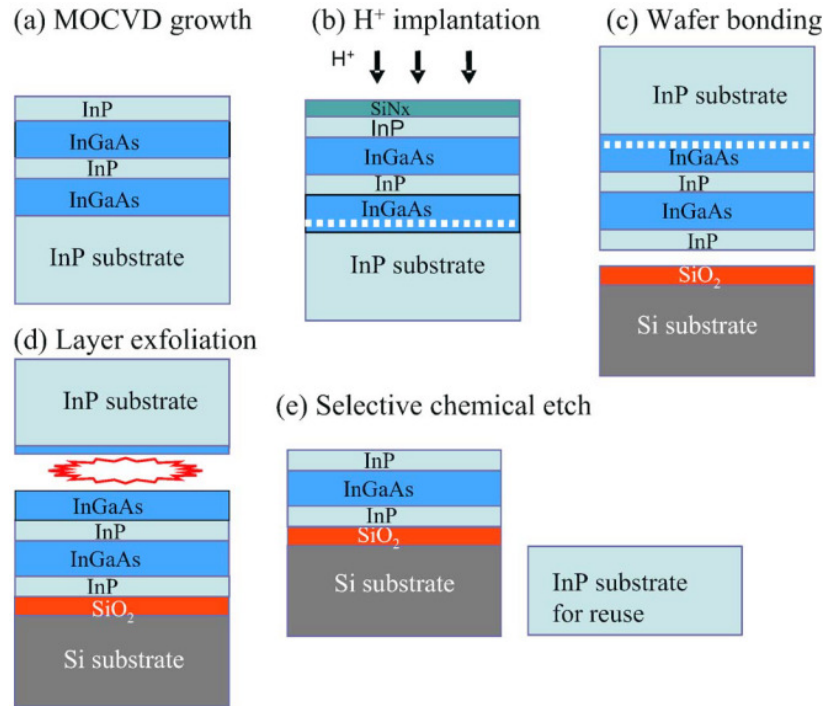


Fig. 4.2: SmartCut™ substrate transfer Process flow, adopted from [38]. Shows the (a) initial epitaxial layer start on temporary substrate, (b) H⁺ implant, (c) wafer bonding, (d) layer exfoliation, and (e) surface preparation.

Au-Sn, Ge-Pd) [39, 40]. For that case, metal is deposited onto the epitaxial layers as the topmost layer. Then it is bonded onto a Si substrate with the same metal deposited on top.

There have been numerous variations to this method. However, there are several issues. There typically the yield is too low for manufacturing. It still requires the use of III-V substrates which are expensive, delicate, and limited in size to ~4 inch diameters. The bonding process requires good alignment, thermal steps, and sometimes mechanical pressure. The interface at the bonded surface is often mechanically unstable and prone to cracking and exfoliation. Additionally, it is not always appropriate to use a semiconductor on insulator or metal. In the end, this can be a fine method for research, but has yet to be demonstrated as manufacturable.

4.1.3. Aspect Ratio Trapping Hetero-Integration

In this method, vertical trenches are etched all the way through an SiO₂ film, to the underlying Si substrate. A selective Ge epitaxial growth is performed, such that Ge only forms

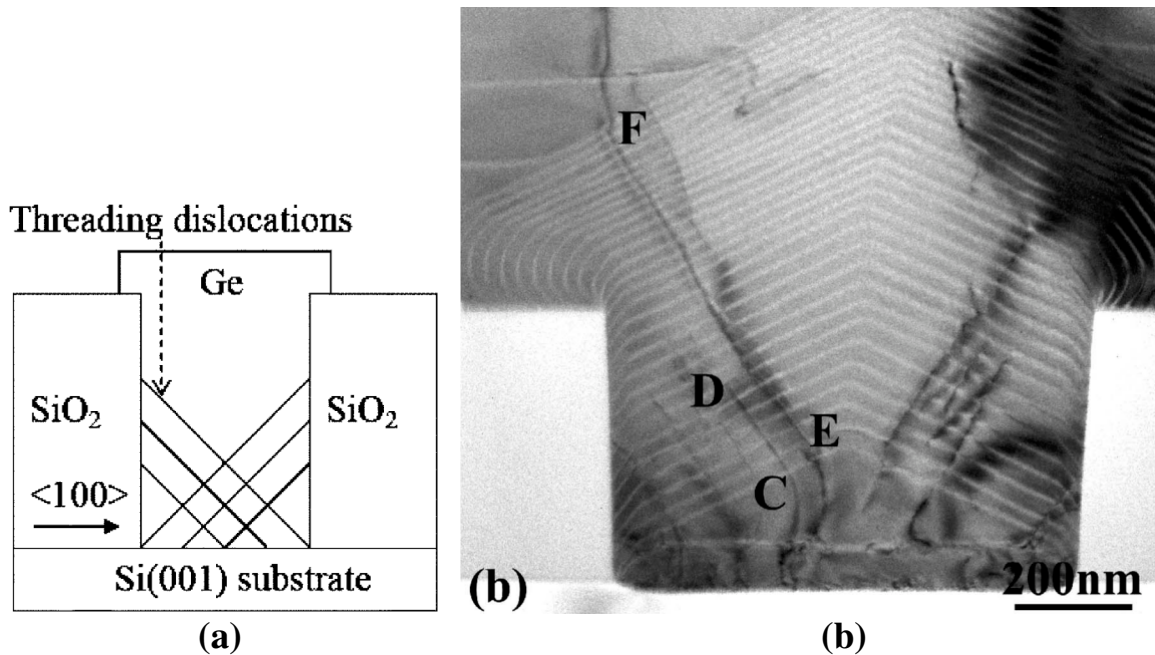


Fig. 4.3: (A) Schematic diagram of threading dislocations being trapped inside an ART trench (adopted from [43]). (b) TEM of overgrown Ge epitaxial growth inside a wide ART trench. White lines are thin layers of SiGe, showing the dynamics of growth inside and over the oxide barriers (adopted from [44]).

on crystalline semiconductors and not the amorphous structure of SiO₂. In this fashion, the Ge begins growing inside the oxide trenches, from the bottom up. The Threading dislocations formed move diagonally away from the Si surface, and towards the SiO₂ sidewalls, where they will terminate. Finally, Ge grown above the terminated threading dislocations will be a high quality virtual substrate.

In Fig. 4.3a, the Ge is grown slightly above the Oxide trenches. At the bottom of the trench, several threading dislocations form and terminate at the oxide interface, forming a “V” shape at the bottom of the trench. In this method, larger aspect ratios between the height and width of the trenches will trap greater numbers of defects. To form the virtual substrate, the oxide walls are overgrown until the growths from adjacent trenches are merged and a desired layer thickness is achieved. However, the progression of growth proceeds on approximately a [311] plane, which is not conducive for device fabrication. Even after full merge of adjacent trenches, the Ge surface contains large hills and valleys (Fig. 4.3b). For a flat surface appropriate

for device fabrication, the virtual substrate process requires a CMP step at the end. Also, from Fig. 4.3b, notice that some of the threading dislocations escape due to the wide trench (small aspect ratio). Additional coalescent dislocations may form where two overgrown trenches merge (not shown here).

ART is an efficient method to reduce TDD by many orders of magnitude. The final film thickness can be a few 100 nm, including the virtual substrate, unlike grad buffers. This method has been shown to work with Ge [41-44], GaAs [42], and InP [45]. However, prior to this work there weren't any device results indicating the electrical quality of the ART substrates.

4.2. Materials Analysis of Ge on Si ART

High quality, crystalline, virtual Ge substrates were provided as part of a collaborative effort to investigate the effects of integrated semiconductors on device performance [41-44]. The virtual Ge substrates were integrated on [100] Si wafers using ART, which has been described in Section 4.1.3. After integration, Ge and GaAs tunnel diodes were fabricated using a variety of

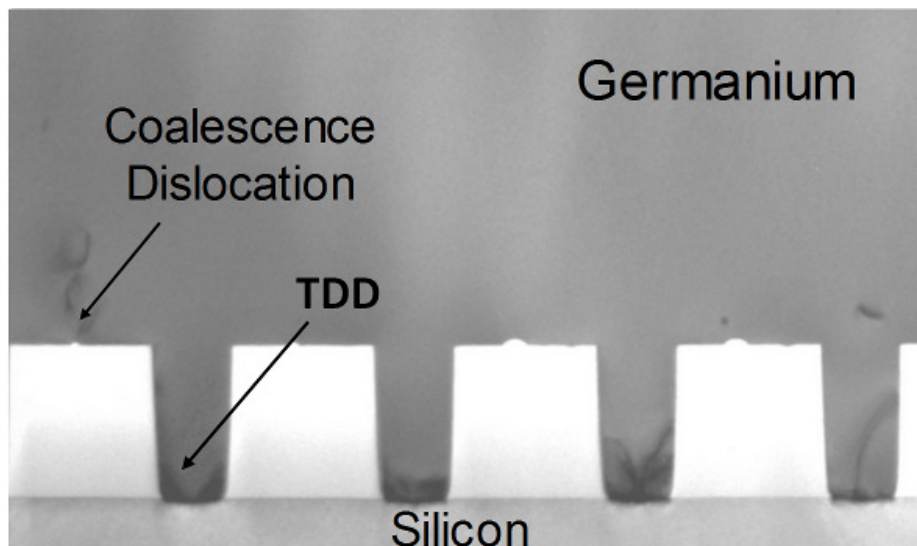


Fig. 4.4: TEM cross-section of coalesced Ge integrated on a Si substrate using ART. The majority of TDD resulting from the 4% lattice mismatch between Ge and Si is trapped by the oxide sidewalls within the trenches. A few extra dislocations are created around the coalescence planes.

processing techniques [1-4].

The Ge virtual substrate preparation began with 490 nm thermal oxide growth. Vertical trenches were etched into the oxide with various widths (100-400 nm) and pitches (250-500 nm). Ge epitaxial layer was selectively grown inside the trenches using reduced pressure chemical vapor deposition (RPCVD). Growth continued above the oxide trenches, until an 825 nm coalesced Ge layer formed. To provide a smooth and flat surface for optimal device fabrication, the Ge layer was planarized via chemical mechanical polishing (CMP).

As expected, a large threading dislocation density (TDD) was created at the Ge/Si interface, as seen in Fig. 4.4. However, the majority of TDD were trapped within the oxide trenches resulting in a high quality crystalline Ge layer only 200 nm above the substrate surface. A small number of coalescence dislocations were formed where the overgrown Ge from two adjacent trenches join together. Without ART, a blanket film of Ge forms a TDD of $\sim 2 \times 10^9 / \text{cm}^3$, due to its 4% lattice mismatch with Si. Increasing the trench pitch (spacing) decreased TDD by greater than 10x (Fig. 4.5b). Increasing the trench aspect ratio (height to width ratio) decreased TDD by approximately 1,000x, down to $\sim 2 \times 10^6 / \text{cm}^3$ (Fig. 4.5a). The visual and quantitative inspection indicates that a high quality virtual Ge substrate has been formed. This indicates that high quality electrical devices are achievable on ART substrates, but does not confirm this hypothesis.

4.3. Ge on Si Tunnel Junction

Initial experiments looked into directly testing the virtual Ge substrates by fabricating Esaki tunnel diodes (TDs). The device fabrication approach used in this study was adopted from Zhao, *et. al* [55]. The present approach differs in two minor ways. First, this study used a lower n-type doping concentration of $5 \times 10^{20} \text{ cm}^{-3}$ rather than $1 \times 10^{21} \text{ cm}^{-3}$. Secondly, the Zhao study utilized evaporated Al rather than sputter deposited Al: 2% Si in the present study. It was

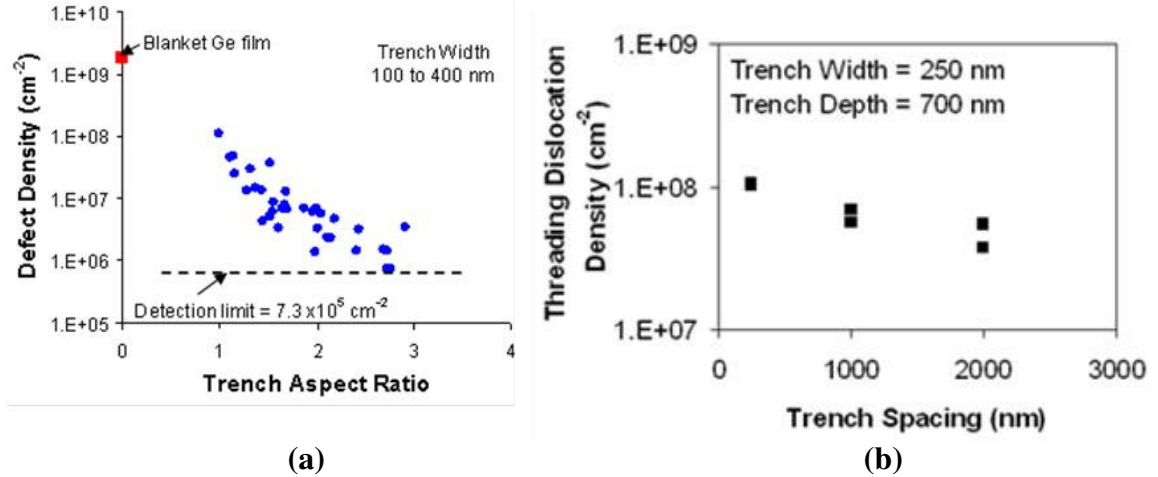


Fig. 4.5: Defect density of virtual Ge substrate integrated on Si via ART. In general, (a) as the aspect ratio (height by width) of the oxide trenches increases TDD decreases. Additionally, (b) increasing the trench pitch (spacing) also decreases TDD. Optimal measured results reduced TDD from $\sim 1.25 \times 10^9 / \text{cm}^3$ for a blanket film, down to $\sim 1.25 \times 10^6 / \text{cm}^3$.

theorized that the addition of 2% Si may act to slow the reaction rate between Al and Ge resulting in a more abrupt alloy junction.

As grown, the Ge layer is undoped. Therefore fabrication began with the introduction of n-type dopants. The virtual substrates were coated with Emulsitone $5 \times 10^{20} \text{ cm}^{-3}$ phosphorosilica spin-on-glass (SOG), and baked at 800°C for five minutes under an N₂ ambient in an AG Associates Heat Pulse 610 Rapid Thermal Annealing (RTA) furnace. This step served to introduce a degenerate level of P into the Ge. The SOG was removed in a 10:1 DI water to HF bath for 25 seconds. A lift-off technique was used to define dots of a 140 nm thick Al: 2 %Si, film deposited via DC sputtering. Alloying of the p-type junction was performed via a spike RTA at 480 - 620°C at a target time of one second in an N₂ ambient. A ramp rate of 150°C/sec. was used for all samples. In practice, the chamber temperature was in the vicinity of the target temperature for three seconds, with some run to run variability. The fabrication procedure was applied to a substrate with coalesced Ge on Si. In this sample, the oxide openings had a width of 250 nm with a 1:1 pitch. Fig. 4.6 illustrates a schematic diagram of Ge on Si Esaki diodes.

4.3.1. Ge ETD Results and Analysis

For all process conditions, negative differential resistance or inflections were observed. Fig. 4.7 shows the dependence of the current voltage characteristics on the alloy temperature. In general a few trends were observed. First, elevating the anneal temperatures resulted in an increase in current density. An optimal fabrication window was found for a phosphorus diffusion at 825°C, five minutes. A maximum peak to valley current ratio (PVCR) of 1.1 with a current density of 4.1 kA/cm² was observed for an alloy temperature of 580°C, for one second. A 1.1 PVCR was also observed at 620°C, one second.

These results experimentally show a similar trend to Zhao [55] with lower peak to valley ratios. It should be noted that the overall current density in the Zhao study of 15 kA/cm² is roughly double the present reported value of 6 kA/cm² in both the control/ART diodes for a comparable anneal of 600°C, one second. This is attributed to a narrow depletion width in the Zhao et. al study due to the higher n-type doping levels. Based on recent publications of P-diffusion in Si, the junction is estimated to be 300 nm deep for these conditions [56].

For the Ge system, it is theorized that the Esaki diode performance can be greatly

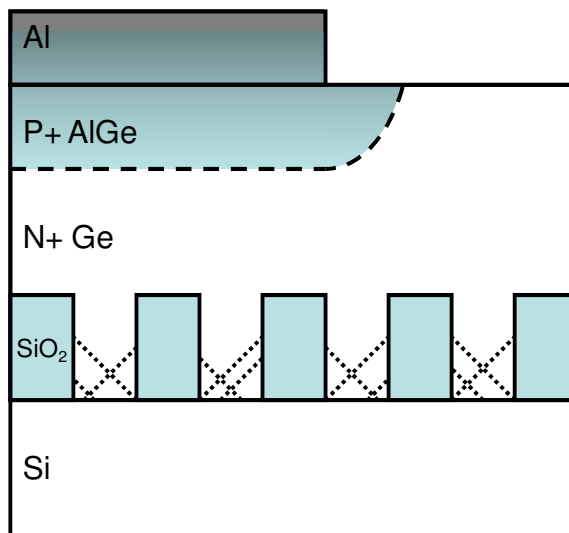


Fig. 4.6: Schematic cross-section of the Ge alloy junction TD.

improved by looking at alternative doping schemes. It should be noted that the highest reported PVCGR for Ge Esaki tunnel diodes is about 10 [57]. Davis and Gibbons further point out that Al alloying typically resulted in lower PVCGR values compared to other approaches as Al consumes Ge during alloying at a much faster rate compared to Sn or In [57, 58]. Chynoweth *et. al* also indicated that alloying Al in Ge results in backward diode performance [59]. Furthermore, it is speculated that it will be possible to realize a III-V on Si Esaki diode using similar techniques, which is expected to have substantially higher performance than either Si or Ge Esaki diodes.

In conclusion, it has been demonstrated Ge Esaki diodes on a Si substrate with a peak-to-valley ratio of 1.1. This result suggests the high quality of Ge epitaxy grown on trench-patterned Si substrate via ART defect-trapping technique. It demonstrates a viable technique for the integration of Ge and III-V materials on Si for devices such as resonant tunnelling diodes, HEMTs and MOSFETs. Furthermore, GaAs based structures may be directly grown on the Ge virtual substrates for improved device performance. In the following section a series of large PVCGR GaAs ETDs are used to evaluate the ART substrates.

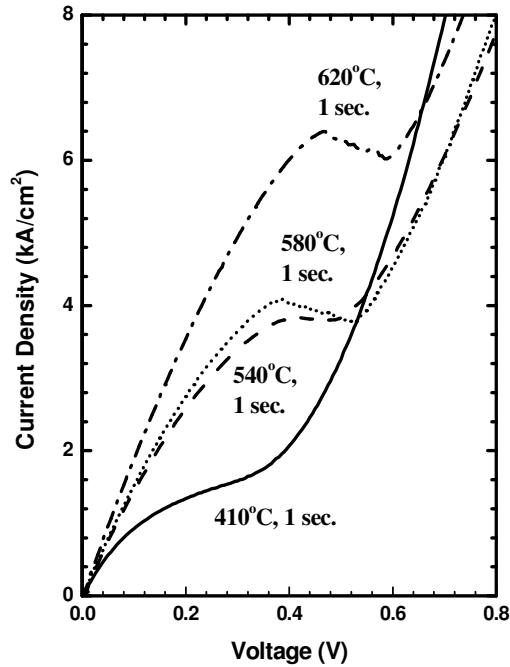


Fig. 4.7: I-V characteristics of Ge on Si ETDs for four separate anneal temperatures.

4.4. GaAs on Si Tunnel Junctions

The direct bandgap and low reduced effective mass of III-V semiconductors generally results in superior tunnel diodes compared to Si and Ge. Furthermore, the larger bandgap of GaAs, but not excessively so, results in tunnel diodes with large PVCs in the range 21-25 [12, 13]. Whereas, the best Si and Ge tunnel diodes have PVCs of 6 [8] and 10 [57], respectively. High PVC in a given material system is a signature of low defect density resulting from low excess current. Therefore, large PVC structures are more sensitive to crystal quality. The highest PVC tunnel diodes have so far been produced by molecular beam epitaxy and attributed to the formation of abrupt heterojunctions and doping profiles and high activated impurity densities.

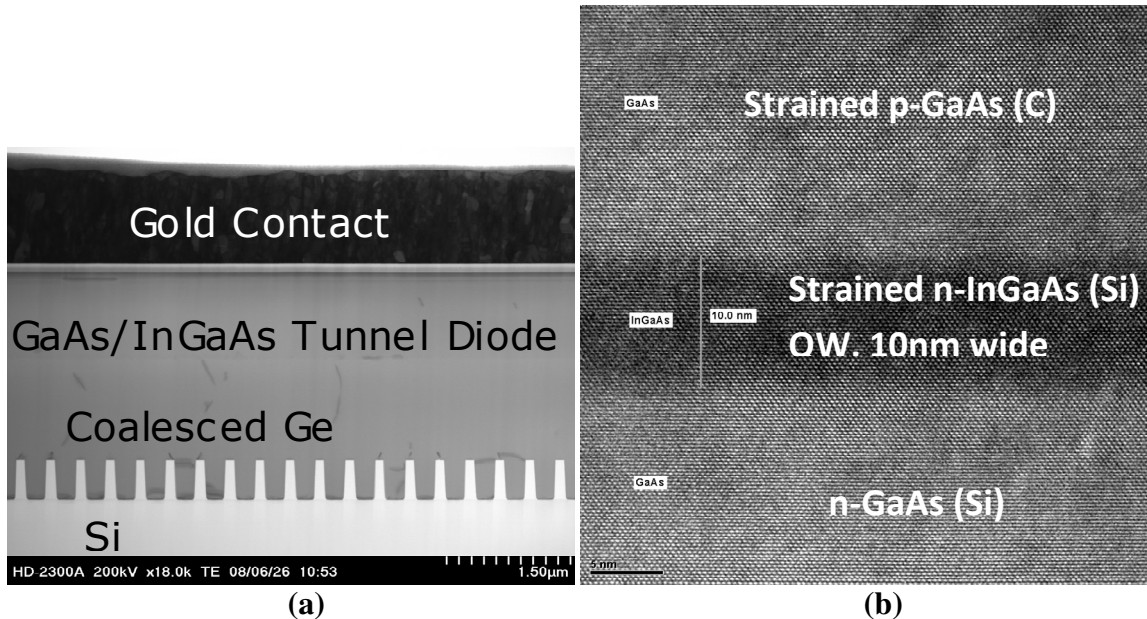


Fig. 4.8: TEM cross-sections of (a) entire GaAs TD on Ge ART layers and (b) a close-up of the TD junction itself. The bulk of the TDD is trapped within the ART structure, though a few defects remain present within the coalesced Ge. Visually, the Ge/GaAs interface traps more of the defects, providing a high quality GaAs virtual substrate. The high resolution micrograph shows a well defined junction with regular crystalline structure.

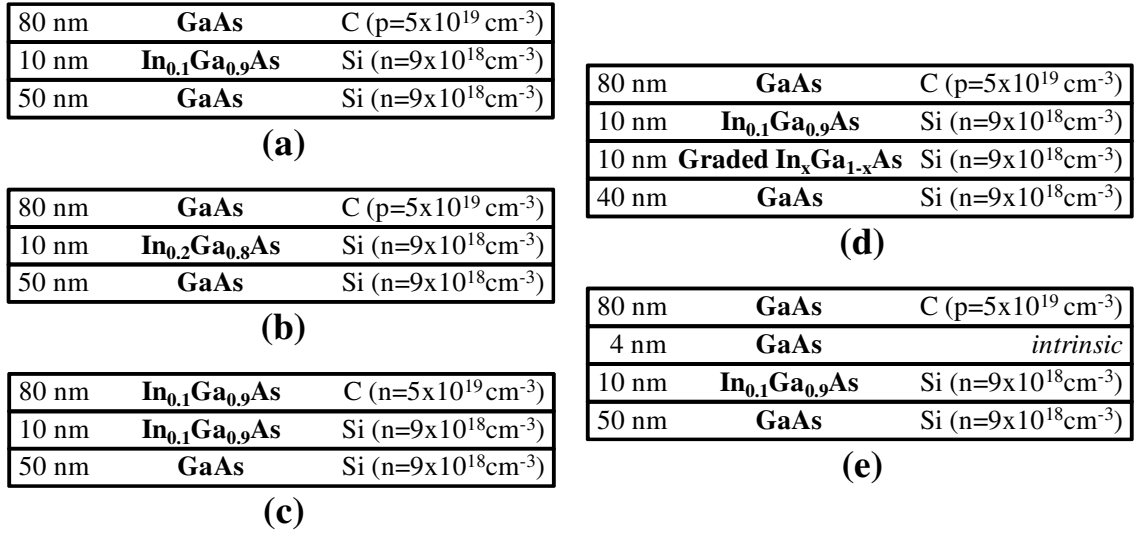


Fig. 4.9: Schematic diagrams of GaAs/InGaAs TDs. All four structures have the same nominal doping concentrations and film thicknesses. Each structure systematically varies material composition; (a) TD1 is a replica of Richard, *et al.* [13], (b) TD2 is a replica of TD1 but with 20% In mole fraction, (c) TD3 contains 10% In on both sides of the junction, (d) TD4 employs a graded heterojunction from 0% to 10% In, and (e) TD5 is a replica of TD1 with a nominally intrinsic GaAs layer inserted between the n- and p-type layers.

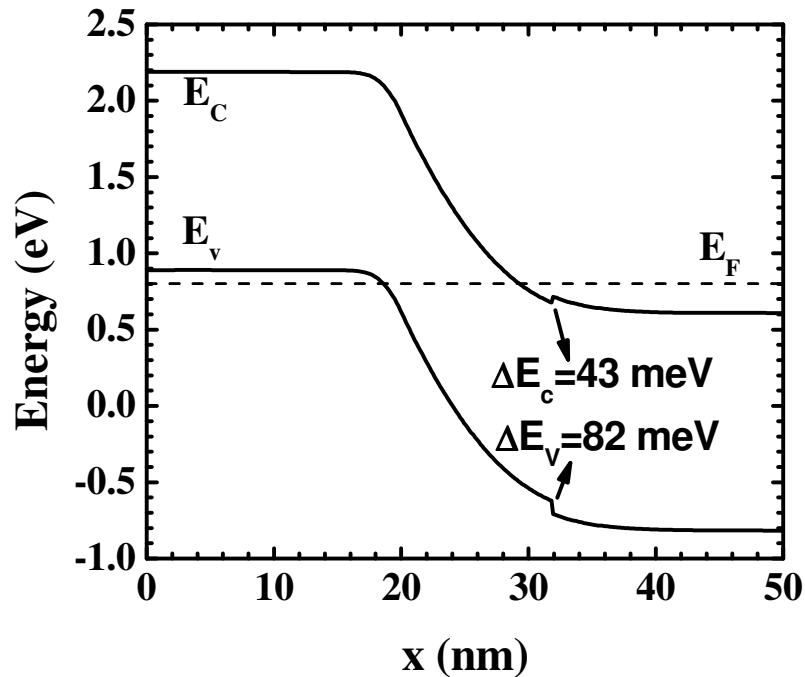


Fig. 4.10: Band diagram of TD3 calculated via OMEN, provided in collaboration with M. Luisier and G. Klimeck from Purdue University. The $\text{In}_{0.1}\text{Ga}_{0.9}\text{As}$ layer is assumed to be biaxially strained.

A series of five GaAs device structures adopted from Richard, *et al.* [13] were grown by MOCVD atop the previously described virtual-Ge substrate (~800 nm), with one example shown in Fig. 4.8. Recall that the virtual-Ge substrate is undoped, and therefore highly resistive. Therefore, a 500 nm thick, n-type GaAs layer was grown directly on top of the Ge providing a low resistivity layer which is used as a virtual ground for electrical measurements. Beneficially, additional dislocations were terminated at the hetero-interface (Fig. 4.8a). The tunnel junction itself (TD1: p-GaAs/n-In_{0.1}Ga_{0.9}As/n-GaAs) is shown in a high resolution TEM in Fig. 4.8b. As can be seen, the layers form a regular diamond crystal with smooth, well defined, sharp hetero-interfaces. From the TEM images, the epitaxial layers look like high quality crystalline semiconductors.

Five separate TD structures were grown, Fig. 4.9, and comprise a study centered around the effects of material composition and hetero-junctions on final device characteristics. All of the structures targeted the same dopant species (C and Si), concentrations ($5 \times 10^{19}/\text{cm}^3$ and $9 \times 10^{18}/\text{cm}^3$, respectively), and total layer thicknesses (80 nm and 60 nm, respectively). All five structures were grown on virtual-Ge substrates integrated on Si via ART. However, some of the structures were also grown directly on Si and GaAs substrates in order to compare electrical results of (i) highly defected epitaxy (directly on Si), (ii) high quality virtual substrates (ART), and (iii) lattice matched substrates (directly on GaAs). TD1 (Fig. 4.9a) is the base structure (duplicating T. A. Richard, *et al.* [13]), places a type I GaAs/InGaAs heterojunction at the tunnel junction. The second structure, TD2 (Fig. 4.9b), increases the In mole fraction to 20%. TD3 (Fig. 4.9c) incases the p/n junction entirely within an In_{0.1}Ga_{0.9}As layer. TD4 (Fig. 4.9c) attempts to minimize the type I band alignments, and thus eliminate additional quantum wells and tunnel barriers, by gradually grading the In content from 0% to 10% over 10 nm. Finally, TD5 is a repeat of TD1 with a 4 nm nominally intrinsic layer inserted at the p-n junction.

A copy of TD1 and TD5 were grown directly on Si substrates (TD1-Si and TD5-Si), no ART or graded buffers. Due to the large lattice mismatch ($\sim 4\%$), the TDD is expected to be very high ($\geq 2 \times 10^9 / \text{cm}^3$) providing extra leakage paths across the tunnel junction. As a result, it is

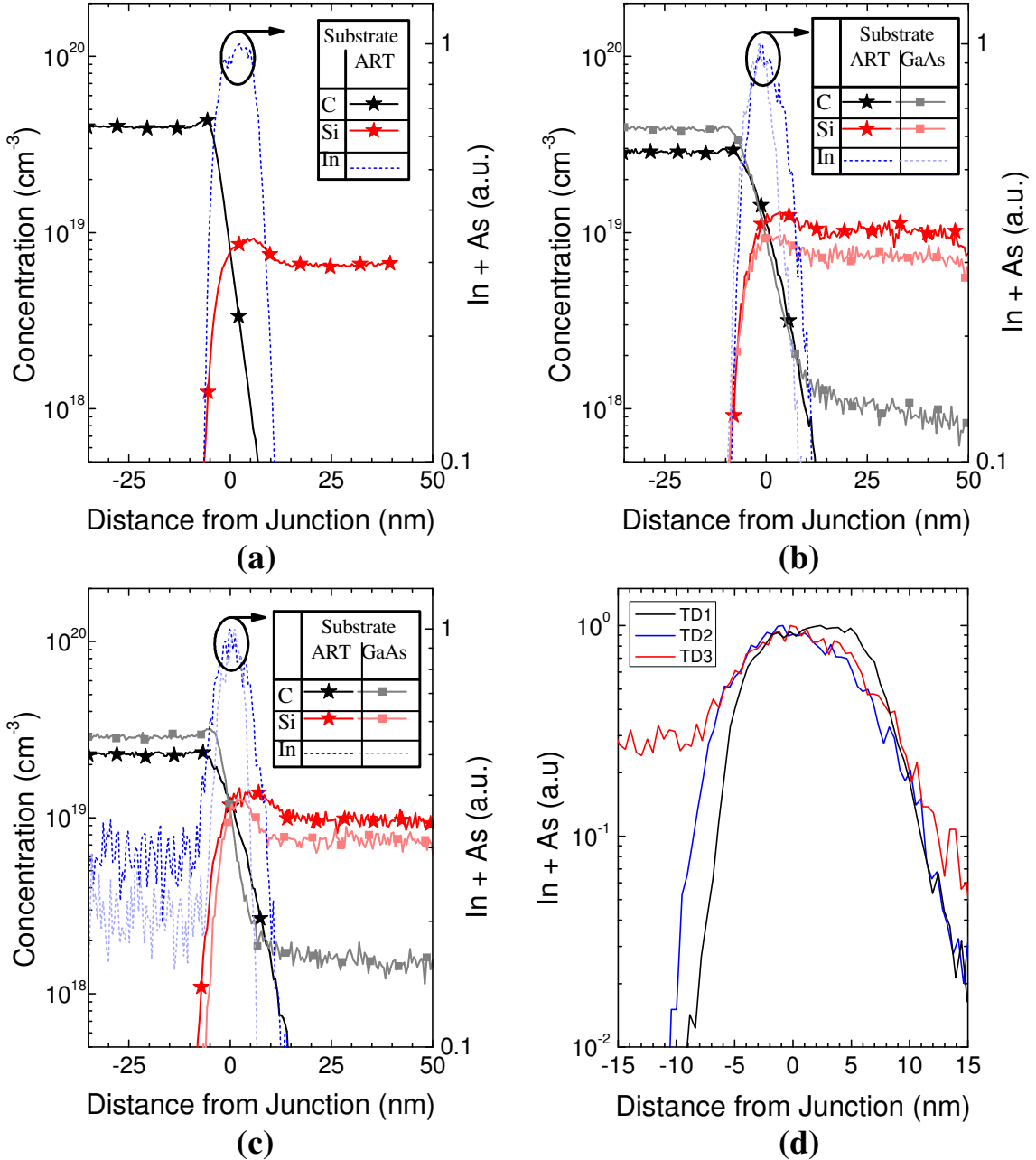


Fig. 4.11: SIMS analysis of C (p-type), Si (n-type) concentrations, and In/As normalized count. Includes results for (a) TD1, (b) TD2 and TD2-GaAs, and (c) TD3 and TD3-GaAs. Finally, (d) is included for direct comparison of In layer location.

expected that these devices will have poor electrical characteristics. Specifically, there should be a dramatic reduction in PVCR, if present at all, and similar or greater magnitude in J_p . Additionally, simultaneous growths of TD2 and TD3 were performed on directly GaAs substrates (TD2-GaAs and TD3-GaAs). Since GaAs substrates are the ideal starting substrates for these TDs, these TDs are expected to have similar, if not better, performance than their counterparts grown on ART substrates. Specifically, J_p should be approximately the same and potentially a lower J_v (increased PVCR) due to a smaller excess current resulting from few defects.

SIMS analysis was used to accurately assess dopant concentrations (Table 4.1 and Fig. 4.11) and the location of the InGaAs layer (Fig. 4.11). However, limitations in resources restricted the analysis to five of the nine structures grown: TD1, TD2, TD2-GaAs, TD3, and TD3-GaAs. The maximum measured doping concentrations adjacent to the tunnel junction (within ~7 nm) ranged approximately 1.7x for C (2.43 to 4.33 $\times 10^{19}$ /cm³) and Si (9.26 to 14.7 $\times 10^{18}$ /cm³), with the reduced average doping remaining fairly constant between 7.63 to 9.16 $\times 10^{18}$ /cm³ (~1.2x). For TD2-GaAs and TD3-GaAs, there is a residual C concentration in the bottom n-type layer, due to the trimethylgallium precursor. One would expect that there would be little variation in J_p due to doping concentrations. However, the magnitude of the minority dopant (providing the minority carriers) is less than, but comparable in magnitude to the primary dopant (providing the majority carriers) near the metallurgical junction. Therefore, counter

Table 4.1: Doping concentrations as measured by SIMS. Middle columns are maximum absolute values measured adjacent to the tunnel junction. Right hand columns are the maximum compensated values; IC-Sil.

Device ($\times 10^{18}$ /cm ³)	Max. Absolute Value			Max. Abs(Si-C) Value		
	C	Si	N*	C	Si	N*
TD1	43.3	9.26	7.63	43.1	8.50	7.10
TD2	29.8	13.0	9.05	29.7	10.7	7.87
TD2-GaAs	40.4	9.71	7.83	40.0	6.80	5.81
TD3	24.3	14.7	9.16	23.6	11.4	7.69
TD3-GaAs	31.8	12.8	9.13	31.0	9.11	7.04

doping effects were taken into account by using the maximum IC-Sil. As a result the doping ranges were reduced to, 2.36 to 4.31 $\times 10^{19}$ /cm³ (~1.8x) for C, 6.80 to 11.4 $\times 10^{18}$ /cm³ (~1.7x) for C, and 5.81 to 7.87 $\times 10^{18}$ /cm³ (~1.4x) for N*. From the modeling results calculated in the previous chapter, J_p is expected to range about 10x, assuming no significant strain effects and homojunction behavior.

Also of interest is the thickness and location of the InGaAs layers. The SIMS analysis had no calibration standard for In. Therefore relative counts/sec. were reported instead of the mole fraction, indicating the location, if not the magnitude of the InGaAs layer. Clearly, the thickness of the InGaAs layer is thinner for the devices grown directly on GaAs substrates (Fig. 4.11b-c) by 3 nm and 6.5 nm for the TD2 and TD3 series, respectively. This indicates that there were a significant differences in the growth interactions between the virtual-GaAs and regular GaAs substrates. As a result, it is expected that TD2 and TD3 will have a larger J_p than TD2-GaAs and TD3-GaAs. However, it is not obvious the effects this will have on the PVCR, which is the main indicator being utilized in this study to qualify crystal quality of the epitaxial layers. Additionally, Fig. 4.11d shows that there is only ~2.5 nm difference in the thickness and location of the InGaAs layers for TD1, TD2, and TD3. This is surprising, since TD3 was design to maintain a 10% InGaAs throughout the entire 80 nm p-type layer. TD3 will still likely have a greater current density than TD1, due to its slightly larger doping density, somewhat thicker In layer, and a non-zero In content in the bulk p-type layer. TD2 should have the largest current densities due to its much larger, but unquantified, In content.

If the growth results are similar for rest of the samples, TD4 should have a current density between TD1 and TD2, thanks to its graded junction removing the extra tunnel barriers. TD5 may also see an increased current density due to the intrinsic layer separating the peak dopant concentrations, minimizing counter doping effects. However, it is extremely difficult to predict the effects that will be measured on PVCR.

4.4.1. Basic Fabrication Process

After the epitaxial layers are grown, the samples are prepared for thermal activation anneals, which are typically needed with CVD based growths. Thermal annealing helps to fully activate the dopants and remove H_2 from the crystal lattice. Increased dopant activation increases both J_p and PVCR, whereas H_2 removal only increases PVCR by reducing J_v . The anneals were performed using an AG 610 Rapid Thermal Processor (RTP), in an N_2 ambient. Temperature was ramped at $\sim 100^\circ\text{C}/\text{sec}$. up to a target temperature, where it was held constant for five minutes, and finally air cooled back to room temperature.

After annealing, the samples were coated with a dual resist layer stack consisting of $\sim 1.1 \mu\text{m}$ of photoresist (PR) on $\sim 400 \text{ nm}$ of LOR 5A (a non-photoactive lift-off resist). The LOR 5A was baked at 180°C for 60 sec., before the PR was coated. The PR was baked for 60 sec. at 90°C . Then, the samples were imaged using a Karl Suss MA150 contact aligner for approximately 25 sec. Finally, the resist stack was developed in CD26 developer for ~ 2 minutes, then rinsed in DI H_2O for ~ 60 seconds. At this point a series of contact holes are formed in the resist stack, with a large undercut present in the LOR 5A layer, as shown in Fig. 4.12a.

Immediately before metal deposition, the sample surface was cleaned using a $\text{HCl}:\text{H}_2\text{O}$ (1:10) solution for 10 seconds. Blanket $\text{Au}/\text{Zn}/\text{Au}$ (20nm/20nm/200nm) metal contacts were thermally evaporated. The shelf-like undercut profile of the resist stack was designed to act as a shadow mask (Fig. 4.12b). The excess contact metal (deposited on top of the PR) was lifted off by soaking the samples in a heated ($\sim 90^\circ\text{C}$) Remover PG bath until completion. After a one

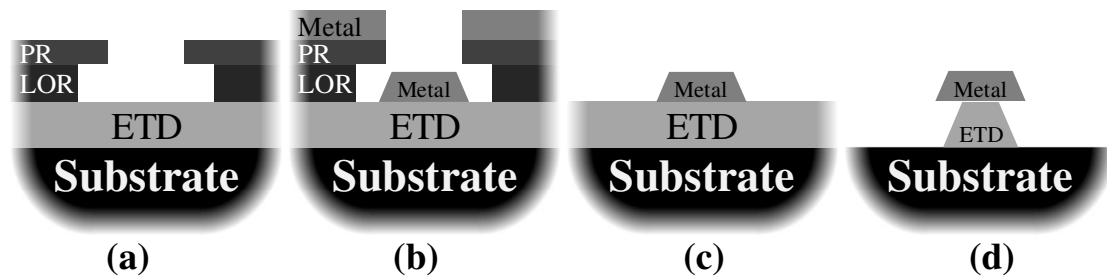


Fig. 4.12: Schematic diagrams showing the basic TD process flow; (a) lift-off resist profile post develop, (b) metal deposition, (c) post metal lift-off, and (d) mesa isolation etch.

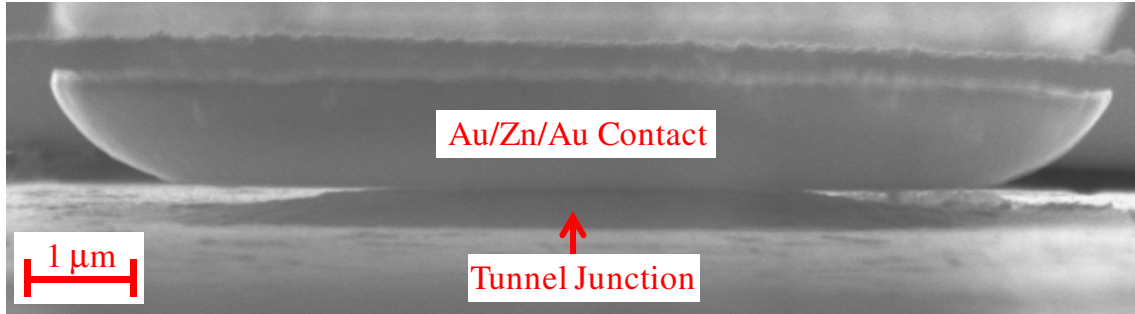


Fig. 4.13: High angle SEM image of GaAs TD on ART substrate. The large undercut ($\sim 2 \mu\text{m}$ on a side) clearly visible is due to the aggressive mesa isolation etch.

minute rinse in DI H_2O , only metal contacts remained on the surface (Fig. 4.12c). Finally, the contact metal was used as a self-aligned etch mask. An $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1:8:80) acid bath was used to etch the GaAs/InGaAs layers in order to electrically isolate the tunnel junctions. The final result was a series of electrically isolated tunnel junctions (Fig. 4.12d), whose cross-sectional area is primarily determined by the metal contact geometry and etch time.

Given its aggressive nature, the tunnel junctions were substantially undercut, which was assessed with high angle SEM inspection (Fig. 4.12). The measured undercuts and device diameters were used to estimate junction areas for accurate current density calculations. Electrical characterization was performed with a Keithley 4200 semiconductor parameter analyzer. Very large area diodes ($>100\times$) were used as virtual grounds for the device under test.

4.4.2. DC Electrical Results

First, an experiment was setup to determine the optimal thermal anneal temperature. Three TD1 samples were fabricated using the basic process previously described with (i) no anneal, (ii) 425°C anneal (following T. A. Richard, *et al.* [13]), and a 480°C anneal. Representative I-V characteristics for each sample is shown in Fig. 4.15. Each measurement was performed on the same size device for direct comparison. The PVCR made dramatic improvements from a minimum of 4, to a maximum of 24, back down to 18 for the “no anneal”, 425°C , and 480°C annealed samples, respectively. These results nearly match the previous GaAs

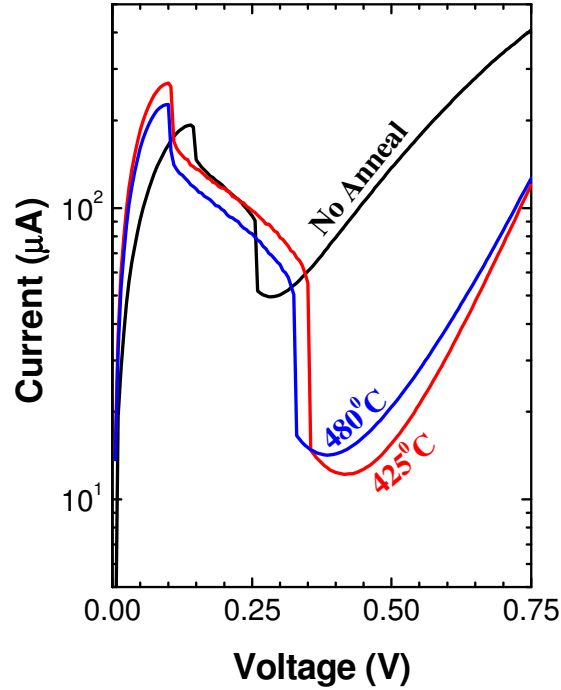


Fig. 4.14: Typical I-V characteristic of three TD1 samples with (i) no anneal (PVCR of 4), (ii) 425°C anneal (PVCR of 24), and (iii) 480°C anneal (PVCR of 18).

record PVCR of 25 [13], and surpassed the previous TD on Si record of 6 [8]. J_p follows a similar trend with the 425°C annealed sample exhibiting the largest current density. Therefore, of the tested conditions, 425°C was selected as the optimal anneal temperature. All of the following results use the optimized anneal temperature determined with this initial experiment.

Next, the effect of a 4 nm intrinsic layers (TD1 and TD5) and direct growth on Si (TD1-Si and TD5-Si) is examined. Shown in Fig. 4.15a are typical I-V characteristics for each device structures, all with similar device geometries. The on ART devices, TD1 and TD5, exhibit greater PVCRs of 24 and 11, respectively. The TDs grown directly on Si, TD1-Si and TD5-Si, have much smaller PVCRs of 3.9 and 4.4, respectively. These results indicate that there is a much greater density of defects for TDs grown on Si, as expected. This conclusion is additionally supported by the general trend of PVCR increasing when current density decreases (until $E_f \approx E_{C,v}$).

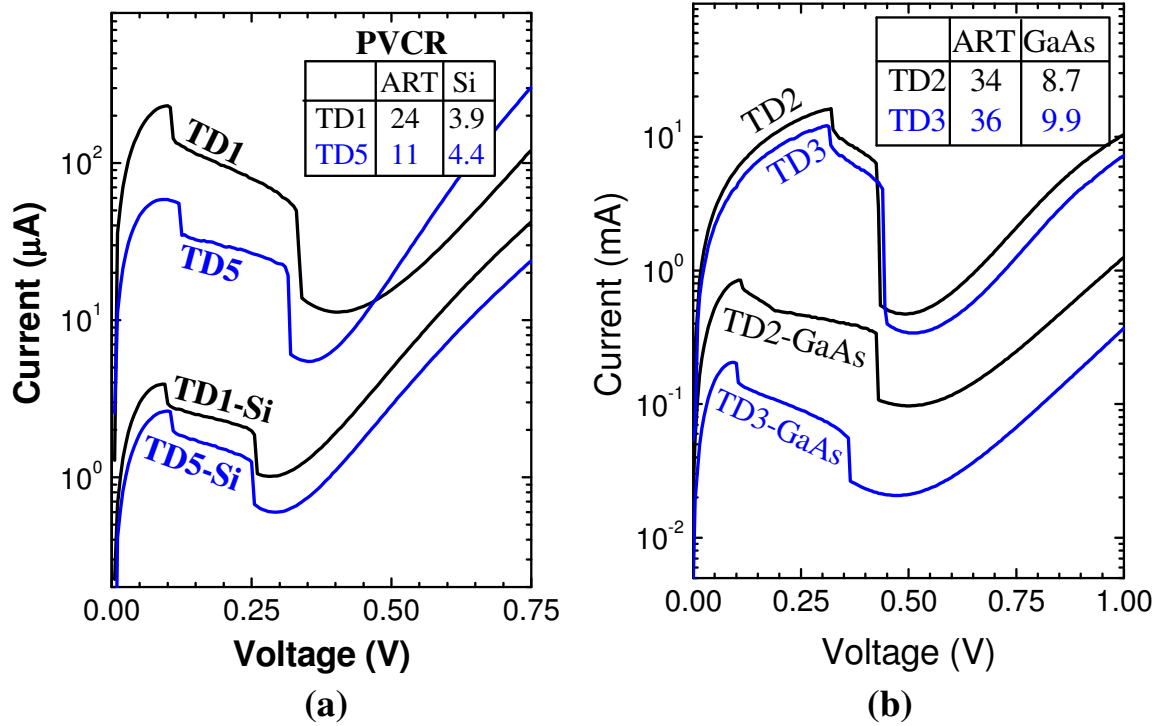


Fig. 4.15: Typical I-V characteristic of $\sim 30 \mu\text{m}$ radii devices for (a) TD1, TD5, TD1-Si, TD5-Si, and (b) TD2, TD3, TD2-GaAs, TD3-GaAs. Devices grown on virtual ART substrates exhibit much greater PVCR and Current, indicating high quality material quality.

The on ART structures (TD1 and TD5) exhibit much larger current magnitudes than TD1-Si and TD5-Si. This is due to smaller BTBT efficiency, likely a result of lower active doping concentrations. Since the devices were grown simultaneously, and fabricated in parallel, it is likely that different growth interactions resulted in slightly different junction structures. This would be similar to the differences between TD grown on ART versus on GaAs substrates detailed in the SIMS results in Section 4.3.

TD1 and TD1-Si have a slightly larger current than TD5 and TD5-Si, which may only be a function of small variations in maximum doping concentrations. Conversely, TD1 has a much larger PVCR than TD5. In fact, the PVCR of TD1 is 4x greater than the previous on Si record [8], and nearly matches the previous GaAs record [13]. Therefore, it does not appear that the inserted intrinsic layer beneficially impacted the I-V characteristics. Furthermore, the virtual

ART substrates provide very high quality semiconductors on which to fabricate devices with highly competitive electrical characteristics.

The next set of experiments (Fig. 4.15b) look at changing the In mole fraction (TD2), the placement of InGaAs (TD3), as well as comparison with simultaneous growths on GaAs substrates (TD2-GaAs and TD3-GaAs). Again, it is immediately apparent that the on ART devices (TD2 and TD3) have much greater PVCRs (34 and 36, respectively) even though the comparison devices were grown directly on GaAs substrates (TD2-GaAs/8.7 and TD3-GaAs/9.9). The CVD epitaxy growth conditions were optimized for the ART substrates. As previously discussed, the SIMS results (Fig. 4.11) clearly show subtle but significant differences between the on ART and on GaAs growths. However, these results do not verify the quality of the epitaxy. In fact, the electrical results would indicate that ART optimized growths will yield poor epitaxial layers on other substrates. The results does not assert that the ART substrates are inherently better than GaAs substrates. That said, TD2 and TD3 surpass previous POCR records for (i) Si substrates and separately for (ii) GaAs based TDs. Furthermore, this supports the claim that high quality semiconductors can be integrated on Si. Specifically, this has been shown here using ART as the integration method.

The current density in the on ART devices is much greater than in the on GaAs. From the SIMS results, Fig. 4.11, it is known that the doping concentrations are slightly reduced and the InGaAs layer is significantly smaller. It is reasonable that those features would significantly reduce the current density. Unexpectedly, TD2-GaAs has a much greater current density than TD3-GaAs even though the former has a much smaller average reduced doping, according to SIMS. This may be an indication of the effect of greater In content in the InGaAs layer. This is supported by a mildly large apparent current measured in TD2 versus TD3.

To better understand the relationship between J_p and doping, the measured values were plotted in Fig. 4.16, along with calculated trendlines for unstrained homojunction TDs using Kane's model [60] as discussed in the previous chapter. It will be shown in the following

chapters that the model accurately predicts InGaAs TD performance. Therefore, it is a good way to benchmark the performance of the fabricated devices.

First, it is apparent that the measured current densities are much greater than the predicted values. Recall that these TDs are under strain and have complex band alignments due to the heterojunction. Therefore they were expected to have larger than predicted current densities. However, TD2 and TD3 are on the 40% In line, with J_p nearly 100x greater than expected. Furthermore, the J_p for TD2 and TD3 are nearly the same, even though the calculated strain for TD2 is ~6.4%, more than 9x larger than TD3. In other words, it is not apparent what the tremendous boost in current density is due to. Secondly, the characteristic trendline encompassing TD1, TD2, TD3, TD2-GaAs, and TD3-GaAs is much steeper slope than predicted the trendlines predicted by the model. This would seem to indicate that these TDs are much more sensitive to doping variations than InGaAs homojunctions. In part, this is due to variations in the

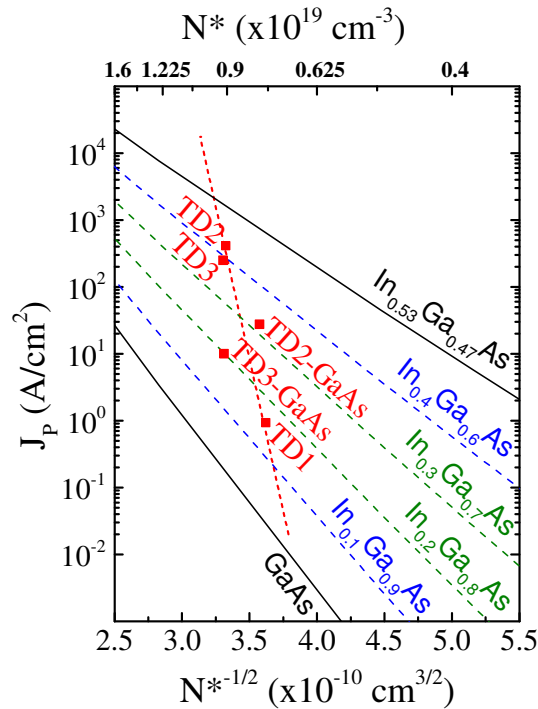


Fig. 4.16: Benchmarking of J_p vs. reduced doping (N^*) for TD1, TD2, TD3, TD2-GaAs, and TD3-GaAs. Measured data is plotted against unstrained InGaAs homojunction trendlines, calculated using Kane's [60] (discussed in the previous chapter, and shown to be accurate in the following chapter). Measured J_p is up to 100x predicted magnitude, with a much steeper trendline.

grown epitaxy layers. For each original TD structures, a much larger study consisting of at least three additional TD growths would be needed, wherein only the doping concentrations were varied. However, structures with steep trendlines may improve SS for TFETs.

High angle SEM inspection of the surface of mesa isolation etched samples revealed a large number of circular trenches, Fig. 4.17. These trenches are etch highlighted defects that propagated from the virtual substrates and through the epitaxy growths. Clearly, from Fig. 4.17, the epitaxial layers are not perfect. These defects will act as tiny shorts, mainly increasing valley currents, thereby reducing calculated PVCs. However, scaling device geometries to smaller dimensions will reduce the number of defects present within the device. Eventually the devices will begin to “miss” the defects, and form between them, thereby maximizing the PVC. Given resolution constraints of contact lithography, the smallest device junctions achieved were approximately 3.5 μm in diameter.

The I-V characteristics with the largest PVCs for TD1, TD2, TD3, and TD4 all occurred with the smallest device sizes, and are shown in Fig. 4.18a. TD4, no previous electrical results discussed, has a maximum PVC of 10. It is believed that the graded InGaAs junction successfully removed any additional tunnel barriers and quantum wells from the TD’s band

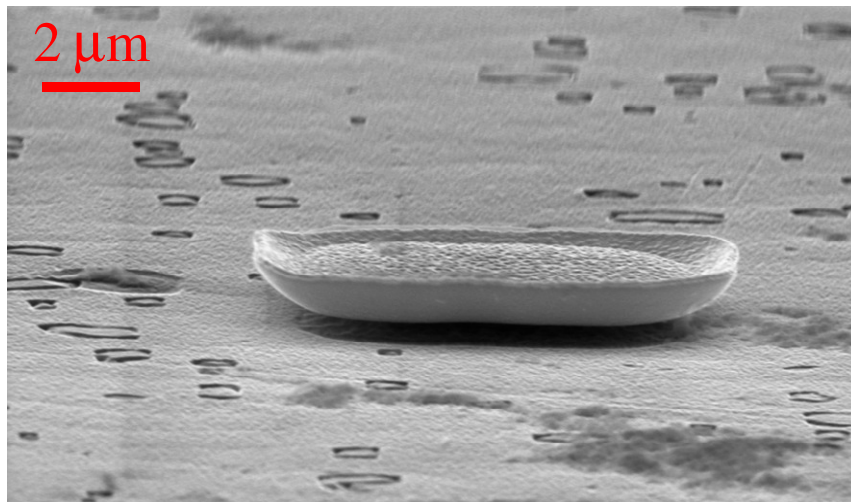


Fig. 4.17: High angle (82°) SEM image of mesa isolation etched TD3. As highlighted by the wet chemical etch, the surface is marked by many large defects (there may be smaller ones not visible here). These defects would tend to degrade device performance.

structures. This did help maintain larger current densities. However, those extra band features tend to filter out excess valley current. As a result, the PVCR was negatively impacted.

Additionally, the TDs were benchmarked against of key TDs reported in literature, Fig. 4.18b and Table 4.2. As can be seen, the TDs fabricated for this study follow the typical trend of sacrificing current density for improved PVCR. The PVCR of TD1 improved by a few points to 27, which surpasses the previous GaAs record of 25 [13]. TD2 made a large improvement in PVCR up to 43 from its previous 34. However, the greatest improvement was measured in TD3 with a record PVCR of 56, which is a 56% improvement. Consequentially, TD3 is measured to have the largest PVCR of any previously reported (i) InGaAs TD or any (ii) TD fabricated on a Si substrate. Additionally, (iii) it is the 3rd largest PVCR ever reported [15, 17]. However, the measured PVCRs did not plateau, indicating that smaller device geometries could yield even larger values (see Section 4.6).

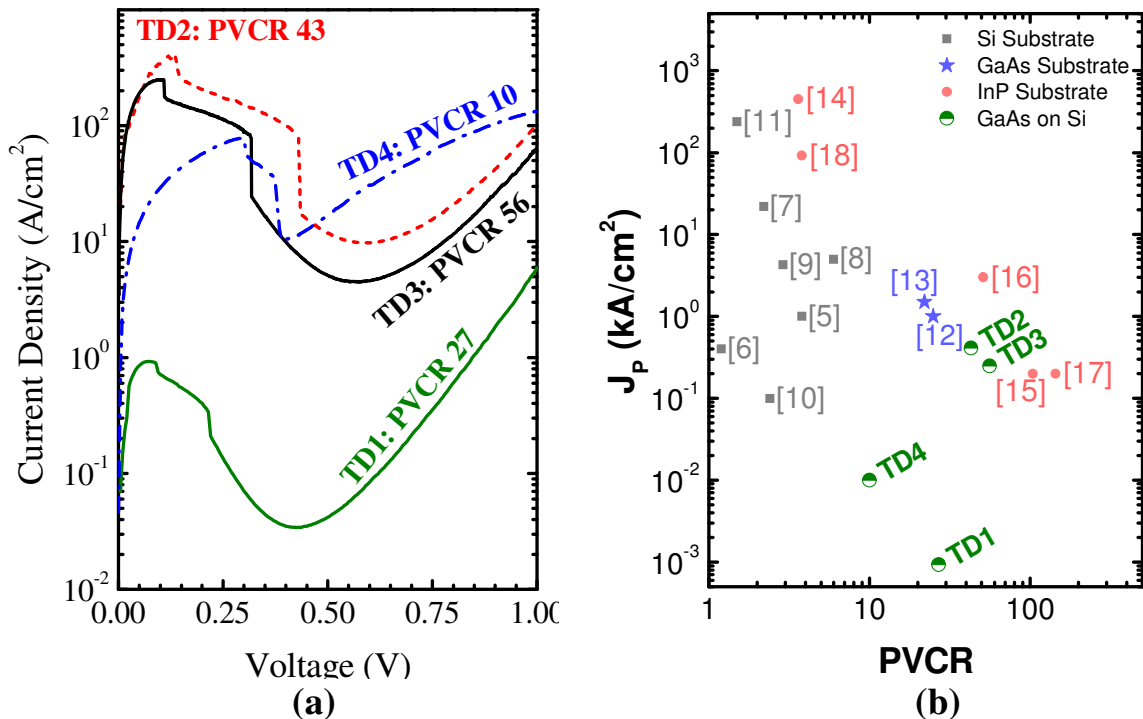


Fig. 4.18: (a) I-V characteristics with the best PVCR's measured for TD1, TD2, TD3, and TD4. (b) Benchmarking of TD1, TD2, TD3, and TD4 against key TDs in literature [5-18]. TD3 has the 3rd largest PVCR over all and the largest of all GaAs TD or TD on a Si substrate

Table 4.2: TD1, TD2, TD3, and TD4 parameters as well as the highest reported PVCRC TDs fabricated on Si, GaAs, and InP substrates.

Type	Substrate	Tunnel Diode	Growth Technique	Jp (A/cm ²)	PVCR	Study
RITD	Si	Si/SiGe	MBE	5000	6	[8] Eberl, 2001
RTD	Si	Si/SiGe	MBE	218,000	3	[11] Chung, 2006
Esaki	GaAs	P ⁺ /N ⁺ GaAs	Alloy	N/A	25	[12] Holonyak, 1960
Esaki	GaAs	GaAs/In _{0.1} Ga _{0.9} As	MOCVD	1500	22	[13] Richard, 1993
RITD	InP	InGaAs/InAlAs	MBE	200	104	[15] Day, 1993
RITD	InP	InGaAs/InAlAs	MBE	200	144	[17] Tsai, 1994
Esaki	Si	GaAs(P⁺) In_{0.1}Ga_{0.9}As(N⁺)	UHVCVD/ MOCVD	9	27	[4] TD1
Esaki	Si	GaAs(P⁺) In_{0.2}Ga_{0.8}As(N⁺)	UHVCVD/ MOCVD	1000	43	[4] TD2
Esaki	Si	In_{0.1}Ga_{0.9}As	UHVCVD/ MOCVD	250	56	[4] TD3
Esaki	Si	GaAs(P⁺) In_{0.1}Ga_{0.9}As(N⁺)	UHVCVD/ MOCVD	65	8	[4] TD4

4.4.3. Temperature Analysis

Many temperature studies of III-V Esaki diodes have been detailed since the 1960s [12, 61, 62]. These reports have focused on alloy junction devices, where localized liquid phase epitaxy is used to introduce a degenerate doping via a carrier metal to a host crystal sometimes resulting in a hump current due to the inclusion of the carrier metal [12, 61]. Devices doped by epitaxy as studied here are not expected to show this sort of defect. However, it was theorized that the integration of III-V on Si could result in unique defects not described in previous publications. In this study, the (i) temperature dependence of these devices, (ii) the insensitivity of tunnel current (forward and Zener) to temperature, and (iii) the absence of mid-gap states in the excess current have been reported.

From Kane's model [60], there is no direct temperature effect on the current density of direct bandgap TDs unlike standard diodes and the SS of CMOS. However, the bandgap and effective mass, both of which affect other material parameters, have a small dependence on

temperature. However, without knowing the rate of change for effective mass with temperature, the model predicts J_p will increase only $\sim 40\%$ per 100°C rise. A previous GaAs, alloy junction, TD reported by Holonyak, *et al.* [12], described a complicated relationship wherein J_p initial increased with temperature, and then began decreasing with temperature at approximately 300 K. At lower temperatures J_p is increasing due to the decrease in bandgap energy (tunnel barrier height). However, after the temperature is increased past some critical value mainly determined by doping concentrations, increases in the density of states will begin limiting E_F . This will make it appear as the diode is doped less at room temperature and therefore, it will have a smaller current density. On the other hand, J_v will always tend to increase with temperature. This is due to the excess current utilizing thermal/phonon energy to help “hop” into and then out of the bandgap, via defect states. Also, sidewall leakage currents will increase with temperature too.

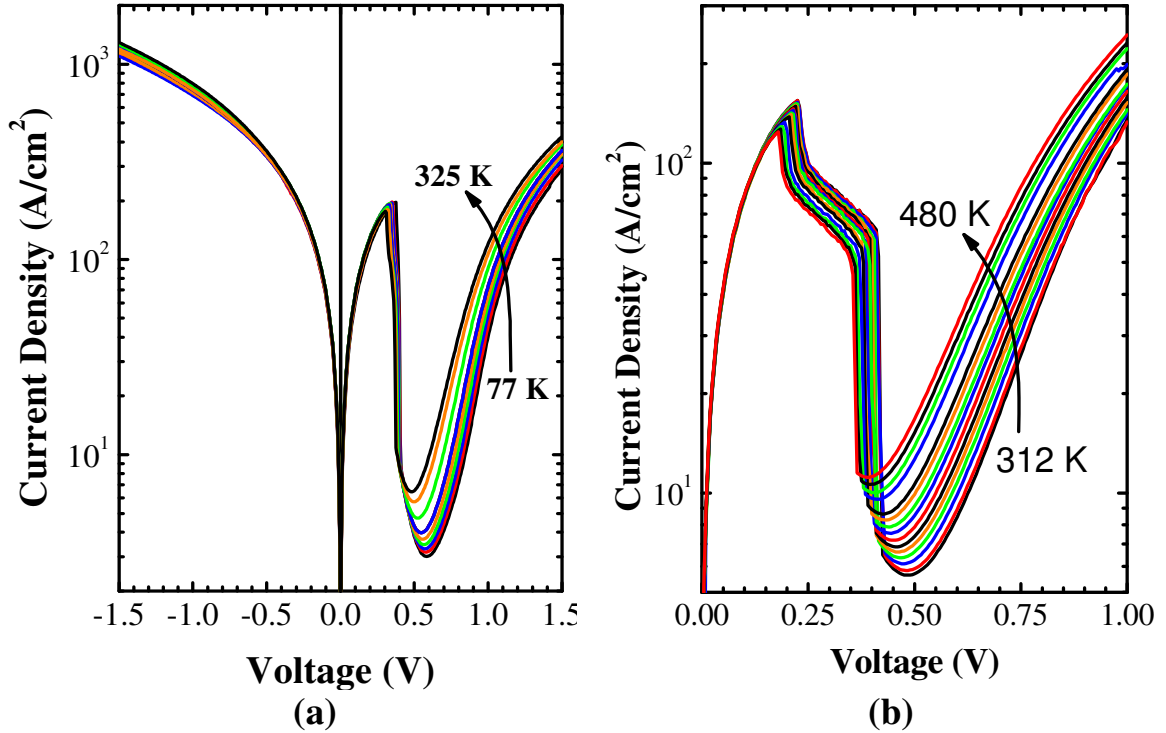


Fig. 4.19: Measured I-V characteristics of TD3 at (a) low temperatures (77 K to 325 K) and (b) high temperatures (312 K to 480 K). Contrary to the model prediction, J_p decreased with temperature. However, J_v increased and J_{Zener} remained fairly constant.

Due to temperature range constraints, two separate measurement setups were used. Low temperature measurements (room temperature down to ~ 77 K) were performed on an SPA system, whereas high temperature (up to $\sim 200^\circ\text{C}$) measurements utilized a Keithley 4200

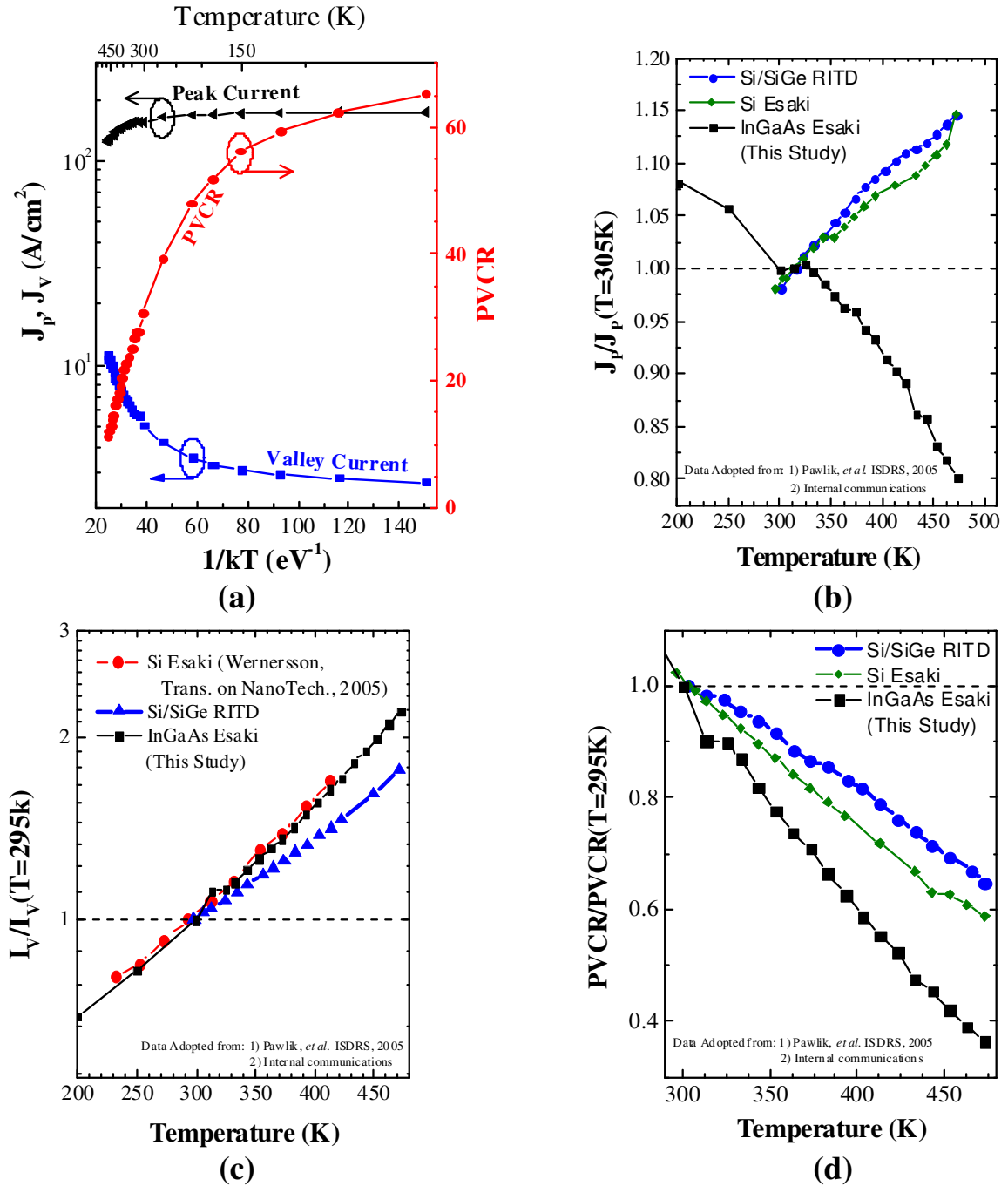


Fig. 4.20: (a) J_p , J_v , and PVCRC versus $1/kT$. Most of the variation occurs at high temperatures with J_v . The other three graphs are normalized (b) J_p , (c) J_v , and (d) PVCRC versus temperature for direct comparison with Si TD.

parameter analyzer. Due to constraints of the probe stations, large area devices ($\sim 32 \mu\text{m}$ diameter) were probed. As expected, the room temperature PVCRCR was limited to ~ 31 , instead of the previous maximum value of 56.

The measured I-V characteristics for the (a) low and (b) high temperature measurements are shown in Fig. 4.19. Due to differences in the probe setup, the low temperature measurements have a larger series resistance. There is very little variation in the Zener current density (J_{Zener}). Interestingly, J_p decreased with temperature over the entire range, which went against the modeling prediction. Therefore, changes in the effective mass and density of states must be playing a dominant role. As expected, J_v increased with temperature. However, no hump current was observed in the post valley characteristics, indicating that there are few midgap states present [46].

To more clearly follow the trend of the key TD parameters J_p , J_v , and PVCRCR have been plotted against $1/kT$, Fig. 4.20a. A small kink in the data can be seen at the switch between low and high temperatures measurements, due to changing between the two separate measurement systems. The PVCRCR ranges from 11 to 65. The range for J_p and J_v was measured to be 125 A/cm^2 to 150 A/cm^2 and 11 A/cm^2 to 2.7 A/cm^2 , respectively. The majority of the variation occurred at temperatures above 300 K. However, the almost negligible change in current density over the 400 K temperature range indicates that J_p is nearly a pure BTBT current. On the other hand, J_v increased a substantial $\sim 4x$ above 200 K. However, an Arrhenius extraction of the valley current taken at the valley voltage (V_v) exhibited an activation energy of 1.8 meV for low temperatures, indicative of a purely quantum mechanical tunneling mechanism.

The key TD parameters were normalized with its own value at room temperature, Fig. 4.20b-d, order to compare with Si and Si/SiGe TD measurements [63]. As expected, J_p for the Si based devices increases with temperature. The percent change is also less than that observed for TD3. Note, that the observed kink in GaAs is due to switching between measurement setups. The valley current for all of the Si and GaAs TDs increased and nearly at the same rate. This

result is another pointer at the high quality nature of the epitaxy grown on ART. Finally, as expected from the previous results, the PVCR of GaAs decreases more rapidly than the Si devices. This is mainly due to the inherent decrease in J_P over the temperature range.

As evidenced in Fig. 4.20, a thermally activated process is present in J_V . To further elucidate this process, the temperature dependent current was extracted for various voltages above the valley voltage (Fig. 4.21a). As indicated by J_P , J_{ZENER} does not show significant temperature dependence indicating high purity BTBT. However, at progressively larger biases beyond V_V , the current density increases more rapidly. Eventually, the current would be dominated by thermal processes.

$$J_{Excess} = J_0 \times \exp\left(\frac{V_a}{nkT}\right) \quad (4.1)$$

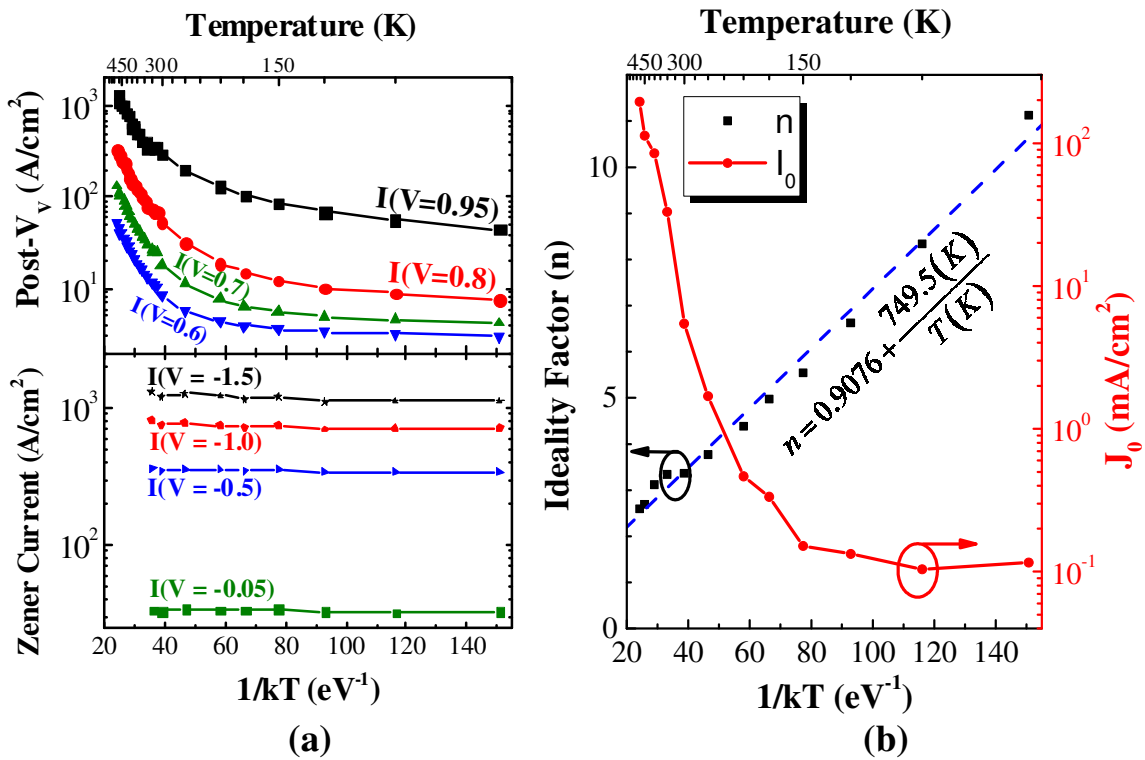


Fig. 4.21: Left (a) is measured current density versus temperature for various voltages. On the right (b) is extracted ideality factors and x-intercepts versus temperature.

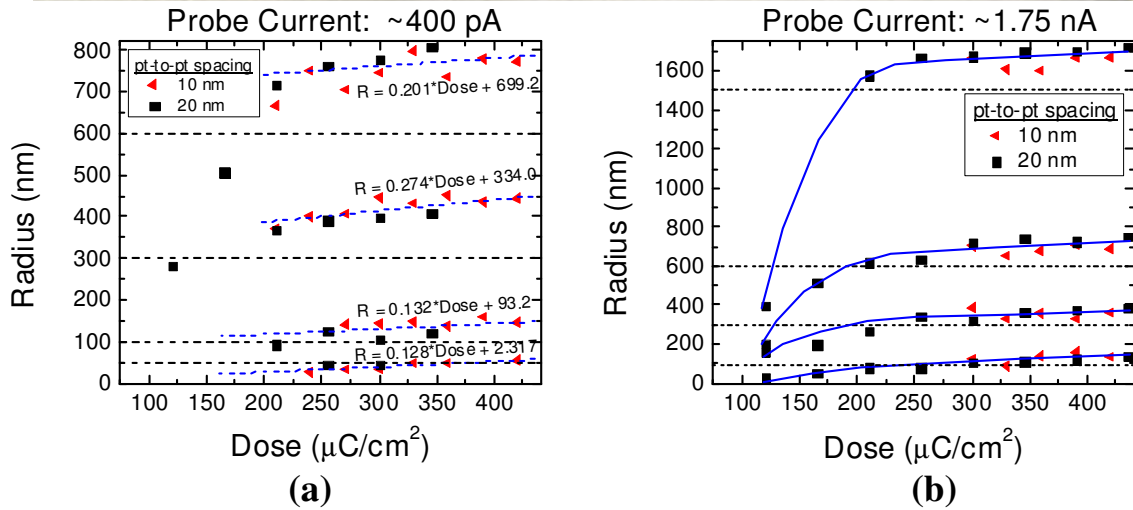
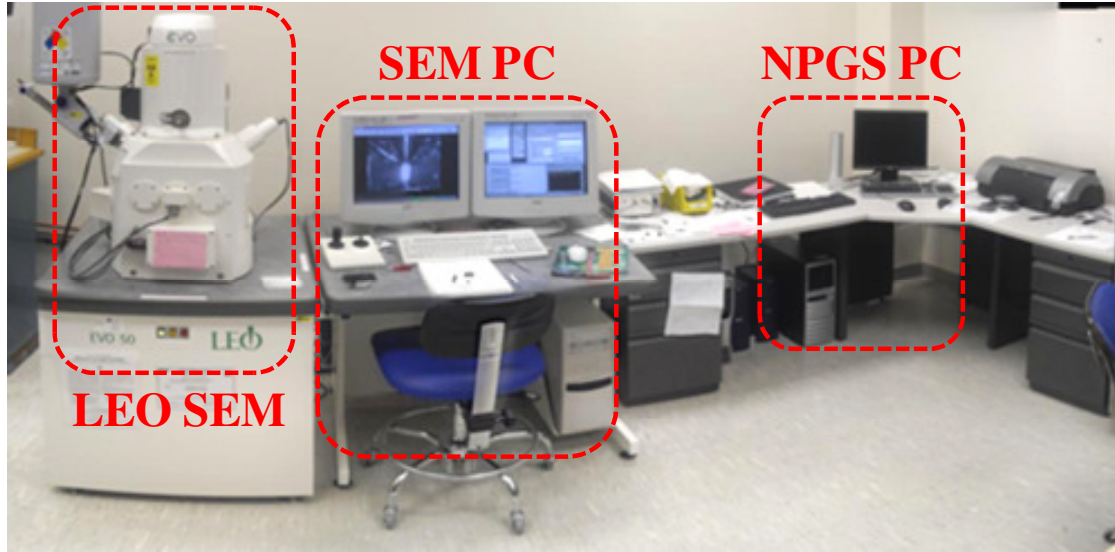


Fig. 4.22: The top picture of the Leo EVO 50 sample SEM and NPGS PC used for this work. On the bottom are measured feature size versus exposure dose for (a) low beam currents ($\sim 400 \text{ pA}$) and (b) large beam currents ($\sim 1.75 \text{ nA}$).

Using the standard excess current equation of a TD (4.1), ideality factors (n) and x -intercepts (J_0) were extracted and graphed in Fig. 4.21b. The ideality factor varies linearly from 2 to 12 via $n = 0.908 + 749.5/T$. Above $\sim 150 \text{ K}$, the excess current mechanism is dominated by a series of thermal processes (e.g., thermionic hole and electron emission over the respective band offsets) which cannot be uniquely deconvolved from the present data. Furthermore, the data clearly reveals that the ART growth of the III-V diode on Si did not introduce mid-gap states as the data is consistent with prior reports of Si and GaAs Esaki diodes.

4.4.4. Deeply Scaled Tunnel Junctions

Up to this point, all of the TDs have been large with radii no smaller than 3 μm . It has already been shown that scaling the junction down has improved the characteristics. However, many have theorized that eventually sidewall leakage effects would begin to dominate the characteristics, and degrade performance. Additionally, if tunnel junctions are to be used on commercial products, they will likely need to be scaled to similar dimensions as the transistor they are integrated with or replacing. To that end, the current fabrication process was expanded to fabricate and electrically test deeply scaled tunnel junctions.

The new fabrication process starts after the mesa isolation etch step from the original process. However, to achieve the ultra-small dimensions desired, electron beam (e-beam) lithography was developed and implemented for this work. To replace the standard PR, a positive e-beam resist (PMMA 950k) was used. A LEO Evo 50 sample SEM system (Fig. 4.22) was installed with a Nano Pattern Generation System (NPGS), which controls the SEM in write mode and drives the e-beam to generate desired layout patterns. A series of test writes were initially performed in order to optimize the e-beam lithography process. The acceleration bias was held constant at 20 kV for all writes, a gold standard was used to tune the beam, and a Faraday cup and pico-ammeter was used to measure probe currents. However, before tuning the beam, the system was warmed up for no less than 1 hour. After meticulously focusing onto the sample surface several exposure dose matrices were created, developed, and inspected. The first set used a low beam current (~ 400 pA) and looked at measured radii of 50nm, 100nm, 300nm, and 600nm versus exposure dose (Fig. 4.22a). The second set used a large beam current (~ 1.75 nA) for mask defined radii of 100nm, 300nm, 600nm, and 1500nm (Fig. 4.22). Each beam current used two different point-to-point spacing exposure settings; (i) 10 nm and (ii) 20 nm. There was no statistically significant difference between the two point-to-point settings, with the bulk of the noise in the data attributed to focus variations. Additionally, the rate in change of

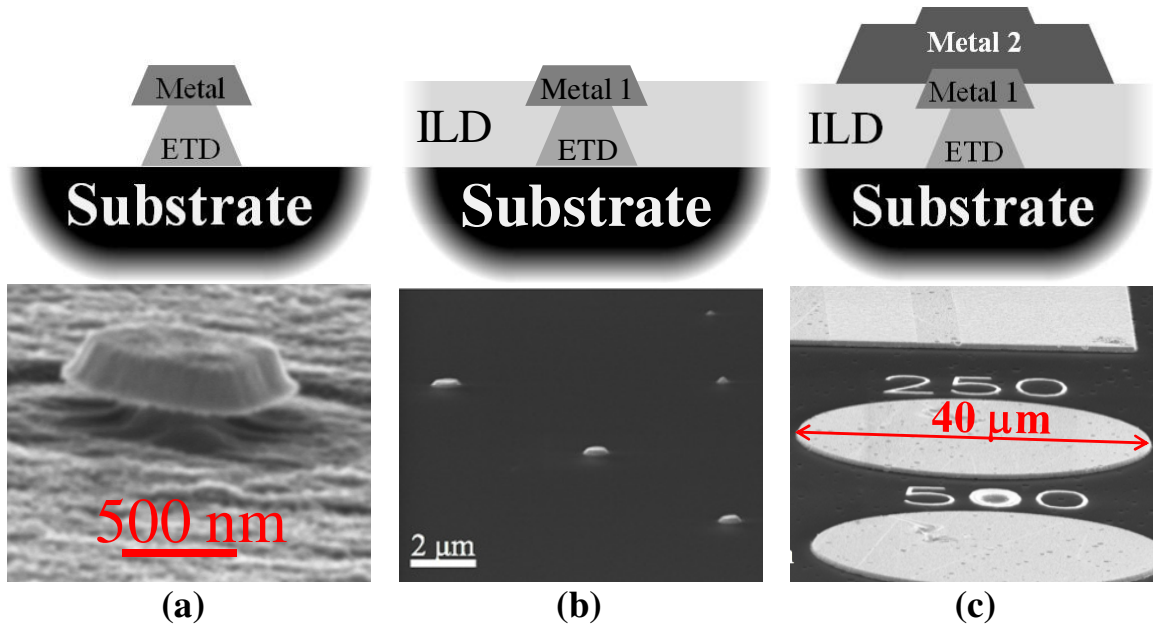


Fig. 4.23: Schematic diagram (top) and high angle SEM images (bottom) of the sub-micron fabrication process after (a) mesa isolation, (b) BCB planarization and etchback, and (c) metal 2 deposition and liftoff.

the measured radii leveled off at $\sim 200 \mu\text{C}/\text{cm}^2$, regardless of beam current. However, for added margin of error, typical exposure doses were set to $300 \mu\text{C}/\text{cm}^2$.

As with the original fabrication process, metal 1 was used as the mesa isolation etch mask. Therefore, metal 1 was required to be scaled sub-micron dimensions so that the tunnel junction itself would achieve the desired size. One typical example is shown in Fig. 4.24a. However, it was not possible to directly probe the formed contact thus requiring a two metal layer process, with an inter-layer dielectric (ILD) in between.

After the mesa isolation etch, the sample was spin coated with bis-benzocyclobutene (BCB) which is a low- K spin on dielectric. The BCB was coated to a thickness of $\sim 1.5 \mu\text{m}$, encapsulating all features by more than $1 \mu\text{m}$, and then baked at 140°C for five minute followed by a cure at 250°C for 60 min. in an N_2 ambient. The resultant sample surface was smooth and flat, with only gradual variations across the entire sample surface. To access the metal 1 contacts, the BCB was isotropically etched back using a 1:4 $\text{O}_2:\text{SF}_6$ dry plasma etch. Initially, fast etches (high power) were used to get within a few 100 nm of the contact metal. Then, slow etches (low

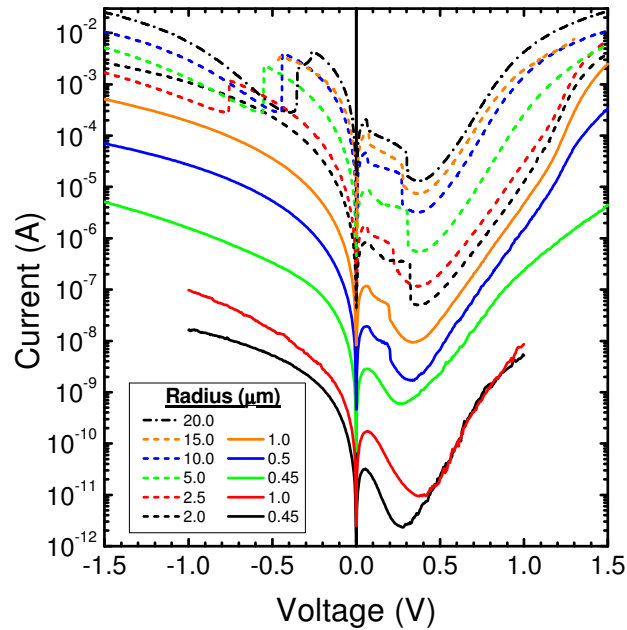


Fig. 4.24: Measured I-V characteristics of TD1 scaled to deep submicron dimensions. I_p ranged eight orders of magnitude, indicating a large range in device dimensions.

power) were used to precisely dial in the final BCB film thickness. Ideally, half of the contact metal thickness would be exposed, encapsulating the sample surface and tunnel junction within the insulative BCB (Fig. 4.24b). Finally, large (40 μm radii) probe pads were patterned and aligned to the metal 1 contact pads using a second e-beam lithography and metal deposition (Fig. 4.24c).

Electrical characterization proceeded using the Keithley 4200 parameter analyzer. Due to the very large area tunnel junction used as a virtual ground, NDR was measured in reverse bias for the larger tunnel junctions under test. Additionally, due to the aggressive nature of the mesa isolation etch, there is a large range in device dimension for each mask defined radii. Therefore, the measured I-V characteristics (Fig. 4.24) show I_p ranging eight orders of magnitude. Some of measured currents were much smaller than expected. The smallest I_p measured was 32 pA, which comes to a calculated radii of 16nm. This assumes that the $4 \text{ A/cm}^2 J_p$ calculated from larger devices with known junction areas does not change over the wide range of currents.

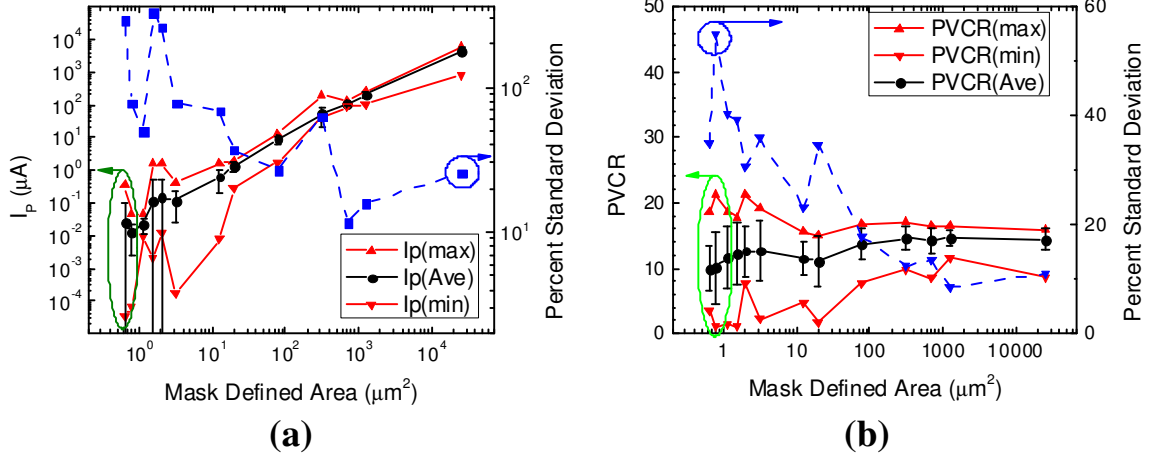


Fig. 4.25: Measured (a) I_p and (b) PVCR versus mask defined area for deep sub-micron scaled TD1 junctions. Due to noise in the actual junction areas, the maximum, average, minimum, and standard deviation of each size is shown.

Both I_p and PVCR were plotted versus mask defined area (Fig. 4.25) in order to quantify the scalability of the tunnel junctions. The average I_p trendline best represents how well the BTBT current scaled with area, and is mostly linear. The slope of the line yields a J_p of $\sim 4 \text{ A/cm}^2$, slightly larger than previously estimated. The standard deviation in I_p increases as the junctions are scaled, which is due to variations in junction areas being effected by lithography and mesa isolation etch deviations across the sample. In following studies, junction uncertainty is minimized by inspecting mesa undercuts and metal 1 dimensions with SEM imaging.

Contrary to previous studies, the average PVCR slightly degrades from 12 to 10 when the junctions are scaled, Fig. 4.25b. However, the maximum PVCR is a better measure of the ultimate capabilities achievable, and it shows a fairly steady improvement 16 to 21. The accumulated results from this study indicates that tunnel junctions can be scaled to ultra small dimension without significant degradation in performance. However, a robust fabrication process is needed in order to obtain consistent and reliable results. Furthermore, the development of the submicron process is critical for characterizing the ultra high BTBT current density ETDs discussed in Chapters 5 and 6.

4.5. Conclusions

Ge and GaAs semiconductor material systems were integrated on Si substrates via ART. Virtual substrates formed by ART have been shown to reduce TDD by over 1,000x, compared to direct epitaxial growth on Si substrates. However, those results do not confirm the electrical quality of the virtual substrates. As a new method for hetero-integration of high quality crystalline materials, a series ETD Structures were fabricated and electrically tested in

The first set of ETD devices utilized alloy junction formation. In a thermal anneal fabrication process, Al was alloyed with n⁺-type Ge virtual substrates. Optimal annealing conditions were found to be 825°C for five minutes, resulting in a maximum PVCR of 1.1 and a J_p of 4.1 kA/cm². The results are commensurate with results on Ge substrates from literature [55, 64], and therefore indicate that the virtual substrates are of high quality.

Following the Ge ETD study, a series of five GaAs/In_{1-x}Ga_xAs were grown on a GaAs-on-Ge ART virtual substrate. Two additional companion ETDs were grown directly on Si, with two more on a GaAs substrate for direct comparison of ideal and worst case results. A new fabrication process was developed for these structures, and serves as the foundation for all ETD structures afterwards. The optimal dopant activation anneal is 425°C for five minute anneal, and resulted in a maximum PVCR of 24 for TD1, which is just below the previous GaAs record of 25 for which this structure was designed after [13] and far beyond the on Si record of 6 [8].

The affect of a 4 nm *i*-layer was studied in TD1 and TD5, as well as direct growth on Si substrates with their companion pieces; TD1-Si and TD5-Si. There respective PVCRs were measured to be 24, 11, 3.9, and 4.4 respectively. The on ART devices had much large PVCR, adding more evidence to the high quality nature of the virtual substrates. Furthermore, TD1 (without *i*-layer) also had a large J_p than TD5 (with *i*-layer), for both the on ART and on Si substrate cases, indicating that the *i*-layer did not improve the ETD electrostatic properties.

The following study increased the In mole fraction to 20% (TD2) and surrounded the p-n junction entirely within a 10% InGaAs layer (TD3). The PVCR of these structures were greatly

improved to 34 and 36, respectively, surpassing the previous GaAs results. Interestingly, the control companion ETDs (TD2-GaAs and TD3-GaAs) exhibited much smaller PVCR of 8.7 and 9.9, respectively. It was determined from SIMS that there was a significant difference in the final device structure, which may have negatively impacted the PVCR, and certainly reduced the J_p for TD2-GaAs and TD3-GaAs. Interestingly, even though they had similar doping concentrations, TD2 had a large J_p than TD3 indicating that the increased In concentration improved BTBT efficiency. The introduction of a In concentration grading reduced PVCR to 10, but had a much larger J_p than TD1. In fact, TD2, TD3, and TD4 all had J_p much greater than predicted by Kane [60], when compared with characteristic homojunction trendlines calculated using the Kane model program discussed in Chapter 3. Finally, further testing revealed devices with PVCR of 43 and 56 for TD2 and TD3, respectively. The PVCR for TD3 is the third largest value reported in literature, strongly indicating that the ART virtual substrates are of very high quality.

High and low temperature (77 K up to 473 K) measurements was performed. J_p decreased slightly with temperature, indicating that it is an almost pure BTBT characteristics. J_v increased with temperature, at a slightly faster rate than J_p . An Arrhenius extraction of from the change in J_v with temperature yielded an activation energy of 1.8 meV, which is nearly negligible. Furthermore, the excess current exhibited a relatively small ideality factor of ~ 3 .

The final study in this chapter developed a deep sub-micron fabrication process, based off of the basic fabrication process. The new process required the development and characterization of an e-beam lithography process, enabling the fabrication of devices down to 50 nm radii. With the new process, TD3 was scaled down to deep submicron dimensions in order to investigate the scaling properties of ETD structures. The average I_p versus junction area was linear, indicating negligible surface leakage currents. Furthermore, in this study the maximum PVCR increased from 16 to 21 as the junctions were scaled. The improvement in PVCR is largely due to improved (smaller) J_v , showing that the substrate is very high quality, but not perfect.

In general, the results from this chapter show that ART can be used to provide high quality virtual substrates on Si, without the need for large graded buffers or substrate transfer processes. Furthermore, defect related leakage currents were not directly observed in the high PVCN ETD structures, indicating that ART provides mechanically and electrically high quality virtual substrates. This conclusion is largely supported by the record high PVCN values achieved, and the small observed variations with temperature. Additionally, the deeply scaled ETD junctions showed no significant signs of surface leakage effects, and actually exhibited improved PVCN.

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CHAPTER 5

In_{0.53}Ga_{0.47}As Esaki Tunnel Diodes

The previous chapter established that high quality virtual substrates can be integrated on Si via ART. Furthermore, the electrostatic qualities of the virtual substrates were verified with high PVCR GaAs/InGaAs ETDs [1-4] and directly benchmarked against a wide variety of ETDs from literature [5-18]. Because of the limited availability of ART virtual substrates, the following work will investigate In_{0.53}Ga_{0.47}As ETDs [18-24], which were fabricated on lattice matched substrates (InP). Additionally, ETDs will be designed and grown as homojunctions to avoid the confounding effects of strain, heterojunction band alignments, and multiple effective masses. Standardizing ETD structures to a basic p⁺-i-n⁻ diode with fixed layer thicknesses and nominally rectangular doping profiles enables direct mapping and modeling of BTBT behavior over a large design space. This methodology may then be used to design structures with targeted characteristics, such as maximizing BTBT current density (tunneling probability). In particular, this work is geared towards optimizing the Source/Body junction of a TFET for improved on-state current density. Therefore, it is important to learn how to maximize BTBT probabilities and current densities.

Additionally, device characteristics from ETDs based off of the standard layer structure are ideal for calibrating BTBT models, including the Kane model [25] discussed in Chapter 3. Typically, BTBT models are calibrated to no more than a couple specific devices covering a limited range device designs. Also, the models often use of various fitting parameters, which may change in a nonphysical way from structure to structure. However, with the guidelines and methods developed in this work, BTBT characteristics can be efficiently investigated over a large design space. The results of which will then be available for model calibrations, adding higher confidence to the quantitative predictions made by those same models.

In this chapter, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ homojunction ETDs will be grown on lattice matched InP substrates. $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ was chosen for a multitude of reasons. (1) It is a direct bandgap semiconductor with very well known material parameters. (2) It has a small effective electron mass and moderate bandgap (~ 0.74 eV) which may allow it to achieve very large BTBT current densities while suppressing unwanted excess tunnel currents. Additionally, (3) there are many sources for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxy, with a large knowledge set and experience in growing very high quality layers with ultra-high doping concentrations ($\sim 10^{20}$ / cm^3) and sharp doping profiles. As such, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is an ideal starting material system to (i) develop the initial experimental procedure, (ii) characterize a large design space using doping concentrations as the control variable, (iii) optimize and achieve greater BTBT current densities, and (iv) apply the Kane model for the entire experiment.

Additionally, there has been much discussion over the scalability of BTBT junctions. There are two main concerns. First, it is not known if surface leakage effects will increase and begin to dominate device characteristics the tunnel junctions are scaled to smaller dimensions. In an ETD, this would be seen as an increase in J_V and decrease in PVCR. If Fermi-level pinning is involved, J_P may also be affected. In a TFET, I_{Off} would increase and the gate would lose electrostatic control. The second concern is carrier quantization effects. A reduction in the standard 3D DOS when confined to 2D or 1D may substantially reduce, or alter, BTBT current densities.

Specifically in this chapter, fabrication and characterization of six distinct $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETD structures is discussed. The low to medium J_P structures only required the standard fabrication process. However, two ultra-high J_P ETDs utilize an improved deep sub-micron process. As such, the scaling properties of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ BTBT are investigated on structures most appropriate for TFETs. Combining these results from other experimental results in literature [18-24], a characteristic trendline for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETDs is established, which relates J_P to doping concentration. Additionally, the Kane model is compared to each devices structure,

and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ characteristic trendline. Ideal band diagrams are also examined for an improved understanding in the theory of operation for the ETD devices.

5.1. Ultra High Current Density $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Esaki Diodes

As before, the ETDs were designed with the p-type layer on top of the n-type layer. In order to improve the doping profiles a thin 3 nm intrinsic layer (*i*-layer) was inserted in the middle of the structure, forming a p-*i*-n diode (Fig. 5.1a). This spacer layer separates the two doping profiles, minimizing doping compensation at the metallurgical junction, thereby maximizing the effectiveness of N_A and N_D . Recall from Section 4.3 that the maximum compensated carrier concentrations adjacent to the tunnel junction was reduced by up to 30%. Additionally, the doping profiles at the p-n junction will be much shaper. The improved doping profiles and concentrations improve electrostatic characteristics of the ETD in two main ways. First, the improved non-compensated doping help increase the built-in voltage (V_{bi}) and decrease depletion widths. Unless the *i*-layer is too thick (typically ~3 nm in this work), the overall depletion width will be reduced, thereby increasing the BTBT current density. Second, there will be much fewer compensated, ionized, dopants near the tunnel junction providing additional

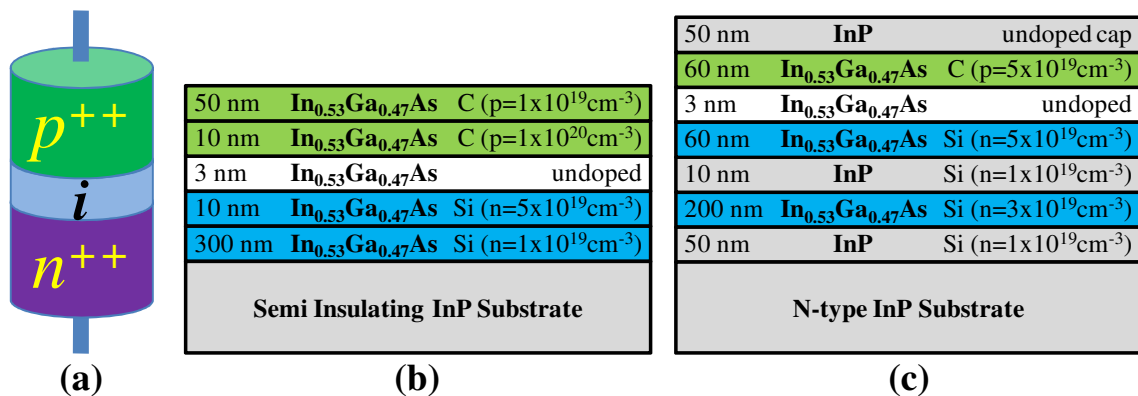


Fig. 5.1: Schematic diagrams of (a) basic p-*i*-n TD, (b) InGaAs-1, and (c) InGaAs-2. InGaAs-1 & -2 have same basic structure (p-*i*-n). To avoid growth defects for InGaAs-1 the maximum doping levels were kept within 10 nm of the junction. On InGaAs-2, a sacrificial InP capping layer protects the anode surface, and additional InP layers in the cathode act as etch stops.

recombination and scattering sites within the bandgap. With fewer defects in the tunnel junction, the excess current will be reduced, improving the ETD's PVCR. Achieving similar doping profile improvements in a TFET would enhance gate control, thereby improving I_{ON} and SS.

The highest doped sample, InGaAs-1 described in Fig. 5.1b, is expected to have the largest J_p . The structure was commercially grown at IQE using MBE, with C and Si as the p- and n-type dopants, respectively. The target doping concentrations for the tunnel junction itself was $10^{20}/\text{cm}^3$ (C) and $5 \times 10^{19}/\text{cm}^3$ (Si). However, to avoid negatively impacting the quality of the epitaxy, those doping concentrations were limited to two separate 10 nm layers surrounding the *i*-layer. These three layers are approximately 23 nm thick and easily contain the predicted ~11 nm depletion width (see Section 5.1.2), and therefore should not impact J_p . The top anode (p-layer) was kept thin (~60 nm) in order to help reduce parasitic series resistances (R_{Series}) and minimize undercut during mesa isolation etch for improved control over junction areas. Conversely, a thick (300 nm) cathode layer (n-type) was grown to help minimize R_{Series} . This was especially important since the structure was grown on a semi insulating (S.I.) InP substrate.

The second sample, InGaAs-2 illustrated in Fig. 5.1c, was grown by metal-organic MBE at Technion, Israel Institute of Technology, by Prof. D. Ritter [23]. The maximum achievable doping for the ETD was slightly less InGaAs-1. Therefore, the target C ($5 \times 10^{19}/\text{cm}^3$) and Si ($5 \times 10^{19}/\text{cm}^3$) concentrations were not limited to two small 10 nm layers. This helped to simplify the p-*i*-n junction and reduce R_{Series} . Additional measures to minimize R_p include an n-type substrate and a 200 nm thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer below the cathode. Three additional InP layers were included in the layer designed. The growth began with a doped InP layer in order to improve the quality of the following epitaxial layers. The second InP layer is placed as an etch stop, to help prevent over etching the ETDs. Finally, the top InP layer is a sacrificial cap which protects the anode surface during storage and is to be removed at the start of fabrication.

SIMS measurements were taken on both InGaAs-1 and InGaAs-2 for accurate assessment of the doping profile slope and maximum concentrations. Contrary to the targets, the C doping concentrations were comparable in magnitude at $9.8 \times 10^{19} / \text{cm}^3$ (InGaAs-1) and $8.6 \times 10^{19} / \text{cm}^3$ (InGaAs-2). Whereas the Si measured in InGaAs-1 was much larger than in InGaAs-2, at $7.4 \times 10^{19} / \text{cm}^3$ and $4.5 \times 10^{19} / \text{cm}^3$, respectively. From the SIMS data, it is also plain that InGaAs-1 has a much sharper doping profile than InGaAs-2, with C/Si slopes of 5.7/2.3 nm/dec and 8.1/15.4 nm/dec, respectively. Given the doping concentrations and junction profiles (to a lesser extent), InGaAs-1 should have a much greater J_p .

Because of the expected magnitude of current densities, and to continue studying the effect of scaling tunnel junction, InGaAs-1 and InGaAs-2 were fabricated using the deep submicron process discussed in Section 4.3.4. However, there were a few minor alterations made to the process. First, no dopant activation anneal was performed since they are rarely needed for MBE grown epitaxy. Therefore, processing began with a simple surface clean (10 seconds in a

		InGaAs-1		InGaAs-2	
		Doping			
		cm^{-3}		cm^{-3}	
C		9.8×10^{19}		8.6×10^{19}	
Si		7.4×10^{19}		4.5×10^{19}	
N*		4.2×10^{19}		3.0×10^{19}	
		Slope			
		nm/dec.		nm/dec.	
C		5.7		8.1	
Si		2.3		15.4	

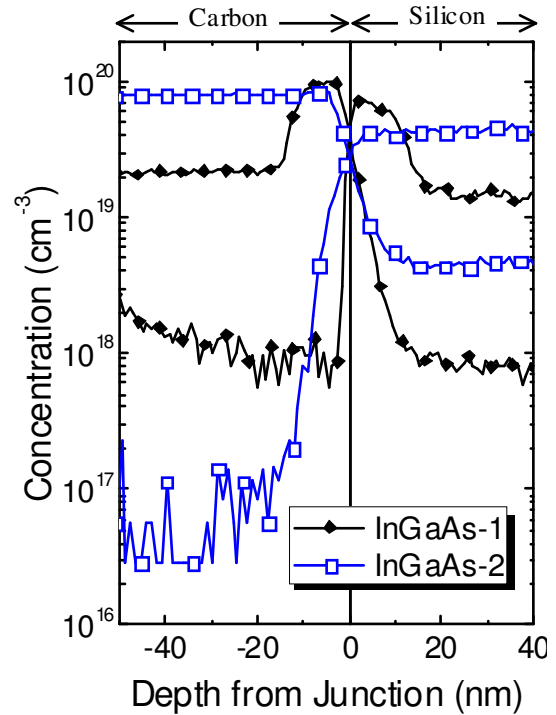


Fig. 5.2: (a) Maximum doping concentrations and profile slopes acquired from (b) SIMS measurements of InGaAs-1 and InGaAs-2.

10:1, HCl:H₂O mixture), followed by lithography level 1. However, InGaAs-2 first requires an InP cap etch in HCl:H₂O (1:1) for 60 seconds. Second, the mesa isolation etch used a citric Acid:H₂O:H₂O₂ acid bath, which is much slower (~1nm/minute) and more controllable. The acid bath itself is mixed in two steps. First, the citric acid:H₂O is mixed 1:1 by weight until the anhydrous citric acid crystals are fully dissolved, and the solution is back to room temperature. Then, immediately before needed, the citric acid/water solution is mixed with H₂O₂ at a 20:1 ratio by volume. This etch is also highly selective against InP.

The final alteration to the process is a tunnel junction area characterization step for improved accuracy when calculating current density. This step also utilized the LEO EVO 50 sample SEM. First, device cross-sections were analyzed with the sample tilted at least to ~87° (Fig. 5.3), thus negating the need to destructively cleave the sample. As is usually the case when chemically etching compound semiconductors, there are different etch profiles depending on the cross-section angle. For the case shown here (Fig. 5.3a), a vertical cut-line shows a cross-section with angled sidewalls (Fig. 5.3b). On the other hand, when looking at a horizontal cut-line, the cross-section the mesa sidewalls are nearly vertical (Fig. 5.3c). The mesa undercut values are taken from the bottom edge of the metal contact, to the mesa tunnel junction edge, located ~60 nm below the bottom of the metal. Using about a dozen measurements, average undercut

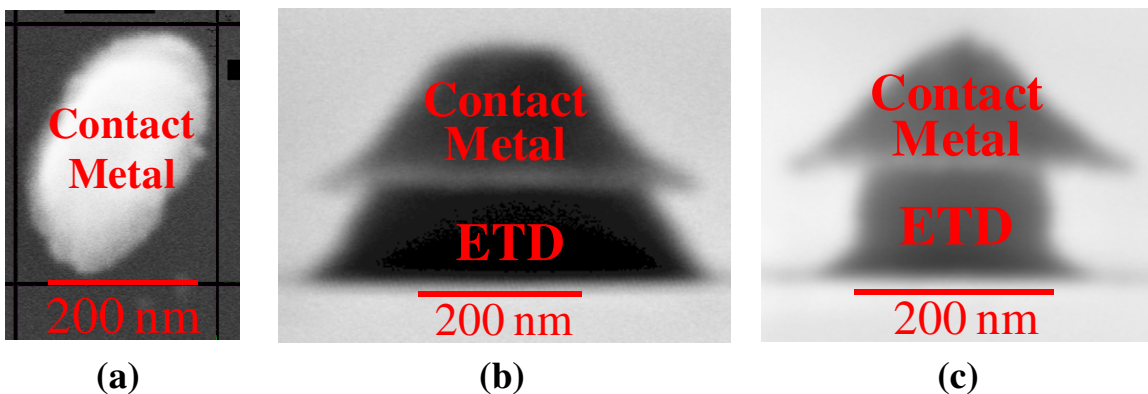


Fig. 5.3: SEM images of ETD after mesa isolation from a (a) top-down, (b) vertical cross-section, and (c) horizontal cross-section view points. Undercut values measured from bottom of contact metal to edge of mesa, 60 nm below contact metal (location of the metallurgical junction).

values are calculated for both the horizontal and vertical outline cross-sections. The undercut values are used to adjust the measured metal contact radii, which require a much more extensive analysis.

Due to process variations (such as drifting beam focus and beam current), each pattern size may have a large variation in printed dimensions across the sample surface. Therefore, the top down areas of each metal contact (below $\sim 2 \mu\text{m}$ radii) was measured in at least six different locations. With ~ 16 device sizes, this required at least ~ 100 images. An ImageJ macro (See

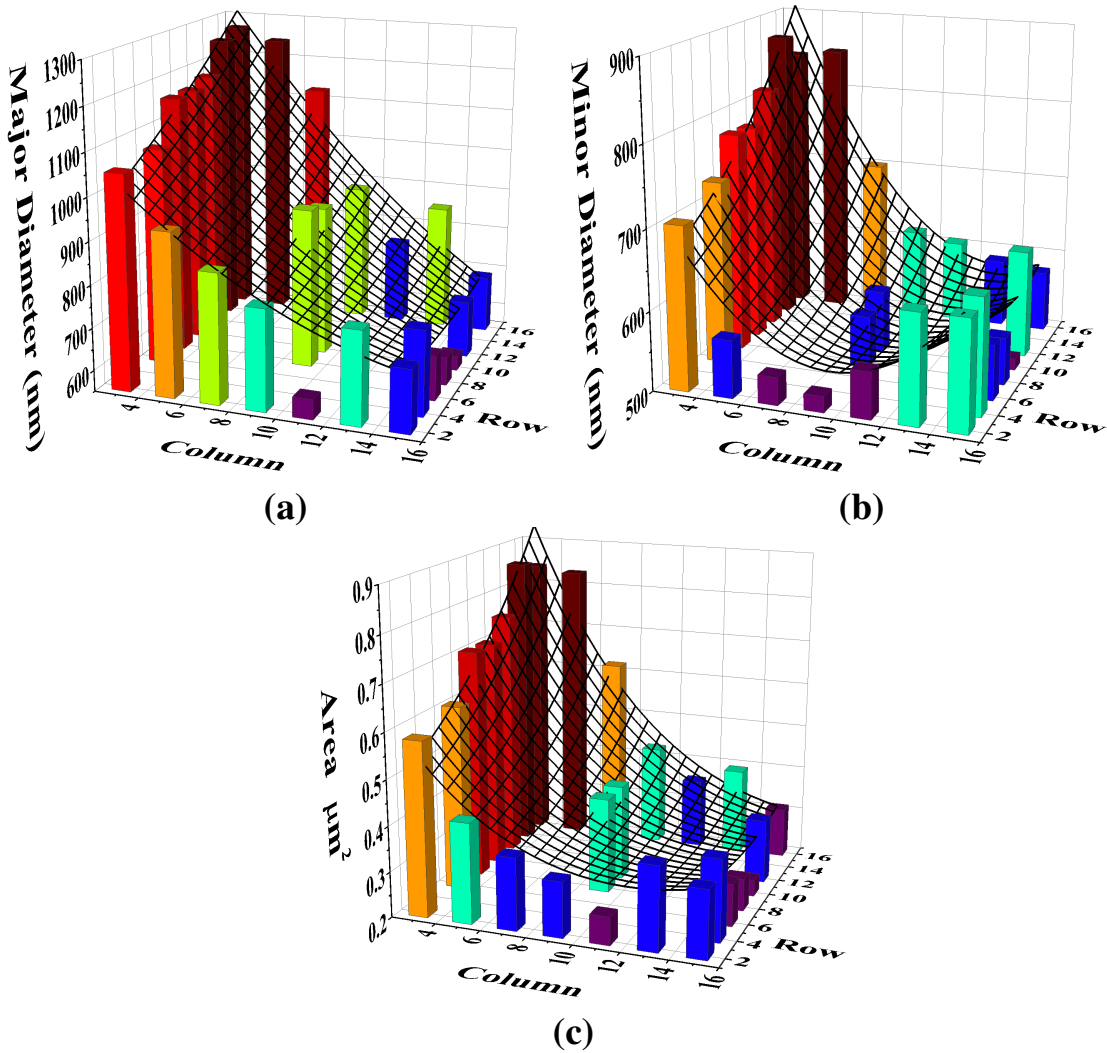


Fig. 5.4: Metal contact (a) major diameters, (b) minor diameters, and (c) areas across InGaAs-1 for 400 nm radii patterns. Major and Minor axis used a surface fit. Area surface was calculated from the surface fits.

appendix) was developed to semi-automate image analysis of the device dimensions. The program output is the major axis, minor axis, and angle of the least squares ellipse fit to the metal contacts. 3D bar plots of the measured major and minor axis (Fig. 5.4a, b) were used to visualize the systematic variations as well as generate a non-linear surface fits (5.1). The surface fits were used to calculate the metal contact areas, which were then compared with the measured areas (Fig. 5.4c) in order to confirm accuracy. Finally, the tunnel junction area of each device was calculated using (5.2). Even with all of the above area analysis, there is still some statistical variation in the junction areas. Therefore, large numbers of electrical measurements (usually more than 200) are needed for high confidence and accuracy.

$$Z = Z_0 + ax + by + cx^2 + dy^2 + fxy \quad (5.1)$$

$$Area = \pi \left(r_{Major} - \Delta r_{Undercut} \right) \times \left(r_{Minor} - \Delta r_{Undercut} \right) \quad (5.2)$$

5.1.1. Electrical Characterization of High Current Density $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETDs

Like the GaAs-based devices from Chapter 4, electrical measurements were performed using a Keithley 4200 semiconductor parameter analyzer. A set of I-V characteristic curves, covering a wide range of devices sizes, are shown in Fig. 5.5 for (a) InGaAs-1 and (b) InGaAs-2. The dimensions listed are average radii calculated from the area analysis performed after mesa isolation etch (described in Section 5.1). For InGaAs-1, device dimensions ranged from 47 nm up to 1.53 μm radii, with I_p covering three orders of magnitude. For InGaAs-2, devices ranged from 84 nm to 2.5 μm radii, with I_p covering a similar range as InGaAs-1. Larger size junctions for both ETDs could not be measured due to the 100 mA current limit on the Keithley 4200. In past literature, large J_p became difficult to measure due to (i) localized heating requiring pulsed measurements, (ii) large device areas, and/or (iii) uncertainties in the junction area [11, 14]. These issues are circumvented by scaling the junctions to deep submicron dimensions. This enabled the direct measurement of the TD's DC characteristics by reducing parasitic resistances to negligible

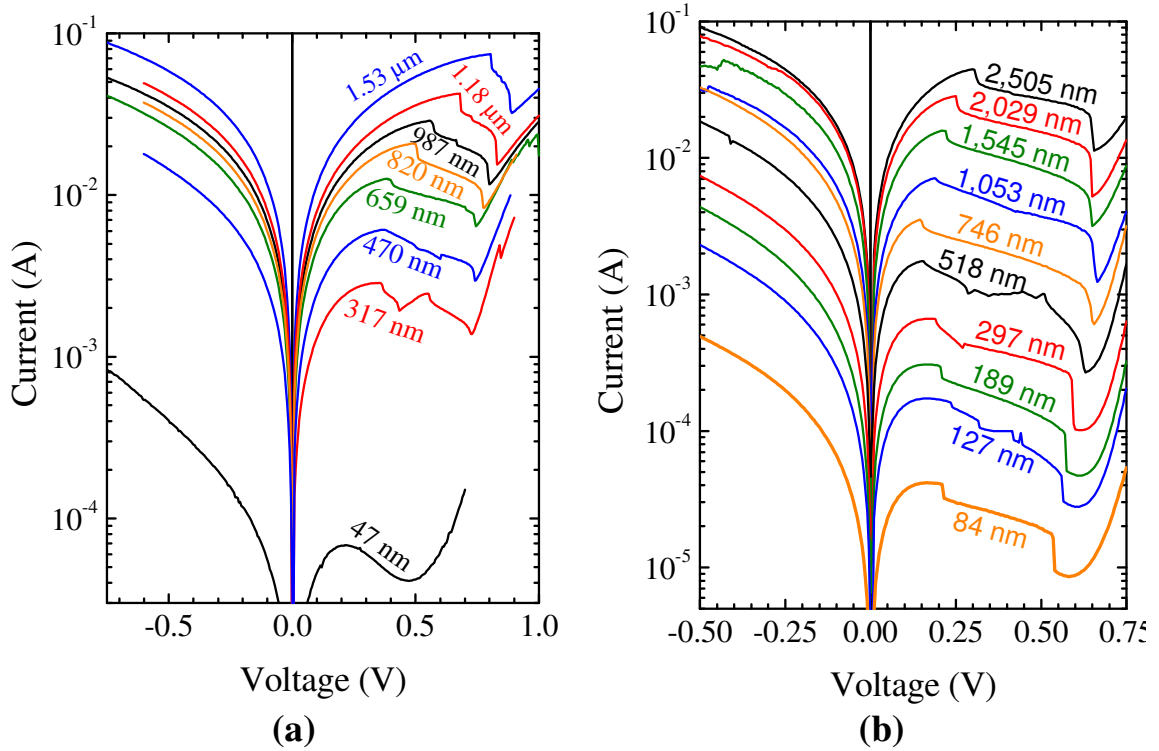


Fig. 5.5: Measured I-V characteristics for (a) InGaAs-1 and (b) InGaAs-2 over a wide range of sizes. Each curve is labeled with its average estimated radius.

levels. Subsequently, the process of calibrating BTBT models to experimental results is simplified.

For comparable sizes, the I_p for InGaAs-1 is significantly larger than InGaAs-2, indicating a larger BTBT current density. The combination of ultra-high current density and soft metal contacts/pads created an uncommon problem during electrical testing. Due to localized heating, occasionally the Au metal above the device would blow apart (Fig. 5.6). This would diminish the electrical connection between the semiconductor and metal, causing noise and increased R_{Series} in the measurements. If care was not taken to minimize the voltage sweep appropriately, a full open would occur. Smaller junctions tended to be more susceptible to this issue. It is also important to understand that reliability few devices smaller than 300 nm radii survived fabrication. There was also less available information for area characterization.

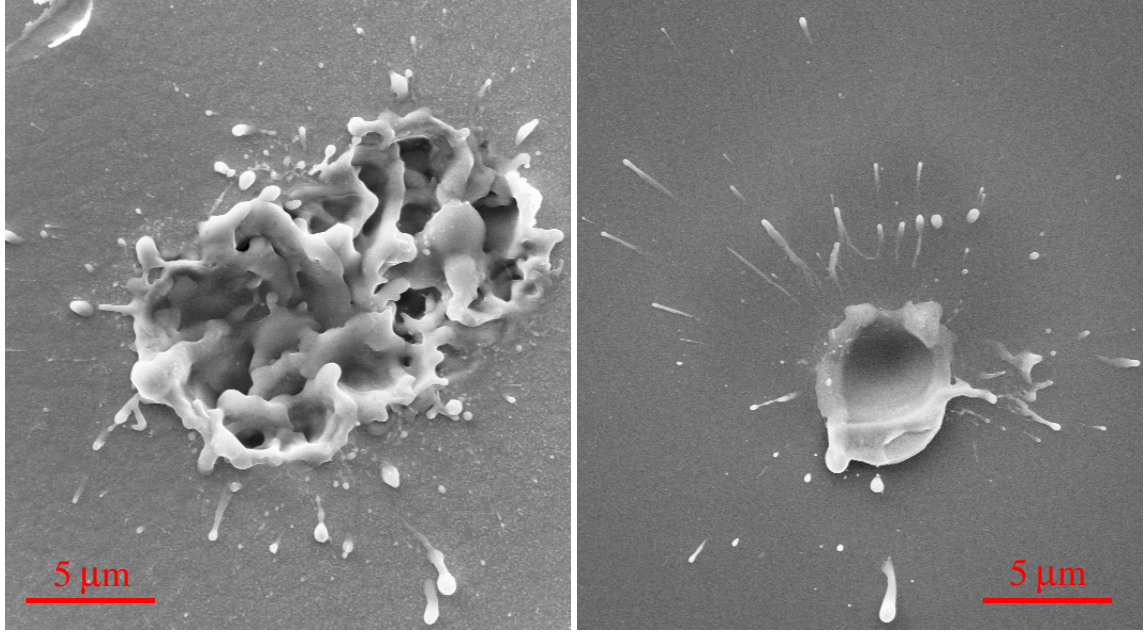


Fig. 5.6: SEM images of Au probe pad blow out due to localized heating. This does not kill the device, but causes problems with measurements (noise and opens).

Resulting in large uncertainty for the calculated areas for the ultra small junctions. Furthermore, there aren't many clean measurements for improved statistical analysis.

In addition to comparing current densities, it is clearly visible from Fig. 5.5 that InGaAs-2 is affected by R_{Series} less than InGaAs-1. This is clearly visible in the I-V characteristics as a positive shift in V_P and V_V , as I_P and I_V increases. R_{Series} clearly becomes significant for device sizes of ~ 300 nm and $1 \mu\text{m}$ for InGaAs-1 and InGaAs-2, respectively. Eventually, if the voltage drop across the R_{Series} becomes too large (larger junction areas or R_{Series}), than the ETD/R_{Series} circuit will behave like a latch and prevent accurate ETD measurements.

Plotting measured I_P versus I_P is very useful for quantifying R_{Series} , and determining the intrinsic V_P of the ETD structures. Equation (5.3) relates measured V_P to the intrinsic V_P of the ETD plus a voltage drop across a constant resistance (R_{Series}) and an area dependent resistance (ρ_{Area}) such as contact resistance, and resistance of the semiconductor mesa. Rearranging (5.3), and a linear equation (5.4) can be formed, where R_{Series} is the slope, and the product $J_P \times \rho_{Area} \times V_P$ is the y-intercept (minimum measurable V_P). Typically, ρ_{Area} is very small and therefore is

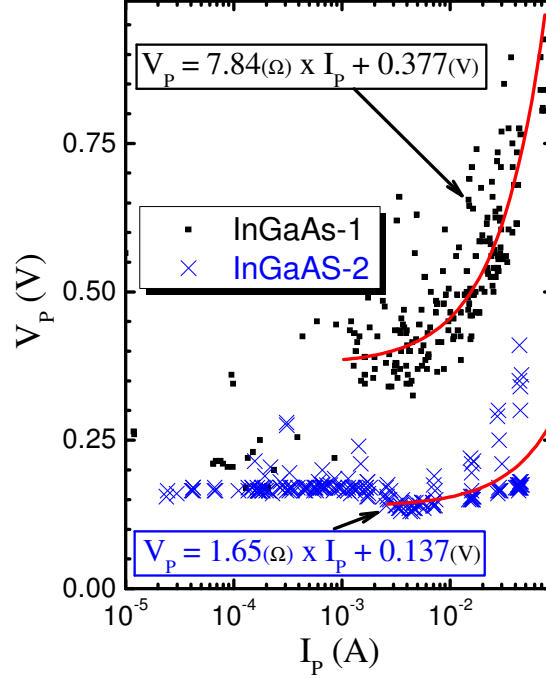


Fig. 5.7: Variation of V_p versus I_p . Slope of the line fit provides average R_{Series} . Y-intercept is the average minimum measurable V_p , which is usually the intrinsic V_p .

negligible. Therefore, the x-intercept of the line fits to Fig. 5.7 are typically the intrinsic V_p . From the line fits, InGaAs-1 has a larger R_{Series} of 7.8 Ω compared to 1.7 Ω for InGaAs-2. Additionally, the intrinsic V_p for InGaAs-1 is estimated to be a much greater 0.38 V versus 0.14 V for InGaAs-2. However, there are many InGaAs-1 devices with much smaller V_p , around 0.2 V. There may be some additional sources of parasitic resistances present in most devices, elevating the y-intercept.

$$V_p (measured) = V_p + I_p \times \left(R_{Series} + \frac{\rho_{Area}}{Area} \right) \quad (5.3)$$

$$V_{P(measured)} = R_{Series} \times I_p + (J_p \times \rho_{Area} + V_p) \quad (5.4)$$

There is a very large spread in PVCR values measured, with an average of 1.9 and 5.1 for InGaAs-1 and InGaAs-2, respectively. Similarly to the GaAs based ETDs from Chapter 4, the average PVCR decreases as junction area is scaled (Fig. 5.8a). However, the maximum PVCR

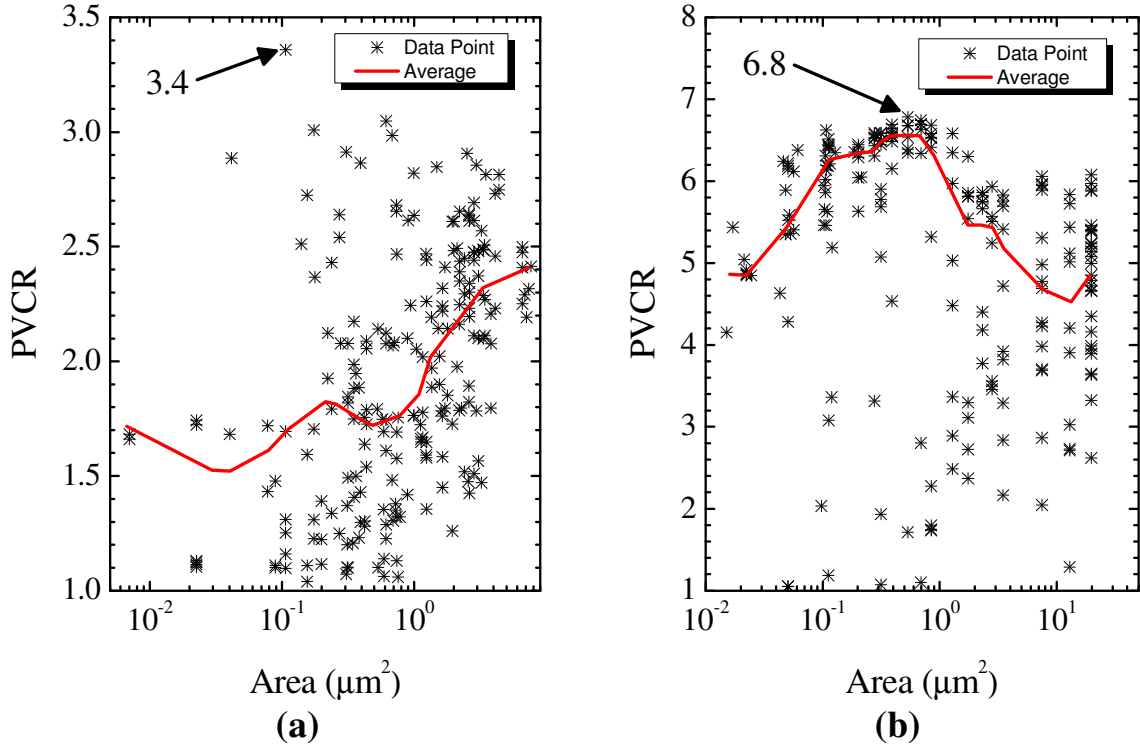


Fig. 5.8: Scaling properties of PVCRC for (a) InGaAs-1 and (b) InGaAs-2. The solid lines indicate smoothed averages of the dataset. The maximum PVCRC improved a small amount as the junctions were scaled.

increases to 3.4, for a 180 nm radii device. On the other hand, InGaAs-2 had a much smaller statistical variation and a much higher average PVCRC of 5.1 (Fig. 5.8b). Unlike InGaAs-1, the average PVCRC increases down to ~ 500 nm Radii, and then flattens out. The maximum PVCRC follows the same trend as the average, reaching 6.8 for a 410 nm Radii. For complete analysis of PVCRC versus junction area, a much larger data set is needed.

It is evident from Fig. 5.9a that I_p is linearly related to the junction area and therefore is not dominated by surface leakage currents. The main exceptions are the result of statistical deviations in the smallest junction areas, which are due to known fabrication variations. This is especially apparent for InGaAs-1, where very few area characterization measurements were taken for the smallest printed features (it was thought that only a few survived fabrication). From these results it is conclusive that BTBT junctions are scalable to deep sub-micron dimensions, a necessary structural requirement for high performance TFETs. Additionally, it is clear the J_p for

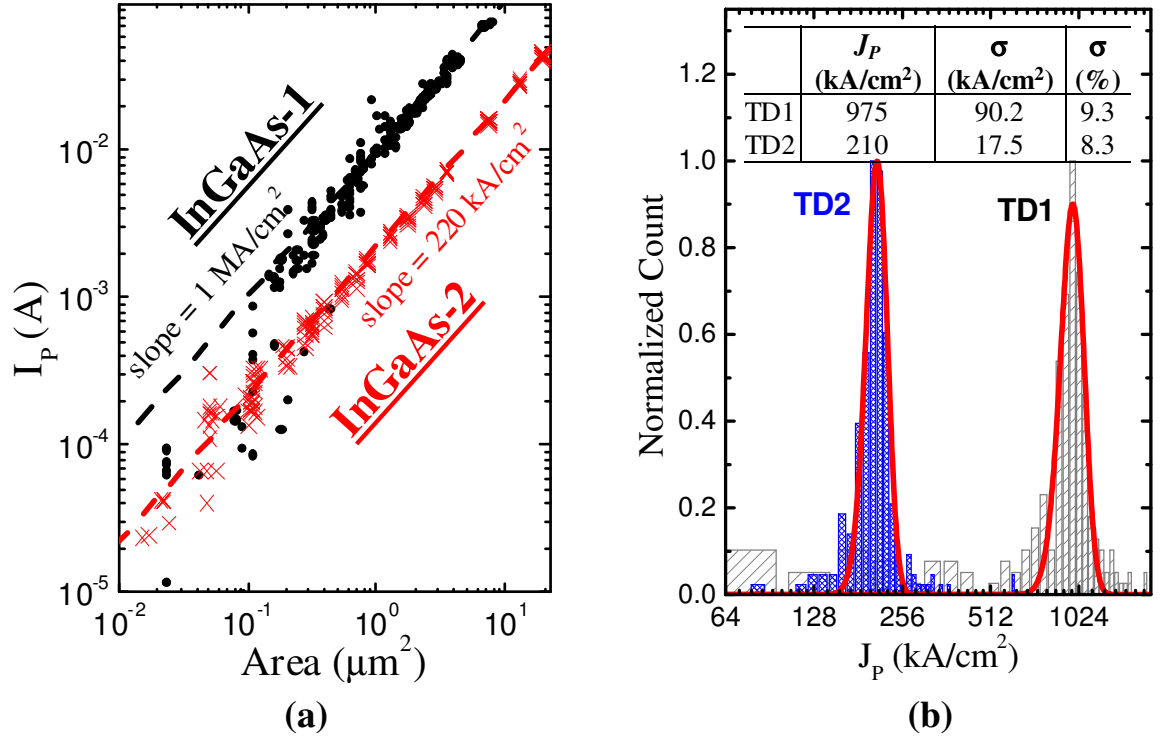


Fig. 5.9: On the left is the (a) scaling properties of I_p for InGaAs-1 and InGaAs-2. On the right are the J_p histograms for both ETDs. The Gaussian fits were used to calculate the average J_p and standard deviation (table inset).

InGaAs-1 is greater than InGaAs-2, which is certainly due to the differences in doping concentrations. The slope of the least squares line fit (dashed lines) to each dataset yields preliminary J_p of 1 MA/cm² and 220 kA/cm² for InGaAs-1 and InGaAs-2, respectively.

To calculate a statistically accurate J_p , a histogram from the 200+ measured devices for each structure was used, Fig. 5.9b. From the Gaussian fit to each data set J_p is 975 kA/cm² and 210 kA/cm² for TD1 and TD2, respectively. The J_p of TD2 is comparable to the highest Si/SiGe ETD current density [11], with a much greater PVCR. TD1 has the largest experimentally observed J_p of any homojunction ETD, and the second largest over-all [23, 24]. Zener current densities of 8 MA/cm² (TD1) and 3 MA/cm² (TD2) were measured at a bias of -0.5 V. It is clear from these results that In_{0.53}Ga_{0.47}As is capable of generating ultra-high BTBT current densities at low applied biases. It is necessary to have large active doping concentrations with fairly sharp doping profiles.

5.1.2. Modeling InGaAs-1 and InGaAs-2

Band diagrams (Fig. 5.10) were calculated using the doping concentrations determined from SIMS (Fig. 5.2a). Fermi energies were calculated using the algorithms developed for the Kane model program discussed in Chapter 3, which assumes a simplified two band theory (only the Γ -valley for electrons). However, an extra option was added for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, which includes the L- and X-valleys for calculating $E_{F,n}$. Also, bandgap narrowing (BGN) effects were also calculated using (5.5) and (5.6), from [26]. Where $\Delta E_{G, \text{Majority}}$ and $\Delta E_{G, \text{Minority}}$ are the changes in E_C and E_V , depending on the majority doping type. The constants – a, b, c, d – can be found in Table 5.1. The final bandgap used is calculated as the average ΔE_G for the n- and p-sides of the junction. This is obviously a first order approximation, by ignoring band edge alignments.

$$\Delta E_{G, \text{Majority}} = a \left(\frac{N_{A,D}}{10^{19}} \right)^{1/3} - b \left(\frac{N_{A,D}}{10^{19}} \right)^{1/2} \quad (5.5)$$

$$\Delta E_{G, \text{Minority}} = c \left(\frac{N_{A,D}}{10^{19}} \right)^{1/4} - d \left(\frac{N_{A,D}}{10^{19}} \right)^{1/2} \quad (5.6)$$

At equilibrium, three band diagrams are shown for both InGaAs-1 (Fig. 5.10a) and InGaAs-2 (Fig. 5.10b). All of the calculations assume that the doping profiles are perfectly square, full depletion approximation, and all bands are parabolic (constant effective mass). The basic band structure assumes the i -layer (d) is 0 nm thick and only the Γ -valley is relevant. The second set of band diagrams inserts a perfect 3 nm i -layer. Finally, E_F is calculated using four bands (Γ , L, and X) and d is was setto 0 nm. A fourth set of band structures were calculated

Table 5.1 Constants for calculating bandgap narrowing (BNG).

	a	b	c	d	Units
N_A	9.2	3.4	11.3	0.23	meV
N_D	47.6	0	3.2	0	meV

Table 5.2 Modeling results for InGaAs-1 and InGaAs-2. The Kane model is not setup to include an *i*-layer (*d*), and therefore all J-V results assume *d* is 0 nm.

	d (nm)	Model Parameters	E_G (eV)	w_d (nm)	Barrier Width (nm)	J_p (kA/cm ²)	E_{F,n}-E_C (eV)	E_V-E_{F,p} (eV)	V_p (V)	n
InGaAs-1	0	2 Band	0.736	10.6	2.53	683	2.18	0.162	0.196	1.31
InGaAs-1	3	2 Band	0.736	11.0	2.63					
InGaAs-1	0	4 Band	0.736	9.06	2.96	343	1.36	0.162	0.177	0.58
InGaAs-1	0	4 Band/BGN	0.662	8.76	2.75	480	1.28	0.162	0.178	0.62
InGaAs-2	0	2 Band	0.736	11.8	3.26	262	1.77	0.148	0.174	1.00
InGaAs-2	3	2 Band	0.736	12.1	3.36					
InGaAs-2	0	4 Band	0.736	10.7	3.59	153	1.31	0.148	0.162	0.54
InGaAs-2	0	4 Band/BGN	0.670	10.4	3.37	218	1.25	0.148	0.163	0.58

using 4-bands, *d* equal to 0 nm, and bandgap narrowing. Those results are tabulated, along with the others, in Table 5.2 but not shown in Fig. 5.10. For easy comparison, the x-axis is centered at the middle of the *i*-layer, with the shaded region indicating the *i*-layer itself. As can be seen, the largest change from the basic model, is the use of 4-bands to calculate $E_{F,n}$. The insertion of a small *i*-layer has minimal effects.

The numerical results for all eight band diagram calculations are listed in Table 5.2. As can be seen, the 3 nm *i*-layer only increases the depletion width (w_d) by only ~ 0.35 nm, increasing the tunnel barrier width a negligible ~ 0.1 nm. Therefore, it is reasonable to ignore the *i*-layer for the J-V modeling. The largest effect comes from using 4-bands to calculate $E_{F,n}$, which reduces w_d from 10.6/11.8 nm (InGaAs-1/InGaAs-2) to 9.06/10.7 nm. Furthermore, the tunnel barrier widths are reduced from 2.53/3.26 nm to 2.63/3.59 for InGaAs-1/InGaAs-2. This is a large reduction of approximately $\sim 40\%$, and certainly effects the calculated BTBT current. Finally adding the effects of BNG narrows w_d by an additional ~ 0.2 nm, and shrinks the bandgap (tunnel barrier height) by 74 meV and 66 meV for InGaAs-1 and InGaAs-2, respectively. From here, simulations will include (i) 2-bands only, (ii) 4-bands, and (iii) 4-bands with BNG.

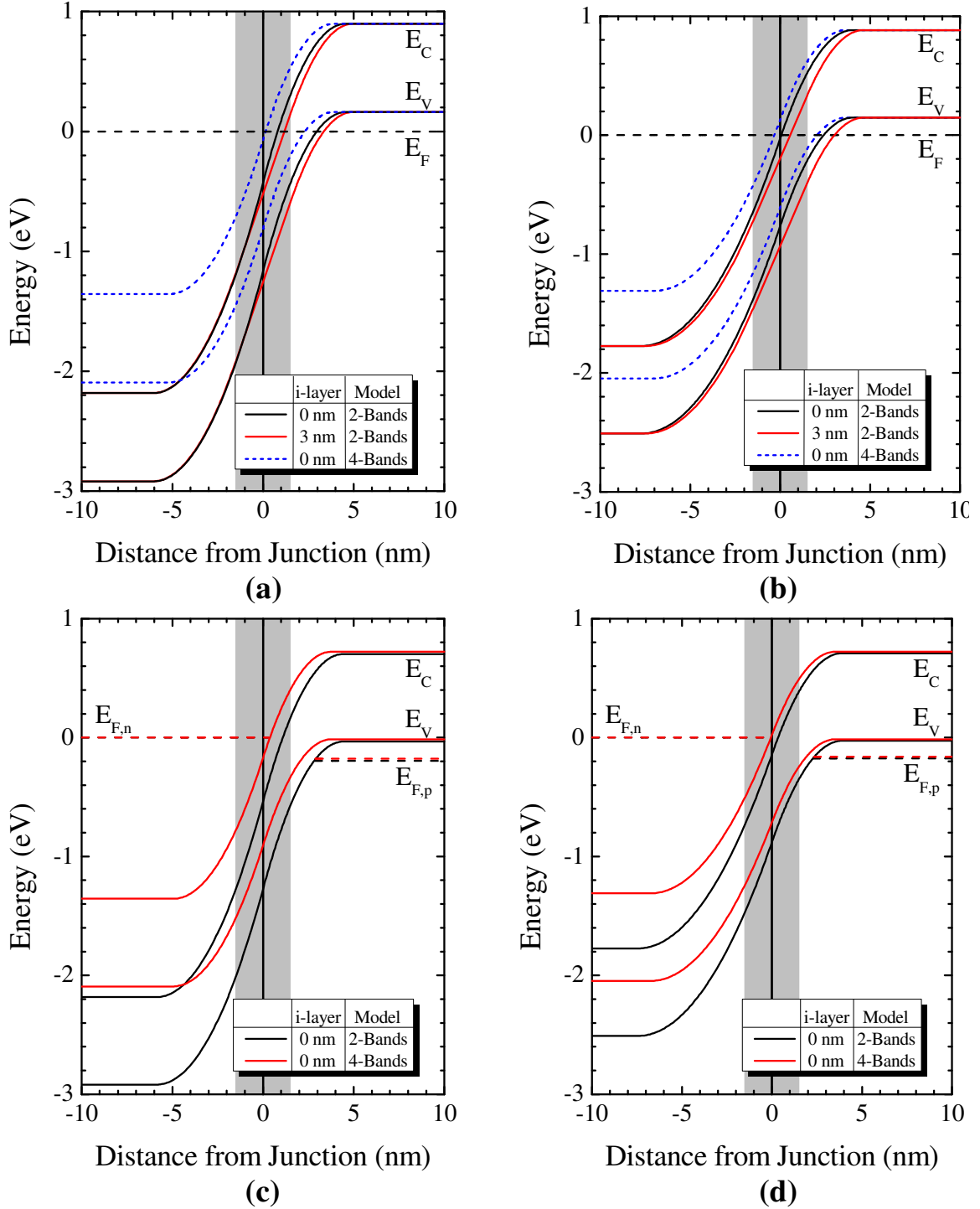


Fig. 5.10: Calculated band diagrams assuming 2-band approximation, abrupt junctions, and full depletion approximation. Top row are at equilibrium for (a) InGaAs-1 and (b) InGaAs-2. The 3 nm *i*-layer has a minimal effect on the tunnel barrier. The Bottom row is biased at the calculated V_p for (a) InGaAs-1 and (b) InGaAs-2. V_p is largely dependent on $E_{F,p}$.

The non-equilibrium band diagrams at the V_p are shown for InGaAs-1 (Fig. 5.10c) and InGaAs-2 (Fig. 5.10d). Notice that V_p occurs when $E_{V,p}$ is shifted just below $E_{F,n}$ for all cases. Additionally, $E_{F,p}$ is nearly the same for all cases, and therefore so is V_p . This is because $E_{F,p}$ is much smaller than $E_{F,n}$, due to their respective density of states and doping concentrations. If $E_{F,n}$ was much larger than $E_{F,p}$, then V_p would closely follow $E_{F,n}$. V_p may be predicted by (5.7). $E_{F,minor}$ is the smaller of the two Fermi potentials, kT is the thermal energy present, and n is some constants (typically less than two). When the two Fermi energies are close to each other, then V_p would be an average of $E_{F,n}$ and $E_{F,p}$, which has been described elsewhere [27].

$$V_p = E_{F,minor} + n \times kT \quad (5.7)$$

From the Kane model, Table 5.2 predicts that J_p will be $\sim 500 \text{ kA/cm}^2$ and $\sim 200 \text{ kA/cm}^2$ for InGaAs-1 and InGaAs-2, respectively. The specific value depends on which parameters are used. The greater values are predicted with the simplest 2-band model. The 4-band model reduces the prediction by $\sim 55\%$. Finally adding in BNG brings J_p band to $\sim 75\%$ of the original value. There is only a small variation in V_p , since it is dominated by $E_{F,p}$. Typical values of “ n ” range between 0.5 and 1.3, with an average of 0.8. In general, “ n ” follows $0.83 \times E_{F,p} + 0.5$.

The calculated J-V results are compared with InGaAs-1 (left) and InGaAs-2 (right) using the 2-bands (Fig. 5.11a, d), 4-bands (Fig. 5.11b, e), and 4-bands and BGN (Fig. 5.11c, f) models. For each curve, a simple exponential line is fitted to the post-valley characteristic as a simple J_{Excess} model. The basic 2-bands model best estimated J_p and the pre-peak BTBT current densities. However, the slope of the NDR region is way too shallow and extended due to the over-estimated V_{bi} prolonging the mesa-like portion of the overlap integral. When J_{Excess} is added to J_{Model} , the PVCR is nearly non-existent for InGaAs-1, and very small for InGaAs-2.

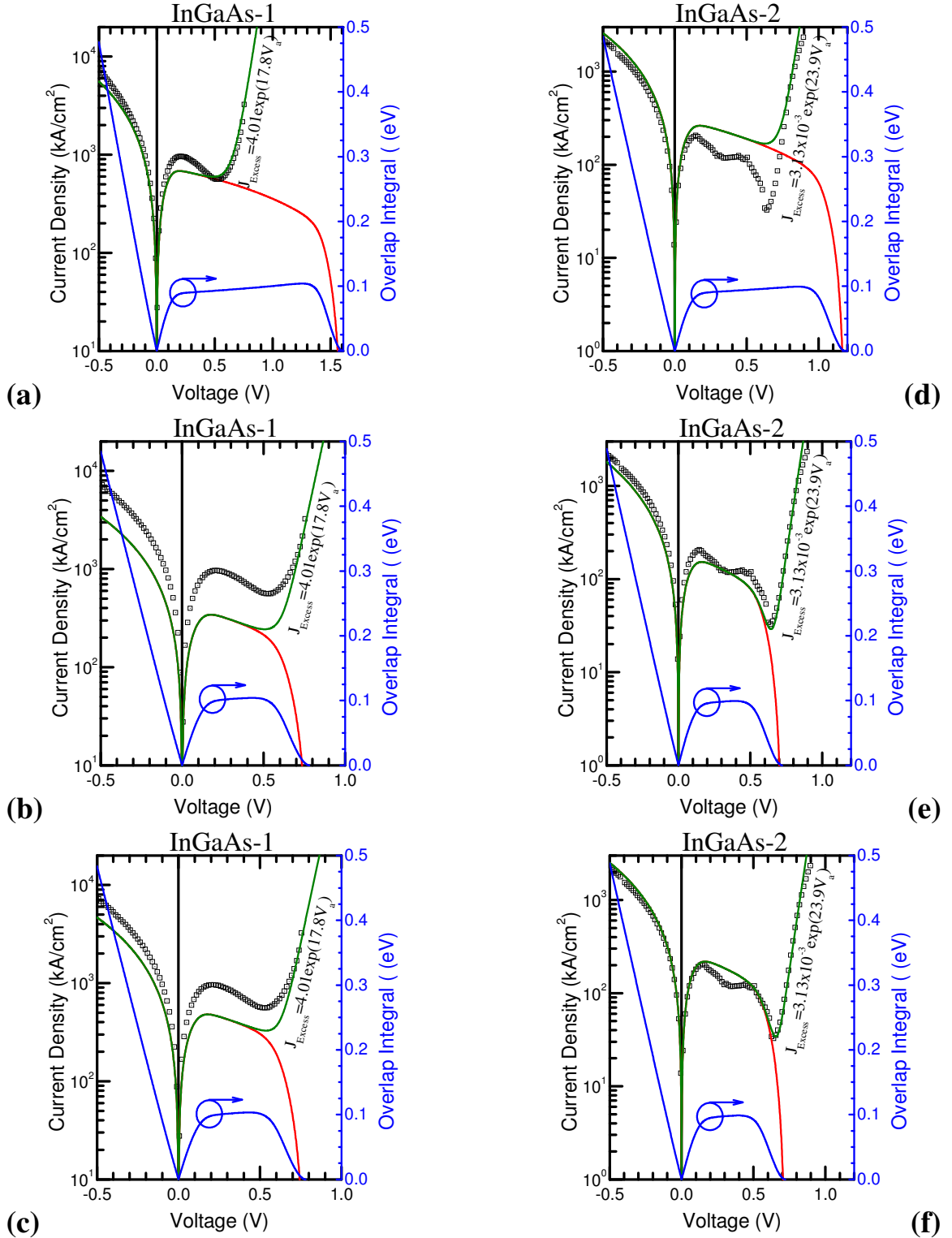


Fig. 5.11: Calculated BTBT J-V characteristics vs. measured for (left) InGaAs-1 and (right) InGaAs-2. Top row (a, d) are 2-band, middle row (b, e) are 4-band, and the bottom row (c & f) are the 4-bands & BGN results. The 2-band model gave the best pre- J_P current densities. Whereas, the 4-band & BGN model gave the best post- J_P results.

Calculating $E_{F,n}$ using the 4-bands model fixes the issue with the NDR region. By using all three electron valleys (Γ , L, and X), the $E_{F,n}$ became substantially smaller, as described in Fig. 5.10, and Table 5.2. As a result, the overlap integral (D) is much shorter in forward bias, which greatly improves the final PVCR close to the measured value. However, the 4-bands model also increased the tunnel barrier width. As a result, the calculated BTBT current density was significantly reduced. The calculated values are still within the same magnitude the measured data.

Adding in BGN to the calculations reduced the tunnel barrier width and height. As a result, the BTBT current densities increased, but not back to their original values. For InGaAs-1, the model still underestimated the current density. For InGaAs-2 the model predicted the same current density as was measured in the fabricated devices. Additionally, with the fitted J_{Excess} , the

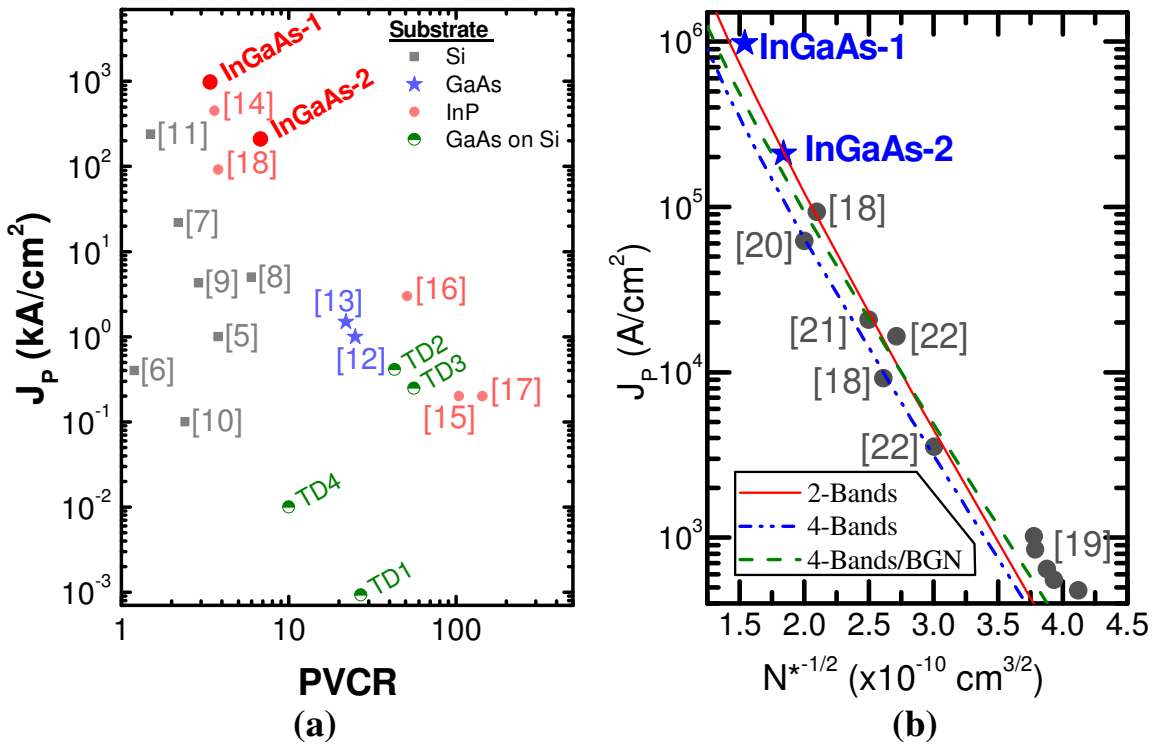


Fig. 5.12: Contrasting InGaAs-1 and InGaAs-2 with previous results and other ETDs from literature by compare J_P versus (a) PVCR [4-18] and (b) reduced average doping (N^*) [18-23]. Solid and Dashed lines are Kane model predictions using 2-bands, 4-bands, and 4-Bands/BGN.

NDR and valley regions are also accurate. Also, notice that J_{Excess} becomes significant as “D” and J_{Model} sharply descend. A small change in J_{Excess} , would cause a very large shift in J_V (minimal change in V_V), thereby causing a large change in PVCR. If J_{Excess} is increased too much, as is the case for the InGaAs-1 device shown above, J_V and the PVCR will only have minor changes due to the mesa-like shape of “D”. Conversely, V_V will shift more dramatically.

Even though the current density magnitude for InGaAs-1 is low, the shape of the curve is very accurate. If the magnitude of the calculated curve is matched to the measurements, the model will accurately predict the J-V characteristics for the bias conditions used here. Therefore, if J_P is known, J_{Model} may be used to predict the rest of the J-V characteristic. Furthermore, given that the primary concern is J_P and pre-peak characteristics, the simple 2-band model is the most accurate for predictions.

5.1.3. Benchmarking In_{0.53}Ga_{0.47}As ETDs

As introduced in Chapter 4, InGaAs-1 and InGaAs-2 are benchmarked against ETDs from literature. First, J_P is plotted against PVCR (Fig. 5.12a). As can be seen, InGaAs-1 has the largest current density shown, and InGaAs-2 is tied for 3rd with a Si/SiGe based device [11]. However, the InGaAs based structure have much greater PVCR than the Si based structures. Therefore, it is reasonable to predict that InGaAs is a better material system for BTBT based devices. However, this does not take doping into consideration.

It has already been established that doping has a large impact on J_P . In Fig. 5.12b, J_P is plotted against the inverse square root of the reduced average doping (N^*) for 11 ETDs in literature as well as InGaAs-1 and InGaAs-2. Even though there are a great number of In_{0.53}Ga_{0.47}As ETDs reported in literature, only those reports that follow the following restrictions were included. These restriction guarantees that the final list is a homogeneous set, with doping being the only significant variable. First, the entire tunnel junction must be In_{0.53}Ga_{0.47}As without any strain. The *i*-layer, if present, may not exceed ~4 nm. There must be a representative I-V

curve present with clear NDR. There needs to be high confidence in the value measured and calculated for J_p . Finally, there must be clear a SIMS plot which may be used to extract the appropriate doping concentrations.

It is clear from Fig. 5.12b, that all of the collected InGaAs ETDs form an exponential line. Also included are trendlines from the Kane model using (i) 2-bands, (ii) 4-bands, and (iii) 4-bands & BGN modeling parameters as discussed in sections 5.1.2. All three lines are very close to each other, with only fairly small differences in slope and magnitude. However, the basic 2-bands line (solid) does the best job over-all of predicting J_p . It is also the closest to a least squares exponential fit to the data (not shown here). Therefore, to simplify the calculations and analysis, the more accurate 2-bands $E_{F,n}$ model will be used for the remaining modeling work.

5.2. Low Current Density In_{0.53}Ga_{0.47}As ETD

The third In_{0.53}Ga_{0.47}As ETD (InGaAs-3 shown in Fig. 5.13a) was designed to be a medium level current density grown by MBE from a 3rd source; Texas State University. A major difference for this design was flipping the structure upside down, and placing the n-type layer on top. The growth began with a 300 nm p-type In_{0.52}Al_{0.48}As, then it switched over to 300 nm of p-type In_{0.53}Ga_{0.47}As. Furthermore, due to constraints in the epitaxy reactor, Be was used as the dopant species instead of C. Similar to InGaAs-1, the maximum N_A concentration is targeted to $5 \times 10^{19} / \text{cm}^3$, and is contained within a 10 nm layer adjacent to the 3 nm *i*-layer. Finally, the entire 60 nm n-type cathode had a target concentration of $4.5 \times 10^{19} / \text{cm}^3$. Using the Kane model, verified for the InGaAs system in the previous Section (5.1.3), J_p is calculated to be approximately 10 kA/cm^2 .

The fabrication began with the deep sub-micron process used for InGaAs-1 and InGaAs-2. However, processing was halted after mesa isolation etch in order to perform preliminary electrical testing of the ETDs. Additionally, Mo was sputtered as the contact metal, instead of the Au/Zn/Au film stack used for all previous samples. As a refractory metal, Mo is a much cleaner

metal (Au contamination can be a huge issue on Si clean rooms), has a work function more appropriate for n-type semiconductors, and there is the potential for patterning with a dry plasma. Since this was the first time working with Mo, several transfer length method (TLM) features were added to the layout. The TLMs were aligned horizontally and vertically to the wafer flat.

5.2.1. Electrical Results for InGaAs-3

Electrical measurements began with the TLM structures. From the results shown in Fig. 5.13b, both sets of TLMs resulted in a straight line, with the Horizontal having the least noise. The results of both TLMs were very close to each other, which one would expect. The average contact resistance ($R_{Contact}$), sheet resistance (R_{Sheet}), transfer length ($L_{Transfer}$), and contact resistivity ($\rho_{Contact}$) measured were 0.37 (Ω), 37 ($\Omega/\text{sq.}$), 1.28 (μm), and 6.0×10^{-7} ($\Omega\text{-cm}^2$), respectively. The contact resistivity is sufficient for these ETD structures.

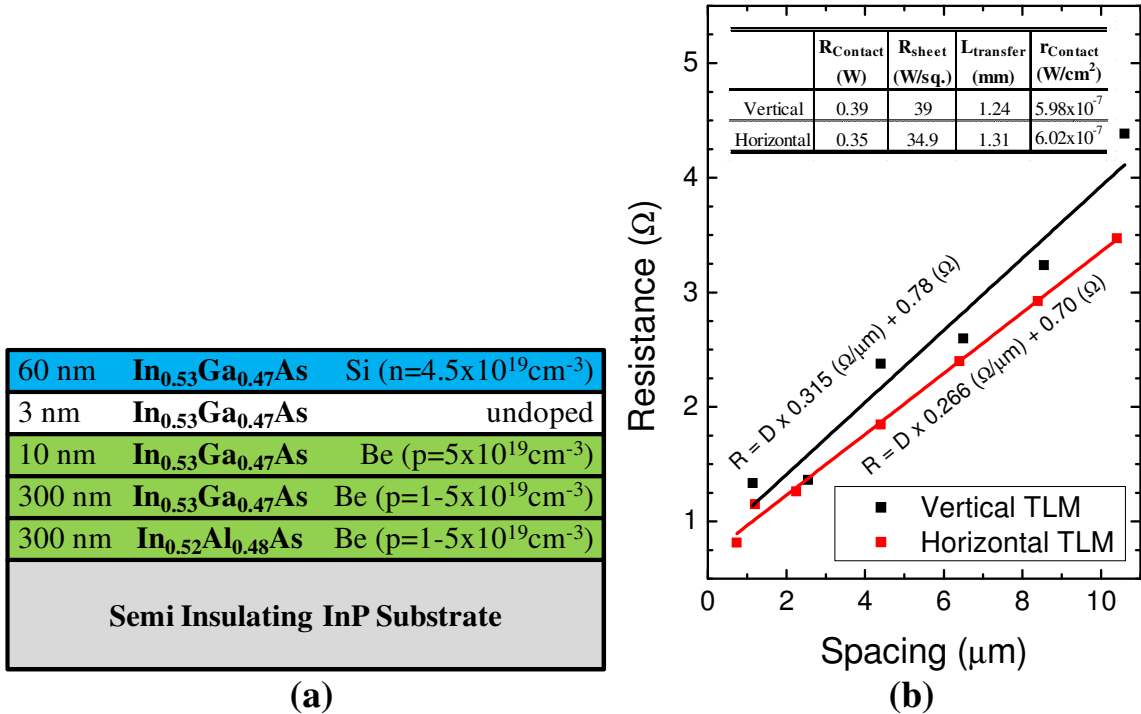


Fig. 5.13: Left, (a) Schematic diagram of InGaAs-3 with original target doping concentrations. Right, (b) vertically and horizontally oriented TLM results for Mo contacts on n-type In_{0.53}Ga_{0.47}As.

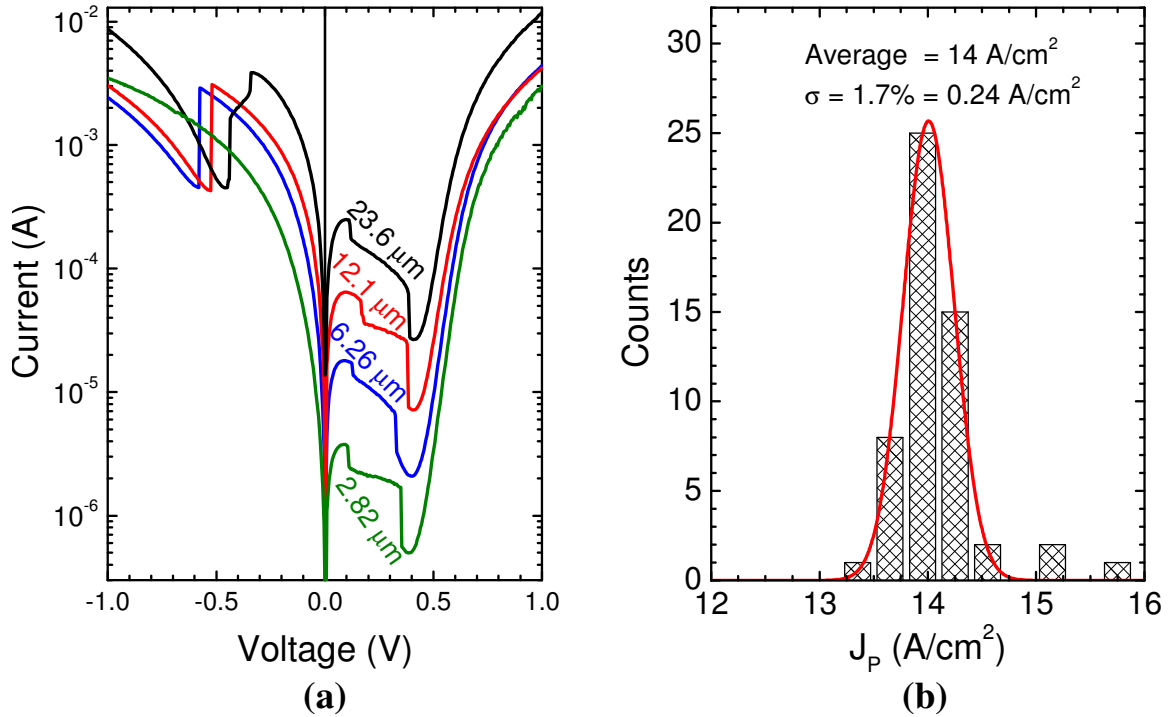


Fig. 5.14: Left, (a) I-V characteristics for InGaAs-3. NDR in reverse bias is from the device used as a virtual short to ground. Right, (b) J_p histogram with Gaussian fit. J_p is much smaller than predicted.

The electrical results of the large area, post-mesa etched ETDs can be found in Fig. 5.14a. The measured I_p ranged two orders of magnitude, and was primarily limited by the (i) largest printed devices and (ii) probe tips diameter ($\sim 2.5 \mu\text{m}$). Smaller features were printed, but without going through the entire sub-micron process, they could not be tested. At larger biases (~ 0.65 V), an external R_{Series} began dominating the I-V characteristics. In reverse bias, the NDR of the device used as a virtual ground is clearly present. Reverse NDR is not visible for the smallest ETD (2.82 μm radii), because its reverse bias current does not achieve I_p for the virtual ground device.

Since the virtual ground device structure is at least 15x greater than the device under test, this indicates that the current density of InGaAs-3 is much less than the previous two ETDs, as expected. For a high confidence level assessment of J_p , another histogram was formed. The Gaussian fit to the distribution gave an average J_p of 14 A/cm², with a very small standard

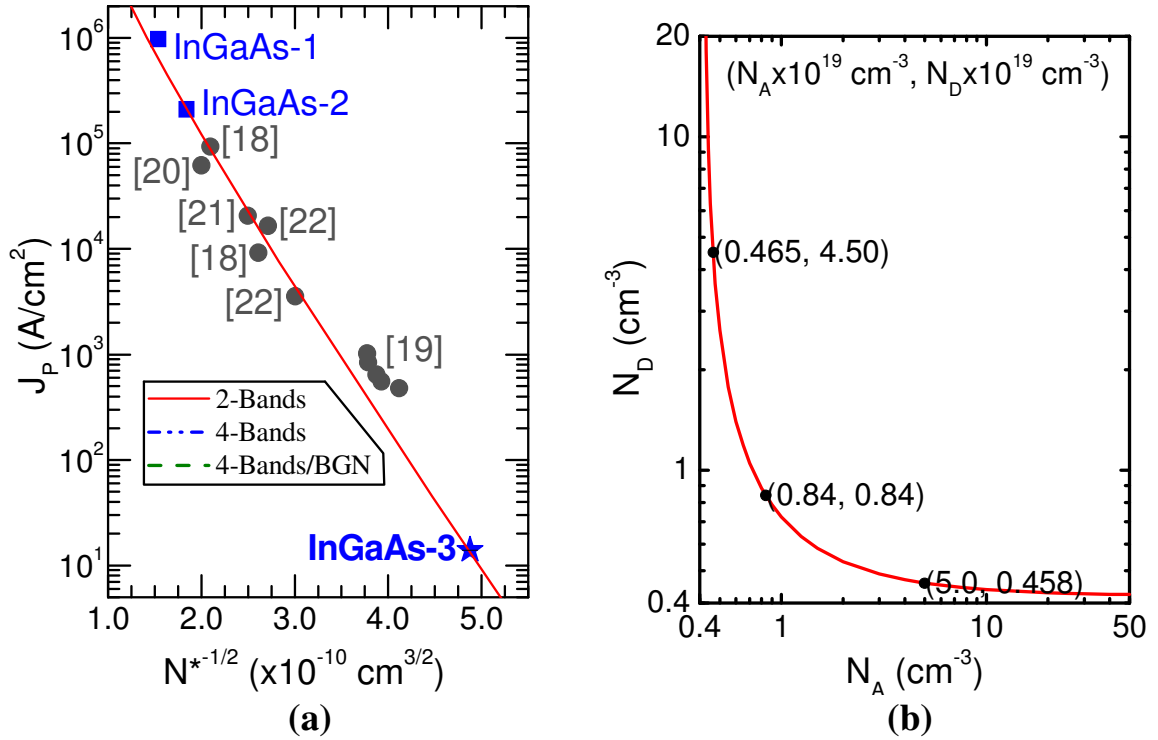


Fig. 5.15: Left, (a) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ trendline including predicted placement of InGaAs-3 (measured J_p of 14 A/cm²). Right, (b) isometric reduced doping curve for an $N^* = 4.2 \times 10^{18}/\text{cm}^3$. Labeled points assume (i) N_A is off target, (ii) $N_A = N_D$, or (iii) N_D is off target.

deviation of 1.7% (0.24 A/cm²). This result is three orders of magnitude smaller than the predicted value.

5.2.2. Investigating the Low J_p of InGaAs-3

Assuming that the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ trendline is still valid for the low J_p measured, there are two main reasons that the structure was so far off in its current density. First, the doping concentration may be much smaller than expected. Second, the *i*-layer may have been grown to large. Both issues could be easily clarified with SIMS. However, the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ trendline was first used to predict the N^* needed to achieve the measured J_p . As labeled in Fig. 5.15a, InGaAs-3 is far removed from all other devices, with an expected N^* of $4.2 \times 10^{18}/\text{cm}^3$. A curve was generated for all possible (within reason) combinations N_A and N_D doping concentrations. The curve asymptotically approaches $x =$ and $y = 4.2 \times 10^{18}/\text{cm}^3$. It is not uncommon for the

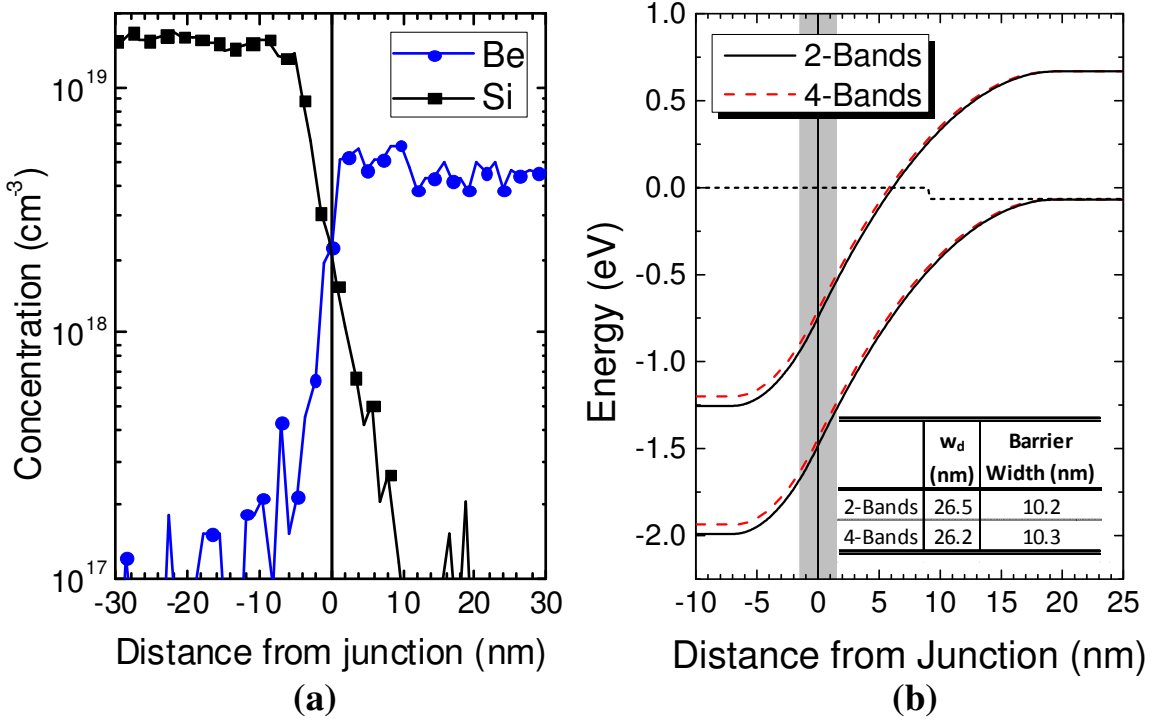


Fig. 5.16: Left, (a) SIMS results for InGaAs-3. Be concentration is much smaller than targeted. Right, (b) calculated band diagram biased at V_p using 2-bands and 4-bands E_F model.

temperature setting an effusion cell to be set for the wrong doping concentration. Therefore, two data points are labeled assuming only one of the target concentrations was achieved. Also included was $N_A = N_D$.

The SIMS results are shown in Fig. 5.16a. The Si doping concentration is a little smaller (36%) than the target, maxing out at $1.59 \times 10^{19} / \text{cm}^3$ near the tunnel junction. However, the bigger error is the Be, which only achieved $5.70 \times 10^{18} / \text{cm}^3$, which is one order of magnitude off of the target. In fact, the Be doping concentration is the same in the 300 nm and 10 nm layers. The measured N^* for InGaAs-3 is exactly equal to the predicted value of $4.2 \times 10^{18} / \text{cm}^3$. Therefore, the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is accurate for a current range of nearly five orders of magnitude, and is useful for predictions.

5.2.3. Simulation Results for InGaAs-3

It is clear that J_P is very small because of the doping concentration. The calculated band diagram, Fig. 5.16b, shows a large w_d and tunnel barrier width of ~ 26 nm and ~ 10 nm, respectively. Additionally, N_A is less than the DOS for holes ($\sim 8.1 \times 10^{18} / \text{cm}^3$), severely limiting the number of open states (holes) for electrons to tunnel into. There is only a small difference between the 2-bands and 4-bands model, indicating that most of the electrons are populating the Γ -valley.

The J-V characteristics of InGaAs-3 were calculated using 2-bands and 4-bands $E_{F,n}$ modeling, Fig. 5.17. BGN was excluded for its vast overestimation of J_P . An exponential line fit to the post-valley characteristic was used as the J_{Excess} , and added to J_{model} . Additionally, measured from the high voltage range in forward bias, a 96.2Ω series resistance was included. Otherwise, as can be seen, the basic model begins to overestimate the current density at moderate voltages. As can be seen, both calculated curves are very close to the measured values. In

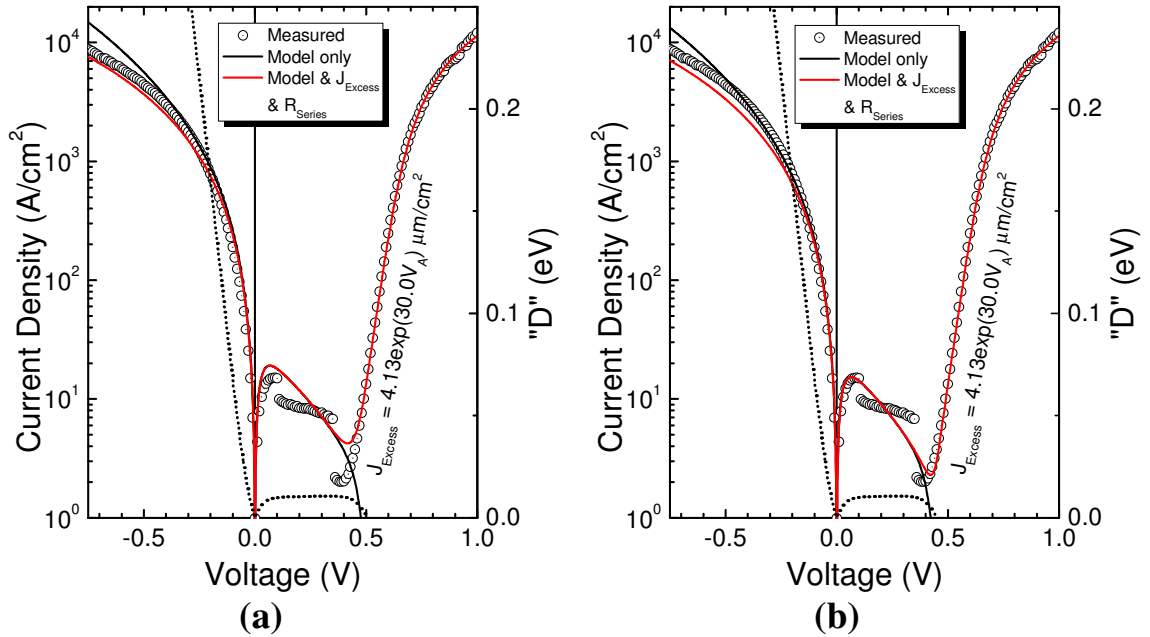


Fig. 5.17: Calculated J-V characteristics using (a) 2-bands and (b) 4-bands. For improved accuracy post valley, J_{Excess} was added via an exponential line fit. Additionally, a $96.2 \Omega R_{Series}$ was added to improve the fit at high current magnitudes.

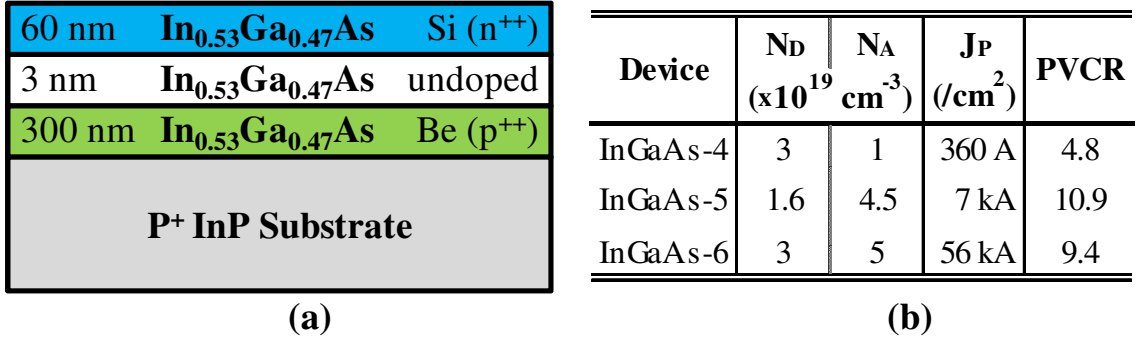


Fig. 5.18: (a) Schematic diagram of medium current density $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETD with (b) doping concentrations, measured J_p , and PVCR for InGaAs-4, InGaAs-5, and InGaAs-6.

reverse bias the 2-bands model (Fig. 5.17) is the most accurate. However, in forward bias, the 4-bands model (Fig. 5.17b) is more accurate. The Kane model has been shown to accurately predict $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ J-V characteristics for high (InGaAs-1 and InGaAs-2) and low (InGaAs-3) current densities. Therefore, one can be confident in its ability to perform well over the entire range. To verify this hypothesis, three medium current density $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETD structures were also fabricated.

5.3. Medium Current Density $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETDs

To help fill out the middle current density range of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ trendline, three additional ETD structure were grown. The structure for (i) InGaAs-4, (ii) InGaAs-5, and (iii) InGaAs-6, shown in Fig. 5.18a, is similar to InGaAs-3. However, structure was grown on a p-type InP substrate, the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer was skipped, and the entire anode (p^{++}) layer was targeted with the maximum doping. The target doping concentrations are listed in Fig. 5.18b. Due to limited resources and improved growth calibrations, SIMS analysis was not performed on these structures. It was assumed that the actually doping concentration was very close to the target values. From the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ trendline, J_p was expected range from approximately ~ 600 A/cm² to ~ 50 kA/cm².

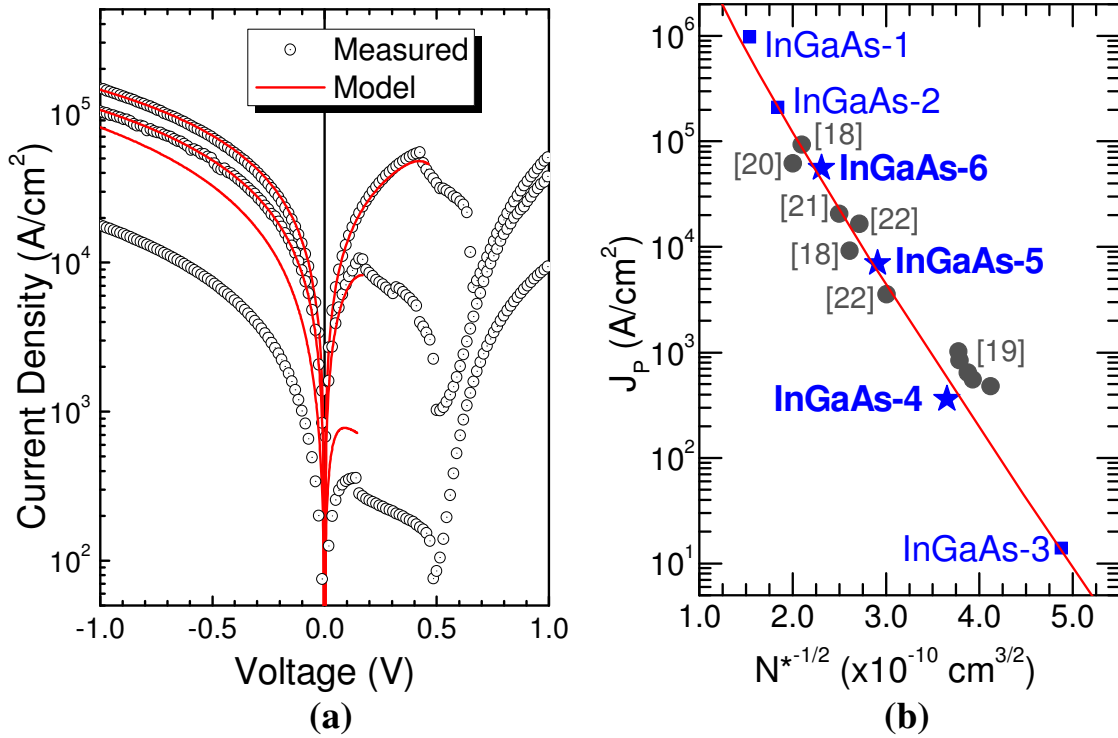


Fig. 5.19: (a) Typical J-V characteristics for InGaAs-4, InGaAs-5, and InGaAs-6. Solid lines are calculated using the basic 2-bands model, cut-off at the measured V_p . A $\sim 6 \mu\Omega\text{-cm}^2$ R_{Series} was added to the model. (b) Characteristic trendline for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, covering five orders of magnitude, including the three additional data points added.

These structure were grown by MBE at Texas State University, the same as InGaAs-3. Since it was known that the current density will not exceed 100 kA/cm^2 , the basic fabrication process was used. Sub-micron devices are only necessary for high current density structures and investigating the scaling properties of tunnel junctions. Additionally, only a few measurements of contact areas are needed for high confidence in the current densities calculated. Furthermore, these measurements area easily performed within one hour using an optical microscope, versus an entire day needed for the deep-submicron process.

As before, no activation anneals were performed, and Mo was used as the contact metal. However, instead of a lift-off lithography process, Mo was first deposited over the entire sample surface. Then contact lithography was performed. Finally, using an $\text{O}_2\text{:SF}_6$ plasma etch, the

exposed Mo was removed, leaving behind Mo contact pads. The subtractive Mo etch resulted in better sidewall morphology, and improved device dimension control versus the lift-off process.

5.3.1. Results for Medium Current Density ETDs

The typical J-V characteristics InGaAs-4, InGaAs-5, and InGaAs-6 are shown in Fig. 5.19a. As J_P increased, V_P also significantly increased. This is a clear indication that there is a relatively large R_{Series} present, which also limits this apparent Zener current density. Using a linear fit to the Zener and forward current at large biases gives a $\sim 6 \mu\Omega\text{-cm}^2$ resistivity, which may be largely due to the Mo contacts. The PVCRs for InGaAs-5 and InGaAs-6 (10.9, and 9.4 listed in Fig. 5.18b) are comparable to InGaAs-2 and InGaAs-3. However, the PVCR of InGaAs-4 is only 4.8, similar to InGaAs-1. It is not evident why the PVCR of InGaAs-4 is much smaller.

The modeled J-V characteristics for all three structures, with the measured R_{Series} , are also shown in Fig. 5.19a. For clarity, the model was only plotted up to the measured V_P . There is very close agreement between the modeled and measured results for InGaAs-5 and InGaAs-6. Because of the magnitude of R_{Series} , the Zener current density for InGaAs-6 is only slightly larger than InGaAs-5. If R_{Series} was smaller there would be a much larger disparity between the two curves. There is a large difference between the measured characteristic and the model for InGaAs-4, with the predicted/measured J_P of 780/360 A/cm². This is most likely due to the doping concentration of the device structure. If the actually doping concentrations differed from the target value by only $\pm 10\%$ ($\pm 5\%$ change in N^*), the predicted J_P varies from 430 A/cm² up to 1.3 kA/cm². Whereas the predicted J_P only ranges 2.6x and 2.2x for InGaAs-5 and InGaAs-6, respectively.

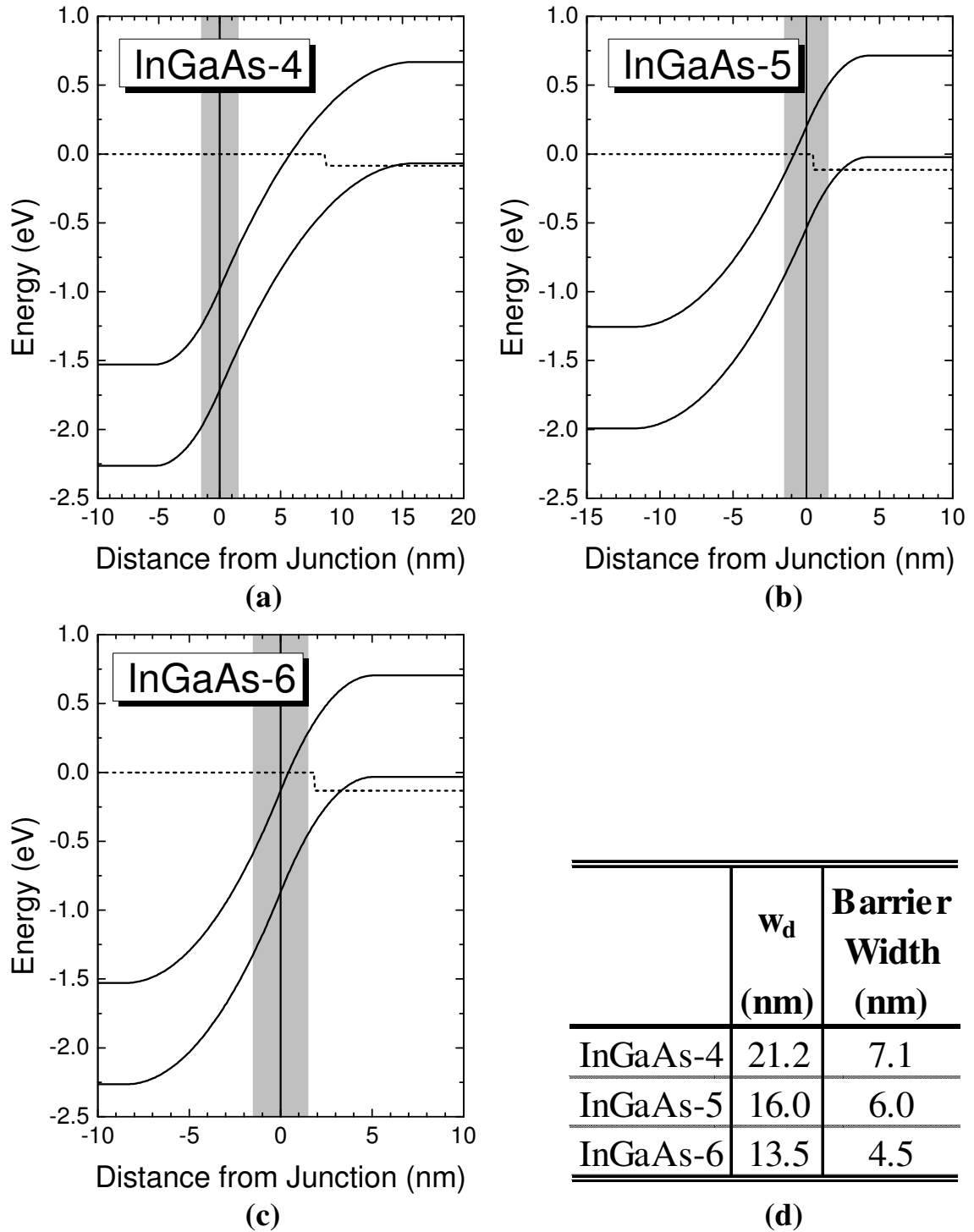


Fig. 5.20: Calculated band diagrams for (a) InGaAs-4, (b) InGaAs-5, and (c) InGaAs-6. The bands were calculated with a 0 nm *i*-layer and an applied bias of V_P as predicted by the Kane model. For easy reference, the quasi-Fermi levels were extended into the bandgap. Bottom right, (d) the depletion and tunnel barrier widths are listed.

In Fig. 5.19b, InGaAs-4, InGaAs-5, and InGaAs-6 are added to the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ trendline. As expected, InGaAs-5 and InGaAs-6 appear very close to the trendline. Recall from Chapter 3, material system trendlines are generated with $N_A = N_D$. As a result, there is a small but significant range in J_p for different ratios of N_A/N_D , of the same reduced average (N^*). Because of that difference, and the slope of the trendline, the InGaAs-4 data point appears much closer to the model than expected.

Calculated band diagrams are shown for each ETD in Fig. 5.20a-c. The bands were calculated using the target doping concentrations, but with an *i*-layer of 0 nm. The applied bias was set to V_p from the Kane model, and E_f was calculated using the basic 2-bands (Γ -valley only). The quasi Fermi energies ($E_{F,n}$ and $E_{F,p}$) were extended into the middle of the bandgap, for easy reference as to the magnitude of V_A (and hence, V_p). As with the previous $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETDs, V_p approximately $nkT + E_{F,p}$. Where *n* is some number, less than two. When $E_{F,p}$ is very close to E_V , V_p seems to decouple from $E_{F,p}$ and becomes constant. The depletion and tunnel barrier widths are listed in Fig. 5.20d. There is a fairly wide range in tunnel barrier widths (7.1 nm down to 4.5 nm), which follows the large range in J_p (from 360 A/cm² up to 56 kA/cm²).

5.4. Conclusions

In this chapter, the deep submicron process developed in Chapter 4 was improved with an extensive area characterization step performed post mesa-isolation etch. This characterization improves estimated junction areas over the entire sample, enabling accurate analysis of BTBT current scaling properties and current densities.

The two ultra-high current density $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETDs (InGaAs-1 and InGaAs-2) were fabricated with the deep submicron process. For each sample, about 100 area measurements and over 200 I-V measurements were used in the analysis. Line fits to V_p versus I_p plots indicated that the intrinsic V_p for InGaAs-1 and InGaAs-2 is 0.377 V and 0.137 V, respectively. I_p scaled linearly with junction area, for both device structures. The smallest InGaAs-1 devices did fall off

of the trendline, but this was due to a lack of measured junction areas and not non-idealities in the electrostatics. Therefore, there were no observed defects in the scaling properties of the tunnel junctions, down to 47 nm radii. Gaussian fits to J_p histograms yielded average J_p of 975 kA/cm² (InGaAs-1) and 210 kA/cm² (InGaAs-2). InGaAs-1 is the largest reported homojunction J_p , and second largest overall. This was accomplished not only because of the epitaxial quality and material parameters, but also the magnitude of doping concentration achieved during growth.

Band diagram calculations showed that the 3 nm *i*-layer adds a negligible width to the tunnel barrier. However, BNG and additional electron valleys (Γ - and X-) can drastically alter $E_{F,n}$ and tunnel barrier widths. Comparing the Kane model to experimental results, the basic 2-band model best matches pre-peak BTBT current density for both devices. However, 4-band $E_{F,n}$ modeling is needed to match the shape of the NDR region. Furthermore, a nearly perfect match between the model and experimental results was achieved for InGaAs-2 with BNG was also included. A more appropriate BNG model may result in an improved output for InGaAs-1. Comparing with results from literature, J_p versus N^* plot shows a clear exponential trendline for In_{0.53}Ga_{0.47}As, with the basic 2-band Kane model accurately fitting the trendline.

The modeled trendline was used to diagnose and predict the actual doping concentration present in InGaAs-3, which was fabricated using the basic process. The basic process was updated with a Mo, a refractory metal more appropriate for manufacturing. A J_p of 14 A/cm² was measured. As predicted from the In_{0.53}Ga_{0.47}As trendline, SIMS analysis confirmed that the reduced average doping of the structure was 4.2×10^{18} /cm³, resulting from ~1/10 targeted Be incorporation. For this device, the basic Kane model was very accurate in predicting the J-V characteristics. However, the 4-bands model made some small improvements in the forward direction.

The last In_{0.53}Ga_{0.47}As fabricated and characterized were of medium to large current density ETDs. InGaAs-4, InGaAs-5, and InGaAs-6 were found to have J_p of 380 A/cm², 7 kA/cm², and 56 kA/cm², respectively. Unlike the previous devices, SIMS analysis was not

performed to confirm doping concentrations. However, the Kane model accurately predicted the J-V characteristics of InGaAs-5 and InGaAs-6. The model small overestimation for InGaAs-4 may be a mostly due inaccurately assumed doping concentration. All of the experimental results fit on the characteristic trendline for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, which covers five orders of magnitude in current density.

Finally, the results from this chapter show that ultra-high current density ETDs can be fabricated and retain good characteristics when scaled down to deep submicron dimensions. The $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ material system follows a simple exponential trendline, which accurately predicts J_P over five orders of magnitude. The Kane model fits the trendline as well as J-V characteristics without any additional fitting parameters. The Kane model has been shown to accurately predict both J_P and J-V characteristics. Therefore, with a given J_P , which is unaffected by R_{Series} , the entire J-V characteristic may be calculated.

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CHAPTER 6

GaAs and InAs Esaki Tunnel Diodes

Previously, the PVCR and J_P of fabricated ETDs [1-4] were directly benchmarked against reports from literature [5-18]. In the last chapter, a characteristic trendline for the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ material system was created with experimental results from literature [18-22] as well as six ETDs from this work [23, 24]. The key results included (i) record high J_P (975 kA/cm^2), (ii) tunnel junctions scaled to deep submicron dimensions (46 nm radii) without any surface leakage or Fermi-level pinning effects observed, (iii) determination of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ characteristic trendline via experimental results and the Kane model, and (iv) accurate modeling of J-V characteristics covering a J_P range of 5 orders of magnitude. [18-27]

This chapter expands on the previous results by expanding the mapping efforts to GaAs and InAs ETDs [24-27]. With its large bandgap (1.4 eV), GaAs will have smaller BTBT current density as compared to $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. However, it is another material system with well known material parameters, a readily available source of experienced epitaxial growers, and can be grown as an unstrained homojunction ETD with similar quality as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. Additionally, are part of the ternary $\text{In}_{1-x}\text{Ga}_x\text{As}$ system, GaAs will represent the BTBT current density floor. Three separate GaAs ETD structures, fabricated with the basic process due to the small J_P expected, will be discussed. Results will be compared with data from literature in order to general a GaAs trendline. Finally, the Kane model will be compared to the experimental results.

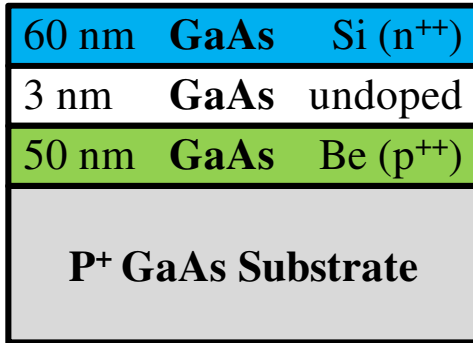
InAs has a much smaller bandgap (0.35 eV), enabling much larger BTBT current densities. As such, its characteristic trendline will be shown to represent the ceiling for the $\text{In}_{1-x}\text{Ga}_x\text{As}$ system. Three InAs ETD structure, fabricated initially using both the basic and deep submicron process, will be discussed. None of the few reports of InAs ETDs from literature [28-30] are appropriate for this work. Therefore, the InAs characteristic trendline is only matched to

the ETDs in this study. As before, the Kane model will be compared with the experimental results. When combined with the GaAs and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ results, the BTBT characteristics for the entire $\text{In}_{1-x}\text{Ga}_x\text{As}$ system can be interpolated. This makes the entire data set and model very powerful for a large range of homojunction ETD structures.

Finally, a unique result observed with the smallest J_p InAs ETDs will be discussed. Specifically, an observed NDR that is due to Mo and Ta contacts to p^{++} InAs. This is the first room temperature report of this phenomenon, and was only observed after the initial fabrication runs. It is proposed that Fermi pinning due to an undesirable interfacial oxide at the InAs surface is the main cause.

6.1. GaAs Esaki Diodes

The GaAs ETDs (Fig. 6.1a) follow a similar structure as the medium current density $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETDs from Section 5.3. The anode was only 50 nm thick, since these structures were grown directly on P^+ GaAs substrates to help minimize R_{Series} . Additionally, the GaAs ETDs were expected to have low current density, reducing the sensitivity to R_{Series} . As before, a 3 nm i -layer preceded the 60 nm cathode. All three GaAs ETDs targeted the same N_D (Be) concentration of $3 \times 10^{19} / \text{cm}^3$. The N_A (Si) concentration was systematically increased from $5 \times 10^{18} / \text{cm}^3$, to $1 \times 10^{19} / \text{cm}^3$, to $5 \times 10^{19} / \text{cm}^3$ for GaAs-1, GaAs-2, and GaAs-3 (Fig. 6.1b),



(a)

Device	N_D ($\times 10^{19} \text{ cm}^{-3}$)	N_A (cm^{-3})	J_p ($/\text{cm}^2$)	PVCR
GaAs-1	3	0.5	11 μA	1.1
GaAs-2	3	1	45 mA	7.5
GaAs-3	3	5	56 A	16

(b)

Fig. 6.1: Left, (a) Schematic diagram of GaAs ETD structures. Right, (b) table of target doping concentrations, as well as measured J_p and PVCR for GaAs-1, GaAs-2, and GaAs-3.

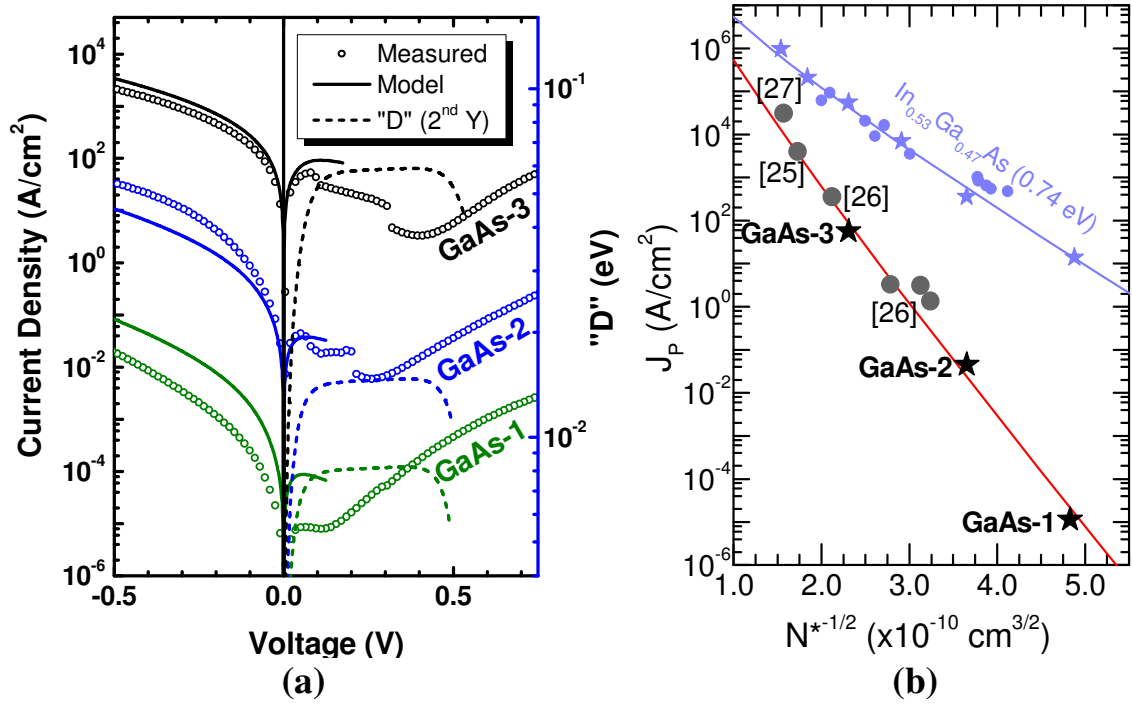


Fig. 6.2: Left, (a) typical J-V characteristics (symbols), modeling results (solid line), and “D” (dashed line; right y-axis) for GaAs-1, GaAs-2, and GaAs-3. Right, (b) GaAs trending (solid line) including data points from literature (circles) and this work (stars) [18-27]. In_{0.53}Ga_{0.47}As ETD trendline included as reference.

respectively.

Fabrication followed the basic process, similar to the medium current density In_{0.53}Ga_{0.47}As ETDs. That is, there was no activation anneal. Blanket Mo was deposited via sputtering as the contact metal. Contact lithography and plasma etch defined metal 1 contact, followed by mesa isolation etch. Limited optical microscope inspection was used to quickly assess junction areas. With its large bandgap (1.42 eV), it was known that the current density of the GaAs ETDs would be small, potentially much smaller than any other ETDs fabricated for this work. Therefore, large junction areas were needed to prevent current magnitudes from becoming too small.

Table 6.1: Modeling results for all three GaAs ETDs. As expected, w_d , tunnel barrier width, $E_{F,p}$, E_V , and J_P proportionately increase with each other. $E_{F,p}$ for GaAs-1 is greater than E_V , and therefore lies within the bandgap.

	w_d (nm)	Barrier Width (nm)	$E_{F,n}-E_C$ (eV)	$E_V-E_{F,p}$ (eV)	n	J_P (/cm ²)	V_P (V)
GaAs-1	25.2	18.8	0.558	-0.0125	2.68	88.1 μ A	0.057
GaAs-2	19.1	14.1	0.558	0.0100	2.20	37.9 mA	0.067
GaAs-3	12.2	8.9	0.558	0.0864	0.835	92.2 A	0.108

6.1.1. Results for GaAs ETDs

Typical J-V characteristics for GaAs-1, GaAs-2, and GaAs-3 are shown in Fig. 6.2a. There is negligible R_{series} present in the measurements, with V_P remaining less than 0.1 V for all ETDs. The magnitude of current density is very small, ranging seven orders of magnitude, and is largely attributed to the large bandgap (large tunnel barrier results in small tunneling probabilities) and low p-type concentration. From Fig. 6.1b, average measured J_P is 11 μ A/cm², 45 mA/cm² and 56 A/cm², for GaAs-1, GaAs-2, and GaAs-3, respectively. The maximum PVCR increases with J_P , from 1.1, to 7.5, to 16. The increase in PVCR is largely attributed to the ratio of $E_{F,p}/E_{F,n}$, discussed below.

The characteristic trendline for GaAs (Fig. 6.2b) is below and much steeper than the previously established In_{0.53}Ga_{0.47}As trendline. Several GaAs ETDs from literature [25-27] achieved much higher J_P , because of the doping concentrations they were able to obtain. In a departure from using SIMS to establish doping concentrations, Oh *et al.* [26] used capacitance measurements to extract depletion widths. For this work, the depletion widths were used to back out N^* for accurate placement in the figure. The trendline calculated from the is practically the same as the least squares exponential line fit to the data points (not shown here). Furthermore, the trendline accurately predicts J_P over 9.5 orders of magnitude, from a medium J_P of 31 kA/cm² [27] down an ultra small 14.5 μ A/cm² from GaAs-1. This occurs over the same approximate doping range as for the In_{0.53}Ga_{0.47}As ETDs.

$$V_p = E_{F,\text{minor}} + n \times kT \quad (6.1)$$

Key model results are listed in Table 6.1 and calculated band diagrams shown in Fig. 6.3.

The calculated depletion (w_d) and tunnel barrier widths rapidly decrease as N_A increases, resulting

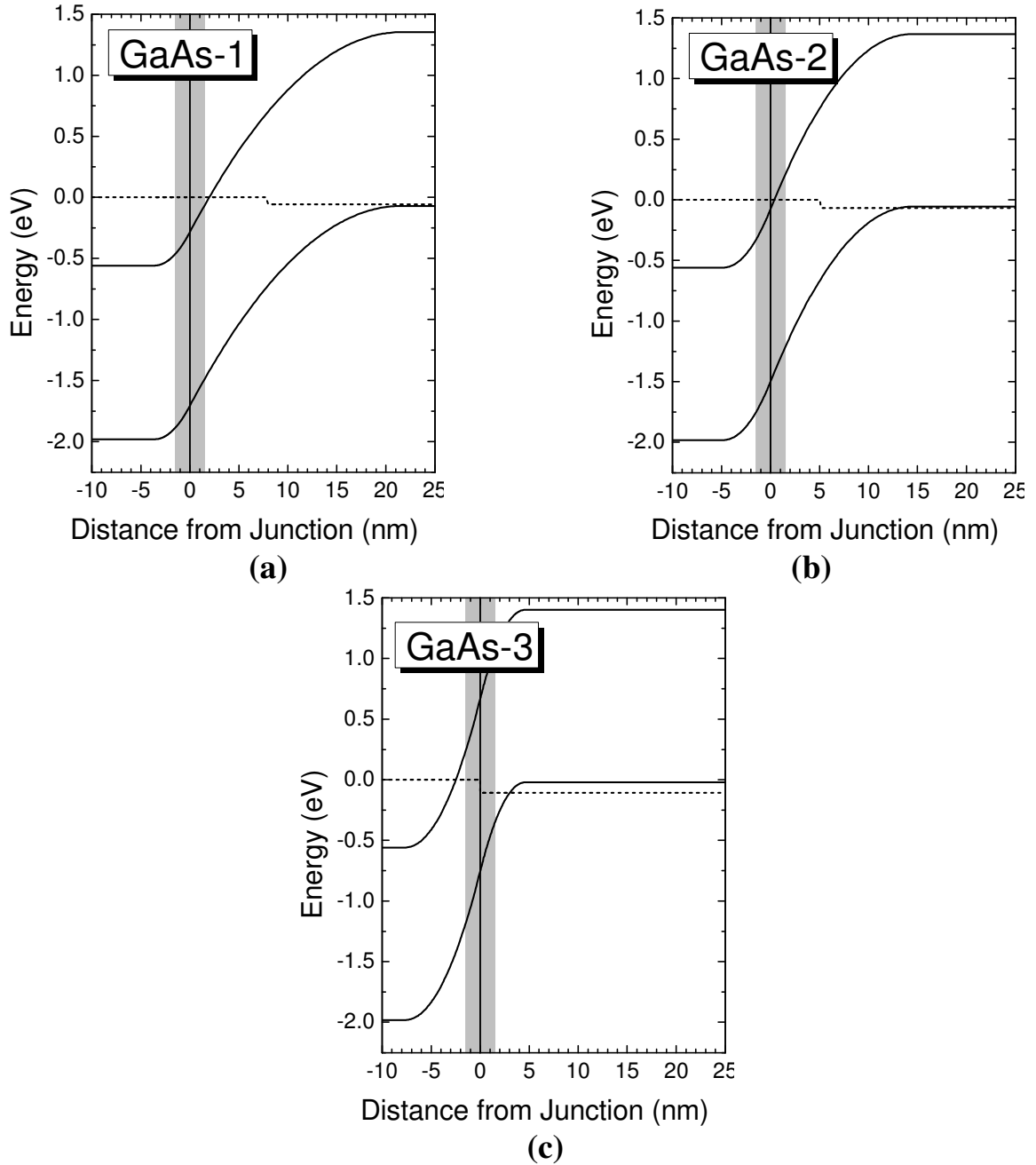
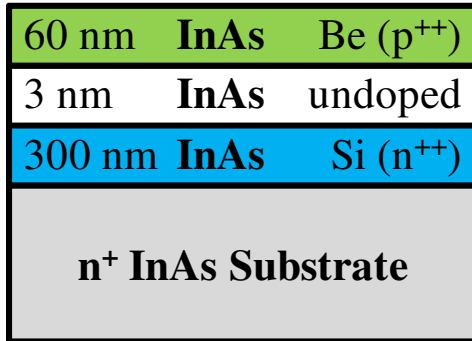


Fig. 6.3: Calculated band diagrams at a bias of V_p for (a) GaAs-1, (b) GaAs-2, and (c) GaAs-3. Only 2-bands $E_{F,n}$ (Γ -valley) calculations were available. Quasi Fermi energies were extended into the bandgap for easy reference. Shaded region is the i -layer.

in exponentially larger increases in J_p . Due to its large DOS for holes ($\sim 9.7 \times 10^{18} / \text{cm}^3$), $E_{F,p}$ is 12.5 meV above E_V for GaAs-1, and only 10 meV below E_V for GaAs-2. Consequentially, V_p is small, nearly constant, decoupled from $E_{F,p}$, and n becomes large (6.1). Since N_A for GaAs-3 is relatively large, $E_V - E_{F,p}$ is big enough to control V_p , reducing n to ~ 0.8 .

The modeled J-V characteristics for the GaAs ETDs (Fig. 6.2a) are shown for reverse bias, and a little beyond V_p in forward. As with the band diagram calculations, the model assumes 2-bands only (Γ -valley). The model accurately predicts the current density for GaAs-2 and GaAs-3, up to V_p . There is a large discrepancy between the model and measurements for GaAs-3. For these ultra low current densities, the differences are likely due to the unknown active doping concentrations. A $\pm 10\%$ doping variation ($\pm 5\% N^*$) in GaAs-1 results in a 17x range in J_p . Even the uncertainty associated with SIMS may not sufficiently characterize the doping profile. However, the model will predict the BTBT current density over the region of interest if J_p is matched to the measured value.

The model does not accurately predict the NDR region. With the small DOS for electrons ($\sim 4 \times 10^{18} / \text{cm}^3$), $E_{F,n}$ (0.56eV) is large enough to start filling the second valley (L-valley) which is ~ 0.5 eV above the Γ -valley. As a result, the modeled NDR is much longer than the measured NDR. Additionally, $E_{F,n}$ is much greater than $E_{F,p}$, causing the overlap integral (D, shown in Fig. 6.2a) to quickly plateau in forward bias, and remain there for almost the entire



(a)

Device	N_D ($\times 10^{19} \text{ cm}^{-3}$)	N_A (cm^{-3})	J_P ($/\text{cm}^2$)	PVCR
InAs-1	0.3	1.8	2.3 kA	2.0
InAs-2	1	1.8	38 kA *	NA
InAs-3	3	1.8		

(b)

Fig. 6.4: Left, (a) Schematic diagram of InAs ETD structures. Right, (b) table of target doping concentrations, as well as measured J_p and PVCR for InAs-1, InAs-2, and InAs-3.

range. Consequentially, in GaAs-1 the BTBT current density post-peak does not have much “time” to drop off before J_{Excess} dominates. As a result, the measured PVCR is very smaller and likely cannot be improved without increasing N_A . For GaAs-2, J_{Excess} did not increase as quickly as J_p , shifting V_p to the right and causing a large increase in PVCR. The PVCR would be increased (and potentially maximized) when $E_{F,n} = E_{F,p}$. Because for that situation, D will consistently rise to $V_p = E_{F,n}$, and then immediately drop off.

6.2. InAs Esaki Diodes

Unlike the previous ETDs, InAs-1, InAs-2, and InAs-3 (Fig. 6.4a) were grown with the p-type layer (anode) on top of the n-type (cathode) layer, in order to help maintain sharp junction profiles. Furthermore, only n-type InAs substrates were available (p-type GaSb has a small lattice mismatched). The p-type dopant species, Be, has relatively large surface segregation. If it

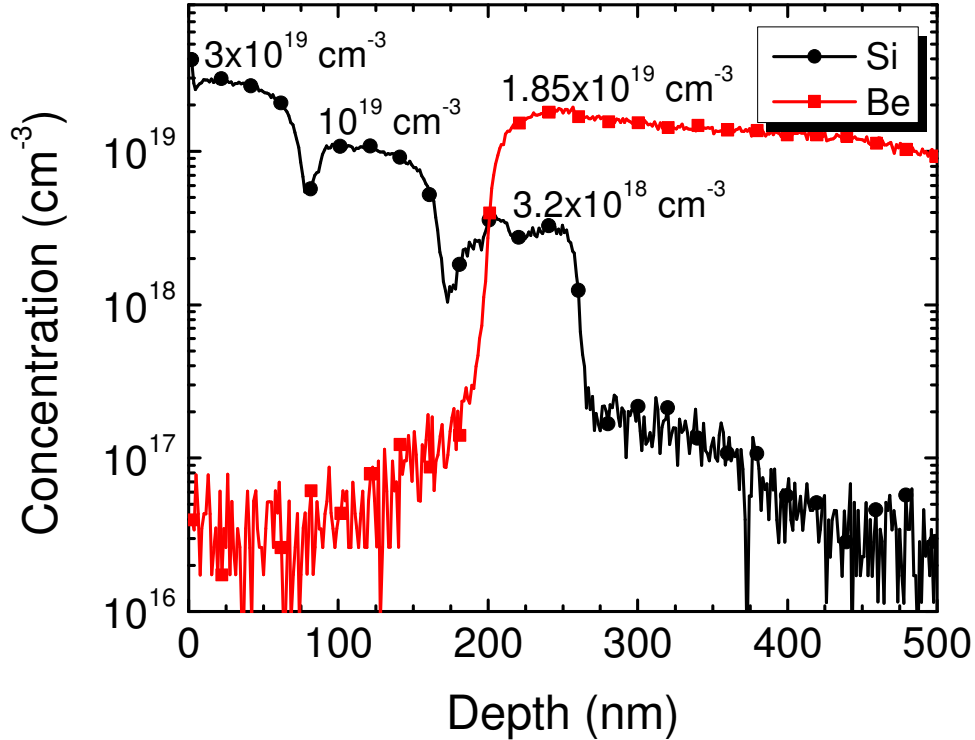


Fig. 6.5: SIMS results of the doping calibration growth for the InAs ETDs. Three Si steps and one Be mesa indicate the doping concentrations for all three InAs ETDs.

were placed in the bottom layer, it may have significantly segregated through the *i*-layer and into the cathode. This could have negatively impacted the I-V characteristics. Since it was expected that InAs would have poor results due to its small bandgap (0.35 eV), it was even more important to consider dopant surface segregation effects.

With the cathode on the bottom, the InAs ETDs were grown by MBE on top of n^+ InAs substrate. The cathode was grown with three separate doping concentrations using Si (Fig. 6.4b); (i) $3 \times 10^{18} / \text{cm}^3$ (InAs-1), (ii) $1 \times 10^{19} / \text{cm}^3$ (InAs-2), and (iii) $3 \times 10^{19} / \text{cm}^3$ (InAs-3). The anode was grown to 60 nm thick and doped with Be at a concentration of $1.8 \times 10^{19} / \text{cm}^3$ for all InAs ETDs. Additionally, Be concentration was held constant because of concerns over the DOS for holes ($6.7 \times 10^{18} / \text{cm}^3$) and the maximum achievable Be ($1.8 \times 10^{19} / \text{cm}^3$) concentration. Under these conditions, $E_V - E_{F,p}$ will only be ~ 50 meV, which does not leave a lot of room for change. Therefore, in order to see the largest spread in J_p , Be was maximized. As with the previous homojunction ETDs, a 3 nm *i*-layer was inserted between the anode and cathode.

A doping calibration growth was used to accurately estimate the average doping concentrations that will be present in the final InAs ETD structures. All four targeted doping

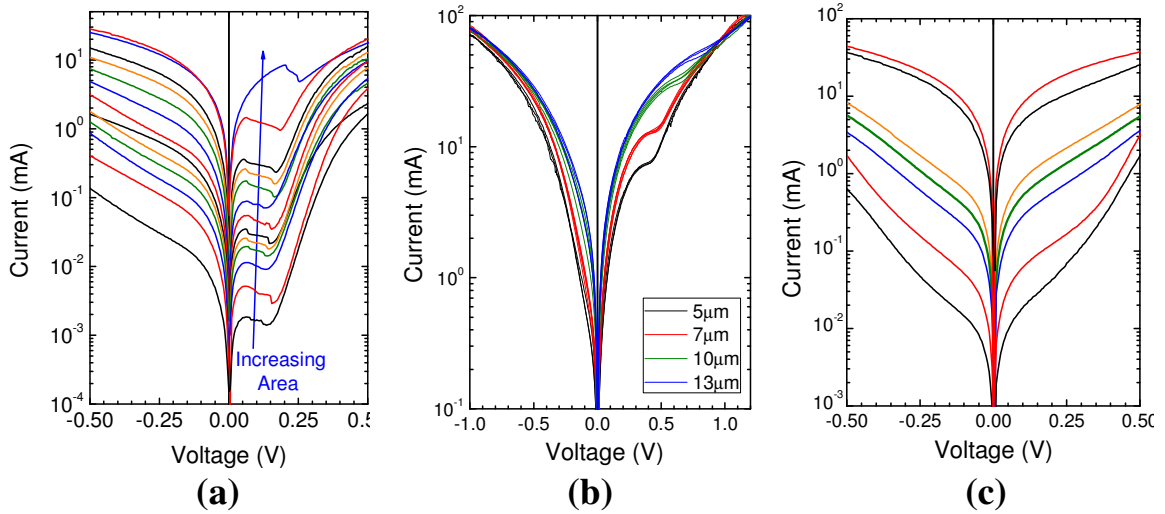


Fig. 6.6: I-V characteristics for (a) InAs-1, (b) InAs-2, and (c) InAs-3. InAs-1 shows clear NDR and I_p scaling with area. InAs-2 shows strong kinks, indicating the location and magnitude of the pure BTBT J_p . InAs-3 mostly looks ohmic.

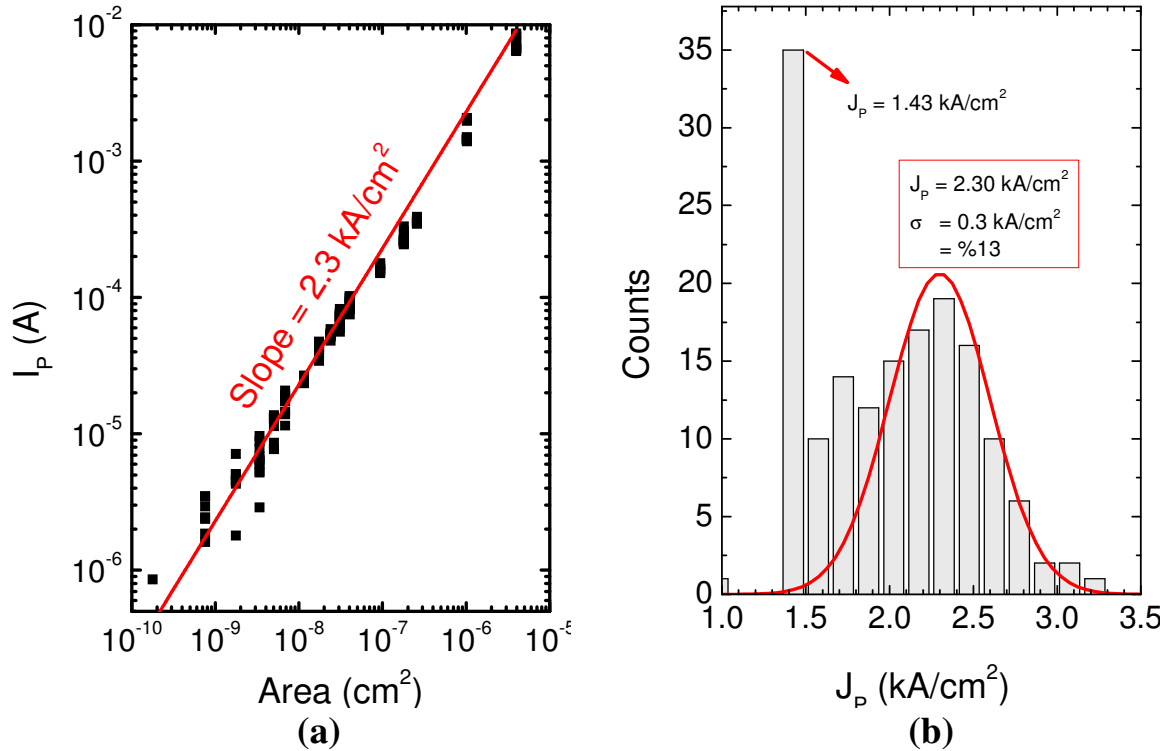


Fig. 6.7: Left, (a) measured I_p versus junction area. Right, (b) histogram of J_p (167 measurements), with Gaussian fit indicating average J_p of 2.3 kA/cm².

concentrations were grown in a 300 nm InAs layer. SIMS analysis was used to verify the doping concentrations (Fig. 6.5). However, junction profile information cannot be extracted from the calibration growth.

All InAs ETDs were fabricated using the basic process, similar to the GaAs ETDs. That is, there was no activation anneal. Blanket Mo was deposited as the contact metal, via sputtering. Contact lithography and plasma etch defined metal 1 contact, followed by mesa isolation etch. Limited optical microscope inspection was used to quickly assess junction areas. Even though InAs has a small bandgap (0.35 eV), the relatively small reduced doping average (N^*), from the small doping concentrations, will limit current densities below 200 kA/cm². Therefore, deeply scaled junction areas were not needed. However, a companion InAs-1 piece was fabricated using the deep submicron process.

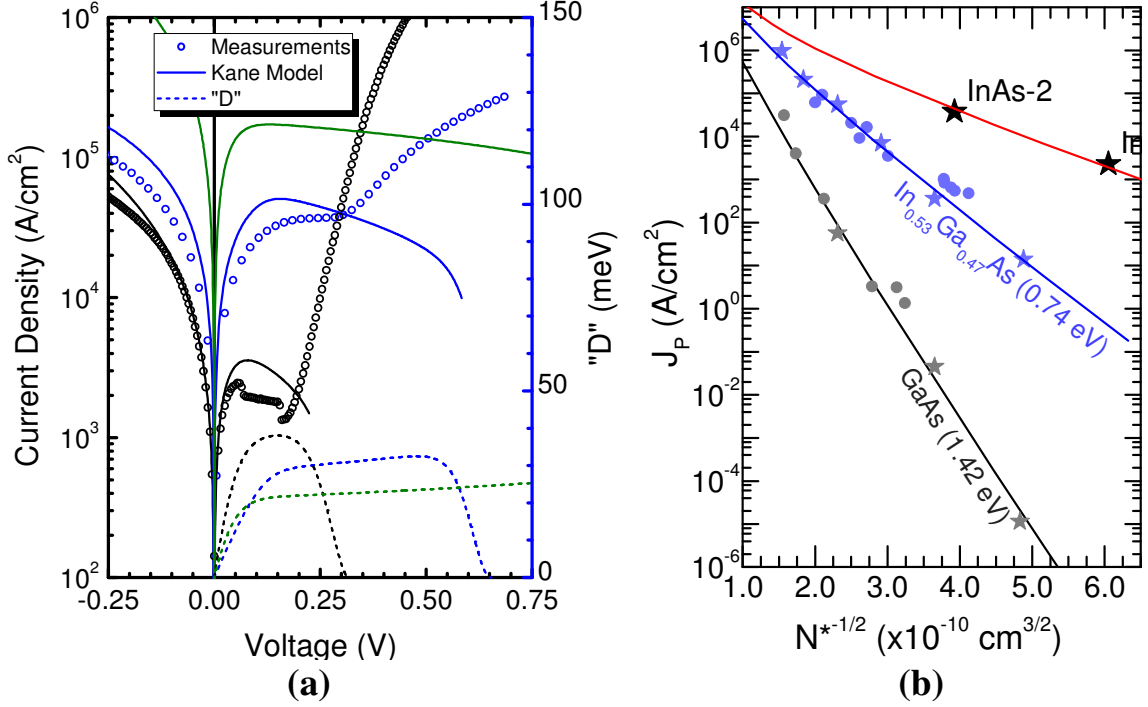


Fig. 6.8: Left, (a) measured J-V characteristics (symbols) as well as modeled characteristics (solid line) and “D” (dashed line). Right, (b) characteristic trendlines for GaAs, $\text{In}_{0.53}\text{As}_{0.47}\text{As}$, and InAs [18-27]. The InAs trendline, calculated from the Kane model, is greater than the previous trendlines.

6.2.1. InAs ETD Electrical Results

The DC I-V electrical characteristics measured for (a) InAs-1, (b) InAs-2, and (c) InAs-3 are shown in Fig. 6.6. In forward bias, InAs-1 shows clear NDR with PVCR up to 2.0 and I_p that appears to scale well with just area. The R_{Series} becomes significant above ~ 1 mA of current, and shifted V_p for the largest devices only. InAs-2 exhibits clear “kinks”, similar to backward diodes. The current magnitude of the kink increases linearly with junction area, indicating that this is an ETD with large I_{Excess} masking, or overtaking, the I_p and I_v . The magnitude of the kink is indicative of the BTBT J_p , but not a precise measurement since it also includes parasitic. There is a significant amount of R_{Series} present, shifting the kink voltage to the right as the junction area (and current) increases. The kink becomes less pronounced as the shift increases. Therefore, the smallest devices show the best characteristics. Finally, InAs-3 did not exhibit any NDR or kink-like behavior. As a result, the BTBT current density for InAs-3 could not be characterized.

From Fig. 6.7a, J_p does in fact scaling linearly with junction area. The slope of the line fit gives a preliminary indication of the average J_p . The Gaussian fit to the histogram in Fig. 6.7b gives a J_p of 2.3 kA/cm², with a standard deviation of 300 A/cm² (13%). There is a second peak in the histogram centered at 1.43 kA/cm². This peak is from a second set of InAs-1 samples whose areas were not corrected for, and therefore the current densities calculated from this set is suspect. However, these samples did provide interesting characteristics in reverse bias, which is discussed in Section 6.2.2. From the position of the kinks, the approximate J_p of InAs-2 is calculated to be 38 kA/cm².

In Fig. 6.8a are two representative J-V curves for InAs-1 and InAs-2 (symbols). From the figure, it is clear that InAs-2 has greater BTBT current density and R_{series} . There are very few reports of InAs ETDs in literature [28-30], none of which fit the criteria for inclusion in this analysis. Therefore, there only two data points to assess the trendline (Fig. 6.8b), and any line fit would be superfluous. The characteristic InAs trendline as calculated by the Kane model (solid line) is shown in Fig. 6.8b, and clearly fits the InAs-1 and InAs-2 data points. Due largely to its small bandgap, the InAs trendline is greater than both the GaAs and In_{0.53}Ga_{0.47}As trendlines. However, InAs has the shallowest slope, indicating a smaller sensitivity to doping variation. In other words, only small doping concentrations are needed to achieve medium BTBT current densities. However, it only possible to increase J_p by a few orders of magnitude, even with maximized doping concentrations.

Table 6.2: Modeling results for all three InAs ETDs. As expected, w_d and tunnel barrier width decrease as doping, $E_{F,n}$, and J_p increase. Interestingly, V_p and “ n ” significantly increases, even though $E_{F,p}$ remains constant.

	w_d (nm)	Barrier Width (nm)	$E_{F,n}-E_C$ (eV)	$E_V-E_{F,p}$ (eV)	n	J_p (/cm ²)	V_p (V)
InAs-1	19.6	11.6	0.269	0.0493	1.11	3.57 kA	0.078
InAs-2	15.3	6.0	0.604	0.0493	2.15	50.7 kA	0.105
InAs-3	15.1	3.5	1.260	0.0493	3.120	172 kA	0.130

Modeled J-V characteristics for all three InAs ETDs are shown in Fig. 6.7a, with the final results listed in Table 6.2. A $150 \mu\Omega\text{-cm}^2 R_{Series}$ was added to InAs-2, for improved matching with the measured data. As can be seen, the modeled J-V characteristics for InAs-1 and InAs-2 is greater than the measurements. However, due to its shallow slope, both devices lie much closer to the InAs trendline (Fig. 6.8b) than is apparent from the modeled J-V characteristics. Furthermore, a 10% doping variation for InAs-1 and InAs-2 outputs a low/high J_P of $2.3/5.6 \text{ kA/cm}^2$ and $38/71 \text{ kA/cm}^2$, respectively. It is likely that the actual doping concentration in the ETDs is approximately 10% lower than the target values.

As with GaAs, $E_{F,n}$ was calculated with only 2-bands (Γ -valley only). The L-valley is $\sim 0.7 \text{ eV}$ above the direct bandgap, and therefore initially one would expect that it would not play a large role in the Fermi energy calculations. However, because of its small DOS for electrons ($1.2 \times 10^{17} / \text{cm}^3$), the L-valley will start to limit $E_{F,n}$ starting with N_D of $\sim 3.5 \times 10^{18} / \text{cm}^3$. Therefore, the predicted NDR for InAs-1 looks to be reasonable. However, for InAs-2 and InAs-3, the NDR region is drawn-out due to the extended mesa-like overlap integral (D) associated with the calculated Fermi energies. Regardless, except at low current densities (N_D concentrations), $E_{F,n}$ will be much greater than $E_{F,p}$, causing “D” to be mesa-like in shape. Combined with a naturally

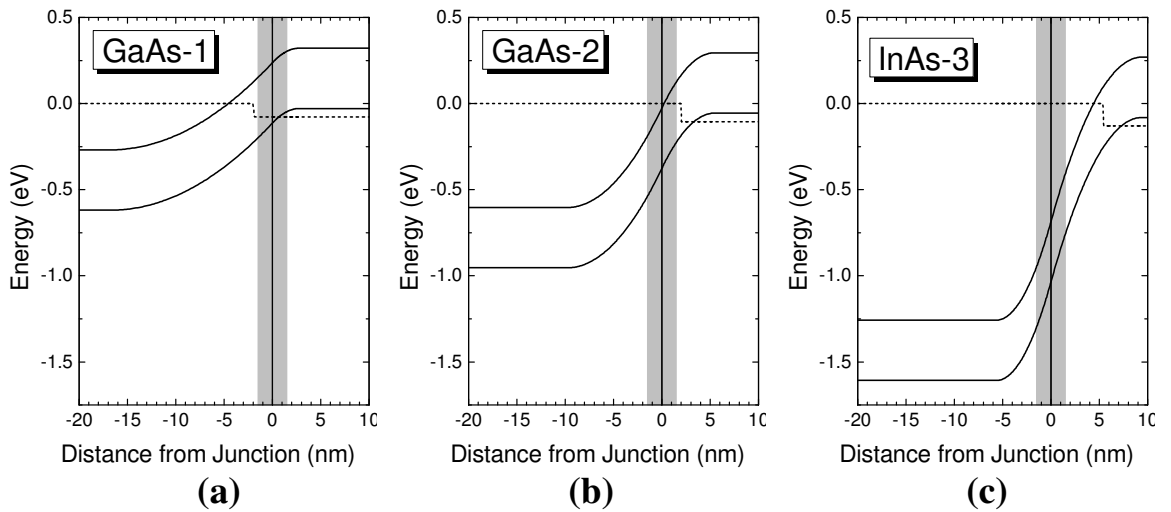


Fig. 6.9: Calculated band structure for (a) InAs-1, (b) InAs-2, and (c) InAs-3. $E_{F,n}$ was calculated using only the Γ -valley.

larger V_P due to the small bandgap of InAs, and any reasonable magnitude in J_{Excess} will begin to swamp out J_V , negating the NDR and forming a “kink” in the characteristic. Additionally, J_{Excess} will typically be relatively large due to InAs small bandgap. Therefore, as a homojunction ETD, is unlikely that InAs can exhibit large J_P .

Contrary to previous ETDs, the maximum “D” value decreased with increasing doping concentration. Recall from Chapter 3, the overlap integral has an inverse dependence on ξ_{ave}/E_G in addition to the direct dependence on $E_{F,smaller}$. Previously, N_A was the main species varied. Due to large DOS for holes on the systems under investigation, the change in $E_{F,p}$ was more significant than the relatively small increase in ξ_{ave}/E_G . However, for the InAs ETDs, the similar increases in $E_{F,n}$ caused very large increases in ξ_{ave}/E_G , as can be seen in the calculated band diagrams in Fig. 6.9. Consequentially, the maximum “D” value decreased with increasing N_D .

Additionally, because of the small bandgap and relatively large $E_{F,n}$, the average electric field (ξ) does not change as rapidly for InAs, then in the previous systems. Consequentially, the tunnel barrier thickness does not change much with V_A . Therefore, V_P shifts to larger than expected biases where Fermi-Dirac statistics requires that greater percentages of available states are filled with electrons in the cathode.

6.2.2. NDR from Metal on P⁺ InAs Contacts

The first couple iterations of InAs-1 fabrication looked at (i) Ta, (ii) Mo, and (iii) Al contacts using the basic fabrication process. The ideal metal workfunction (ϕ_m) for Ta (4.2 eV), Mo (4.6 eV), and Al (4.2 eV) indicates that these metals should form Schottky contacts. Unexpectedly, NDR was observed in reverse bias during electrical characterization of the Mo and Al contacts (Fig. 6.11). As can be seen, the reverse bias peak scales with the area of the ETD under test with a smaller J_P . Therefore, is clear that the observed NDR is related to the InAs mesa and contact metal of the forward biased ETD structure. Otherwise, the I_P would be constant

or scaling independent of the device under test (DUT), such as the forward bias characteristic of the ETD used as the virtual short to ground.

The Mo contact had a much larger J_p of 720 A/cm^2 versus the Al contact, with 160 A/cm^2 J_p . It is believed that the metal-semiconductor interface is to the root source of this NDR. Several past reports [31-35] have observed this phenomenon at cryogenic temperatures, but never before has it been reported with room temperature measurements. It has been proposed that the key to forming NDR at the metal-InAs interface is due to the unusual level of Fermi pinning for InAs. Unlike most other III-V semiconductors, the surface E_F will be pinned near the conduction band. Thus, with contact to p-type InAs, a surface inversion channel is formed (Fig. 6.10a). Generally it is believed that the Fermi pinning is due to thin dielectrics, on the order of monolayers, forming on the InAs surface. After fabrication of these samples, it was discovered that a small leak was present in the system. Consequently, a low base pressure was not achieved ($\sim 5 \text{ } \mu\text{Torr}$), and therefore that was a lot of O_2 in the chamber during deposition. This was likely the source of a non-ideal interfacial layer, providing Fermi pinning of the InAs surface. Subsequent InAs ETD fabrication had very low base pressures ($< 1 \text{ } \mu\text{Torr}$), much less O_2 present,

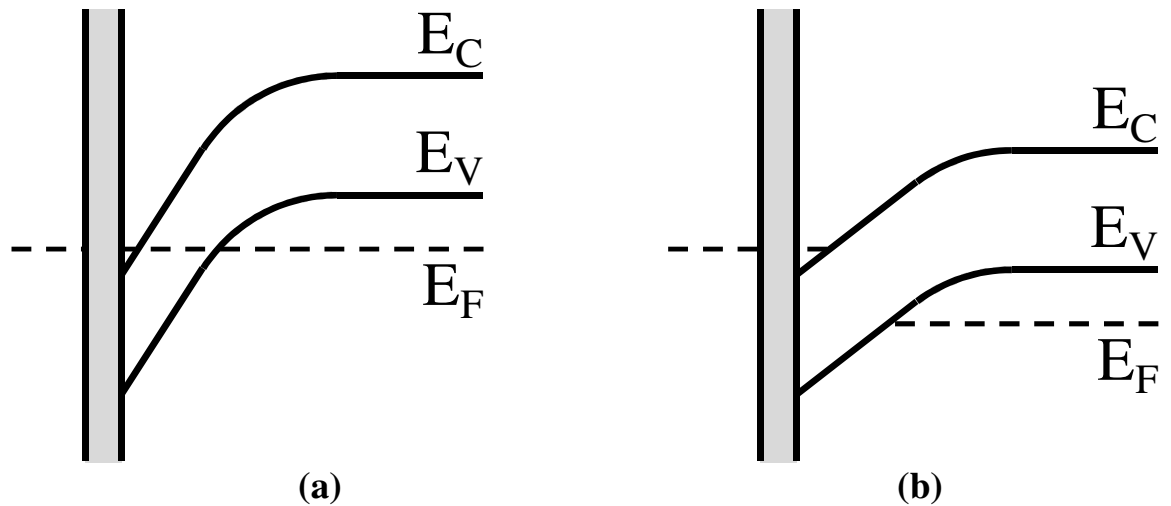


Fig. 6.10: Proposed band diagrams of the metal-InAs interface at (a) equilibrium and (b) with an applied bias. Between the metal and InAs is an ultra thin insulative layer providing an additional tunnel barrier, and Fermi level pinning at the interface.

and therefore a better metal-InAs interface, with less Fermi pinning.

When the metal-InAs junction is under a small positive bias (the ETD is reverse biased), electrons in the metal contact can tunnel into the surface channel, and then through the bandgap, into the hole states present below E_V and above E_F . Therefore, as expected, an immediate rise in current would be measured. Biasing a little further aligns the InAs bandgap with the E_F in the metal region, significantly blocking current flow from the metal to InAs (Fig. 6.10b). As with basic ETDs, one would expect that increased Fermi energies (below E_V in the p^+ InAs bulk, and above E_C at the pinned surface) would increase J_p . The doping in this study is 20x to 200x greater than in those from literature [31-35]. At the concentrations used in the papers, $E_{F,p}$ is not even below E_V . However, cooling to cryogenic temperatures would increase $E_{F,p}$ and reduce I_{Excess} , making an NDR visible. Whereas, in this study $E_{F,p}$ is already shifted below E_V , enabling the observance of NDR at room temperature.

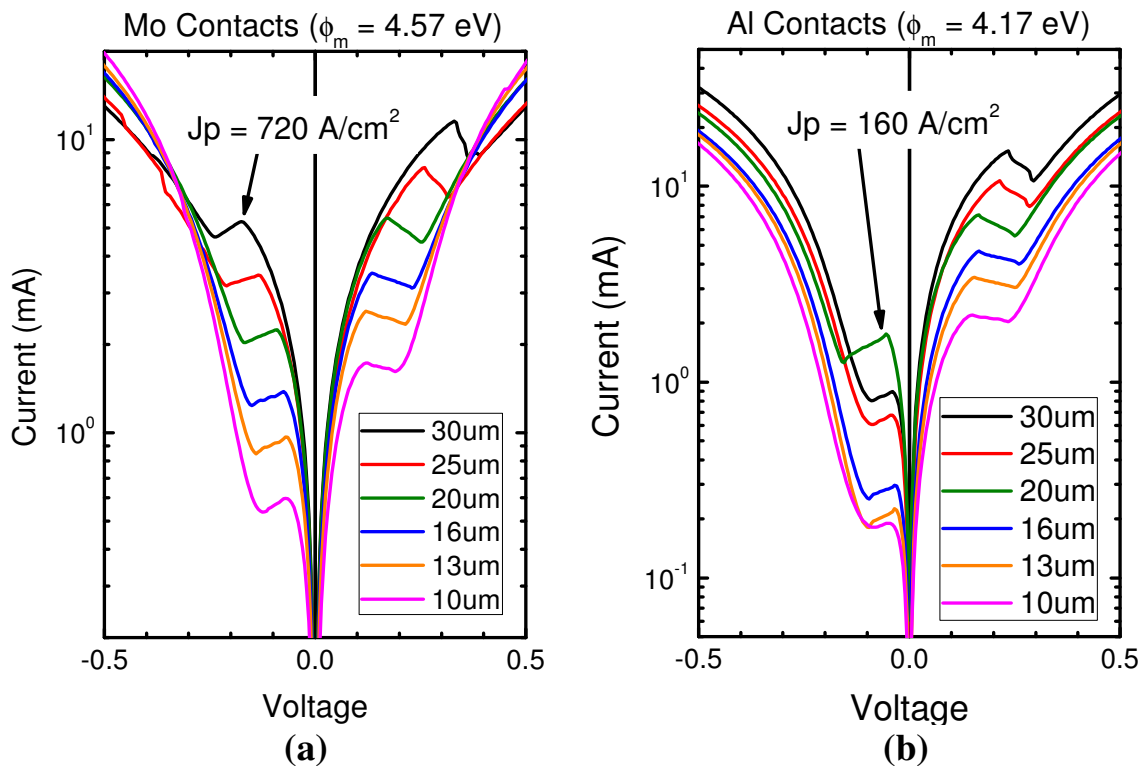


Fig. 6.11: Measured I-V characteristics displaying NDR in reverse bias due to the (a) Mo and (b) Al metal contacts to p^{++} InAs.

6.3. Conclusions

The BTBT characteristics of GaAs and InAs were investigated. With these result, and those for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ from Chapter 5, the entire $\text{In}_{1-x}\text{Ga}_x\text{As}$ ternary system is known. The GaAs ETDs represent the BTBT floor, whereas InAs has a greater trendline than the other two. However, due to the material properties and maximum achievable doping for InAs, it cannot achieve J_p as high as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. Therefore, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ would be the best candidate for an unstrained homojunction TFET. On the other hand, one is not concerned about turning off the BTBT (leakage currents), than InAs may still be beneficial. Conversely, it low BTBT current densities are needed, then GaAs is an ideal material system.

Three GaAs ETDs were fabricated with measured J_p of $11 \mu\text{A}/\text{cm}^2$, $45 \text{ mA}/\text{cm}^2$, and $56 \text{ A}/\text{cm}^2$ for GaAs-1, GaAs-2, and GaAs-3, respectively. Over 6.5 orders of magnitude in J_p were covered, ranging from the ultra low current density (GaAs-1) to moderately low (GaAs-3). A few devices from literature achieved moderate to high current density [25-27]. Ultimately, the maximum achievable doping concentration combined with the bandgap of GaAs (1.42 eV) limits J_p to less than $100 \text{ kA}/\text{cm}^2$. As expected, the characteristic trendline of GaAs was less than $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. However, it is a much steeper slope, covering 10.5 orders of magnitude compared to five for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. This clearly shows that GaAs is much more sensitive to doping variation. Additionally, the Kane model accurately predicts the GaAs characteristic trendline and J-V characteristics.

Three InAs ETDs were fabricated. However, InAs-3, which had the largest doping, did not exhibit any NDR or characteristic “kinks” indicating the presence of J_p , most likely a result of very large excess currents. InAs-2 behaved more like a backwards diode, due to a sever “kink” at approximately the location of its BTBT J_p at $\sim 38 \text{ kA}/\text{cm}^2$. InAs-1 was the only device to clearly show a peak, worth a J_p of $2.3 \text{ kA}/\text{cm}^2$ and maximum PVCR of 2.0. Without any extra data points from literature, only InAs-1 and InAs-2 were used to verify the characteristic trendline

predicted by the Kane model. The Kane model matched fairly close to the experimental results, validating the model's accuracy for InAs. In addition to the InAs homojunction results, NDR in reverse bias was observed for the initial InAs-1 runs using Mo and Al contacts. This was explained as a surface inversion channel due to Fermi pinning, a phenomenon that is so far unique to InAs. This is the first report of metal to p⁺ InAs NDR at room temperature. The measured J_p values were 720 A/cm² and 160 A/cm² for Mo and Al, respectively. Further experimentation would need to be performed in order to determine the controllability of the characteristic.

Finally, this chapter completes the comprehensive mapping of the In_{1-x}Ga_xAs ternary system. Experimental results were the basis of determining the range of achievable J_p , and characteristic trendlines. The Kane model was shown to accurately fit the system and predict device characteristics. The results from this work may be used to design homojunction ETDs with specific device characteristics, or judge the suitability of a particular In_{1-x}Ga_xAs system for a particular application. Furthermore, the experimental results may be used to calibrate finite element BTBT models in order to improve their ability to quantitatively predict the behavior of more complicated and potentially useful device structures.

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CHAPTER 7

Universal BTBT Model

In this chapter the composite $\text{In}_{1-x}\text{Ga}_x\text{As}$ characteristic BTBT map is presented. The full mapping utilizes two plots, which related J_p with (i) doping concentration and (ii) bandgap (tunnel barrier height). From the $\text{In}_{1-x}\text{Ga}_x\text{As}$ map, it is determined that the maximum J_p measured in this work (975 kA/cm^2 from InGaAs-1) can be improved by no more than $\sim 3x$. From the final $\text{In}_{1-x}\text{Ga}_x\text{As}$ characteristic BTBT map, a new universal BTBT model (UBM) will be presented, discussed, and compared with the Kane model as well as the homojunction experimental results. The new model utilizes two fitting parameters, but provides a closed form analytical equation for the computation of J_p over a wide range of materials and doping conditions. There are no other reports of such a model in literature, including a similar approach by Solomon, *et al.* [1]. Furthermore, it is believed that physical meaning can be attributed to the fitted parameters with the help of the Kane model [2] for reference.

7.1. Final Mapping of $\text{In}_{1-x}\text{Ga}_x\text{As}$ BTBT Characteristics

The comprehensive map of J_p for the $\text{In}_{1-x}\text{Ga}_x\text{As}$ ternary system is shown in Fig. 7.1. On the left (Fig. 7.1a) is the familiar plot of J_p versus $N^{*1/2}$ for (i) GaAs, (ii) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and (iii) InAs. The solid data points are experimental results from this work, open points are from literature, and the solid lines are calculated using Kane's model [2]. Those three material systems show the minimum, central, and maximum characteristic trendlines – respectively - for the capabilities of $\text{In}_{1-x}\text{Ga}_x\text{As}$. The trendlines themselves are exponential by nature, except for a small upward bend at very large doping and small bandgaps. The experimental results reside close to the theoretical trendlines (within a 10% margin of error in doping concentration). Largely due to its E_G (1.42 eV), GaAs achieved ultra-low J_p of 11 ($\mu\text{A/cm}^2$) and ΔJ_p range of

~9.5 orders of magnitude which is much larger than the other systems. InAs has the largest trendlines, however ΔJ_P only ranges one order of magnitude due to its small bandgap (0.35 eV) and DOS (N_C/N_V of $0.12/6.7 \times 10^{18} /\text{cm}^3$). In fact, this limited the maximum J_P to $38 \text{ kA}/\text{cm}^2$, which is approximately the same value as the maximum GaAs ETD. The $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ trendline is nearly halfway between GaAs and InAs, covering five orders of magnitude. Even with its larger bandgap (0.74 eV) than InAs, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ achieved the largest J_P of $975 \text{ MA}/\text{cm}^2$.

Concerning homojunction TFET structures, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ would be a better option than InAs or GaAs. It can achieve very large and small BTBT currents. In other words, it is the most promising at achieving desirable I_{On} as well as I_{On}/I_{Off} ratios. InAs would provide large I_{On} , but low I_{On}/I_{Off} ratios, which would result in unacceptable noise margins and off-state power consumption. GaAs would likely provide a much larger I_{On}/I_{Off} ratio, as well as better SS.

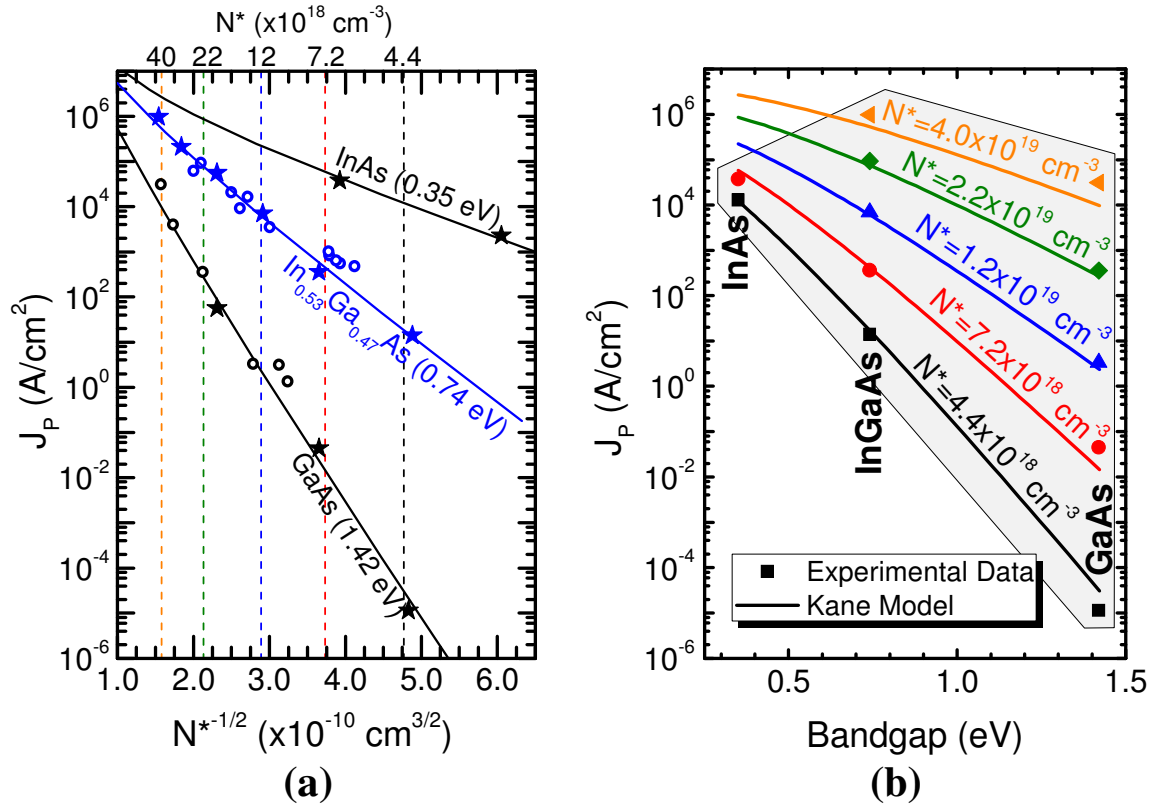


Fig. 7.1: Left (a), standard J_P versus doping for GaAs, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and InAs ETDs. Vertical cutlines indicate N^* values used for the right hand plot. (b) Shows the relationship between J_P and E_G for various N^* . Solid lines are calculation results from the KMP.

However, its large bandgap prevents very large BTBT currents, limiting its ability to supply current densities necessary to drive large integrated circuits and thereby negating its attractiveness as a material system for TFETs. However, in circuit applications that are driven primarily by voltage without the need for large drive current densities, GaAs may be an excellent choice.

The characteristic trendlines in Fig. 7.1a quantify the relationship between J_p versus doping, and show a general relationship with E_G ($J_p \propto 1/E_G$). The exact relationship between J_p and E_G , which represents the tunnel barrier height, is shown in Fig. 7.1b. Specifically, the composition of $\text{In}_{1-x}\text{Ga}_x\text{As}$ is stepped from $x = 1$ (InAs) to 0 (GaAs) and evaluated at a specific N^* . Thus, each line quantifies the relationship between E_G and J_p , for a given N^* . The data points are experimental results closest to the vertical cut-lines in Fig. 7.1a. The lowest InAs point is taken as the logarithmic average between InAs-1 and InAs-2, since the target N^* is roughly in the middle of the two experimental results. Typically there is a small deviation between the target N^* and experimental N^* value, resulting in a small deviation between the data points and model. Excepting a small deviation, there is generally an exponential relationship between J_p and E_G (tunnel barrier height), which was expected. The slope of each trend decreases as doping increases. In general, J_p changes less rapidly as (less sensitive to) N^* increases and E_G decreases. Furthermore, J_p appears to approach a common value beyond the plotted values and well beyond what is physically achievable with ($\text{In}_{1-x}\text{Ga}_x\text{As}$). However, additional material systems with smaller bandgaps, or heterojunction ETDs of Type II and III band alignments may have effective bandgaps less than InAs, and continue the trends established in this work.

The shaded region in Fig. 7.1b covers that area where experimental results exist. In other words, within this design space an appropriately designed and fabricated ETD is likely to exhibit NDR in forward bias and have J_p close to the predicted value. As it stands, it is less likely structures designed outside of the shaded region will operate as well. Therefore, the maximum J_p that can be reliably achieved are $\text{In}_{1-x}\text{Ga}_x\text{As}$ ETDs with %In mole fractions of 50% to 65%. Higher doping concentrations are needed to significantly surpass 1 MA/cm^2 for $\text{In}_{1-x}\text{Ga}_x\text{As}$ ETDs.

However, even by increasing the doping concentrations to reasonable maximum levels ($\sim 10^{20} / \text{cm}^3$) the greatest achievable J_p is $\sim 2 \text{ MA/cm}^2$, a fairly small improvement in on the results reported in this work.

The comprehensive BTBT mapping of the $\text{In}_{1-x}\text{Ga}_x\text{As}$ system (Fig. 7.1) is a powerful tool. The example above clearly shows that the maximum J_p cannot be extended much beyond the current record of 975 kA/cm^2 . This can be used to determine the optimal achievable drive current that an unstrained, homojunction $\text{In}_{1-x}\text{Ga}_x\text{As}$ TFET can achieve. More importantly, this work provides extensive, self-consistent, experimental results that is already being used for the calibration of TCAD BTBT models. Furthermore, the models can be calibrated not only for a single material system, but specifically for (i) GaAs, (ii) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and (iii) InAs and the ability to interpolate the remainder of the ternary system. Additionally, the $\text{In}_{1-x}\text{Ga}_x\text{As}$ map can be used to design ETDs by designating a desired J_p and determining the requisite In composition and doping concentration, or vice versus. There may be the need for a few iterations in device design to fine tune the results, but this is far more efficient than approximations from previous experiments. Finally, the method of fabrication, testing, analysis, and mapping may be extended to any number of additional materials systems, including heterojunction ETDs.

7.2. Universal BTBT Model

At the start of Chapter 3 four desirable features for an analytical BTBT model were listed. Ultimately, the best convergence of those features would be a so called universal BTBT model (UBM). Ideally, the UBM would be a (i) closed form analytical expression, without any complex functions (the four basic arithmetic functions, exponents, and exponentials). There would (ii) not be any fitting parameters, with only standard (iii) material constants used to delineate the output of various material systems. Finally, it would be equally applicable in (iv) forward and reverse bias.

In 2004, Solomon, *et al.* [1] presented a universal model developed for Si to account for tunneling leakage current in p-n junctions associated with MOSFETs. After the appropriate transformations are made, the model is compact and easy to work with. It is likely that the procedure can be adapted to work with other material systems. However, a different set of approximations, transformations, and fitting parameters may be needed, which does not conform to the goal equally applicable across material systems (feature (iii)). It is also not obvious if it would work in forward bias at all, let alone predict J_p , which is a key parameter that enables to computation of the BTBT J-V characteristics.

Largely through directed trial and error, it was discovered that there does exist a very simple exponential relationship between J_p , depletion width (w_d), E_G , and relative tunneling effect mass (m_r), as described by (7.1) and (7.2). Fig. 7.2a shows a plot of J_p versus $T_{material}$ for a wide

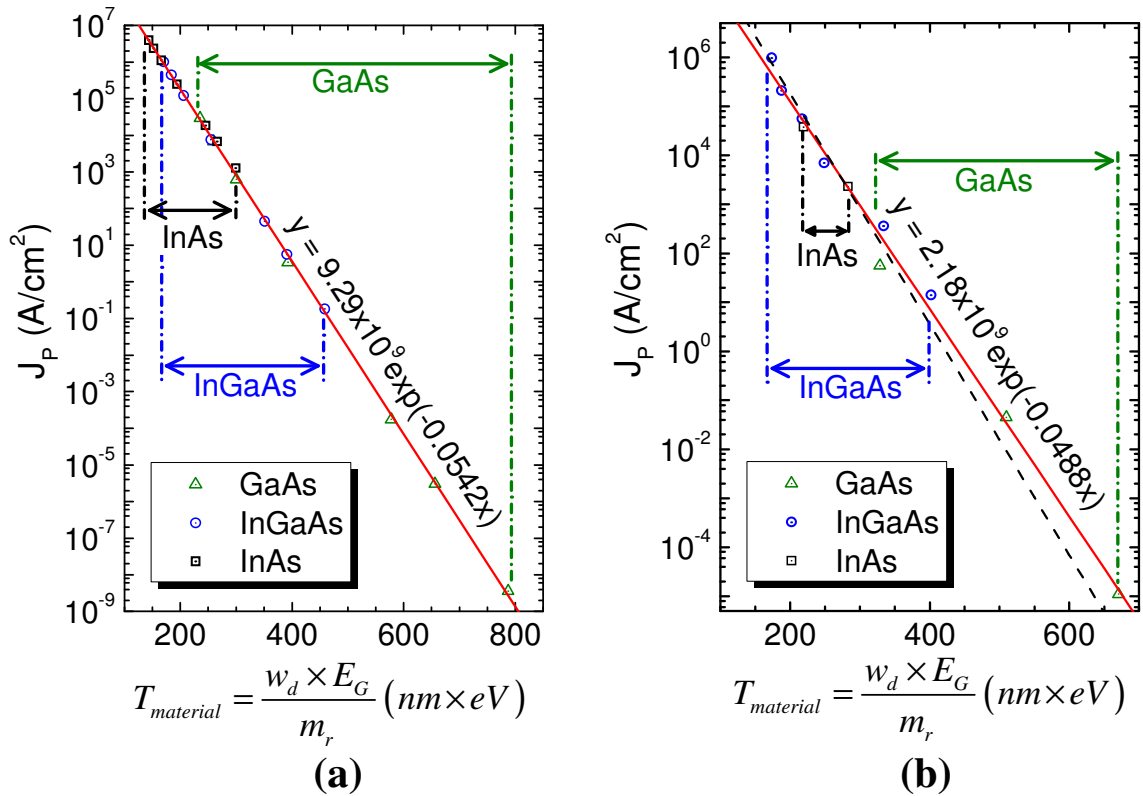


Fig. 7.2: Universal model transformation applied to the (a) Kane model ($N_A = N_D$), as well as, (b) experimental results from this work. The dashed line in (b) is the exponential fit from (a). Most deviations in the experimental data are a result of $N_A \neq N_D$.

range of N^* values for (i) GaAs, (ii) $\text{In}_{1-x}\text{Ga}_x\text{As}$, and (iii) InAs as predicted by the Kane model. Those three material systems were chosen because this work has already shown that the model agrees well with the experimental results. In Fig. 7.2a, there are only very small deviations between the calculated data points from KMP and the exponential line fit, some of which is likely due to the use of w_d at a V_A of 0 V. Even though the UBM uses fitted parameters, they are constant over the three material systems used in Fig. 7.2.

$$J_p = A \exp(\beta \times T_{\text{material}}) \quad (7.1)$$

$$T_{\text{material}} = \frac{w_d \times E_G}{m_r} \quad (7.2)$$

Fig. 7.2b shows the UBM applied to the experimental results reported in Chapter 5 and 6. As can be seen, there the data forms another exponential line. The exponential fit to the experimental data has a slightly shallower slope (solid line) as compared to the exponential line from Fig. 7.2a (dashed line). A significant amount of the deviation present is due to $N_A \neq N_D$. Additionally, notice that the range on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ fully encompasses InAs, and the maximum GaAs shifted to the right, which conforms to the mapping analysis performed in Section 7.1.

In (7.2), E_G and m_r are simple material parameters, but w_d is a structure parameter. It helps to provide intuitive insight, but requires additional computation. Using standard the standard depletion approximation, T_{material} becomes (7.3), which requires the built in bias (V_{bi}) and N^* (a supplied device design parameter). The super-degenerate approximation for E_f can be used to derive an appropriate equation for V_{bi} , (7.4). This results in a simplified closed form, analytical model, that is accurate across multiple material systems without modifying any parameters. Notice that N_D and N_A cannot be combined as N^* . Therefore, different ratios of N_A/N_D but with the same N^* will have some minor variations in J_p , which is observable in Fig. 7.2b. However, the model can be further simplified for the case of $N_A = N_D$. The built in bias can

be rewritten in the form of $V_{bi} \approx E_G + \gamma N^{*2/3}$, where γ is defined in (7.5). Notice that V_{bi} has no direct dependence on temperature ($N_{C/V}^{2/3}$ is proportional to kT), which is a result of using super-degeneracy. Consequently, the only temperature variation visible from the output of UBM are the result of E_G , ϵ_s , and m_r changing with temperature. Generally, those parameters do not change rapidly with temperature and some of the changes will compensate for each other, thereby causing only small changes in the models output. This conforms with the temperature analysis performed in Chapter 4, and conventional theory.

$$T_{material} = \frac{\sqrt{2\epsilon_s} E_G}{\sqrt{qm_r}} \sqrt{\frac{V_{bi}}{N^*}} \quad (7.3)$$

$$V_{bi} \approx E_G + (kT) \left(\frac{3\sqrt{\pi}}{4} \right)^{2/3} \left[\left(\frac{N_D}{N_C} \right)^{2/3} + \left(\frac{N_A}{N_V} \right)^{2/3} \right] \quad (7.4)$$

$$\gamma = (kT) \left(\frac{3\sqrt{\pi}}{4} \right)^{2/3} \left[N_C^{-2/3} + N_V^{-2/3} \right] \quad (7.5)$$

Characteristic terndlines versus N^* were recreated for (i) GaAs, (ii) InGaAs, (iii) GaSb, (iv) InAs, and (v) InSb using KMP (solid lines) and UBM (data points). However, a small multiplicative correction factor was added to the intercept/slope of the exponential line fit for InAs (1.1/0.45), GaSb (1/4.3), and InSb (1.165/1.165). With further analysis and comparison to the Kane model, it is expected that the constants to the exponential line fit can be related to physical parameters. This would negate the need for fitted parameters and explaining the small changes needed to improve accuracy. In Fig. 7.3a, the solid points use the unaltered constants. As can be seen, the correction factor for InAs only made small improvements to the fit. Notice that the UBM is able to accurately account for the small upward curvature to the characteristic trendlines that is clearly visible for InAs and InSb.

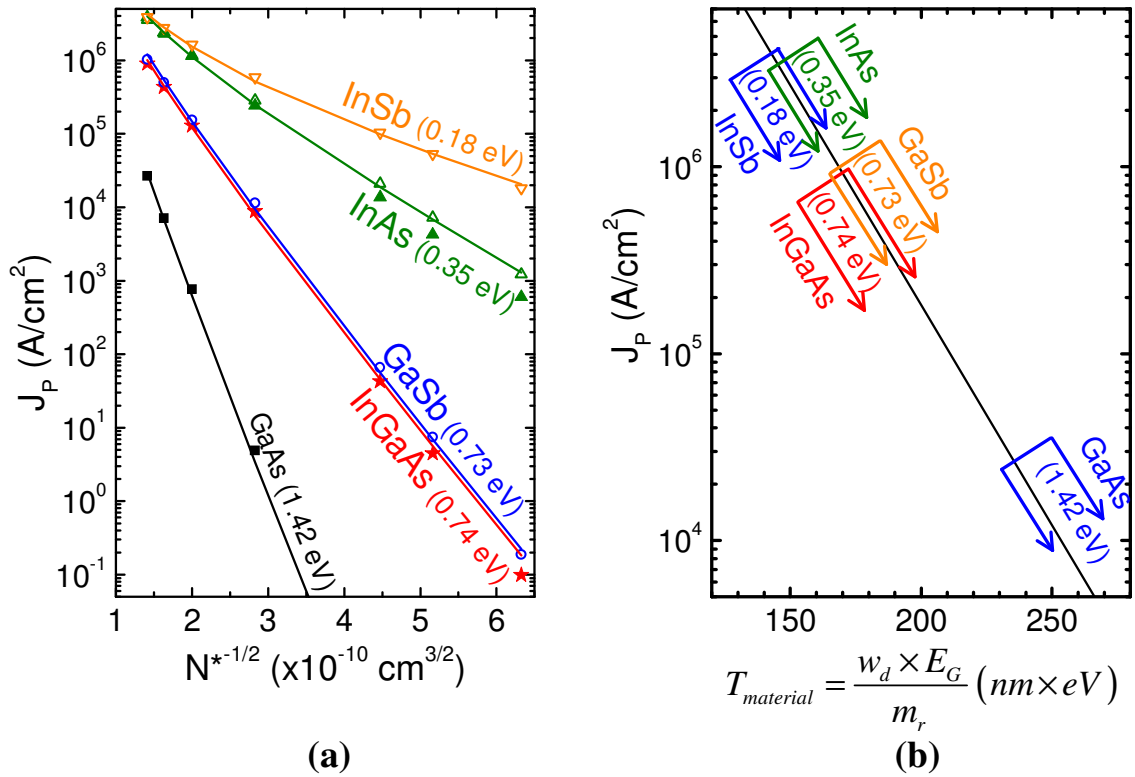


Fig. 7.3: Left (a), characteristic trendlines for (i) GaAs, (ii) In_{0.53}Ga_{0.47}As, (iii) GaSb, (iv) InAs, (v) InSb calculated by Kane (solid) and UBM (data points). The solid points use the base-line UBM, where the open points use correction factors. Right (b), UBM trendline (solid) marked with the predicted maximum J_P .

Finally, Fig. 7.3b plots J_P versus $T_{material}$, with the approximate maximum achievable J_P , ignoring non-idealities. It was assumed that the maximum achievable doping concentration is $\sim 10^{20}$ /cm³, which is reasonable for most material systems. Notice that as E_G becomes smaller, the effect on J_P decreases, which was previously observed in Section 7.1. In generally, UBM is in very good agreement with Kane model, whose accuracy for several of the material systems has been verified with experimental in this work. UBM is a closed form analytical equation, that does not use any complex functions. It currently uses two fitted parameters, which work across multiple material systems. Its applicability has not been applied to other biasing conditions. Therefore, the UBM presented here is much closer to the ideal universal tunneling model than Solomon [1], and some additional development in order to appropriately relate the fitted parameters to physical constants and parameters. Regardless, as it currently stands, UBM is another powerful tool for mapping ETD characteristics, and designing ETD structures.

7.2.1. Model Limitations

As with any model, the UBM is only accurate for some range of conditions. Since this model is matched to Kane's BTBT model, one can expect similar limitations. That is, unstrained homojunction ETDs made with direct bandgap material systems. Additionally, the doping profiles should be approximately square with a negligible i -layer. Furthermore, the final form of the model uses super degeneracy to calculate Fermi energies. Therefore, it is reasonable to expect greater deviations at lower doping concentrations. On the other hand, significant deviations may occur at ultra high doping concentrations due to the position and curvature (for effect mass considerations) of the "L" and "X" valleys.

Specifically, the model has only been fitted to the experimental results discussed in this work: $\text{In}_{1-x}\text{Ga}_x\text{As}$. There may be a different form needed for other material systems if the shapes of their characteristic trendlines are significantly different. For instance, strained and heterojunction ETDs will likely exhibit unique trendline shapes. Furthermore, there may be no simple UBM modification to correct for the unique tunneling barriers formed in heterojunction ETDs.

References for Chapter 7

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CHAPTER 8

Conclusions

Previously, it was determined from the characteristic BTBT map that the maximum J_p measured in this work (975 kA/cm² from InGaAs-1) can only be improved upon by $\sim 3\times$ for the In_{1-x}Ga_xAs ternary system. For dramatic improvements to the maximum current density the basic ETD structures must be modified using (i) δ -doping, (ii) strain, (iii) Type II band alignment, and/or (iv) Type III band alignments. This chapter will begin with discussing the four basic methods for increasing BTBT current density.

In its current form, the Kane model program (KMP) is ready for distribution and use by other groups, which has always been part of the intent for KMP. However, there are many improvements that can be made. (1) The UBM can be added as an additional BTBT model. (2) A tool for comparing and matching experimental and modeled characteristics within KMP. (3) Graphical analysis of I-V, band diagram, carrier distribution, and overlap integral structure. Finally, (4) modifications and improvements to the Kane model for improved accuracy to a larger range of device structures.

Finally, an overview of the work completed in this dissertation will be discussed as two separate groups. The first group discusses Tools and procedures developed for the completion of this work and continued development of the field. The second group relates to the experimental results and how they advanced the field of BTBT devices.

8.1. Beyond Unstrained Homojunction Esaki Diodes

There are four structural adaptations that can be made to the basic ETD in order to improve BTBT current densities beyond the mapped design space in this work without resorting solely to semiconductors with smaller E_G or higher doping capabilities. Specifically, (i)

δ -doping, (ii) strain, (iii), Type II band alignments, and (iv) Type III band alignments. These variations, and combinations thereof, have dominated efforts in literature to optimize BTBT current density and/or PVCR. However, the experiments typically involve no more than a few ETD structures which ultimately cannot be used to generate a characteristic trendline as described in this work. Additionally, a lack of compiled baseline data in literature has made it difficult to determine the effectiveness of the variations described below.

The simplest adaptations are δ -doping layers (Fig. 8.1a). This method is credited as one major enhancement enabling Si/SiGe ETDs to achieve J_P and PVCR up to ~ 200 kA/cm² [1] and 6 [2], respectively. In this method, epitaxial growth is halted on one, or both, sides of the i -layer. However, deposition of the dopants is continued, ideally forming a monolayer of dopant atoms at the surface. In practice, the dopants will continue to segregate and diffuse. Nonetheless, extremely large doping concentrations are achievable for an ultra thin layer. Consequentially, the

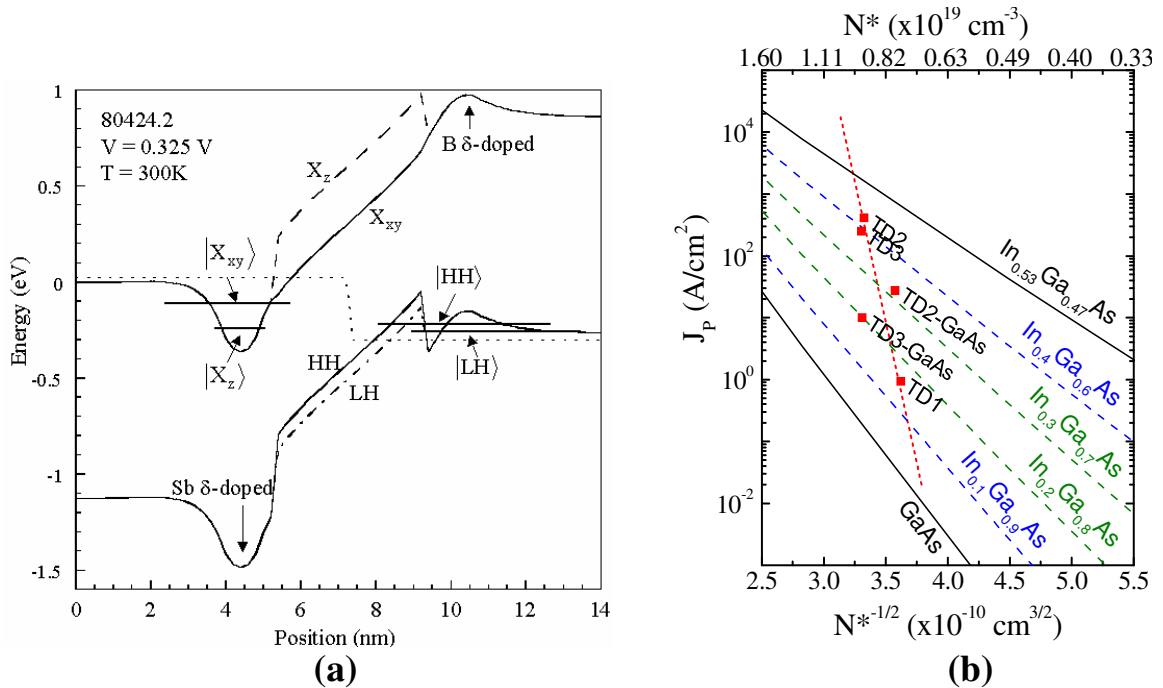


Fig. 8.1: Left (a), Si/SiGe resonant interband ETD band diagram illustrating (adopted from [1]) δ -doping and Type II band alignment. Right (b), GaAs/InGaAs heterojunction ETDs. The measured J_P for each structures far exceeds the 10% (TD1, TD3, and TD3-GaAs) and 20% (TD2 and TD2-GaAs) In_xGa_{1-x}As characteristic trendlines.

depletion region can be confined mostly within the i -layer. The BTBT current density is thereby dominated by the i -layer thickness instead of doping concentration, which typically is more controllable and can result in enhanced BTBT characteristics [3].

Strain has been beneficially used to enhance MOSFET characteristics by improving carrier mobilities and increasing drive currents [4-7]. Similarly, E_G and m_r can be manipulated by strain. Recall, from Chapter 4, the GaAs/InGaAs heterojunction ETDs produced J_p far greater than the predicted 10% and 20% In content characteristic trendlines (Fig. 8.1b). This enhancement is largely due to the insertion of a thin, strained, $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer near the tunnel junction. The band alignment at the hetero-interface is very small (< 100 meV) and of type I. In other words, a standard homojunction $\text{In}_x\text{Ga}_{1-x}\text{As}$ ETD would provide similar, if not better BTBT probabilities. Therefore, the effect of strain on various material parameters was enough to enhance the tunnel characteristics.

Heterojunctions may also be used to engineer an improved tunnel barrier, enhancing BTBT without strain. If the heterojunction ETD results in a type II band alignment (Fig. 8.2a) [8], the energy region with BTBT ($E_{v,p} - E_{c,n}$) has a much smaller tunnel barrier width than either material by itself. The smallest barrier width occurs in a small region indicated by the shaded circle and quantified as $\Delta E = 80$ meV in Fig. 8.2a. This staggered bandgap results in a characteristic trendline greater than either material involved, included InAs. However, notice that the tunnel barrier height remains equal to E_G on their respective sides of the junctions. As a result, J_{Excess} is reduced by the larger bandgap material, improving PVCR (or I_{Off} in a TFET).

The Staggered gap ETD can be improved upon by increasing the band offset until a broken gap (Type III) heterojunction is formed (Fig. 8.2b) [8]. In this case, the shaded circle indicates a region ($\Delta E = -70$ meV) where the tunnel barrier width is ideally 0 nm. In other words, the band structure forms more of a pipeline in which carriers are free to move from one side to

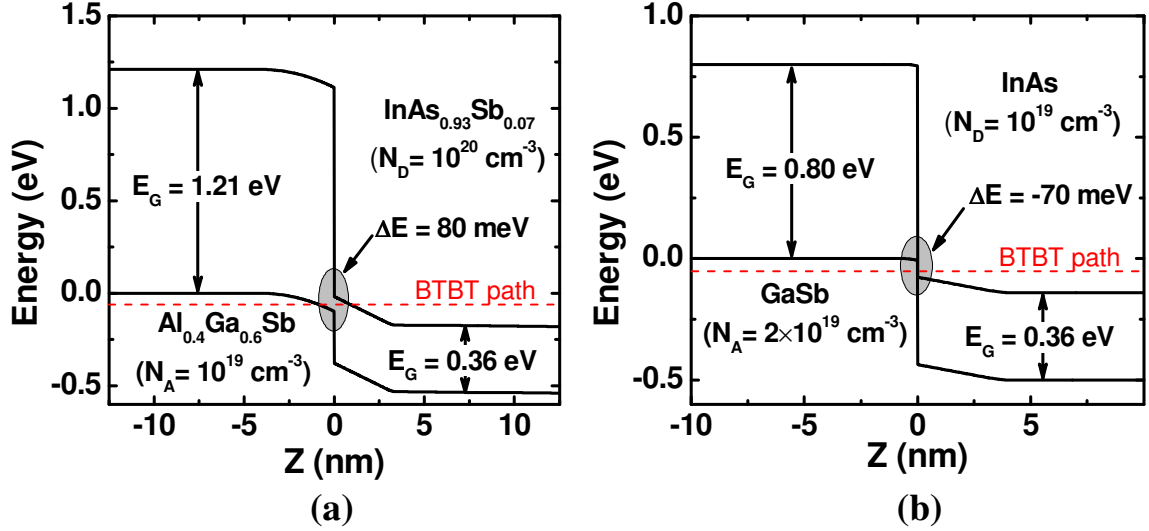


Fig. 7.2: Band diagrams showing the improved tunneling barrier widths for a (a) type II staggered gap and (b) type III broken gap heterojunction ETDs (adopted from [8]).

the other with very little effort. Consequentially, very large BTBT current densities are achievable [8] while maintaining relatively large PVCR.

Implementing one or more of the above ETD structure adaptations can greatly enhance BTBT characteristics, and greatly increases the number of structure designs. However, by following the device mapping procedure developed in this work, the behavior of any particular system can be systematically characterized with a limited number of fabrication runs. All that remains is choosing the structure design to implement, which can be narrowed down by considering (i) application, (ii) available material systems, (iii) maximum desired complexity, (iv) realistic band diagrams, and (v) material parameters as well as their dependence on strain.

8.2. Enhancements to the Kane Model Program

The Kane model program (KMP) developed for this work provides a straight forward GUI for operation. The KMP provides many useful tools including (i) J-V calculation, (ii) N^* sweep, (iii) basic band diagrams, and (iv) overlap integral structures, which are all described in Chapter 3. The program can be distributed for use by other research groups. There are several additions that can be made to KMP for improved analysis and modeling capabilities. (1) The

easiest to implement would be the addition of UBM calculations. Whenever the standard Kane model is ran, the program can also calculate UBM for quick and easy comparison between the two models and experimental results. Additionally, a new function can be added to sweep E_G , $N_{A/D}$, and m_r . If UBM is verified for variable temperature or applied bias, than that functionality can also be added to the tool.

(2) A matching tool for directly comparing an input J-V characteristic (Ex. Experimental measurement) to the Kane mode. KMP can be programmed to automatically match the biasing conditions of the input data, and compute an r-square fit with the Kane model. Additionally, an empirical fit to the J_{Excess} and user defined R_{Series} may be added for enhanced matching capabilities. A 3rd generation evolution may include some automated fitting procedures.

(3) Another tool would combine the J-V plotting feature with (i) band diagram, (ii) carrier distribution, and (iii) overlap integral structure ($D'(E)$ from Section 3.2.3). Each plot of the additional plots could be turned on or off as desired by the user. The carrier distribution plots would be drawn directly on the band diagram for greater impact and easier analysis. Ideally, the user would adjust a slider bar on the J-V plot in order to designate V_A for the other plots, which will be updated automatically. If the refresh/calculation rate is fast enough, the updates can be live, allowing the user to see the changes occurring in a smooth “movie-like” fashion.

(4) There are a couple adaptations to the Kane model that would potential provide added accuracy or functionality. First, (i) a user designated i -layer can be added to the model parameters (w_d and ξ), more closely mimicking the ETD designs. Second, (ii) graded doping profiles. First iteration would most likely assume exponential decay. Additional functions, or even generic user profiles may be implemented afterwards. The third addition would be (iii) enabling BNG and multi-band E_F functional to any material system. Finally, (iv) the greatest challenge would be expanding the model to work with heterojunctions. It is not known if this can be done without making unreasonable assumptions and approximations, or restrictions on appropriate heterojunctions. However, from this work it is evident that hetrojunction ETDs are

Table 8.1: Breakdown of the different ETD structures fabricated and characterized for this work.

Ge On ART	GaAs/InGaAs				Homojunctions			
	On ART	On GaAs	On Si	Total	GaAs	InGaAs	InAs	Total
1	5	2	2	9	3	6	3	12
Total Device Count = 22								

needed to make large enhancements to BTBT current densities. Therefore, adopting the model to heterojunctions would enable to continued usefulness of the Kane model, and KMP, into the next generation of ETD structures.

As indicated, some of the suggested modification would not require much effort (#1, parts of #2, #4-i & iii). Some of the additions may not be easy to implement, but there is a clear path to do so (#2, remainder of #3, and #4-ii). However, it is not clear the path to modifying the Kane mode for heterojunction ETD structures. It may be no more difficult than using material parameters “a” and “b” on the p- and n- side of the junction, respectively. But modify the bandgap to the ΔE band alignment at the hetero-interface. The calculation may need to be piecewise depending on doping concentrations, V_A , and tunneling energy. It is likely that a much more sophisticated adaptation may be needed, beyond the scope of KMP. In which case it may be best to move onto a TCAP platform. Regardless, KMP is a great tool for modeling, predicting, and understanding the operation of homojunction ETDs. This is the first step to engineering heterojunctions with enhanced characteristics.

8.3. Summation of Work Completed

Many tools and procedures were developed in order to complete this work. Some of the tools and procedures were novel for the location the work was completed. Others are novel to the field and provide a great advancement for the BTBT community. In either case, these tools and procedures are, and will be, the foundation for continued BTBT development. Similarly, the results of the work completed add a great deal to the knowledge base of the community. The developed theoretical knowledge will shape the design and understanding of future experiments.

On the other hand, the experimental results will be used for model calibration, device design and optimization, and determination of material limitations

8.3.1. Developed Tools and Procedures

The Ge-Al alloy process for Ge ETDs was a new process. In particular, the use of spin-on-glass for introducing n-type dopants in to the Ge, and the thermal process for forming the p-type Al-Ge alloy junction. Junction alloying was the original and primary method of ETD fabrication [9-11]. However, after the development of epitaxial growth methods, it fell out of favor and became a lost art. This method should continually be looked into as a replacement to standard forms of doping. It is known that alloy junction can form high quality and sharp doping profiles for high quality ETD characteristics. Additionally, it is conceivable that this method can be used to provide horizontally tunnel junctions, instead of purely vertical structure which epitaxial methods are generally limited too. Furthermore, the alloyed junction is fundamentally a heterojunction with unique material qualities.

For the homojunction ETD structures, a novel deep sub-micron fabrication process was developed off of a baseline, self-aligned procedure. (1) Within the sub-micron process, E-Beam lithography was developed. This included the (i) operation of the SEM system and the NPGS software, (ii) chemicals involved with the process, (iii) layout design and implementation, and (iv) determination of optimal E-beam conditions. (2) The ILD planarization and etch back step utilizing BCB required the development of appropriate coating, etching, and metrology procedures. (3) Finally, the key to accurately scaling and current density analysis was the development of appropriate area characterization. The development of the deep submicron fabrication process enables the measurement of ultra-high current density ETDs (i) by reducing the effects of R_{Series} , (ii) minimizing uncertainty in junction areas, and (iii) negating the need for pulsed measurements to reduce the effects of localized heating. Additionally, this enables the study of scaling junction areas from very large areas down to deep sub-micron dimensions. Such

analysis is useful for determining changes in (i) BTBT current density, (ii) surface leakage effects, (iii) and electrically active defects. Future developments may be able to scale devices down to dimensions where the DOS start to follow 2D and 1D confinement, which may provide significantly different BTBT characteristics. Ultimately, TFETs will operate with 2D and 1D confinement. To date there is no experimental study that clearly identifies the effect of quantum confinement on BTBT.

Proper characterization and analysis procedures were developed. The material characterization procedures in this work were primarily limited to SIMS analysis to verify layer thicknesses, and quantify doping profiles. Future work should expand upon materials analysis techniques to include, but not limited by, EDX, XRD, and AFM. This will become extremely important for heterojunction systems. Other methods to determine active or present doping profiles may also become necessary. This work developed the techniques for characterizing the DC electrical characteristics of ETDs. These methods enable parameters such as J_p and PVCR to be reported with high confidence. It also enables the use of junction characteristics and scaling properties for materials analysis. The BTBT mapping techniques presented here is a powerful method of efficiently and consistently assessing the capabilities of a given material system, as well as benchmarking with other materials. Additionally, the mapped trendlines can be used by device and circuit designers for predicting or determining optimal device characteristics and limit the number of development runs needed.

There were no modifications made to the original Kane model [13]. However, a VB.net program was developed to automate the (i) material parameter retrieval, (ii) E_F calculations, (iii) Kane model calculation, (iv) band diagram calculations, and (v) overlap integral analysis. In general, KMP is a powerful tool for understanding the operation of and project the behavior of homojunction ETDs. This can be done on a qualitative and quantitative level, including the production of material BTBT maps. The development of UBM is a novel model, which provides a simple equation for “back-of-the-envelope” type calculations as well as a more direct method of

benchmarking and comparing various ETD structures and materials systems with each other. Further developments of the model may provide physical meaning the fitted parameters and enable full I-V characteristics. It is likely that the model will follow a form similar to some of the empirical models reported in literature [14].

8.3.2. Experimental Results

For this work, 22 unique ETD structure were designed, fabricated, and electrically tested. 10 of the devices were a part of the virtual substrate integration on Si. These ETDs were used to verify the electrical quality of the ART integrated virtual substrates. The remaining 12 ETDs were used to mapping and characterizing the BTBT behavior of the $\text{In}_{1-x}\text{Ga}_x\text{As}$ ternary system. Finally, The Kane [13] and UBM models were compared and calibrated to the experimental results.

The first diode, an Al-Ge alloy junction had comparable PVCR to similar device fabricated on Ge substrates. The difficulty of the alloy process, and availability of epitaxial growths shifted the efforts towards GaAs/InGaAs ETDs. Five structures were grown on ART virtual substrates, with two companion pieces grown on GaAs, two grown on Si. The PVCR of the on ART ETDs (up to 56 for TD-3) were greater than their on Si and GaAs companions. Additionally, the PVCR of TD1-2,3, and 4 surpasses the previous GaAs record of 24. Furthermore, a 1.8 meV activation energy was extracted from the low-to-high temperature measurements. This all indicates that the ART virtual substrates are of a high quality, with few electrically active defects present. The deep submicron scaling experiment showed that ETD device characteristics do not necessarily degrade with as the sidewall surface area to junction cross-sectional area increases. In fact, the device characteristics improved.

Mapping of the $\text{In}_{1-x}\text{Ga}_x\text{As}$ ternary system, which utilized 12 ETD structures, began with the fabrication of two ultra-high current density $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETDs. These two structures directly indicate the maximum J_p ($\sim 1 \text{ MA/cm}^2$) achievable. Furthermore, the deep submicron

scaling conclusively show that the BTBT characteristics do not degrade down to dimensions of at least 50 nm radii. However, there is currently not conclusive experiment indicating the effects of scaling down to 2D and 1D quantum confinement. InGaAs-3 ($J_p = 14 \text{ A/cm}^2$) showed that the Kane model and characteristic trendlines can be used to accurately predict doping concentrations after J_p is measured and before SIMS analysis. The final InGaAs ETDs filled in the middle of the characteristic trendline, showing that it is a consistent exponential line.

The three GaAs ETDs were enough to fill its characteristic trendline. The GaAs characteristic trendline is less than $\text{In}_{1-x}\text{Ga}_x\text{As}$, which was expected due to their respective bandgaps (1.42 eV and 0.74 eV). GaAs-1 provided the smallest J_p ($11 \mu\text{A/cm}^2$), with the system covering the largest range of values (9.5 orders of magnitude). The GaAs trendline indicates that GaAs ETDs are limited to J_p less than 100 kA/cm^2 , well below what is needed for TFETs.

Only two of the three InAs ETDs could be used to provide data points for a trendline. The InAs characteristic trendline is greater than the previous two. However, because of its small bandgap (0.35 eV), J_{Excess} limited observable J_p to $\sim 40 \text{ kA/cm}^2$, which is well below the maximum $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ETD value. An unexpected result with InAs was the observation of NDR due to the metal- p^+ InAs junction. This is the first room temperature report of this phenomenon, and is theorized to be due Fermi level pinning at the InAs surface, forming a thin n^+ surface channel.

Finally, the Kane model and UBM were matched to the experimental results. Both models accurately predict J_p for the $\text{In}_{1-x}\text{Ga}_x\text{As}$ ternary system, can be used to interpolate between the experimental results. Additionally, the Kane model accurately predicts full BTBT J-V characteristics, which can be used to device and circuit designers.

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APPENDIX A

Kane Model Program

The screenshot displays the Kane Model Program interface. At the top, there are control buttons: Run, Ef Only, N* Sweep, and EF2 BNG. The material is set to In(0.53)Ga(0.47)As. The Temperature (K) is 300, and X Composition is 0. The Start voltage is -0.5 V and dV is 0.001 V.

Variable	Number	Units
Material	In(0.53)Ga(0.47)As	
Temperature	300	K
Eg(300 K)	0.736472545757...	eV
er	13.9	
m*/m0 (tunneling)	0.039157392611...	
Vp	0.143	V
jp	1.21295e5	A/cm ²

Variable	N-type	P-type	Units
m*/m0	0.04445	0.469502...	
Nc.v	2.352e17	8.073e18	cm ⁻³
n,p(target)	5e19	5e19	cm ⁻³
n,p(calculated)			cm ⁻³
Efn,p-Ev	1.8494	-0.0996	eV

IV Sweep	N* Sweep (jp)	N* Sweep (Vapp)	BandDiagram	D'(E)
G _{an}	V _a	J _d (A/cm ²)	"D"	V _a = 0 V
	-0.5	-1.9469e6	-4.77162e-1	V _a = V _p
	-0.499	-1.94146e6	-4.76171e-1	V _b -V _a (V)
	-0.498	-1.93603e6	-4.75181e-1	1.94897e0
	-0.497	-1.93061e6	-4.7419e-1	W _d (nm)
	-0.496	-1.92519e6	-4.732e-1	1.09439e1
	-0.495	-1.91977e6	-4.72209e-1	W _n (nm)
	-0.494	-1.91436e6	-4.71219e-1	5.2674e0

Appendix A.1: Main window for PIVET.

The following is the main body code for the Kane model program (KMP), 0. The program is written with VB.net, using the Microsoft Visual Studio development environment. Description of the programs operation and function can be found in

Section 3.5.

```
Imports System.Math
Public Class Form1
    Dim xApp As New
        Microsoft.Office.Interop.Excel.Application
        Dim xBook As
            Microsoft.Office.Interop.Excel.Workbook =
                xApp.Workbooks.Open(System.IO.Directory.GetCurrentDirectory() &
                    "\ETD_Calculations.xlsx")
        Private Sub Form1_Load(ByVal sender As
            System.Object, ByVal e As System.EventArgs)
            Handles MyBase.Load
                Dim path(1) As String
                Dim xsheet As
                    Microsoft.Office.Interop.Excel.Worksheet
```

```

Integer Dim SheetCount, Mat_Count, i As Integer
Dim SheetExists(1) As Boolean
path(0) = System.IO.Directory.GetCurrentDirectory() & "\FTD_Calculations.xlsx"
If System.IO.File.Exists(path(0)) = True Then
Else
xBook = xApp.Workbooks.Add
xBook.SaveAs(path(0))
End If
SheetCount = xBook.Worksheets.Count
If SheetCount > 0 Then
For i = 1 To SheetCount Step 1
If xBook.Worksheets(i).name = "Fermi_Integral" Then
SheetExists(0) = True
End If
Else
SheetExists(0) = False
End If
If xBook.Worksheets(i).name = "Mat_Systems" Then
SheetExists(1) = True
End If
Else
SheetExists(0) = False
End If
Me.Visible = True
If SheetExists(0) = False Then
Me.Refresh()
xBook.Worksheets.Add.name = "Fermi_Integral"
xBook.Worksheets("Fermi_Integral").cells(1, 1).value = "Y"
xBook.Worksheets("Fermi_Integral").cells(1, 2).value = "Y"
xBook.Worksheets("Fermi_Integral").cells(1, 2).value = "Fermi_Integral"
Calculate_Integral(xBook.Worksheets("Fermi_Integral"), 6, -8.13)
End If
If SheetExists(0) = True Then
xsheet = xBook.Worksheets("Mat_Systems")
Mat_Count = xsheet.Application.WorksheetFunction.CountA(xsheet.Range("A:A"))
For i = 1 To Mat_Count Step 1
Mat_Sys.Items.Add(xsheet.Cells(i, 1).text)
Next
Else
Mat_Sys.SelectedText = "Si"
End If
xBook.Save()
For i = 1 To 6 Step 1
DGrid1.Rows.Add()
Next
For i = 1 To 4 Step 1
DGrid2.Rows.Add()
Next
xBook.Worksheets("Fermi_Integral").cells(1, 1).value = "Y"
xBook.Worksheets("Fermi_Integral").cells(1, 2).value = "Fermi_Integral"
Calculate_Integral(xBook.Worksheets("Fermi_Integral"), 6, -8.13)

```

```

DGrid1.Item(0, 2).Value = "Eg(300 K)"
DGrid1.Item(0, 3).Value = "er"
DGrid1.Item(0, 4).Value = "m*/m0 (tunneling)"
DGrid1.Item(0, 5).Value = "Vp"
DGrid1.Item(0, 6).Value = "Jp"
DGrid1.Item(1, 0).Value = "Si"
DGrid1.Item(1, 1).Value = "300"
DGrid1.Item(1, 2).Value = "1.12"
DGrid1.Item(1, 3).Value = "11.68"
DGrid1.Item(1, 4).Value = "0.16"
DGrid1.Item(2, 0).Value = ""
DGrid1.Item(2, 1).Value = "K"
DGrid1.Item(2, 2).Value = "ev"
DGrid1.Item(2, 5).Value = "v"
DGrid1.Item(2, 6).Value = "A/cm^2"
*****
*****
DGrid2.Item(0, 0).Value = "m*/m0"
DGrid2.Item(0, 1).Value = "NC,v"
DGrid2.Item(0, 2).Value = "n,p(target)"
DGrid2.Item(0, 3).Value = "n,p(calculated)"
DGrid2.Item(0, 4).Value = "Efn,p-Ev"
DGrid2.Item(1, 0).Value = "1.08"
DGrid2.Item(1, 1).Value = ""
DGrid2.Item(1, 2).Value = "5e19"
DGrid2.Item(1, 3).Value = ""
DGrid2.Item(1, 4).Value = ""
DGrid2.Item(2, 0).Value = "0.81"
DGrid2.Item(2, 1).Value = ""
DGrid2.Item(2, 2).Value = "5e19"
DGrid2.Item(2, 3).Value = ""
DGrid2.Item(2, 4).Value = ""
DGrid2.Item(3, 0).Value = ""
DGrid2.Item(3, 1).Value = "cm^-3"
DGrid2.Item(3, 2).Value = "cm^-3"
DGrid2.Item(3, 3).Value = "cm^-3"
DGrid2.Item(3, 4).Value = "ev"

```

```

*****
*****
DGrid1.Item(0, 0).Value = "Material"
DGrid1.Item(0, 1).Value = "Temperature"

```

```

For i = 0 To 154 Step 1
  DGrid3.Rows.Add()
  DGrid3.Item(0, i).Value = i /
  " "n"
  DataGridView1.Item(4, 6).Value =
  'eV*Sec
  h_bar = 0.0000000000000000658211899
  c = 299792000.0 'm/Sec
  e0 = 0.000000000000000008854188 'F/cm
  k = 0.00008617343 'eV/K
  T = DGrid1.Item(1, 1).Value 'K
  kT = k * T 'eV
  er = DGrid1.Item(1, 3).Value
  Eg = DGrid1.Item(1, 2).Value 'eV
  mr(0) = DGrid2.Item(1, 0).Value 'N-
  type
  mr(1) = DGrid2.Item(2, 0).Value 'P-
  type
  mr(2) = DGrid1.Item(1, 4).Value
  'Tunneling
  es = e0 * er 'F/cm
  m_eff(0) = mr(0) * m0 / c ^ 2 'eV
  (N-type)
  m_eff(1) = mr(1) * m0 / c ^ 2 'eV
  (P-type)
  m_eff(2) = mr(2) * m0 / (c ^ 2) 'eV
  (Tunneling)
  Nc(0) = 0.000001 * Sqrt(1 / 2) *
  (m_eff(0) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-
  3/eV
  Nc(1) = (kT ^ 1.5) * Nc(0) 'cm^-3
  Nv(0) = 0.000001 * Sqrt(1 / 2) *
  (m_eff(1) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-
  3/eV
  Nv(1) = (kT ^ 1.5) * Nv(0) 'cm^-3
  DGrid2.Item(1, 1).Value =
  Nc(1).ToString("0.###e0") 'N-type
  DGrid2.Item(2, 1).Value =
  Nv(1).ToString("0.###e0") 'P-type
  Nd = DGrid2.Item(1, 2).Value 'N-type
  Na = DGrid2.Item(2, 2).Value 'P-type
  Eg = BNG(Nd, Na, Eg)
  If CheckBox1.Checked = True Then
    Efn = Fermi_Levels2(xSheet, Nd,
  Nc(1)) 'Only accurate for InGaAs (53/47)
  Else
  Microsoft.Office.Interop.Excel.Worksheet
  Dim xSheet As
  Dim path As String
  Dim i, j, steps, rows As Integer
  Dim pi, q, m0, h_bar, c, e0, k, T,
  kT As Double
  Dim er, Eg, mr(2), m_eff(2), Nc(1),
  Nv(1), es As Double
  Dim Na, Nd, Efn, Efp, Vbi As Double
  Dim Va, X, E_bar, eV, Edel, Estep,
  D, tempD, terms(2), Vp, Jp As Double
  path =
  System.IO.Directory.GetCurrentDirectory() &
  "\ETD_Calculations.xlsx"
  xSheet =
  xBook.Worksheets("Fermi_Integral")
  pi = 3.1415926536
  q = 1.602176E-19 'C
  m0 = 510998.91 'eV
  DGrid3.Item(3, 0).Value = "Va = 0 V"
  DGrid3.Item(4, 0).Value = "Va = Vp"
  DGrid3.Item(3, 1).Value = "Vbi-Va"
  DGrid3.Item(3, 3).Value = "Wd (nm)"
  DGrid3.Item(3, 5).Value = "Wn (nm)"
  DGrid3.Item(3, 7).Value = "Wp (nm)"
  DGrid3.Item(3, 9).Value = "E-field"
  (V/cm) "
  DGrid3.Item(3, 11).Value = "Pre-
  factor (1/ohm-cm/eV)"
  DGrid3.Item(4, 11).Value = "Arg.
  (cm/V) "
  DGrid3.Item(3, 13).Value = "Efn
  (eV) "
  DGrid3.Item(4, 13).Value = "Efp
  (eV) "
  DGrid3.Item(3, 15).Value = "Nd (cm^-
  3) "
  DGrid3.Item(4, 15).Value = "Na (cm^-
  3) "
  DGrid3.Item(3, 17).Value = "Vp (V) "
  DGrid3.Item(4, 17).Value = "Jp
  (A/cm^2) "
  DGrid3.Item(3, 20).Value = "D (eV) "
  DataGridView1.Rows.Add(203)
  DataGridView1.Item(4, 0).Value = "i-
  layer (nm)"
  DataGridView1.Item(5, 0).Value = 0
  DataGridView1.Item(4, 1).Value = "Wd
  (nm) "
  DataGridView1.Item(4, 2).Value = "TB
  Width (nm)"
  DataGridView1.Item(4, 3).Value =
  "Ave. E-Field (V/cm)"
  DataGridView1.Item(4, 4).Value =
  "Efn-Ec (eV)"
  DataGridView1.Item(4, 5).Value =
  "Evp-Efp (eV)"

```

```

Efn = Firmi_Levels(xSheet, Nd,
Nc(1)) ', Nc(0))
End If

Efn = Eg - Efn * kT
DGrid2.Item(1, 4).Value =
Efn.ToString("0.#####")

'P-type region
Efp = Firmi_Levels(xSheet, Na,
Nv(1)) ', Nv(1))
Efp = Efp * kT
DGrid2.Item(2, 4).Value =
Efp.ToString("0.#####")

DGrid1.Refresh()
DGrid2.Refresh()
DGrid3.Refresh()

Vp = 0
Jp = 0
Vbi = Efn - Efp 'eV
Dim temp(1) As Double
Vapplied(Efn, Efp, Eg)
steps = DGrid3.RowCount - 2
For j = 0 To steps Step 1
Va = DGrid3.Item(0, j).Value
' (Efn + Efp - Eg) / 2 'eV
X = 100 * Sqrt(q * (Vbi - Va) *
Na * Nd / (2 * es * (Na + Nd))) 'V/m
E_bar = h_bar * X * Sqrt(2) /
(pi * Sqrt(m_eff(2) * Eg)) 'eV
Estep = (Vbi - Va - Eg) / 500
D = 0
For i = 0 To 500 Step 1
eV = Estep * i
If eV < Vbi - Eg - Va - eV
Then
Edel = eV
Else
Edel = Vbi - Eg - Va -
eV
End If
temp(0) = eV + Eg
temp(1) = -Vbi + Va + Eg +
eV

D = D + (Fcv(temp(0), Efn,
kT) - Fcv(temp(1), Efp, kT)) * (1 - Exp(-2 *
Edel / E_bar)) * Estep
Next
terms(0) = (q * X / (36 * pi *
h_bar ^ 2)) * Sqrt(2 * m_eff(2) / Eg) /
10000
terms(1) = Exp(-pi *
Sqrt(m_eff(2)) * (Eg ^ 1.5) / (2 * Sqrt(2) *
h_bar * X))

DGrid3.Item(1, j).Value > Jp
Then
Jp = DGrid3.Item(1, j).Value
Vp = DGrid3.Item(0, j).Value
tempD = D
End If
Next
rows = DGrid3.RowCount
If rows < 21 Then
For i = 1 To 21 - rows Step 1
DGrid3.Rows.Add()
Next
End If
DGrid3.Item(3, 0).Value = "Va = 0 V"
DGrid3.Item(4, 0).Value = "Va = Vp"
DGrid3.Item(3, 1).Value = "Vbi-Va
(V)"
DGrid3.Item(3, 3).Value = "Wd (nm)"
DGrid3.Item(3, 5).Value = "Wn (nm)"
DGrid3.Item(3, 7).Value = "Wp (nm)"
DGrid3.Item(3, 9).Value = "E-field
(V/cm)"
DGrid3.Item(3, 11).Value = "Pre-
factor (1/ohm-cm)"
DGrid3.Item(4, 11).Value = "Arg.
(cm/V)"
DGrid3.Item(3, 13).Value = "Efn
(eV)"
DGrid3.Item(4, 13).Value = "Efp
(eV)"

D = D + (Fcv(temp(0), Efn,
kT) - Fcv(temp(1), Efp, kT)) * (1 - Exp(-2 *
Edel / E_bar)) * Estep
Next
terms(0) = (q * X / (36 * pi *
h_bar ^ 2)) * Sqrt(2 * m_eff(2) / Eg) /
10000
terms(1) = Exp(-pi *
Sqrt(m_eff(2)) * (Eg ^ 1.5) / (2 * Sqrt(2) *
h_bar * X))

DGrid3.Item(1, j).Value = (D *
terms(1)).ToString("0.#####e0")
DGrid3.Item(2, j).Value =
D.ToString("0.#####e0")

If DGrid3.Item(1, j).Value > Jp
Then
Jp = DGrid3.Item(1, j).Value
Vp = DGrid3.Item(0, j).Value
tempD = D
End If
Next
rows = DGrid3.RowCount
If rows < 21 Then
For i = 1 To 21 - rows Step 1
DGrid3.Rows.Add()
Next
End If
DGrid3.Item(3, 0).Value = "Va = 0 V"
DGrid3.Item(4, 0).Value = "Va = Vp"
DGrid3.Item(3, 1).Value = "Vbi-Va
(V)"
DGrid3.Item(3, 3).Value = "Wd (nm)"
DGrid3.Item(3, 5).Value = "Wn (nm)"
DGrid3.Item(3, 7).Value = "Wp (nm)"
DGrid3.Item(3, 9).Value = "E-field
(V/cm)"
DGrid3.Item(3, 11).Value = "Pre-
factor (1/ohm-cm)"
DGrid3.Item(4, 11).Value = "Arg.
(cm/V)"
DGrid3.Item(3, 13).Value = "Efn
(eV)"
DGrid3.Item(4, 13).Value = "Efp
(eV)"

DGrid3.Item(3, 15).Value = "Nd (cm^-
3)"
DGrid3.Item(4, 15).Value = "Na (cm^-
3)"
DGrid3.Item(3, 17).Value = "Vp (V)"
DGrid3.Item(4, 17).Value = "Jp
(A/cm^2)"
DGrid3.Item(3, 20).Value = "D (eV)"

X = 1000000 * Sqrt(2 * es * (Nd +
Na) * (Efn - Efp) / (q * Nd * Na))
DGrid3.Item(3, 2).Value = (Efn -
Efp).ToString("0.#####e0")
DGrid3.Item(3, 4).Value =
X.ToString("0.#####e0") 'Wd (nm)"
DGrid3.Item(3, 6).Value = (X * Na /
(Na + Nd)).ToString("0.#####e0") 'Wn (nm)"
DGrid3.Item(3, 8).Value = (X * Nd /
(Na + Nd)).ToString("0.#####e0") 'Wp (nm)"
DGrid3.Item(3, 10).Value = (Sqrt(q *
(Efn - Efp) * Na * Nd / (2 * es * (Na +
Nd)))) * Sqrt(2 * es * (Na +
Nd)) * Sqrt(2 * es * (Nd +
Na) * (Efn - Efp - Vp) / (q * Nd * Na))
DGrid3.Item(4, 2).Value = ((Efn -
Efp) - Vp).ToString("0.#####e0") 'Vbi-Vp
(V)"
DGrid3.Item(4, 4).Value =
X.ToString("0.#####e0") 'Wd (nm)"
DGrid3.Item(4, 6).Value = (X * Na /
(Na + Nd)).ToString("0.#####e0") 'Wn (nm)"
DGrid3.Item(4, 8).Value = (X * Nd /
(Na + Nd)).ToString("0.#####e0") 'Wp (nm)"
DGrid3.Item(4, 10).Value = (Sqrt(q *
(Efn - Efp - Vp) * Na * Nd / (2 * es * (Na +
Nd)))) * Sqrt(2 * es * (Na +
Nd)) * Sqrt(2 * es * (Nd +
Na) * (Efn - Efp - Vp) / (q * Nd * Na))
DGrid3.Item(4, 2).Value = ((Efn -
Efp) - Vp).ToString("0.#####e0") 'Vbi-Vp
(V)"
DGrid3.Item(4, 4).Value =
X.ToString("0.#####e0") 'Wd (nm)"
DGrid3.Item(4, 6).Value = (X * Na /
(Na + Nd)).ToString("0.#####e0") 'Wn (nm)"
DGrid3.Item(4, 8).Value = (X * Nd /
(Na + Nd)).ToString("0.#####e0") 'Wp (nm)"
DGrid3.Item(4, 10).Value = (Sqrt(q *
(Efn - Efp - Vp) * Na * Nd / (2 * es * (Na +
Nd)))) * Sqrt(2 * es * (Na +
Nd)) * Sqrt(2 * es * (Nd +
Na) * (Efn - Efp - Vp) / (q * Nd * Na))
DGrid3.Item(4, 12).Value = (-pi *
Sqrt(2 * m_eff(2) / Eg) / (100 * 36 * pi *
h_bar ^ 2)).ToString("0.#####e0") 'Pre-
factor (1/ohm-cm/eV)"
DGrid3.Item(4, 12).Value = (-pi *
Sqrt(m_eff(2)) * (Eg ^ 1.5) / (100 * 2 *

```



```

Sqrt(2) * h_bar)) .ToString("0.#####e0")
  "Arg. (cm/V) "
  DGrid3.Item(3, 14).Value =
  Efn.ToToString("0.#####") "Efn (eV) "
  DGrid3.Item(4, 14).Value =
  Efp.ToToString("0.#####") "Efp (eV) "
  DGrid3.Item(3, 16).Value = Nd "Nd
(cm^-3) "
  DGrid3.Item(4, 16).Value = Na "Na
(cm^-3) "
  DGrid3.Item(3, 18).Value = Vp "Vp
(V) "
  DGrid3.Item(4, 18).Value =
  Jp.ToToString("0.#####e0") "Jp (A/cm^2) "
  DGrid3.Item(4, 20).Value =
  tempD.ToToString("0.#####e0") "D (eV) "

  If DGrid3.Item(0, steps).Value <>
  Efn - Efp - Eg Then
  DGrid3.Item(0, steps + 1).Value
  = Efn - Efp - Eg
  Va = DGrid3.Item(0, steps +
  1).Value * (Efn + Efp - Eg) / 2 'eV
  X = 100 * Sqrt(q * (Vbi - Va) *
  Na * Nd / (2 * es * (Na + Nd))) 'V/m
  Sqrt(2) / (pi * Sqrt(m_eff(2) * Eg / (c ^
  2))) 'eV
  Estep = (Vbi - Va - Eg) / 10
  D = 0
  For i = 0 To 10 Step 1
  eV = Estep * i
  If eV < Vbi - Eg - Va - eV
  Then
  Edel = eV
  Else
  Edel = Vbi - Eg - Va -
  eV
  End If
  D = D + (Fcv(eV + Eg, Efn,
  kT) - Fcv(-eV, Efp, kT)) * (1 - Exp(-2 *
  Edel / E_bar)) * Estep
  Next
  rows = Int((Vvend - Vstart) / dV)
  For i = 0 To rows Step 1
  DGrid3.Rows.Add()
  DGrid3.Item(0, i).Value = Vstart
  Next
  End Sub
  Public Function Firmi_levels(ByVal
  xSheet As
  Microsoft.Office.Interop.Excel.Worksheet,
  ByVal n_target As Double, ByVal Ncv As
  Double) ' , ByVal Ncv0 As Double)
  'This provides something
  Dim Y, Fintegral, temp(), Alpha As
  Double
  Fintegral = n_target * Sqrt(Pi) / (4
  * Ncv)
  Y = -Log(n_target / Ncv)
  'If the doping is small enough, the
  sample is not degenerate
  'Therefore, the standard equation is
  good
  If y >= 6 Then
  GoTo TheEnd
  End If
  Dim i, row(2), RowCount, steps As
  Integer
  Dim Table(,) As Object
  Dim starty As Double
  RowCount =
  xSheet.Application.WorksheetFunction.Count(x
  Sheet.Range("A:A")) + 1
  'Initial guess using modified Eq 26a
  (pp. 19 in Size 3rd edition)
  'Initial guess using degenerate Ef
  statistics.

```

```

Alpha = (3 * Sqrt(PI) / (4 * Ncv)) ^
(2 / 3)
Y = -Alpha * n_target ^ (2 / 3)
row(1) = Int((6 - y) * 100) + 3 'row
closest to this result

If Fintegral >
xSheet.Cells(RowCount, 2).value Then
Do While Fintegral >
xSheet.Cells(RowCount, 2).value
starty =
Calculate_Integral(xSheet,
starty - 0.01, starty - 1)
RowCount =
xSheet.Application.WorksheetFunction.Count(x
Sheet.Range("A:A")) + 1
Loop
row(2) = RowCount
row(0) = RowCount - 100
GoTo SearchPoint
End If

If row(1) > RowCount Then
row(1) = RowCount
End If

'y(0) to low; y(1) current; y(2) to
high
If xSheet.Cells(row(1), 2).value >
Fintegral Then
'-----
row(2) = row(1)
steps = Int((row(1) - 2) / 100)
For i = 1 To steps Step 1
'Make sure the row to check
is not below the minimum of "2"
If row(1) - 100 > 1 Then
row(1) = row(1) - 100
Else
row(1) = 2
End If
End If

+ 1
row(2) = row(1)
steps = Int((row(1) - 2) / 100)
For i = 1 To steps Step 1
'Make sure the row to check
is not above RowCount
If row(1) + 100 < RowCount
Then
row(1) = row(1) + 100
Else
row(1) = RowCount
End If
End If

'Check if Fint(check) - Fint
at row(1) - is less than target Fint
If xSheet.Cells(row(1),
2).value < Fintegral Then
'Update lower bound
row(0) = row(1)
Else
'Upper bound for
Fint(check) found. Update row and exit for
Loop
row(2) = row(1)
End If

'Check if Fint(check) - Fint
at row(1) - is greater than target Fint
If xSheet.Cells(row(1),
2).value > Fintegral Then
'Update upper bound
row(2) = row(1)
Else
'Lower bound for
Fint(check) found. Update row and exit for
Loop
row(0) = row(1)
i = 10000000.0
End If
End If

SearchPoint:
ReDim Table(row(2) - row(0) + 1, 2)
Table = xSheet.Cells(row(0),
1).Resize(row(2) - row(0) + 1, 2).Value
For i = 1 To row(2) - row(0) + 1
Step 1
If Table(i, 2) < Fintegral Then
row(0) = i
ElseIf Table(i, 2) > Fintegral
Then
row(2) = i
i = 200
Else
row(0) = i
row(2) = i
End If
Next
'Interpolate to find "y_target"
y = Table(row(0), 1) + (Fintegral -
Table(row(0), 2)) * (Table(row(2), 1) -
Table(row(0), 1)) / (Table(row(2), 2) -
Table(row(0), 2)))
TheEnd:
'***Note: Ef = Eg - y * kT
Firmi_Levels = y
End Function
Public Function Firmi_Levels2(ByVal
xSheet As
Microsoft.Office.Interop.Excel.Worksheet,
ByVal N As Double, ByVal Nc As Double)

```



```

If Y(3) < 6 Then
    F(3) = xSheet.Cells(row(3),
2) .value
Else
    F(3) = (Sqrt(PI) / 4) * Exp(-
Y(3))
End If
If Y(1) < 6 Then
    F(4) = F(1) + m(2) * F(2) + m(3) *
row(1) = row(1) + 1
row(2) = row(2) + 1
row(3) = row(3) + 1
If Y(1) < 6 Then
    F(1) = xSheet.Cells(row(1),
2) .value
Else
    F(1) = (Sqrt(PI) / 4) * Exp(-
Y(1))
End If
If Y(2) < 6 Then
    F(2) = xSheet.Cells(row(2),
2) .value
Else
    F(2) = (Sqrt(PI) / 4) * Exp(-
Y(2))
End If
If Y(3) < 6 Then
    F(3) = xSheet.Cells(row(3),
2) .value
Else
    F(3) = (Sqrt(PI) / 4) * Exp(-
Y(3))
End If
F(5) = F(1) + m(2) * F(2) + m(3) *
Y(0) = Y(1) - 0.01 * (F(0) - F(4)) /
(F(5) - F(4))
Y(1) = Y(0)
Y(2) = Y(1) + dy(2)
Y(3) = Y(1) + dy(3)
Return Y(0)
End Function
Public Function BNG(ByVal Nd As Double,
ByVal Na As Double, ByVal Eg As Double)
Dim ABCD(1, 3), dEmaj(1), dEmin(1),
dEg(1) As Double
'Constants for Na
ABCD(1, 0) = 0.0092
ABCD(1, 1) = 0.0034
ABCD(1, 2) = 0.0113
ABCD(1, 3) = 0.00023
'Constants for Nd
ABCD(0, 0) = 0.0476
ABCD(0, 1) = 0
ABCD(0, 2) = 0.0032
ABCD(0, 3) = 0
dEmaj(0) = ABCD(0, 0) * (Nd /
1.0E+19) ^ (1 / 3) + ABCD(0, 1) * (Nd /
1.0E+19) ^ 0.5
dEmin(0) = ABCD(0, 2) * (Nd /
1.0E+19) ^ 0.25 + ABCD(0, 3) * (Nd /
1.0E+19) ^ 0.5
dEmaj(1) = ABCD(1, 0) * (Na /
1.0E+19) ^ (1 / 3) + ABCD(1, 1) * (Na /
1.0E+19) ^ 0.5
dEmin(1) = ABCD(1, 2) * (Na /
1.0E+19) ^ 0.25 + ABCD(1, 3) * (Na /
1.0E+19) ^ 0.5
dEg(0) = dEmaj(0) + dEmin(0)
dEg(1) = dEmaj(1) + dEmin(1)
If CheckBox2.Checked = True Then
Return (Eg - (dEg(0) + dEg(1)) /
2)
Else
Return Eg
End If
End Function
Public Sub Calculate_Integral(ByVal
xSheet As
Microsoft.Office.Interop.Excel.Worksheet,
ByVal StartY As Double, ByVal EndY As
Double)
Dim i, j, StartRow, row As Integer
Dim sum, Y, Dx3 As Double
sum = xSheet.Cells(2, 1).value
StartRow =
xSheet.Application.WorksheetFunction.Count(x
Sheet.Range("A:A")) + 2
Dx3 = 0.001 / 3
For i = 0 To ((StartY - EndY) * 100)
Step 1
    row = StartRow + i
    Y = StartY - i / 100
    xSheet.Cells(row, 1).value = Y
    sum = 0
    For j = 1 To 10000 Step 2
        sum = sum + Dx3 *
(Integrand(Y, 0.001 * (j - 1)) + 4 *
Integrand(Y, 0.001 * j) + Integrand(Y, 0.001
* (j + 1)))
    Next
    If Y < -90 Then
        For j = 10001 To 20000 Step
2
            sum = sum + Dx3 *
(Integrand(Y, 0.001 * (j - 1)) + 4 *
Integrand(Y, 0.001 * j) + Integrand(Y, 0.001
* (j + 1)))
        Next
    End If
    TextBox3.Text = "Populating
Fermi-integral Table (" & Y & "/" & EndY &
")"
    TextBox3.Refresh()
    xSheet.Cells(row, 2).value = sum
Next
End Sub
Public Function Integrand(ByVal Y As
Double, ByVal x As Double) As Double

```

```

^ 2)
Integrand = (x ^ 2) / (1 + Exp(y + x
^ 2))
End Function
Private Sub Button2_Click(ByVal sender
As System.Object, ByVal e As
System.EventArgs) Handles Button2.Click
Dim xSheet As
Microsoft.Office.Interop.Excel.Worksheet
Dim path As String
Dim k, T, h_bar, pi, m0, c As Double
Dim mr(1), m_eff(1), Eg, Ef(2), kT
As Double
Dim n_target, p_target, Nc, Nv As
Double
path =
System.IO.Directory.GetCurrentDirectory() &
"\FTD_Calculations.xlsx"
xSheet =
xBook.Worksheets("Fermi_Integral")
pi = 3.1415926536
m0 = 510998.91 'eV
h_bar = 0.00000000000000000658211899
'ev*Sec
c = 299792000.0 'm/Sec
Eg = DGrid1.Item(1, 2).Value 'eV
T = DGrid1.Item(1, 1).Value 'K
kT = k * T 'eV
mr(0) = DGrid2.Item(1, 0).Value 'N-
type
mr(1) = DGrid2.Item(2, 0).Value 'P-
type
m_eff(0) = mr(0) * m0 / c ^ 2 'eV
m_eff(1) = mr(1) * m0 / c ^ 2 'eV
Nc = 0.000001 * Sqrt(1 / 2) *
(m_eff(0) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-3
Nv = 0.000001 * Sqrt(1 / 2) *
(m_eff(1) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-3
n_target = DGrid2.Item(1, 2).Value
'N-type
System.IO.Directory.GetCurrentDirectory() &
"\FTD_Calculations.xlsx"
xSheet =
xBook.Worksheets("Fermi_Integral")

```

```

Eg = BNG(Nd, Na, Eg)
'Firmi_Levels1()
'N-type region
If CheckBox1.Checked = True Then
    Efn = Firmi_Levels2(xSheet, Nd,
'Only accurate for InGaAs (53/47)
Else
    Efn = Firmi_Levels(xSheet, Nd,
Nc(1) ', Nc(0))
End If
Efn = Eg - Efn * kT
DGrid2.Item(1, 4).Value =
Efn.ToString("0.####")
'P-type region
Efp = Firmi_Levels(xSheet, Na,
Nv(1) ', Nv(1))
Efp = Efp * kT
DGrid2.Item(2, 4).Value =
Efp.ToString("0.####")
Vbi = Efn - Efp
X = Sqrt(i_layer ^ 2 + 2 * es * (Vbi - Va) * (Na * Nd)) -
i_layer 'cm
Xn = X * (Na / (Na + Nd))
Xp = X * (Nd / (Nd + Na))
DataGridView1.Item(5, 1).Value = (X
+ i_layer) * 1000000.0
DataGridView1.Item(5, 2).Value = Eg
* 1000000.0 / ((Vbi - Va) / (X + i_layer))
'RGB Width (nm)
DataGridView1.Item(5, 3).Value =
(Vbi - Va) / (X + i_layer)
DataGridView1.Item(5, 4).Value = Efn
- Eg
DataGridView1.Item(5, 5).Value = Efp
If Efn - Eg < -Efp Then
    DataGridView1.Item(5, 6).Value =
(Efn - Eg) / 0.0259
Else
    DataGridView1.Item(5, 6).Value =
Efp / 0.0259
End If
DataGridView1.Item(3, 103 +
i).Value = -Va
Next
End Sub
Private Sub Calc_DofE()
Dim xSheet As
Microsoft.Office.Interop.Excel.Worksheet
Dim path As String
Dim i, j, steps, rows As Integer
Dim pi, q, m0, h_bar, c, e0, k, T,
kT As Double
Dim er, Eg, mr(2), m_eff(2), Nc(1),
Nv(1), es As Double
Dim Na, Nd, Efn, Efp, Fnp(2), Vbi As
Double
Dim Va, X, E_bar, eV, Edel, Estep,
D, tempD, terms(2), Vp, Jp As Double
path =
System.IO.Directory.GetCurrentDirectory() &
"\ETD_Calculations.xlsx"
xSheet =
xBook.Worksheets("Fermi_Integral")
pi = 3.1415926536
q = 1.602176E-19 'C
m0 = 510998.91 'eV
h_bar = 0.0000000000000000658211899
'ev*Sec
c = 299792000.0 'm/Sec
e0 = 0.00000000000000008854188 'F/cm
k = 0.00008617343 'eV/K
T = DGrid1.Item(1, 1).Value 'K
kT = k * T 'eV
er = DGrid1.Item(1, 3).Value
Eg = DGrid1.Item(1, 2).Value 'eV
mr(0) = DGrid2.Item(1, 0).Value 'N-
type
mr(1) = DGrid2.Item(2, 0).Value 'P-
type
mr(2) = DGrid1.Item(1, 4).Value
'Tunneling
End If
Cp = q * Na / (2 * es)
Cn = q * Nd / (2 * es)
dx = Xn / 100
For i = 0 To 100 Step 1
    Xstep = dx * i - Xn - i_layer /
2
    V(0) = Cn * (Xn + Xstep +
i_layer / 2) ^ 2 - Efn + Eg
DataGridView1.Item(0, i).Value =
(Xstep) * 1000000
DataGridView1.Item(1, i).Value =
V(0) - Eg
DataGridView1.Item(2, i).Value =
V(0)
DataGridView1.Item(3, i).Value =
0
Next
For i = 0 To 1 Step 1
    Xstep = (i * i_layer) - i_layer
/ 2
    V(0) = Cn * Xn * (2 * Xstep + Xn
+ i_layer) - Efn + Eg
DataGridView1.Item(0, 101 +
i).Value = (Xstep) * 1000000
DataGridView1.Item(1, 101 +
i).Value = V(0) - Eg
DataGridView1.Item(2, 101 +
i).Value = V(0)
DataGridView1.Item(3, 101 +
i).Value = 0
Next
dx = Xp / 100
For i = 0 To 100 Step 1
    Xstep = dx * i + i_layer / 2
    V(0) = (Vbi - Va) - Cp * (Xstep
- Xp - i_layer / 2) ^ 2 - Efn + Eg
DataGridView1.Item(0, 103 +
i).Value = (Xstep) * 1000000.0
DataGridView1.Item(1, 103 +
i).Value = V(0) - Eg
DataGridView1.Item(2, 103 +
i).Value = V(0)

```

```

es = e0 * er 'F/cm
m_eff(0) = mr(0) * m0 / c ^ 2 'eV
(N-type)
m_eff(1) = mr(1) * m0 / c ^ 2 'eV
(P-type)
m_eff(2) = mr(2) * m0 / (c ^ 2) 'eV
(Tunneling)
Nc(0) = 0.00001 * Sqrt(1 / 2) *
(m_eff(0) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-
3/eV
Nc(1) = (kT ^ 1.5) * Nc(0) 'cm^-3
Nv(0) = 0.00001 * Sqrt(1 / 2) *
(m_eff(1) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-
3/eV
Nv(1) = (kT ^ 1.5) * Nv(0) 'cm^-3
DGrid2.Item(1, 1).Value =
Nc(1).ToString("0.###e0") 'N-type
DGrid2.Item(2, 1).Value =
Nv(1).ToString("0.###e0") 'P-type

Nd = DGrid2.Item(1, 2).Value 'N-type
Na = DGrid2.Item(2, 2).Value 'P-type

Eg = BNG(Nd, Na, Eg)

'Firmi_Levels1()
'N-type region
If CheckBox1.Checked = True Then
Nc(1) 'Only accurate for InGaAs (53/47)
Else
Efn = Firmi_Levels(xSheet, Nd,
Nc(1) ', Nc(0))
End If

Efn = Eg - Efn * kT
DGrid2.Item(1, 4).Value =
Efn.ToString("0.####")

'P-type region
Efp = Firmi_Levels(xSheet, Na,
Nv(1) ', Nv(0))
Efp = Efp * kT
DGrid2.Item(2, 4).Value =
Efp.ToString("0.####")

DGrid1.Refresh()

DGrid2.Refresh()
DGrid3.Refresh()

Vp = 0
Jp = 0
Vbi = Efn - Efp 'eV
Dim temp(1) As Double
Va = TextBox1.Text
X = 100 * Sqrt(q * (Vbi - Va) * Na *
Nd / (2 * es * (Na + Nd))) 'V/m
E_bar = h_bar * X * Sqrt(2) / (pi *
Sqrt(m_eff(2) * Eg)) 'eV

Estep = (Vbi - Va - Eg) / 500
D = 0
For i = 0 To 500 Step 1
eV = Estep * i
If eV < Vbi - Eg - Va - eV Then
Edel = eV
Else
Edel = Vbi - Eg - Va - eV
End If
temp(0) = eV + Eg
temp(1) = -Vbi + Va + Eg + eV

Fnp(0) = Fcv(temp(0), Efn, kT)
Fnp(1) = Fcv(temp(1), Efp, kT)
Fnp(2) = (Fnp(0) - Fnp(1))
tempD = (1 - Exp(-2 * Edel /
D = Fnp(2) * tempD
DofE.Item(0, i).Value = eV
DofE.Item(1, i).Value = Fnp(0)
DofE.Item(2, i).Value = Fnp(1)
DofE.Item(3, i).Value = Fnp(2)
DofE.Item(4, i).Value = tempD
DofE.Item(5, i).Value = D

Next
End Sub

Private Sub
Mat_Sys_SelectedIndexChanged(ByVal sender As
System.Object, ByVal e As System.EventArgs)
Handles Mat_Sys.SelectedIndexChanged

```



```

xBook.Worksheets("DOS_mr_h").cells(Row,
3).value() = X
    DGrid1.Item(1, 0).Value =
xBook.Worksheets("Bandgap").cells(Row,
1).value
    DGrid1.Item(1, 1).Value =
Temperature
    DGrid1.Item(1, 2).Value =
xBook.Worksheets("Bandgap").cells(Row,
2).value
    DGrid1.Item(1, 3).Value =
xBook.Worksheets("Rel_Dielectric_Const").cel
1s(Row, 2).value
    DGrid1.Item(1, 4).Value =
xBook.Worksheets("Tunneling_mr").cells(Row,
2).value

    DGrid2.Item(1, 0).Value =
xBook.Worksheets("DOS_mr_e").cells(Row,
2).value
    DGrid2.Item(2, 0).Value =
xBook.Worksheets("DOS_mr_h").cells(Row,
2).value
    End Sub
    Private Sub DGrid4_KeyUp(ByVal sender As
Object, ByVal e As
System.Windows.Forms.KeyEventArgs) Handles
DGrid4.KeyUp
    If Control.ModifierKeys =
Keys.Control Then
        Select Case e.KeyCode
            Case Keys.V
                Paste(DGrid4)
        End Select
    End If
End Sub

    Private Sub DGrid5_KeyUp(ByVal sender As
Object, ByVal e As
System.Windows.Forms.KeyEventArgs) Handles
DGrid5.KeyUp
    If Control.ModifierKeys =
Keys.Control Then
        Select Case e.KeyCode
            Case Keys.V
                Paste(DGrid5)
        End Select
    End If
End Sub
    Private Sub Paste(ByVal dgrid As
DataGridView)
        Dim clipboard As String
        Dim temp1(), temp2() As String
        Dim size, i, j, RowCount, row, col
        As Integer
        col = dgrid.CurrentCell.ColumnIndex
        row = dgrid.CurrentCell.RowIndex
        RowCount = dgrid.RowCount
        'base-0
        'base-0
        clipboard =
System.Windows.Forms.Clipboard.GetText
        temp1 = clipboard.Split(vbNewLine)
        size = temp1.Length
        'base-1
        If RowCount < size + row Then
            dgrid.Rows.Add(size + row -
RowCount)
        End If
        For i = 0 To size - 1 Step 1
            temp2 = temp1(i).Split(vbTab)
            For j = 0 To temp2.Length - 1
                Step 1
                    dgrid.Item(col + j, row +
i).Value = temp2(j)
            Next
        Next
    End Sub
    Private Sub N_Sweep(ByVal dgrid As
DataGridView)
        Dim i As Integer
        For i = 1 To 6 Step 1
            dgrid.Rows.Add()
        Next
    End Sub
    Private Sub N_Sweep_Jp()
        Dim i, rows As Integer
        Dim Nad(,), Nstar As Double
        rows = DGrid4.RowCount - 1
        '0-base
        If IsNumeric(DGrid4.Item(0,
rows).Value) Then
            Else
                rows = rows - 1
            End If
            ReDim Nad(1, rows)
            For i = 0 To rows Step 1
                Nad(0, i) = DGrid4.Item(0,
i).Value
                'Nd
                Nad(1, i) = DGrid4.Item(1,
i).Value
                'Na
                Nstar = Nad(0, i) * Nad(1, i) /
(Nad(0, i) + Nad(1, i))
                DGrid4.Item(2, i).Value =
Nstar.ToString("0.#####e0")
                DGrid4.Item(3, i).Value = Sqrt(1
/ Nstar).ToString("0.#####e0")
            Next
        End Sub
    Dim xSheet As
Microsoft.Office.Interop.Excel.Worksheet

```



```

Dim path As String
Dim j, L, steps As Integer
Dim pi, q, m0, h_bar, c, e0, T, k,
kT As Double
Dim er, Eg, mr(2), m_eff(2), Nc, Nv,
es As Double
Dim Na, Nd, Efn, Efp, Vbi As Double
Dim Va, X, E_bar, eV, Edel, Estep,
D, terms(2), Vp, Jp(1) As Double

path =
System.IO.Directory.GetCurrentDirectory() &
"\FTD_Calculations.xlsx"
xSheet =
xBook.Worksheets("Fermi_Integral")

pi = 3.1415926536
q = 1.602176E-19 'C
m0 = 510998.91 'eV
h_bar = 0.0000000000000000658211899
'eV*Sec
c = 299792000.0 'm/Sec
e0 = 0.0000000000008854188 'F/cm
k = 0.00008617343 'eV/K
T = DGrid1.Item(1, 1).Value 'K
kT = k * T 'eV

er = DGrid1.Item(1, 3).Value
Eg = DGrid1.Item(1, 2).Value 'eV
mr(0) = DGrid2.Item(1, 0).Value 'N-
type
mr(1) = DGrid2.Item(2, 0).Value 'P-
type
mr(2) = DGrid1.Item(1, 4).Value
'Tunneling
es = e0 * er 'F/cm
m_eff(0) = mr(0) * m0 / c ^ 2 'eV
m_eff(1) = mr(1) * m0 / c ^ 2 'eV
m_eff(2) = mr(2) * m0 / (c ^ 2) 'eV
(Tunneling)
Nc = 0.000001 * Sqrt(1 / 2) * (kT *
m_eff(0) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-3
Nv = 0.000001 * Sqrt(1 / 2) * (kT *
m_eff(1) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-3
DGrid2.Item(1, 1).Value =
Nc.ToString("0.###e0") 'N-type
DGrid2.Item(2, 1).Value =
Nv.ToString("0.###e0") 'P-type

For i = 0 To rows Step 1
Nd = DGrid4.Item(0, i).Value 'N-
type
Na = DGrid4.Item(1, i).Value 'P-
type
Nstar = Nd * Na / (Nd + Na)
DGrid4.Item(2, i).Value =
Nstar.ToString("0.###e0")
DGrid4.Item(3, i).Value = (Nstar
^ -0.5).ToString("0.###e0")

Eg = DGrid1.Item(1, 2).Value 'eV
Eg = ENG(Nd, Na, Eg)
DGrid4.Item(11, i).Value =
Eg.ToString("0.###e0")

'Fermi_Levels1()
'N-type region
'Fermi_Levels1()
'N-type region
If CheckBox1.Checked = True Then
Efn = Fermi_Levels2(xSheet,
Nd, Nc) 'Only accurate for InGaAs (53/47)
Else
Efn = Fermi_Levels(xSheet,
Nd, Nc) ', Nc(0))
End If

Efn = Eg - Efn * kT
DGrid4.Item(9, i).Value =
Efn.ToString("0.###e0")
'P-type region
Efp = Fermi_Levels(xSheet, Na,
Nv)
Efp = Efp * kT
DGrid4.Item(10, i).Value =
Efp.ToString("0.###e0")

DGrid1.Refresh()
DGrid2.Refresh()

DGrid2.Item(1, 1).Value =
Nc.ToString("0.###e0") 'N-type
DGrid2.Item(2, 1).Value =
Nv.ToString("0.###e0") 'P-type

For j = 0 To rows Step 1
Nd = DGrid4.Item(0, j).Value 'N-
type
Na = DGrid4.Item(1, j).Value 'P-
type
Nstar = Nd * Na / (Nd + Na)
DGrid4.Item(2, j).Value =
Nstar.ToString("0.###e0")
DGrid4.Item(3, j).Value = (Nstar
^ -0.5).ToString("0.###e0")

Eg = DGrid1.Item(1, 2).Value 'eV
Eg = ENG(Nd, Na, Eg)
DGrid4.Item(11, j).Value =
Eg.ToString("0.###e0")

'Fermi_Levels1()
'N-type region
'Fermi_Levels1()
'N-type region
If CheckBox1.Checked = True Then
Efn = Fermi_Levels2(xSheet,
Nd, Nc) 'Only accurate for InGaAs (53/47)
Else
Efn = Fermi_Levels(xSheet,
Nd, Nc) ', Nc(0))
End If

Efn = Eg - Efn * kT
DGrid4.Item(9, j).Value =
Efn.ToString("0.###e0")
'P-type region
Efp = Fermi_Levels(xSheet, Na,
Nv)
Efp = Efp * kT
DGrid4.Item(10, j).Value =
Efp.ToString("0.###e0")

DGrid1.Refresh()
DGrid2.Refresh()

DGrid3.Refresh()
DGrid4.Refresh()

Vp = 0
Jp(0) = -1
Vbi = Efn - Efp 'eV
Dim temp(1) As Double
steps = 1000 * (Efn - Efp - Eg)
'DGrid3.RowCount - 2
For j = 0 To steps Step 1
Va = j / 1000
'DGrid3.Item(0, j).Value ' (Efn + Efp - Eg) /
2 'eV
X = 100 * Sqrt(q * (Vbi -
(2 * es * (Na + Nd))) 'V/m
E_bar = h_bar * X * Sqrt(2)
/ (pi * Sqrt(m_eff(2) * Eg)) 'eV
Estep = (Vbi - Va - Eg) /
D = 0
For L = 0 To 500 Step 1
eV = Estep * L
If eV < Vbi - Eg - Va -
Edel = eV
Else
Edel = Vbi - Eg - Va
End If
temp(0) = eV + Eg
temp(1) = -Vbi + Va + Eg
D = D + (Fcv(temp(0),
Efn, kT) - Fcv(temp(1), Efp, kT)) * (1 -
Exp(-2 * Edel / E_bar)) * Estep
Next
terms(0) = (q * X / (36 * pi
* h_bar ^ 2)) * Sqrt(2 * m_eff(2) / Eg) /
10000
terms(1) = Exp(-pi *
Sqrt(m_eff(2)) * (Eg ^ 1.5) / (2 * Sqrt(2) *
h_bar * X))
terms(2) = (4 * Sqrt(2 *
m_eff(2)) * (Eg ^ 1.5) / (3 * h_bar))

```

```

terms(1))
    Jp(1) = (D * terms(0) *
        If Jp(1) > Jp(0) Then
            Jp(0) = Jp(1)
            Vp = Va
        Else
            j = steps + 100
        End If
    Next
    DGrid4.Item(4, i).Value = Vp
    DGrid4.Item(5, i).Value =
        Jp(1).ToString("0.####e0")
    DGrid4.Item(6, i).Value =
        terms(0).ToString("0.####e0")
    DGrid4.Item(7, i).Value =
        D.ToString("0.####e0")
    DGrid4.Item(8, i).Value =
        Log(terms(1)).ToString("0.####e0")
    DGrid4.Item(12, i).Value =
        X.ToString("0.####e0")
    Next
End Sub
Private Sub N_Sweep_Va()
    Dim i, rows As Integer
    Dim Nad(), Nstar As Double
    rows = DGrid5.RowCount - 1 '0-base
    If IsNumeric(DGrid5.Item(0,
        rows).Value) Then
        Else
            rows = rows - 1
        End If
    ReDim Nad(1, rows)
    For i = 0 To rows Step 1
        Nad(0, i) = DGrid5.Item(0,
            i).Value 'Nd
        Nad(1, i) = DGrid5.Item(1,
            i).Value 'Na
        Nstar = Nad(0, i) * Nad(1, i) /
            (Nad(0, i) + Nad(1, i))

```

```

        DGrid5.Item(2, i).Value =
            Nstar.ToString("0.####e0")
        DGrid5.Item(3, i).Value = Sqrt(1
            / Nstar).ToString("0.####e0")
        Next
        Dim xSheet As
            Microsoft.Office.Interop.Excel.Worksheet
        Dim path As String
        Dim j, L, steps As Integer
        Dim pi, q, m0, h_bar, c, e0, T, k,
            kT As Double
        es As Double
        Dim er, Eg, mr(2), m_eff(2), Nc, Nv,
            Na, Nd, Efn, Efp, Vbi As Double
        Dim Va, X, E_bar, eV, Edel, Estep,
            D, terms(2), Vp, Jp(1) As Double
        path =
            System.IO.Directory.GetCurrentDirectory() &
            "\ETD_Calculations.xlsx"
        xSheet =
            xBook.Worksheets("Fermi_Integral")
        pi = 3.1415926536
        q = 1.602176E-19 'C
        m0 = 510998.91 'eV
        h_bar = 0.00000000000000000658211899
            'eV*Sec
        c = 299792000.0 'm/Sec
        e0 = 0.00000000000008854188 'F/cm
        k = 0.00008617343 'eV/K
        T = DGrid1.Item(1, 1).Value 'K
        kT = k * T 'eV
        er = DGrid1.Item(1, 3).Value
        Eg = DGrid1.Item(1, 2).Value 'eV
        mr(0) = DGrid2.Item(1, 0).Value 'N-
            type
        mr(1) = DGrid2.Item(2, 0).Value 'P-
            type
        mr(2) = DGrid1.Item(1, 4).Value
            'Tunneling
        es = e0 * er 'F/cm
        m_eff(0) = mr(0) * m0 / c ^ 2 'eV
            (N-type)
        DGrid1.Refresh()

```

```

        m_eff(1) = mr(1) * m0 / c ^ 2 'eV
            (P-type)
        m_eff(2) = mr(2) * m0 / (c ^ 2) 'eV
            (Tunneling)
        Nc = 0.000001 * Sqrt(1 / 2) * (kT *
            m_eff(0) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-3
        Nv = 0.000001 * Sqrt(1 / 2) * (kT *
            m_eff(1) / (pi * h_bar ^ 2)) ^ 1.5 'cm^-3
        DGrid2.Item(1, 1).Value =
            Nc.ToString("0.####e0") 'N-type
        DGrid2.Item(2, 1).Value =
            Nv.ToString("0.####e0") 'P-type
        Va = TextBox1.Text 'j / 1000
        'DGrid3.Item(0, j).Value 'Efn + Efp - Eg) /
            2 'eV
        For i = 0 To rows Step 1
            Nd = DGrid5.Item(0, i).Value 'N-
                type
            Na = DGrid5.Item(1, i).Value 'P-
                type
            Nstar = Nd * Na / (Nd + Na)
            DGrid5.Item(2, i).Value =
                Nstar.ToString("0.####e0")
            DGrid5.Item(3, i).Value = (Nstar
                ^ -0.5).ToString("0.####e0")
            Eg = DGrid1.Item(1, 2).Value 'eV
            DGrid5.Item(11, i).Value =
                Eg.ToString("0.####e0")
            'N-type region
            Efn = Fermi_Levels(xSheet, Nd,
                Nc)
            Efp = Eg - Efn * kT
            DGrid5.Item(9, i).Value =
                Efn.ToString("0.####e0")
            'P-type region
            Efp = Fermi_Levels(xSheet, Na,
                Nv)
            Efp = Efp * kT
            DGrid5.Item(10, i).Value =
                Efp.ToString("0.####e0")
            DGrid1.Refresh()

```

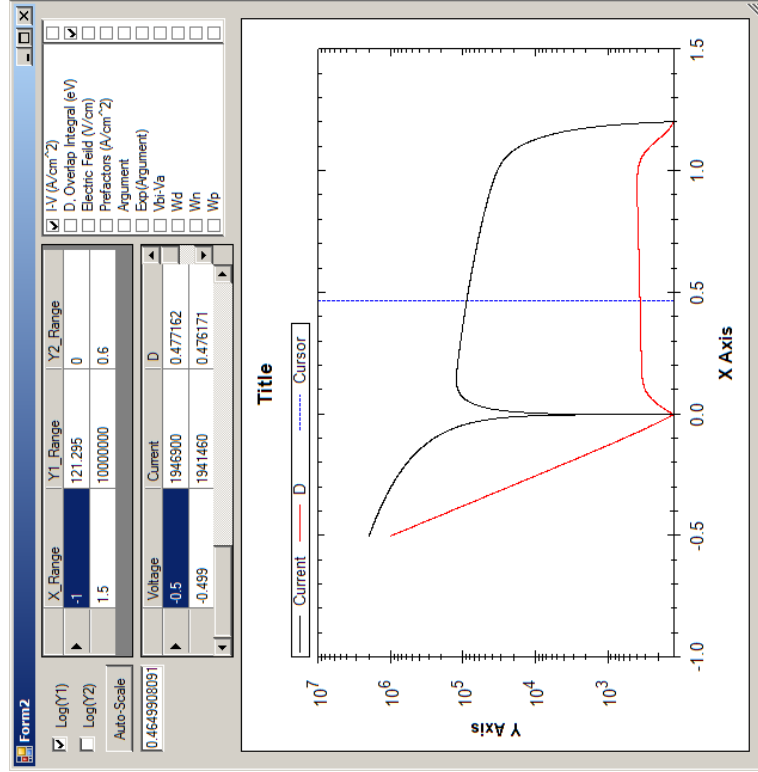

The following code controls the J-V

```

Imports ZedGraph
Imports System.Math
Public Class Form2
    Private Sub Form2_Load(ByVal sender As
System.Object, ByVal e As System.EventArgs)
Handles MyBase.Load
        End Sub

```

be found in Chapter 3.5.



Appendix A.2: Secondary window plotting J-V results.

```

Public Sub New(ByVal IVD(,) As Double,
ByVal parameters() As Double)
InitializeComponent()

Dim Graph1 As GraphPane =
zgl.GraphPane
Dim LeftCurve, RightCurve, Cursor As
LineItem
Dim DataLeft, DataRight, line As New
PointPairList
Dim i, count As Integer

count = IVD.GetLength(1) - 1
For i = 0 To count Step 1
    DataLeft.Add(IVD(0, i), IVD(1,
i))
    DataRight.Add(IVD(0, i), IVD(2,
i))
Next

LeftCurve =
Graph1.AddCurve("Current", DataLeft,
Color.Black, SymbolType.None)
RightCurve = Graph1.AddCurve("D",
DataRight, Color.Red, SymbolType.None)
Graph1.CurveList("D").IsY2Axis =
True

zgl.AxisChange()
Graph1.YAxis.Scale.Min =
parameters(10) / 1000
Graph1.YAxis.Type = AxisType.Log

line.Add((Graph1.XAxis.Scale.Min +
Graph1.XAxis.Scale.Max) / 2,
Graph1.Y2Axis.Scale.Min)
line.Add((Graph1.XAxis.Scale.Min +
Graph1.XAxis.Scale.Max) / 2,
Graph1.YAxis.Scale.Max)
Cursor = Graph1.AddCurve("Cursor",
line, Color.Blue, SymbolType.None)
Cursor.Line.Style =
Drawing2D.DashStyle.Dash

AxisRange.Rows.Add()
AxisRange.Rows.Add()

```

```

AxisRange.Item(0, 0).Value =
Graph1.XAxis.Scale.Min
AxisRange.Item(0, 1).Value =
Graph1.XAxis.Scale.Max
AxisRange.Item(1, 0).Value =
Graph1.YAxis.Scale.Min
AxisRange.Item(1, 1).Value =
Graph1.YAxis.Scale.Max
AxisRange.Item(2, 0).Value =
Graph1.Y2Axis.Scale.Min
AxisRange.Item(2, 1).Value =
Graph1.Y2Axis.Scale.Max

zgl.Refresh()

Dim Curves(9) As String
Curves(0) = "I-V (A/cm^2)"
Curves(1) = "D, Overlap Integral
(eV)"
Curves(2) = "Electric Feild (V/cm)"
Curves(3) = "Prefactors (A/cm^2)"
Curves(4) = "Argument"
Curves(5) = "Exp(Argument)"
Curves(6) = "Vbi-Va"
Curves(7) = "Wd"
Curves(8) = "Wn"
Curves(9) = "Wp"

For i = 0 To Curves.Length - 1 Step
1
False)
Y1Axis.Items.Add(Curves(i),
Y2Axis.Items.Add(" ", False)
Next
count = Y1Axis.Items.Count
Y2Axis.SetBounds(Y2Axis.Bounds.Location.X,
Y2Axis.Bounds.Location.Y,
Y2Axis.Bounds.Width, 4 + count * 15)
Y1Axis.SetBounds(Y1Axis.Bounds.Location.X,
Y1Axis.Bounds.Location.Y,
Y1Axis.Bounds.Width, 4 + count * 15)
Y1Axis.SetItemCheckState(0,
CheckState.Checked)

Y2Axis.SetItemCheckState(1,
CheckState.Checked)
Lists.Columns.Add("Voltage",
"Current")
Lists.Columns.Add("D", "D")
Lists.Columns.Add("E-Feild", "E-
Feild")
Lists.Columns.Add("Pre-F", "Pre-F")
Lists.Columns.Add("Arg", "Arg")
Lists.Columns.Add("Exp(Arg)",
"Exp(Arg)")
Lists.Columns.Add("Vbi-Va", "Vbi-
Va")
Lists.Columns.Add("Wd", "Wd")
Lists.Columns.Add("Wn", "Wn")
Lists.Columns.Add("Wp", "Wp")
count = IVD.GetLength(1) - 1
For i = 0 To count Step 1
Lists.Rows.Add()
Lists.Item(0, i).Value = IVD(0,
i)
Lists.Item(1, i).Value = IVD(1,
i)
Lists.Item(2, i).Value = IVD(2,
i)
Lists.Item(3, i).Value =
parameters(4) * Sqrt(1 - IVD(0, i) /
parameters(0))
Lists.Item(4, i).Value =
parameters(5) * Lists.Item(3, i).Value *
IVD(2, i)
Lists.Item(5, i).Value =
Abs(parameters(6) / Lists.Item(3, i).Value)
Lists.Item(6, i).Value = Exp(-
Lists.Item(5, i).Value)
parameters(0) - IVD(0, i)
Lists.Item(8, i).Value =
parameters(1) * Sqrt(1 - IVD(0, i) /
parameters(0))
Lists.Item(9, i).Value =
parameters(2) * Sqrt(1 - IVD(0, i) /
parameters(0))

Lists.Item(10, i).Value =
parameters(3) * Sqrt(1 - IVD(0, i) /
parameters(0))
Next
End Sub
Private Sub LogY1_CheckedChanged(ByVal
sender As System.Object, ByVal e As
System.EventArgs) Handles
LogY1.CheckedChanged
Dim Graph1 As GraphPane =
zgl.GraphPane
If LogY1.Checked = True Then
Graph1.YAxis.Type = AxisType.Log
Else
Graph1.YAxis.Type =
AxisType.Linear
End If
zgl.Refresh()
End Sub
Private Sub LogY2_CheckedChanged(ByVal
sender As System.Object, ByVal e As
System.EventArgs) Handles
LogY2.CheckedChanged
Dim Graph1 As GraphPane =
zgl.GraphPane
If LogY2.Checked = True Then
Graph1.Y2Axis.Type =
AxisType.Log
Else
Graph1.Y2Axis.Type =
AxisType.Linear
End If
zgl.Refresh()
End Sub
Private Sub AxisRange_KeyUp(ByVal sender
As Object, ByVal e As
System.Windows.Forms.KeyEventArgs) Handles
AxisRange.KeyUp
If e.KeyCode = Keys.Enter Then
e.SuppressKeyPress = True

```

```

Dim Graph1 As GraphPane =
    NewData.Add(Lists.Item(0,
        i).Value, Lists.Item(index, i).Value)
    Next
    Curve =
    Graph2.AddCurve(Lists.Columns(index).Name,
        NewData, Color.Black, SymbolType.None)
    Else
    Graph2.CurveList.Remove(Graph2.CurveList(Lists
        ts.Columns(index).Name))
    End If
    End Sub
    Private Sub AutoScale_Click(ByVal sender
        As System.Object, ByVal e As
        System.EventArgs) Handles AutoScale.Click
        Dim graph1 As GraphPane =
        zgl1.GraphPane
        zgl1.AxisChange()
        AxisRange.Item(0, 0).Value =
        Graph1.XAxis.Scale.Min
        AxisRange.Item(0, 1).Value =
        Graph1.XAxis.Scale.Max
        AxisRange.Item(1, 0).Value =
        Graph1.YAxis.Scale.Min
        AxisRange.Item(1, 1).Value =
        Graph1.Y2Axis.Scale.Min
        AxisRange.Item(2, 0).Value =
        Graph1.Y2Axis.Scale.Max
        graph1.Y2Axis.Scale.Max
        zgl1.Refresh()
    End Sub
    Private Sub zgl1_MouseMove(ByVal sender
        As Object, ByVal e1 As
        System.Windows.Forms.MouseEventArgs) Handles
        zgl1.MouseMove
        ' Save the mouse location
        Dim mousePt As New PointF(e1.X,
            e1.Y) ' (e.X, e.Y)
        ' Find the Chart rect that contains
        the current mouse location
    End Sub
    Private Sub zgl1_SelectedIndexChanged(ByVal sender As
        Object, ByVal e As System.EventArgs) Handles
        Y2Axis.SelectedIndexChanged
        Dim i, index, count As Integer
        Dim Graph1 As GraphPane =
        zgl1.GraphPane
        Dim Curve As LineItem
        Dim Data As New PointFPairList
        index = Y2Axis.SelectedIndex + 1
        If Y2Axis.GetItemChecked(index - 1)
            = True Then
            If Y1Axis.GetItemChecked(index -
                1) = True Then
                Graph1.CurveList.Remove(Graph1.CurveList(Lists
                    ts.Columns(index).Name))
            End If
            count = Lists.RowCount - 1
            For i = 0 To count Step 1
                Data.Add(Lists.Item(0,
                    i).Value, Lists.Item(index, i).Value)
            Next
            Curve =
            Graph1.AddCurve(Lists.Columns(index).Name,
                Data, Color.Red, SymbolType.None)
        End If
    End Sub
    Private Sub zgl1_SelectedIndexChanged(ByVal sender As
        Object, ByVal e As System.EventArgs) Handles
        Y2Axis.SelectedIndexChanged
        Dim i, index, count As Integer
        Dim Graph2 As GraphPane =
        zgl1.GraphPane
        Dim Curve As LineItem
        Dim NewData As New PointFPairList
        index = Y1Axis.SelectedIndex + 1
        If Y1Axis.GetItemChecked(index - 1)
            = True Then
            If Y2Axis.GetItemChecked(index -
                1) = True Then
                Graph2.CurveList.Remove(Graph2.CurveList(Lists
                    ts.Columns(index).Name))
            End If
            count = Lists.RowCount - 1
            For i = 0 To count Step 1
                Y2Axis.SetItemCheckedState(index - 1,
                    CheckState.Unchecked)
            Next
            Graph2.CurveList.Remove(Graph2.CurveList(Lists
                ts.Columns(index).Name))
            Y2Axis.SetItemCheckedState(index - 1,
                CheckState.Unchecked)
        End If
        count = Lists.RowCount - 1
        For i = 0 To count Step 1

```

```

Dim pane As GraphPane =
sender.MasterPane.FindChartRect(mousePt)

' If pane is non-null, we have a
valid location. Otherwise, the mouse is not
' within any chart rect.
If Not pane Is Nothing Then

    Dim x, y As Double
    ' Convert the mouse location to
    X, Y scale values
    pane.ReverseTransform(mousePt,
    x, y)

    Dim curve1 As CurveItem
    Dim list As IPointListEdit
    Dim mypane As GraphPane =
    zg1.GraphPane

    Dim lastIndex, indexWidth,
    TempIndex As Integer
    Dim dataM = New PointPairList
    zg1.GraphPane.CurveList.Remove(zg1.GraphPane
    .CurveList("Cursor"))

    IndexWidth = Int((LastIndex / 20)
    dataM.Add(x,
    mypane.YAxis.Scale.Min)
    dataM.Add(x,
    mypane.YAxis.Scale.Max)
    Dim myCurve As LineItem =
    mypane.AddCurve("Cursor", dataM, Color.Blue,
    SymbolType.None)
    Drawing2D.DashStyle.Dash
    TextBox1.Text = x

    zg1.Refresh()
    TextBox1.Refresh()
    End If

End Sub

Private Sub TextBox1_KeyUp(ByVal sender
As Object, ByVal e As
System.Windows.Forms.KeyEventArgs) Handles
TextBox1.KeyUp
    If e.KeyCode = Keys.Enter Then

```

```

e.SuppressKeyPress = True
Dim Graph1 As GraphPane =
zg1.GraphPane
Dim Cursor As LineItem
Dim line As New PointPairList

zg1.GraphPane.CurveList.Remove(zg1.GraphPane
.CurveList("Cursor"))

    line.Add(TextBox1.Text,
    Graph1.YAxis.Scale.Min)
    line.Add(TextBox1.Text,
    Graph1.YAxis.Scale.Max)
    Cursor =
    Graph1.AddCurve("Cursor", line, Color.Blue,
    SymbolType.None)
    Drawing2D.DashStyle.Dash
    zg1.Refresh()
    End If
End Sub

End Class

```

APPENDIX B

ImageJ Area Analysis Macro

The macro prompts the user to select a directory containing all of the image files to be ran. ImageJ runs one file at a time, beginning by automatically determining the region of interest and maximizing the zoom to fit that region. The macro is paused and the image is then made available for the user to define the device edge. Additionally, various image processing tools become available to speed up the analysis. Finally, the user continues the macro, whereupon the device dimensions are automatically fitted with an ellipse and the results are recorded as well as the final image. Magnification, device location, and mask defined size values are automatically extracted from the image files.

```
macro "Measure Ellipse Batch (Manual mode)" {
    requires("1.33s");
    run("Set Measurements...", " display area fit ");
    run("Clear Results");
    dir = getDirectory("Choose a Directory ");
    list = getFileList(dir);
    setBatchMode(false);

    for (i=0; i<list.length; i++) {
        path = dir+list[i];
        open(path);

        fname=toLowerCase(getInfo("image.filename")); //toLowerCase(File.name);
        //*****
        //Find bounds of partial field (Origin is top-left corner of image);
        // 1) Left Edge
        // 2) Right Edge
        // 3) Top
        // 4) Bottom

        run("RGB Color");
        y=384;
        x=512;
        do {
            x=x-1;
```



```

        v = getPixel(x,y);
        red = (v>>16)&0xff; // extract red byte (bits 23-17)
        green = (v>>8)&0xff; // extract green byte (bits 15-8)
        blue = v&0xff; // extract blue byte (bits 7-0)
    } while (red!=0 || green!=255 || blue!=0);
    Xmin=x+1;

    x=512;
    do {
        x=x+1;
        v = getPixel(x,y);
        red = (v>>16)&0xff; // extract red byte (bits 23-17)
        green = (v>>8)&0xff; // extract green byte (bits 15-8)
        blue = v&0xff; // extract blue byte (bits 7-0)
    } while (red!=0 || green!=255 || blue!=0)
    Xmax=x-1;

    x=512;
    y=384;
    do {
        y=y-1;
        v = getPixel(x,y);
        red = (v>>16)&0xff; // extract red byte (bits 23-17)
        green = (v>>8)&0xff; // extract green byte (bits 15-8)
        blue = v&0xff; // extract blue byte (bits 7-0)
    } while (red!=0 || green!=255 || blue!=0);
    Ymin=y+1;

    y=384;
    do {
        y=y+1;
        v = getPixel(x,y);
        red = (v>>16)&0xff; // extract red byte (bits 23-17)
        green = (v>>8)&0xff; // extract green byte (bits 15-8)
        blue = v&0xff; // extract blue byte (bits 7-0)
    } while (red!=0 || green!=255 || blue!=0);
    Ymax=y-1;

    //run("Revert");
run("32-bit");
    RangeX=(Xmax-Xmin);
    RangeY=(Ymax-Ymin);

    makeRectangle(Xmin, Ymin, RangeX, RangeY);
    run("To Selection");
//*****

//*****
//Extracting magnification directly from TIFF file tag

```

```

//Gets the tag, and parses it to get the pixel size information
tagnum=34118;
tag = call("TIFF_Tags.getTag", path, tagnum);
i0 = indexOf(tag, "Mag = ");
    if (i0===-1) exit ("Scale information not found");

i1 = indexOf(tag, "=", i0);
i2 = indexOf(tag, "X", i1);
    if (i1===-1 || i2===-1 || i2 <= i1+4)
        exit ("Parsing error! Maybe the file structure changed?");

text = substring(tag,i1+1,i2+1);

//Parse text string to find magnification number
TextSize = lengthOf(text);
Mag = "";
j = 0;

do {
    Char = substring(text, j, j+1);
    if (Char!=" " && Char!="K" && Char!="M" && Char!="X")

        Mag=Mag+Char;
        j = j+1;
} while (Char!="K" && Char!="M" && Char!="X");

if (Char=="K")
    Mag = parseFloat(Mag)*1000;
else if (Char=="K")
    Mag = parseFloat(Mag)*1000000;
else
    Mag = parseFloat(Mag)*1;

Dist = 365856*Mag/60000;
run("Set Scale...", "distance="+Dist+" known=680799.42 pixel=1 unit=nm");
//*****

//*****
//Perform thresholding

run("Threshold...");
setAutoThreshold("Minimum");
waitForUser("(1) Adjust thresholding, \n(2) Do Wand to outline, \n(3) Selection
Brush for adjustments, \n(4) Click 'OK' when done \n - 'r' to revert image \n - 'shift + t' adjust
threshold levels");
//*****

run("Measure");
row = nResults-1;
fname=getResultLabel(row);

```

```

LocX = parseFloat(substring(fname,1,2));
LocY = parseFloat(substring(fname,3,4));
LocCol = substring(fname,5,6);
    LocCol = charCodeAt(LocCol,0)-64;
LocRow = parseFloat(substring(fname,6,7));
    if (LocRow==0) LocRow = 10;

    if (LocCol<6) {
        if (LocRow==1) MDL = 0.1;
        else if (LocRow==2) MDL = 0.3;
        else if (LocRow==3) MDL = 0.5;
        else if (LocRow==4) MDL = 0.7;
        else if (LocRow==7) MDL = 0.9;
        else if (LocRow==8) MDL = 1.2;
        else if (LocRow==9) MDL = 1.6;
        else if (LocRow==10) MDL = 2.0;
    }
    else {
        if (LocRow==1) MDL = 0.2;
        else if (LocRow==2) MDL = 0.4;
        else if (LocRow==3) MDL = 0.6;
        else if (LocRow==4) MDL = 0.8;
        else if (LocRow==7) MDL = 1.0;
        else if (LocRow==8) MDL = 1.4;
        else if (LocRow==9) MDL = 1.8;
        else if (LocRow==10) MDL = 3.0;
    }

    if (LocRow==5 || LocRow==6){
        if (LocCol==1 || LocCol==2) MDL = 4.0;
        if (LocCol==3) MDL = 10;
        if (LocCol==8) MDL = 20;
        if (LocCol==9 || LocCol==10) MDL = 5.0;
    }

    setResult("X",row,LocX);
    setResult("Y",row,LocY);
    setResult("Column",row,LocCol);
    setResult("Row",row,LocRow);
    setResult("Length (um)",row,MDL);
    updateResults();

        setForegroundColor(255, 255, 0);
        run("Revert");

        run("Draw");
        saveAs("Tiff", dir + "Output_" + fname);
        close();
    }
}

```

APPENDIX C

Fabrication & Processing Traveler

The following is a table containing the fabrication process used for this work. The left hand column contains the fabrication procedure as well as required information and metrology results for continued processing. The right hand column is for additional comments and results.

1) Cleave Sample a) Width: b) Height: c) Markings?	
2) Surface Prep? a) InP cap etch b) Other?	
3) Lithography 1 a) IPA Clean b) Dehydration bake c) Spin LOR 5A i) Ramp up: 2 sec to 500 RPM ii) Stay: 2 sec @ 500 RPM iii) Ramp up: 2 sec to 4000 RPM iv) Stay: 45 sec @ 4000 RPM v) Ramp Down: ~3-5 sec d) Spin PMMA i) Ramp up: 2 sec to 500 RPM ii) Stay: 2 sec @ 500 RPM iii) Ramp up: 2 sec to 4000 RPM iv) Stay: 45 sec @ 4000 RPM v) Ramp Down: ~3-5 sec e) Bake @ 1800C for 10 min. f) Exposure i) Rows, Col ii) Die spacing (Rows, Col) iii) Alignment Cross iv) I_{Filament} (A) v) $I_{\text{Probe}}/I_{\text{Start}}/I_{\text{Finish}}$ vi) Stage tilt vii) AutoFocus ($z=Ax+By+C$) (1) $Y = Ax + By, +C$ (2) RMS g) Develop PMMA i) MIBK:IPA (1:3) – 75 sec	

<ul style="list-style-type: none"> ii) Blow dry (no DI rinse) h) Develop LOR5A <ul style="list-style-type: none"> i) CD26:DI (1:1) – 75 sec ii) CD26 – 10 sec iii) Di Rinse & blow dry i) Inspect with Optical microscope j) SEM inspection (optional) 	
<ul style="list-style-type: none"> 4) Metal #1 Deposition <ul style="list-style-type: none"> a) Prepare NANO 38 for evaporator <ul style="list-style-type: none"> i) Replace kapton tape ii) Replace NPRL Au boat with ours iii) Add Au to boat (~3.5) iv) Replace Zn pellet (if needed) v) Check thickness monitor crystal vi) Remove sample platen vii) Close door b) DI:HCl (10:1) – 10 sec. <ul style="list-style-type: none"> i) DI rinse & blow dry c) Load samples d) Pump down chamber (< 5e-6 Torr) e) Setup Recipe <ul style="list-style-type: none"> i) Layer 1: Au, 20nm ii) Layer 2: Zn, 20nm iii) Layer 3: Au, 160m f) Run recipe <ul style="list-style-type: none"> i) Layer 1 (use “auto/manual”) ii) Layer 2: fully automated iii) Layer 3 (use “auto/manual”) g) Finish <ul style="list-style-type: none"> i) Vent chamber & remove samples ii) Remove our Au boat and replace with NPRL’s iii) Pump down chamber 	
<ul style="list-style-type: none"> 5) Lift-Off <ul style="list-style-type: none"> a) Heat PG Remover <ul style="list-style-type: none"> i) 80⁰C – 90⁰C (set temp to ~115⁰C) ii) 1st beaker: lift-off iii) 2nd beaker: clean-up b) Rinse & blow dry c) Optical inspect d) O2 Ash (Lam 490) e) HCl:DI (1:1) f) IPA Rinse g) Optical inspect h) Profilometry (metal thickness) 	
<ul style="list-style-type: none"> 6) Mesa Isolation Etch <ul style="list-style-type: none"> a) Citric Acid: H₂O₂ (20:1) <ul style="list-style-type: none"> i) ~1 nm/min b) Profilometry (metal + mesa) 	

<ul style="list-style-type: none"> i) Etch depth (mesa thick.) c) Etch rate? d) SEM inspect <ul style="list-style-type: none"> i) Metal thickness ii) Mesa thickness 	
<ul style="list-style-type: none"> 7) Level 1 electrical testing <ul style="list-style-type: none"> a) Observe NDR? <ul style="list-style-type: none"> i) Sizes measured? ii) $J_p, J_v, PVCR$? b) Observations: 	
<ul style="list-style-type: none"> 8) BCB Coat <ul style="list-style-type: none"> a) Set "Blue M" oven to 140°C w/N₂ b) Set hot plate to 140°C c) IPA Clean d) Dehydration bake e) Spin AP3000 <ul style="list-style-type: none"> i) Ramp up: 2 sec to 500 RPM ii) Stay: 2 sec @ 500 RPM iii) Ramp up: 2 sec to 3000 RPM iv) Stay: 60 sec @ 3000 RPM v) Ramp Down: ~3-5 sec f) Spin BCB <ul style="list-style-type: none"> i) Ramp up: 2 sec to 500 RPM ii) Stay: 2 sec @ 500 RPM iii) Ramp up: 2 sec to 3000 RPM iv) Stay: 60 sec @ 3000 RPM v) Ramp Down: ~3-5 sec g) Bake @ 1400C >5min. h) Cure in "Blue M" oven <ul style="list-style-type: none"> i) Place sample in oven (flat) ii) Ramp oven to 250°C (w/N₂) iii) Start timer when temp > 245°C iv) Cure for 60 min. v) Remove samples & turn oven off 	
<ul style="list-style-type: none"> 9) BCB Etch back <ul style="list-style-type: none"> a) Fast Etch (400-600 nm/min) <ul style="list-style-type: none"> i) SF₆:O₂ (sccm) ii) Pressure & electrode spacing iii) Power b) Slow Etch (200-300 nm/min) <ul style="list-style-type: none"> i) SF₆:O₂ (sccm) ii) Pressure & electrode spacing iii) Power c) Measure BCB thick: Nanospec (nm) <ul style="list-style-type: none"> i) Refractive index = 1.54 ii) 5 locations away from edge <ul style="list-style-type: none"> (1) On top and below big bar d) BCB to Etch ($t_{BCB} - t_{final_BCB}$) <ul style="list-style-type: none"> i) $t_{final_BCB} = (t_{mesa} + t_{metal})$ ii) ****BCB measures thick. when it is thin (<~500 nm)***** 	

<ul style="list-style-type: none"> e) Fast Etch BCB: <ul style="list-style-type: none"> i) Etch time (total) ii) Measure: t_{BCB} (STDev) (nm) iii) Calculate: $t_{BCB} - t_{final_BCB}$ (nm) iv) Rate: R_{fast} (nm/min) f) Slow Etch BCB: <ul style="list-style-type: none"> i) Etch for some time ii) Measure: t_{BCB} (STDev) (nm) iii) Calculate: $t_{BCB} - t_{final_BCB}$ (nm) iv) Rate: R_{fast} (nm/min) g) SEM Inspect: h) Post BCB electrical testing i) Observe NDR? <ul style="list-style-type: none"> i) Sizes measured? ii) $J_p, J_v, PVCR$? j) Observations: 	
<ul style="list-style-type: none"> 10) Lithography 2 <ul style="list-style-type: none"> a) IPA Clean b) Dehydration bake c) Spin LOR 5A: 1st Coat <ul style="list-style-type: none"> i) Ramp up: 2 sec to 500 RPM ii) Stay: 2 sec @ 500 RPM iii) Ramp up: 2 sec to 4000 RPM iv) Stay: 45 sec @ 4000 RPM v) Ramp Down: ~3-5 sec d) Bake @ 1800C for 1 min. e) Spin LOR 5A: 2nd coat <ul style="list-style-type: none"> i) Ramp up: 2 sec to 500 RPM ii) Stay: 2 sec @ 500 RPM iii) Ramp up: 2 sec to 4000 RPM iv) Stay: 45 sec @ 4000 RPM v) Ramp Down: ~3-5 sec f) Spin PMMA <ul style="list-style-type: none"> i) Ramp up: 2 sec to 500 RPM ii) Stay: 2 sec @ 500 RPM iii) Ramp up: 2 sec to 4000 RPM iv) Stay: 45 sec @ 4000 RPM v) Ramp Down: ~3-5 sec g) Bake @ 1800C for 10 min. h) Exposure <ul style="list-style-type: none"> i) Rows, Col ii) Die spacing (Rows, Col) iii) $I_{Filament}$ (A) iv) $I_{Probe}/I_{Start}/I_{Finish}$ v) Stage tilt i) Develop PMMA <ul style="list-style-type: none"> i) MIBK:IPA (1:3) – 75 sec ii) Blow dry (no DI rinse) j) Develop LOR5A <ul style="list-style-type: none"> i) CD26:DI (1:1) – 135 sec ii) CD26 – 10 sec 	

<ul style="list-style-type: none"> iii) Di Rinse & blow dry k) Inspect with Optical microscope l) SEM inspection (optional) 	
<p>11) Metal #1 Deposition</p> <ul style="list-style-type: none"> a) Prepare NANO 38 for evaporator <ul style="list-style-type: none"> i) Replace kapton tape ii) Replace NPRL Au boat with ours iii) Add Au to boat (~6) iv) Check thickness monitor crystal v) Remove sample platen vi) Close door b) Load samples c) Pump down chamber (< 5e-6 Torr) d) Setup Recipe <ul style="list-style-type: none"> i) Layer 3: Au, 400m e) Run recipe <ul style="list-style-type: none"> i) Layer 3 (use “auto/manual”) f) Finish <ul style="list-style-type: none"> i) Vent chamber & remove samples ii) Remove our Au boat and replace with NPRL’s iii) Pump down chamber 	
<p>12) Lift-Off</p> <ul style="list-style-type: none"> a) Heat PG Remover <ul style="list-style-type: none"> i) 80⁰C – 90⁰C (set temp to ~115⁰C) ii) 1st beaker: lift-off iii) 2nd beaker: clean-up b) Rinse & blow dry c) Optical inspect 	
<p>13) Processing Completed: proceed to Electrical Testing</p>	


```

1) / 2
FileNumber(0) = (FileName.Length -
SendFileNames(1) = FileName(0)
For i = 1 To FileNumber(0) Step 1
FileNumber(1) = i
Messages1.Text = "File " &
FileNumber(1) & " of " & FileNumber(0) & "
<" & FileName(2 * i) & ">:"
Messages1.Refresh()
SendFileNames(0) = FileName(2 *
SendFileNames(2) = FileName(2 *
Analyze_File(SendFileNames,
identifiers, FileNumber)
Next
end_of_program:
Messages1.Text = "I am finished.
Please let me rest."
Messages2.Text = "I am finished.
Please let me rest."
Messages1.Refresh()
Messages2.Refresh()
End Sub
Private Sub Analyze_File(ByVal
filename() As String, ByVal identifiers() As
String, ByVal FileNumber As Array) (ByVal
filename0 As String, ByVal filename1 As
String, ByVal filename2 As String, ByVal
identifiers() As String, ByVal FileNumber As
Array)
Dim i, counter, sheetcount,
output(1), row As Integer
Dim settings(5), Data0(,), Data1(,),
Area(), Temperatures(), scalar As Double
Dim xlApp, x2App As New
Microsoft.Office.Interop.Excel.Application
'Excel.Application
*****
Dim xlbook, x2book As
Microsoft.Office.Interop.Excel.Workbook
Dim xlsheet As
Microsoft.Office.Interop.Excel.Worksheet
'Dim filename(2) As String
Dim Algorithms As New Get_Algorithm
'PIVET_algorithms.Format
Dim Formats As New Get_FileFormat
*****
'Create output excel file
xlApp.Visible = False
xlApp.DisplayAlerts = False
x2book = xlApp.Workbooks.Add
If
(filename(1) & "\output\" & filename(2))
System.IO.Directory.Exists(filename(1) +
"output") = False Then
System.IO.Directory.CreateDirectory(filename
(1) + "output\")
End If
x2book.SaveAs(filename(1) &
"output\" & filename(2))
'Create Worksheets
' (1) Combined IV data
' (2) Extracted Data
' --> And Populate it
sheetcount = x2book.Sheets.Count
x2book.Worksheets.Add(After:=x2book.Workshee
ts(sheetcount), Count:=2)
x2book.Worksheets(sheetcount +
1).Name = "Combined IV"
x2book.Worksheets(sheetcount +
2).Name = "Extracted Data"
x2book.Worksheets("Extracted
Data").cells(1, 1).value = "File Name"
x2book.Worksheets("Extracted
Data").cells(1, 2).value = "Append"
x2book.Worksheets("Extracted
Data").cells(1, 3).value = "X"
x2book.Worksheets("Extracted
Data").cells(1, 4).value = "Y"
*****
'Look at File name for identifiers:
' (0) Algorithm
' (1) file format
' (2) forward/reverse peaks
' (3) Second Algorithm for
comparison
'If one isn't found, user must
supply one.
If ConstAlg.Checked = False Then
ReDim identifiers(3) 'As String
identifiers =
analyze_name(filename(0) ', AlgTypes,
FFormats, FR)
'ReDim Preserve identifiers(3)
Dim GetAlg2 As New
Get_Algorithm2
'PIVET_algorithms.Get_Algorithm2
GetAlg2.ShowDialog()
identifiers(3) =
GetAlg2.Selected_Alg2
End If

```

```

x2book.Worksheets("Extracted
Data").cells(1, 5).value = "Grid"
x2book.Worksheets("Extracted
Data").cells(1, 6).value = "Temperature"
x2book.Worksheets("Extracted
Data").cells(1, 7).value = Geometry.Text & "
(" & Units.Text & ")"
x2book.Worksheets("Extracted
Data").cells(1, 8).value = "Undercut"
x2book.Worksheets("Extracted
Data").cells(1, 9).value = "Width (X)"
x2book.Worksheets("Extracted
Data").cells(1, 10).value = "Height (Y)"
x2book.Worksheets("Extracted
Data").cells(1, 11).value = "Diameter (um)"
x2book.Worksheets("Extracted
Data").cells(1, 12).value = "Area (cm2)"
x2book.Worksheets("Extracted
Data").cells(1, 13).value = "Vp (Rev.)"
x2book.Worksheets("Extracted
Data").cells(1, 14).value = "Vv (Rev.)"
x2book.Worksheets("Extracted
Data").cells(1, 15).value = "Ip (Rev.)"
x2book.Worksheets("Extracted
Data").cells(1, 16).value = "Iv (Rev.)"
x2book.Worksheets("Extracted
Data").cells(1, 17).value = "Jp (A/cm2)"
x2book.Worksheets("Extracted
Data").cells(1, 18).value = "Jv (A/cm2)"
x2book.Worksheets("Extracted
Data").cells(1, 19).value = "PVCr (Rev.)"
x2book.Worksheets("Extracted
Data").cells(1, 20).value = "Vp (For.)"
x2book.Worksheets("Extracted
Data").cells(1, 21).value = "Vv (For.)"
x2book.Worksheets("Extracted
Data").cells(1, 22).value = "Ip (For.)"
x2book.Worksheets("Extracted
Data").cells(1, 23).value = "Iv (For.)"
x2book.Worksheets("Extracted
Data").cells(1, 24).value = "Jp (A/cm2)"
x2book.Worksheets("Extracted
Data").cells(1, 25).value = "Jv (A/cm2)"
x2book.Worksheets("Extracted
Data").cells(1, 26).value = "PVCr (For.)"

x2book.Worksheets("Sheet1").delete()

x2book.Worksheets("Sheet2").delete()
x2book.Worksheets("Sheet3").delete()
x2book.Save()

Messages2.Text = "Output File
Created and Formatted."
Messages2.Refresh()

'*****
***
'Open File
'Get initial settings
Select Case identifiers(1)
Case Is = "K4200"
Messages2.Text = "Working
with a Keithley 4200 Formatted input File"
Messages2.Refresh()

x1book =
x2App.Workbooks.Open(filename(0))
settings =
Formats.K4200_settings(x1book)
settings(0) = settings(0) -
2
'settings;
(0) # of worksheets = #
of IV curves
(1) compliance
(2) Starting voltage
(3) voltage step
(4) voltage = 0 V
(5) number of data
points

Case Is = "PSU"

x2book.Worksheets("Sheet2").delete()
Messages2.Text = "Working
with a PSU Formatted input File"
Messages2.Refresh()

settings(0) = 1

Case Is = "NPRL"
Case Else
GoTo skip_analysis
End Select
'*****
***
'loop for each dataset
counter = 1
row = 1
For i = 0 To (settings(0) - 1) Step
1
Messages2.Text = "Data Set " &
(i + 1) & " of " & settings(0)
Messages2.Refresh()

'*****
***
'Collect data set
Select Case identifiers(1)
Case Is = "K4200"
If i >= 1 Then
x1sheet =
x1book.Worksheets(i + 3)
x2book.Worksheets("Extracted
Data").cells(row + 1, 1).value = x1book.Name
'x1book.Worksheets(i + 3).name

x2book.Worksheets("Extracted
Data").cells(row + 1, 2).value =
x1book.Worksheets(i + 3).name

```

```

Else
  x1sheet =
  x1book.Worksheets(i + 1)
  x2book.Worksheets("Extracted
Data").cells(row + 1, 1).value = x1book.Name
'x1book.Worksheets(i + 3).name
x2book.Worksheets("Extracted
Data").cells(row + 1, 2).value =
x1book.Worksheets(i + 3).name
End If
Data0 =
Formats.K4200_All(x1sheet)
x2book.Worksheets("Combined IV").cells(1,
counter + 1).value = x1sheet.Name
Case Is = "PSU"
Data0 =
Formats.PSU_All(filename(0))
x2book.Worksheets("Combined IV").cells(1,
counter + 1).value = filename(2)
Case Is = "NPRL"
Case Else
  GoTo skip_analysis
End Select
  x2book.Worksheets("Extracted
Data").cells(row + 1, 11).value = "=sqrt(I"
& (row + 1) & "-2*H" & (row + 1) & ")*(J" &
(row + 1) & "-2*H" & (row + 1) & ")")
  x2book.Worksheets("Combined
IV").cells(2,
counter).resize(Data0.GetLength(0), 2).value
= Data0
  x2book.Worksheets("Combined
IV").cells(1, counter).value = "Voltage"
  counter = counter + 2
  row = row + 1
  *****
  Data").cells(row, 13).Value = Data1(0,
output(0)) 'Vpeak
  x2book.Worksheets("Extracted
Data").cells(row, 14).Value = Data1(0,
output(1)) 'Vvalley
  x2book.Worksheets("Extracted
Data").cells(row, 15).Value = Data1(1,
output(0)) 'Ipeak
  x2book.Worksheets("Extracted
Data").cells(row, 16).Value = Data1(1,
output(1)) 'Ivalley
  x2book.Worksheets("Extracted
Data").cells(row, 17).value = "=0" & row &
"/I" & row 'Jpeak
  x2book.Worksheets("Extracted
Data").cells(row, 18).value = "=P" & row &
"/I" & row 'Jvalley
  x2book.Worksheets("Extracted
Data").cells(row, 19).Value = "=0" & row &
"/P" & row 'PVCr
End If
  *****
  'use desired algorithm
  Select Case identifiers(3)
    Case Is = "Sean1"
      output =
Algorithms.PVF_Seal_v1(Data1, settings(1))
    Case Is = "Sean2"
      output =
Algorithms.PVF_Seal_v2(Data1, settings(1))
    Case Is = "David1"
      output =
Algorithms.PVF_David_v1(Data1, settings(1))
    Case Is = "David2"
      output =
Algorithms.PVF_David_v2(Data1)
    Case Is = "None"
      output =
Algorithms.PVF_Skip_Analysis
  End Select
  *****
  If identifiers(0) <> "None"
Then
  x2book.Worksheets("Extracted

```

```

                GoTo skip_analysis
            End Select
        *****
        If identifiers(3) <> "None"
            Then
                x2book.Worksheets("Extracted
                Data").cells(settings(0) + row + 3,
                13).Value = Data1(0, output(0)) 'Vpeak

                x2book.Worksheets("Extracted
                Data").cells(settings(0) + row + 3,
                14).Value = Data1(0, output(1)) 'Vvalley

                x2book.Worksheets("Extracted
                Data").cells(settings(0) + row + 3,
                15).Value = Data1(1, output(0)) 'Ipeak

                x2book.Worksheets("Extracted
                Data").cells(settings(0) + row + 3,
                16).Value = Data1(1, output(1)) 'Ivalley

                x2book.Worksheets("Extracted
                Data").cells(settings(0) + row + 3,
                17).value = "=O" & settings(0) + row + 3 &
                "/" & settings(0) + row + 3 'Jpeak

                x2book.Worksheets("Extracted
                Data").cells(settings(0) + row + 3,
                18).value = "=P" & settings(0) + row + 3 &
                "/" & settings(0) + row + 3 'Jvalley

                x2book.Worksheets("Extracted
                Data").cells(settings(0) + row + 3,
                19).Value = "=O" & settings(0) + row + 3 &
                "/" & settings(0) + row + 3 'PVCr

                End If
            End If
        *****

        GoTo skip_analysis
            End Select
        *****
        'If there is a peak and valley
        in quadrant 1 (Forward)
        If identifiers(2) = "FandR" Or
        identifiers(2) = "Forward" Then
            *****
            'Get reverse bias data
            'convert to quadrant 1
            Data1 =
            Algorithms.Forward_Data(Data0)
            *****
            'use desired algorithm
            Select Case identifiers(0)
                Case Is = "Sean1"
                    output =
                    Algorithms.PVF_Seal_v1(Data1, settings(1))
                Case Is = "Sean2"
                    output =
                    Algorithms.PVF_Seal_v2(Data1, settings(1))
                Case Is = "David1"
                    output =
                    Algorithms.PVF_David_v1(Data1, settings(1))
                Case Is = "David2"
                    output =
                    Algorithms.PVF_David_v2(Data1)
                Case Is = "None"
                    GoTo skip_analysis
            End Select
        *****
        If identifiers(0) <> "None"
            Then
                x2book.Worksheets("Extracted
                Data").cells(row, 20).Value = Data1(0,
                output(0)) 'Vpeak

                x2book.Worksheets("Extracted
                Data").cells(row, 21).Value = Data1(0,
                output(1)) 'Vvalley

                x2book.Worksheets("Extracted
                Data").cells(row, 22).Value = Data1(1,
                output(0)) 'Ipeak

                x2book.Worksheets("Extracted
                Data").cells(row, 23).Value = Data1(1,
                output(1)) 'Ivalley

                x2book.Worksheets("Extracted
                Data").cells(row, 24).value = "=V" & row &
                "/" & row 'Jpeak

                x2book.Worksheets("Extracted
                Data").cells(row, 25).value = "=W" & row &
                "/" & row 'Jvalley

                x2book.Worksheets("Extracted
                Data").cells(row, 26).Value = "=V" & row &
                "/" & row 'PVCr

                End If
            End If
        *****
        'use desired algorithm
        Select Case identifiers(3)
            Case Is = "Sean1"
                output =
                Algorithms.PVF_Seal_v1(Data1, settings(1))
            Case Is = "Sean2"
                output =
                Algorithms.PVF_Seal_v2(Data1, settings(1))
            Case Is = "David1"
                output =
                Algorithms.PVF_David_v1(Data1, settings(1))
            Case Is = "David2"
                output =
                Algorithms.PVF_David_v2(Data1)
            Case Is = "None"
                Case Else
        *****
    
```



```

Dim str, AFP (3) As String
If AFP (0) = "" Then
    Dim GetAlg As New Get_Algorithm
    GetAlg.ShowDialog()
    AFP (0) = GetAlg.Selected_Algo
End If

If AFP (1) = "" Then
    Dim GetFormat As New
    GetFormat.ShowDialog()
    AFP (1) =
    GetFormat.Selected_Format
End If

If AFP (2) = "" Then
    Dim GetFR As New FandR_Peaks
    'PIVET.FandR_Peaks
    GetFR.ShowDialog()
    AFP (2) = GetFR.selected_FR
End If

AFP (3) = ""

Return AFP
End Function

Public Sub find_outliers(ByVal xlsheet
As Microsoft.Office.Interop.Excel.Worksheet,
ByVal Fand_orR As String)
    Dim i, j, k, l, row_count, color,
    col_mod As Integer
    Dim Data0(,), averages(), STDev() As
    Double
    Dim col(4) As Char

    row_count =
    xlsheet.Application.WorksheetFunction().CountA(xlsheet.Range("A:A")) - 2
    xlsheet.Cells(row_count + 3, 1) =
    "Average"
    xlsheet.Cells(row_count + 4, 1) =
    "STDev"

    For l = 0 To 1 Step 1
        ReDim Data0(4, row_count),
        averages(4), STDev(4)
        If l = 0 Then
            If Fand_orR = "FandR" Or
            "Forward" Then
                col_mod = 12
                col(0) = "L"
                col(1) = "M"
                col(2) = "P"
                col(3) = "Q"
                col(4) = "R"
            End If
        Else
            If Fand_orR = "FandR" Or
            "Reverse" Then
                col_mod = 5
                col(0) = "E"
                col(1) = "F"
                col(2) = "I"
                col(3) = "J"
                col(4) = "K"
            End If
        End If

        For i = 0 To row_count Step 1
            Data0(0, i) =
            xlsheet.Cells(i + 2, col_mod).value()
            Data0(1, i) =
            xlsheet.Cells(i + 2, col_mod + 1).value()
            Data0(2, i) =
            xlsheet.Cells(i + 2, col_mod + 4).value()
            Data0(3, i) =
            xlsheet.Cells(i + 2, col_mod + 5).value()
            Data0(4, i) =
            xlsheet.Cells(i + 2, col_mod + 6).value()
            For j = 0 To 4 Step 1
                averages(j) = Data0(j),
                averages(j) + averages(j)
            Next
            xlsheet.Cells(row_count + 3, 1) =
            col_mod.value() = "AVERAGE(" & col(0) &
            "2:" & col(0) & (row_count + 2) & ")"
            xlsheet.Cells(row_count + 4, 1) =
            col_mod.value() = "STDEV(" & col(0) &
            "2:" & col(0) & (row_count + 2) & ")"
        Next
    Next
End Sub

Dim str, AFP (3) As String
If AFP (0) = "" Then
    Dim GetAlg As New Get_Algorithm
    GetAlg.ShowDialog()
    AFP (0) = GetAlg.Selected_Algo
End If

If AFP (1) = "" Then
    Dim GetFormat As New
    GetFormat.ShowDialog()
    AFP (1) =
    GetFormat.Selected_Format
End If

If AFP (2) = "" Then
    Dim GetFR As New FandR_Peaks
    'PIVET.FandR_Peaks
    GetFR.ShowDialog()
    AFP (2) = GetFR.selected_FR
End If

AFP (3) = ""

Return AFP
End Function

Public Sub find_outliers(ByVal xlsheet
As Microsoft.Office.Interop.Excel.Worksheet,
ByVal Fand_orR As String)
    Dim i, j, k, l, row_count, color,
    col_mod As Integer
    Dim Data0(,), averages(), STDev() As
    Double
    Dim col(4) As Char

    row_count =
    xlsheet.Application.WorksheetFunction().CountA(xlsheet.Range("A:A")) - 2
    xlsheet.Cells(row_count + 3, 1) =
    "Average"
    xlsheet.Cells(row_count + 4, 1) =
    "STDev"

    For l = 0 To 1 Step 1
        ReDim Data0(4, row_count),
        averages(4), STDev(4)
        If l = 0 Then
            If Fand_orR = "FandR" Or
            "Forward" Then
                col_mod = 12
                col(0) = "L"
                col(1) = "M"
                col(2) = "P"
                col(3) = "Q"
                col(4) = "R"
            End If
        Else
            If Fand_orR = "FandR" Or
            "Reverse" Then
                col_mod = 5
                col(0) = "E"
                col(1) = "F"
                col(2) = "I"
                col(3) = "J"
                col(4) = "K"
            End If
        End If

        For i = 0 To row_count Step 1
            Data0(0, i) =
            xlsheet.Cells(i + 2, col_mod).value()
            Data0(1, i) =
            xlsheet.Cells(i + 2, col_mod + 1).value()
            Data0(2, i) =
            xlsheet.Cells(i + 2, col_mod + 4).value()
            Data0(3, i) =
            xlsheet.Cells(i + 2, col_mod + 5).value()
            Data0(4, i) =
            xlsheet.Cells(i + 2, col_mod + 6).value()
            For j = 0 To 4 Step 1
                averages(j) = Data0(j),
                averages(j) + averages(j)
            Next
            xlsheet.Cells(row_count + 3, 1) =
            col_mod.value() = "AVERAGE(" & col(0) &
            "2:" & col(0) & (row_count + 2) & ")"
            xlsheet.Cells(row_count + 4, 1) =
            col_mod.value() = "STDEV(" & col(0) &
            "2:" & col(0) & (row_count + 2) & ")"
        Next
    Next
End Sub

Dim str, AFP (3) As String
If AFP (0) = "" Then
    Dim GetAlg As New Get_Algorithm
    GetAlg.ShowDialog()
    AFP (0) = GetAlg.Selected_Algo
End If

If AFP (1) = "" Then
    Dim GetFormat As New
    GetFormat.ShowDialog()
    AFP (1) =
    GetFormat.Selected_Format
End If

If AFP (2) = "" Then
    Dim GetFR As New FandR_Peaks
    'PIVET.FandR_Peaks
    GetFR.ShowDialog()
    AFP (2) = GetFR.selected_FR
End If

AFP (3) = ""

Return AFP
End Function

Public Sub find_outliers(ByVal xlsheet
As Microsoft.Office.Interop.Excel.Worksheet,
ByVal Fand_orR As String)
    Dim i, j, k, l, row_count, color,
    col_mod As Integer
    Dim Data0(,), averages(), STDev() As
    Double
    Dim col(4) As Char

    row_count =
    xlsheet.Application.WorksheetFunction().CountA(xlsheet.Range("A:A")) - 2
    xlsheet.Cells(row_count + 3, 1) =
    "Average"
    xlsheet.Cells(row_count + 4, 1) =
    "STDev"

    For l = 0 To 1 Step 1
        ReDim Data0(4, row_count),
        averages(4), STDev(4)
        If l = 0 Then
            If Fand_orR = "FandR" Or
            "Forward" Then
                col_mod = 12
                col(0) = "L"
                col(1) = "M"
                col(2) = "P"
                col(3) = "Q"
                col(4) = "R"
            End If
        Else
            If Fand_orR = "FandR" Or
            "Reverse" Then
                col_mod = 5
                col(0) = "E"
                col(1) = "F"
                col(2) = "I"
                col(3) = "J"
                col(4) = "K"
            End If
        End If

        For i = 0 To row_count Step 1
            Data0(0, i) =
            xlsheet.Cells(i + 2, col_mod).value()
            Data0(1, i) =
            xlsheet.Cells(i + 2, col_mod + 1).value()
            Data0(2, i) =
            xlsheet.Cells(i + 2, col_mod + 4).value()
            Data0(3, i) =
            xlsheet.Cells(i + 2, col_mod + 5).value()
            Data0(4, i) =
            xlsheet.Cells(i + 2, col_mod + 6).value()
            For j = 0 To 4 Step 1
                averages(j) = Data0(j),
                averages(j) + averages(j)
            Next
            xlsheet.Cells(row_count + 3, 1) =
            col_mod.value() = "AVERAGE(" & col(0) &
            "2:" & col(0) & (row_count + 2) & ")"
            xlsheet.Cells(row_count + 4, 1) =
            col_mod.value() = "STDEV(" & col(0) &
            "2:" & col(0) & (row_count + 2) & ")"
        Next
    Next
End Sub

```



```

"2:" & col(4) & (row_count + 2) & ") "
'averages(4)

For j = 1 To 3 Step 1
Select Case j
Case Is = 1
color = 65535
Case Is = 2
color = 49407
Case Is = 3
color = 255
End Select

For i = 0 To row_count
Step 1

For k = 0 To 1 Step
If j * STDev(k)
As System.Object, ByVal e As
System.EventArgs Handles Button1.Click
Dim FileName() As String
SendFileNames(2) As String
Dim FileName(1), FileCount, i,
RowCount, row As Integer
Dim xlapp As New
Microsoft.Office.Interop.Excel.Application
Dim X1Book, X2Book As
Microsoft.Office.Interop.Excel.Workbook
Dim X1Sheet, X2Sheet As
Microsoft.Office.Interop.Excel.Worksheet

'*****
***
'Get Filename information:
' (1) path\file_name
' (0) path\
' (2) \file_name.
FileName = GetFileName()
If FileName(0) = "False" Then
Messages1.Text = "No File"
Messages2.Text = "No File"
Messages1.Refresh()
Messages2.Refresh()
Goto TheEnd
Else

.patternrintandshade = 0

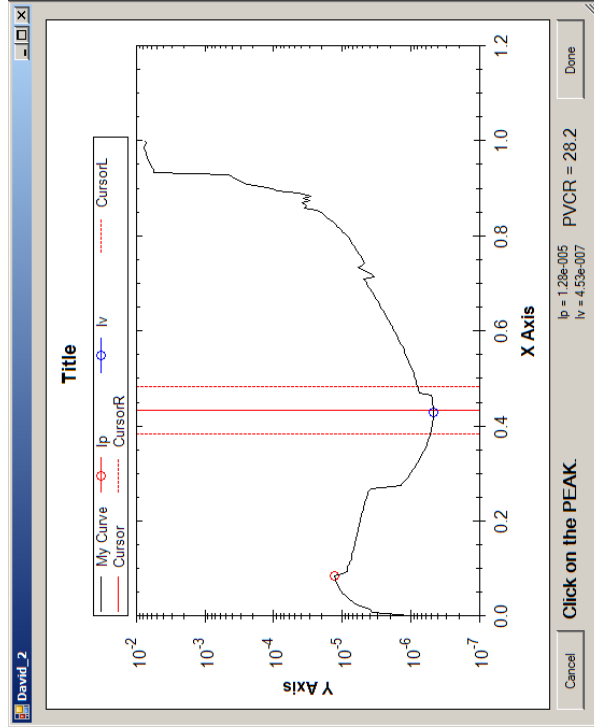
'*****
***
'Create output excel file
xlapp.Visible = False
xlapp.DisplayAlerts = False
If System.IO.File.Exists(FileName(0)
+ "Compiled.xlsx") = True Then
X2Book =
xlapp.Workbooks.Open(FileName(0) +
"Compiled.xlsx")
Else
X2Book = xlapp.Workbooks.Add
X2Book.SaveAs(FileName(0) +
"Compiled.xlsx")
X2Book.Worksheets(1).name =
"Extracted Data"
X2Book.Worksheets("Extracted
Data").cells(1, 1).value = "File Name"
X2Book.Worksheets("Extracted
Data").cells(1, 2).value = "Append"
X2Book.Worksheets("Extracted
Data").cells(1, 3).value = "X"
X2Book.Worksheets("Extracted
Data").cells(1, 4).value = "Y"
X2Book.Worksheets("Extracted
Data").cells(1, 5).value = "Grid"
X2Book.Worksheets("Extracted
Data").cells(1, 6).value = "Temperature"
X2Book.Worksheets("Extracted
Data").cells(1, 7).value = Geometry.Text &
("& Units.Text & ")

```

```

X2Book.Worksheets("Extracted
Data").cells(1, 8).value = "Undercut"
X2Book.Worksheets("Extracted
Data").cells(1, 9).value = "Width (X)"
X2Book.Worksheets("Extracted
Data").cells(1, 10).value = "Height (Y)"
X2Book.Worksheets("Extracted
Data").cells(1, 11).value = "Diameter (um)"
X2Book.Worksheets("Extracted
Data").cells(1, 12).value = "Area (cm2)"
X2Book.Worksheets("Extracted
Data").cells(1, 13).value = "Vp (Rev.)"
X2Book.Worksheets("Extracted
Data").cells(1, 14).value = "Vv (Rev.)"
X2Book.Worksheets("Extracted
Data").cells(1, 15).value = "Ip (Rev.)"
X2Book.Worksheets("Extracted
Data").cells(1, 16).value = "Iv (Rev.)"
X2Book.Worksheets("Extracted
Data").cells(1, 17).value = "Jp (A/cm2)"
X2Book.Worksheets("Extracted
Data").cells(1, 18).value = "Jv (A/cm2)"
X2Book.Worksheets("Extracted
Data").cells(1, 19).value = "PVCR (Rev.)"
X2Book.Worksheets("Extracted
Data").cells(1, 20).value = "Vp (For.)"
X2Book.Worksheets("Extracted
Data").cells(1, 21).value = "Vv (For.)"
X2Book.Worksheets("Extracted
Data").cells(1, 22).value = "Ip (For.)"
X2Book.Worksheets("Extracted
Data").cells(1, 23).value = "Iv (For.)"
X2Book.Worksheets("Extracted
Data").cells(1, 24).value = "Jp (A/cm2)"
X2Book.Worksheets("Extracted
Data").cells(1, 25).value = "Jv (A/cm2)"
X2Book.Worksheets("Extracted
Data").cells(1, 26).value = "PVCR (For.)"
X2Book.Save()
End If
X2Sheet =
X2Book.Worksheets("Extracted Data")
For i = 1 To FileCount Step 1
Messages1.Text = "File #" & i &
" of " & FileCount
Messages1.Refresh()
Next
Messages2.Text = FileName(i * 2)
Messages2.Refresh()
X1Book =
X2Book.Save()
X2Book.Close()
X1Book.Close()
X1Sheet =
X1Book.Worksheets("Extracted Data")
RowCount =
X1Sheet.Application.WorksheetFunction.CountA TheEnd:
(X1Sheet.Range("B:B")) - 1
If RowCount > 0 Then
row =
X2Sheet.Application.WorksheetFunction.CountA
(X2Sheet.Range("B:B")) + 1
X2Sheet.Cells(row,
1).resize(RowCount, 26).value =
X1Sheet.Cells(2, 1).resize(RowCount,
26).value
X2Book.Save()
End If
End Sub
End Class

```



Appendix D.2: Window for manually picking peak and valley locations (algorithm David-2).

After execution a series of windows will open asking for desired input information. If selected, the David-2 algorithm will open a new window displaying the current I-V characteristic, and requires the user to point out the peak and valley (Appendix D.2). The following code is associated with the “David-2” algorithm.

```

Public Class David_2
    Public values(1), index(1) As Integer

    Private Sub David_2_Load(ByVal sender As System.Object, ByVal e As System.EventArgs) Handles MyBase.Load
        Label1.Text = "Click on the PEAK."

        Dim LastIndex, IndexWidth, IndexMain As Integer
        Dim mypane As GraphPane = zg1.GraphPane

        Dim list As IPointListEdit
        Dim dataL As New PointPairList
        Dim dataM As New PointPairList
        Dim dataR As New PointPairList
        Dim Peak = New PointPairList
        Dim Valley = New PointPairList

        Dim LastIndex, IndexWidth, IndexMain As Integer
        Dim mypane As GraphPane = zg1.GraphPane

        Dim list As IPointListEdit
        Dim dataL As New PointPairList
        Dim dataM As New PointPairList
        Dim dataR As New PointPairList
        Dim Peak = New PointPairList
        Dim Valley = New PointPairList

        list = mypane.CurveList("MyCurve").Points
        LastIndex = list.Count - 1
        IndexMain = Int(LastIndex / 2)
        IndexWidth = Int(LastIndex / 20)

        dataL.Add(list(IndexMain - IndexWidth).X, mypane.YAxis.Scale.Min)
        dataL.Add(list(IndexMain - IndexWidth).X, mypane.YAxis.Scale.Max)
        dataM.Add(list(IndexMain).X, mypane.YAxis.Scale.Min)
        dataM.Add(list(IndexMain).X, mypane.YAxis.Scale.Max)
        dataR.Add(list(IndexMain + IndexWidth).X, mypane.YAxis.Scale.Min)
        dataR.Add(list(IndexMain + IndexWidth).X, mypane.YAxis.Scale.Max)

        Dim myCurveL As LineItem = mypane.AddCurve("CursorL", dataL, Color.Red, SymbolType.None)
        myCurveL.Line.Style = Drawing2D.DashStyle.Dash

        Dim myCurve As LineItem = mypane.AddCurve("Cursor", dataM, Color.Red, SymbolType.None)
        Dim myCurveR As LineItem = mypane.AddCurve("CursorR", dataR, Color.Red, SymbolType.None)
        myCurveR.Line.Style = Drawing2D.DashStyle.Dash

        Peak.Add(list(IndexMain).X, list(IndexMain).Y)
        Dim PeakPoint As LineItem = mypane.AddCurve("Ip", Peak, Color.Red, SymbolType.Circle)
        Valley.Add(list(IndexMain).X, list(IndexMain).Y)
        Dim ValleyPoint As LineItem = mypane.AddCurve("Iv", Peak, Color.Blue, SymbolType.Circle)

        list = mypane.CurveList("MyCurve").Points
        LastIndex = list.Count - 1
        IndexMain = Int(LastIndex / 2)
        IndexWidth = Int(LastIndex / 20)

        dataL.Add(list(IndexMain - IndexWidth).X, mypane.YAxis.Scale.Min)
        dataL.Add(list(IndexMain - IndexWidth).X, mypane.YAxis.Scale.Max)
        dataM.Add(list(IndexMain).X, mypane.YAxis.Scale.Min)
        dataM.Add(list(IndexMain).X, mypane.YAxis.Scale.Max)
        dataR.Add(list(IndexMain + IndexWidth).X, mypane.YAxis.Scale.Min)
        dataR.Add(list(IndexMain + IndexWidth).X, mypane.YAxis.Scale.Max)

        Dim myCurveL As LineItem = mypane.AddCurve("CursorL", dataL, Color.Red, SymbolType.None)
        myCurveL.Line.Style = Drawing2D.DashStyle.Dash

        Dim myCurve As LineItem = mypane.AddCurve("My Curve", data, Color.Black, SymbolType.None)
        mypane.YAxis.Type = AxisType.Log
        zg1.AxisChange()
        zg1.Refresh()

        End Sub

        Private Sub zg1_MouseMove(ByVal sender As ZedGraph.ZedGraphControl, ByVal e1 As System.Windows.Forms.MouseEventArgs) Handles zg1.MouseDown
            ' Save the mouse location
            Dim mousePt As New PointF(e1.X, e1.Y) ' (e.X, e.Y)

            ' Find the Chart rect that contains the current mouse location
            Dim pane As GraphPane = sender.MasterPane.FindChartRect(mousePt)

            ' If pane is non-null, we have a valid location. Otherwise, the mouse is not within any chart rect.
            If Not pane Is Nothing Then
                Dim x, y As Double
                ' Convert the mouse location to X, Y scale values
            End If
        End Sub

        Public Sub New(ByVal data2(,) As Double, ByVal length As Integer)
            InitializeComponent()

            Dim i As Integer
            Dim mypane As GraphPane = zg1.GraphPane
            Dim data = New PointPairList

            For i = 0 To length Step 1
                data.Add(data2(0, i), data2(1, i))
            Next

            Dim myCurve As LineItem = mypane.AddCurve("My Curve", data, Color.Black, SymbolType.None)
            mypane.YAxis.Type = AxisType.Log
            zg1.AxisChange()
            zg1.Refresh()

            End Sub

            Private Sub zg1_MouseMove(ByVal sender As ZedGraph.ZedGraphControl, ByVal e1 As System.Windows.Forms.MouseEventArgs) Handles zg1.MouseDown
                ' Save the mouse location
                Dim mousePt As New PointF(e1.X, e1.Y) ' (e.X, e.Y)

                ' Find the Chart rect that contains the current mouse location
                Dim pane As GraphPane = sender.MasterPane.FindChartRect(mousePt)

                ' If pane is non-null, we have a valid location. Otherwise, the mouse is not within any chart rect.
                If Not pane Is Nothing Then
                    Dim x, y As Double
                    ' Convert the mouse location to X, Y scale values
                End If
            End Sub
        End Sub
    End Class

```

```

x, y)
pane.ReverseTransform(mousePt,
    Dim myCurveR As myCurveR As
    LineItem = mypane.AddCurve("CursorR", dataR,
    Color.Red, SymbolType.None)
    myCurveR.Line.Style
    = Drawing2D.DashStyle.Dash
    Else
    Dim myCurveL As
    LineItem = mypane.AddCurve("CursorL", dataL,
    Color.Blue, SymbolType.None)
    myCurveL.Line.Style
    = Drawing2D.DashStyle.Dash
    Dim myCurve As
    LineItem = mypane.AddCurve("Cursor", dataM,
    Color.Blue, SymbolType.None)
    myCurve.Line.Style
    = Drawing2D.DashStyle.Dash
    End If
End If

dataL.Add(list(0).X,
mypane.YAxis.Scale.Min)
dataL.Add(list(0).X,
mypane.YAxis.Scale.Max)
Else
dataL.Add(list(TempIndex - IndexWidth).X,
mypane.YAxis.Scale.Min)
dataL.Add(list(TempIndex - IndexWidth).X,
mypane.YAxis.Scale.Max)
End If

dataM.Add(list(TempIndex).X,
mypane.YAxis.Scale.Min)
dataM.Add(list(TempIndex).X,
mypane.YAxis.Scale.Max)

If (TempIndex +
IndexWidth) > LastIndex Then
dataR.Add(list(LastIndex).X,
mypane.YAxis.Scale.Min)
dataR.Add(list(LastIndex).X,
mypane.YAxis.Scale.Max)
Else
dataR.Add(list(TempIndex + IndexWidth).X,
mypane.YAxis.Scale.Min)
dataR.Add(list(TempIndex + IndexWidth).X,
mypane.YAxis.Scale.Max)
End If

If Label1.Text = "Click
on the PEAK." Then
    Dim myCurveL As
    LineItem = mypane.AddCurve("CursorL", dataL,
    Color.Red, SymbolType.None)
    myCurveL.Line.Style
    = Drawing2D.DashStyle.Dash
    Dim myCurve As
    LineItem = mypane.AddCurve("Cursor", dataM,
    Color.Red, SymbolType.None)
    End If
Return
End Sub

pane.ReverseTransform(mousePt,
    Dim curvel As CurveItem
    Dim list As IPointListEdit
    Dim i As Integer
    Dim mypane As GraphPane =
    Dim LastIndex, IndexWidth,
    TempIndex As Integer
    Dim dataL = New PointPairList
    Dim dataM = New PointPairList
    Dim dataR = New PointPairList
    curvel =
    list = curvel.Points
    LastIndex = list.Count - 1

    For i = 0 To (LastIndex - 1)
        If list(i).X > x Then
            If (list(i).X - x) < (x
            - list(i - 1).X) Then
                TempIndex = i
            Else
                TempIndex = i - 1
            End If

            zgl1.GraphPane.CurveList.Remove(zgl1.GraphPane
            .CurveList("CursorL"))
            zgl1.GraphPane.CurveList.Remove(zgl1.GraphPane
            .CurveList("Cursor"))
            zgl1.GraphPane.CurveList.Remove(zgl1.GraphPane
            .CurveList("CursorR"))
            IndexWidth =
            Int(LastIndex / 20)
            If (TempIndex -
            IndexWidth) < 0 Then

```

```

        Private Sub zgl_click(ByVal sender As System.Object, ByVal e1 As System.Windows.Forms.MouseEventArgs) Handles zgl.Click
            ' Save the mouse location
            Dim mousept As New PointF(e1.X, e1.Y)

            ' Find the Chart rect that contains the current mouse location
            Dim pane As GraphPane = sender.MasterPane.FindChartRect(mousept)

            ' If pane is non-null, we have a valid location. Otherwise, the mouse is not within any chart rect.
            If Not pane Is Nothing Then
                Select Case Label1.Text
                    Case Is = "Click on the PEAK."
                        Max(index(0), index(1))
                        Label1.Text = "Click on the VALLEY."
                    Case Is = "Click on the VALLEY."
                        Label2.Text = "Ip = " & zgl.GraphPane.CurveList("My Curve").Points(values(0)).Y.ToString("e2")
                    Case Is = "Click on the VALLEY."
                        Min(index(0), index(1))
                        Label1.Text = "Click on the PEAK."
                    Case Is = "Click on the PEAK."
                        Label3.Text = "Iv = " & zgl.GraphPane.CurveList("My Curve").Points(values(1)).Y.ToString("e2")
                End Select
            End Select

            If zgl.GraphPane.CurveList("My Curve").Points(values(1)).Y <> 0 Then
                Label4.Text = "PVCR = " & (zgl.GraphPane.CurveList("My Curve").Points(values(0)).Y / zgl.GraphPane.CurveList("My Curve").Points(values(1)).Y).ToString("F1")
            End If
        End If

        Label1.Refresh()

        Return
    End Sub

    Private Sub Done_Click(ByVal sender As System.Object, ByVal e As System.EventArgs) Handles Done.Click
        Me.Close()
    End Sub

    Private Sub Cancel_Click(ByVal sender As System.Object, ByVal e As System.EventArgs) Handles Cancel.Click
        Dim i As Integer
        For i = 0 To 1 Step 1
            values(i) = 0
        Next
        Me.Close()
    End Sub

    Private Sub Max(ByVal IndexL As Integer, ByVal IndexR As Integer)
        Dim i As Integer
        Dim Ip As Double
        Dim mypane As GraphPane = zgl.GraphPane
        Dim list As IPointListEdit
        Dim Peak = New PointPairList
        Dim Valley = New PointPairList

        Peak = mypane.CurveList("Ip").Points
        list = mypane.CurveList("My Curve").Points
        Iv = Peak(0).Y
        For i = IndexL To IndexR Step 1
            If list(i).Y < Iv Then
                Iv = list(i).Y
            End If
        Next

        zgl.GraphPane.CurveList.Remove(zgl.GraphPane.CurveList("Iv"))
        Valley.Add(list(values(1)).X, list(values(1)).Y)
        Dim ValleyPoint As LineItem = mypane.AddCurve("Iv", Valley, Color.Blue, SymbolType.Circle)
    End Sub

    End Class

```