TRUTH TABLE TEST FIXTURE FOR PMOS GATE ARRAY

By

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ABSTRACT

An improved test fixture, used to evaluate the functionality of logic circuits designed using a PMOS technology based gate array, was tested and, when necessary, repaired. It was enhanced so as to allow it to accomodate two automatic probers operating at maximum capacity. An improved truth table test fixture was designed as a future replacement of the existing system.

INTRODUCTION

The importance of Test Engineering to the fabrication of integrated circuits upto their packaged form can simply not be measured. Any one particular wafer may survive all in line testing requirements (such as proper beta and sheet resistance values) but this is no guarantee that any or all of the devices contained on that wafer will function as the circuit designers had intended. The challenge confronting the test engineer, therefore, is to be able to assure that his/or her system is free from any anamolies that may cause the passing of bad parts and the rejection of good. These anamolies, more commonly referred to as "noise", are often difficult to locate and remove. This is especially true with any automatic prober test system. Sources of noise within such systems can be generated because of the system's lack of user friendliness and also because there exists continuity problems from probes to cabling and or from cabling to the interface hardware. Noise produces a senseless loss of money and effort and must be eliminated.

The problem of noise within an IC test system carries a different significance when it starts to interfere with the educational process. This is especially true in the Introductory Microelectronic Engineering course, EMCR 210. The laboratory associated with this course is the freshmen's first exposure to some important aspects of their chosen field. These aspects include a logic design, equivalent circuit layout, IC implementation of the circuit with a NOR logic gate array, device fabrication and finally device testing. This project requires five weeks to complete and would be especially rewarding if the fabricated devices can be evaluated and results compared to design. Realization of

this goal could be severely hampered if the test fixture used did not function properly or was too confusing to operate efficiently. Because of the number of students in the class and the number of die on each wafer, an inefficient test system design can lead to the loss of the project's educational impact.

In order to understand what is required of an efficient, user-friendly test fixture, the specifics of the gate array design must be discussed. The gate array itself is shown in Figure 1. It is a 3x4 four input NOR matrix equipped with 22 pads to be used for inputs, outputs, ground or supply. A typicallogic circuit design is shown in Figure 2. This circuit is a 3x8 decoder designed here at RIT.

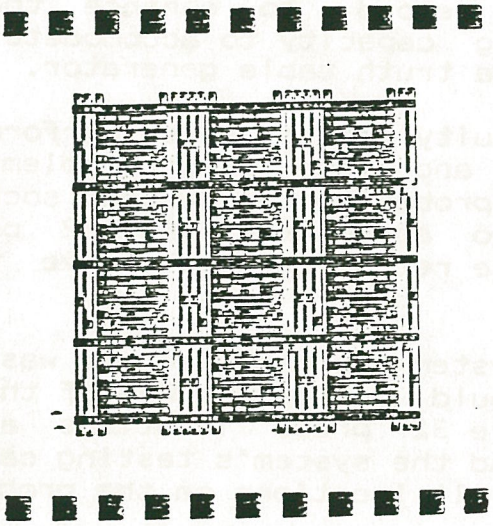

FIGURE 1

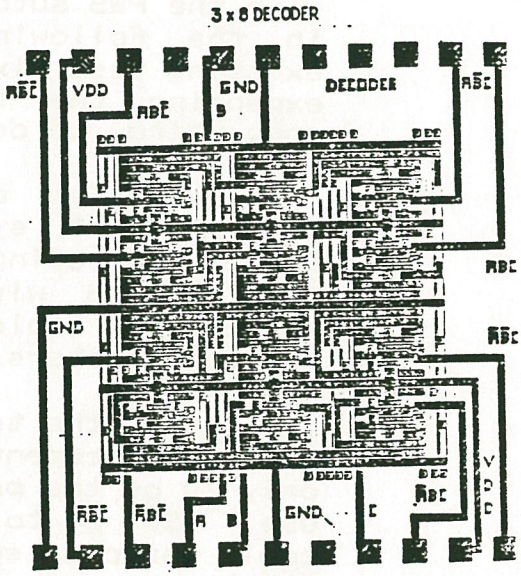

FIGURE 2

The present test system used to verify freshman gate array designs is shown in Figure 3. It consists of an automatic prober by Pacific West Systems (PWS) connected via cables to one of two 40 pin sockets. The first 32 of these pins are connected to a row of numbered plugs which correspond to the 32 possible probe sites on the PWS probers. A bank of power supplies is provided above the plugs and a bank of multimeters is supplied below. Desired voltages are achieved at chip inputs by connecting the supply to the proper numbered plug. Desired

TYPICAL SET UP

TO TEST GATE ARRAYS USING

PRESENT SYSTEM

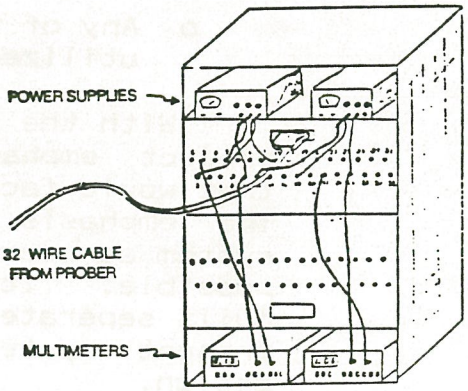

FIGURE 3

voltages are sensed at chip outputs by connecting a multimeter to the desired plug. In order to test the decoder with this system, at least three power supplies and one multimeter must be provided. One can see where confusion may arise as the students step through the eight different logic levels on the inputs while constantly switching the multimeter to the proper output. It should also be obvious that testing of one die in this manner would consume a considerable amount of time and testing of many die would certainly take a full three hour lab period.

EXPERIMENTAL

The primary objective of this project was to provide RIT with a guaranteed test fixture to be used in conjunction with the PWS automatic probers. This goal was accomplished in the following manner; first, to test and repair the existing test fixture, second, to enhance the system by expanding the testing capacity to accomodate both probers and, third, to design a truth table generator.

Extensive continuity tests were performed on the present test system and some minor problems were noted. Cables connecting the prober to the 40 pin socket did not have enough wires to accomodate the 32 possible probe locations. Cables were retrofitted to solve this problem for both probers.

After the test system was repaired, it was noted that some enhancements could be made. One of the probers had only 20 of the possible 32 probe locations available for use. So as to expand the system's testing capacity, a new cable was created and all locations on the probe card were soldered.

After extensive testing of this fixture, it was declared that the fixture was guaranteed for the following conditions.

- Both probers could now be used simultaneously.
- Any of the 32 probe locations on each card could utilized.

With the work on the present test fixture complete, project emphasis switched to designing a new test fixture that would facilitate the testing of gate array designs. The emphasis of the design was placed upon making this system as user friendly, as efficient and as versatile as possible. It was also decided that the new system would be built seperate of the existing. This would enable the present system to remain as a safety net for the proposed design.

Figure 4 depicts the layout of the proposed truth table test fixture for PMOS gate array designs. A cable from one of the two probers would plug into the 40 pin socket. The three way switch would determine whether the pin would be ground (or logic low), supply (or logic high), or an output. This achieves the versatility aspect of the design because each pin could be used in any one of the five possibel modes that needed when testing logic circuits. The LEDs are included so as to show what level an input is set to or what level an output is being sensed to be. This helps to achieve the user friendliness aspect of the design because they visually assist the student in determining what state an input or output is in.

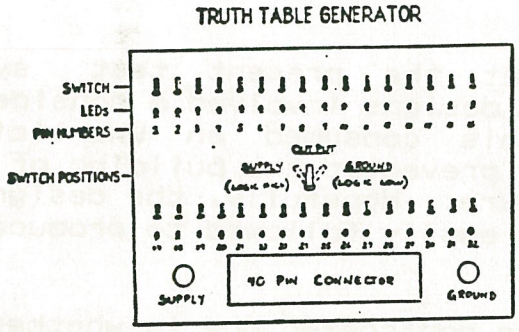

FIGURE 4

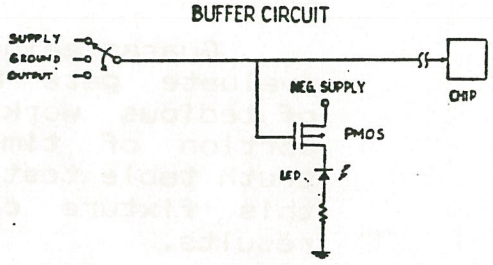

FIGURE 5

In order to implement this design of a truth table test fixture, operational theory of a LED had to be explored. It is known that a LED has a forward voltage of approximately 1.2 Volts and requires about 15 milliamps of current in order to operate. These facts present no problem to the circuit design when a pin is going to be used as an input because the power supply can easily provide the required current and voltage for LED operation. However, the current needs of a LED do present a problem if the pin is to be used as an output. Because the chip could never supply the required current to drive an LED, a buffer circuit had to be designed. This circuit is shown in Figure 5. A high impedance element, such as the PMOS transistor shown, must be used so as to provide the needed current. In this configuration, the PMOS transistor will act as a switch. When the voltage on the output line is less than the threshold voltage of the transistor, the transistor will turn on allowing current to pass from source to drain. By considering the channel resistance of the transistor and the required current to operate the LED, a resistor value, R, can be determined. A drawback to this buffer circuit is that it fixes the value of logic high to the threshold voltage of the PMOS transistor. For example, if the threshold voltage was -2.0 Volts, the LED would light only if the output voltage was less this value. Other buffer circuits could be considered to circumvent this problem. For example, an operational amplifier could be used as a comparator with a potentiometer to adjust the reference voltage.

CONCLUSION / FUTURE CONSIDERATIONS

At present, the only proven and well behaved device fabrication process at RIT is PMOS. This technology has enabled logic circuits to be designed and devices to be fabricated. Testing of these devices has produced mixed results in the past. This is especially true for those devices designed around a NOR logic gate array used almost exclusively in a freshmen level course. The need to facilitate the testing of these devices was apparent. For this reason, the intention of this project was to, first, to guarantee the present test system and, second, to design and build a new system that would easily test PMOS gate array designs.

Guaranteeing that the present test system could evaluate gate array designs involved a considerable amount of tedious work. This consumed an unanticipated large portion of time and prevented the building of the designed truth table test fixture. Hopefully, the design layout of this fixture can be easily followed to produce the desired results.

The problem to be confronted now is whether or not the truth table test fixture will be able to expand with the advancements being made in process design. It is obvious that if RIT starts to fabricate devices built with newly proposed CMOS processes, the truth table generator would not be able to test them satisfactorily, rendering it obsolete. This fact points out very clearly the need for RIT to enhance its testing abilities so as to keep pace with improvements being made in the fab.

ACKNOWLEDGEMENTS

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