300 BAUD MODEM DESIGN

by

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ABSTRACT

The 300 bps MODEM was researched and is in the process of being designed and built. The relatively low speed of a 300 bps MODEM allows for an asynchronous design therefore eliminating much of the timing control necessary at higher speeds. The result is a low speed functional MODEM.

INTRODUCTION

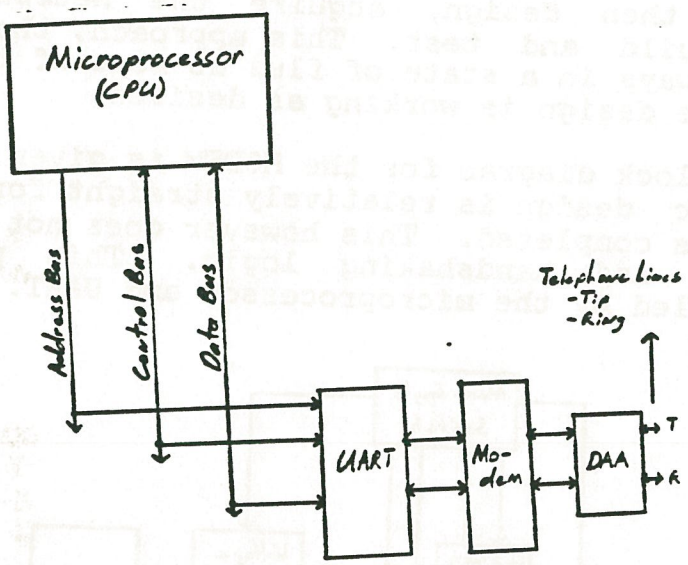
This paper deals with the design of a 300 baud MODEM using frequency-shift-keying(FSK) demodulation and modulation of analog and digital signals. A MODEM is used for communication between computers and/or peripherals when large distances are involved. This is because of the driving capabilities of the electronics and the intrinsic impedance of the the cable. 300 baud is a relatively slow data rate compared to microprocessors which operate in the microseconds. This slow data rate allows for asynchronous design which has an advantage of less control logic and internal timing than a synchronous design.

The design incorporates the use of a microprocessor and a UART, therefore the design is basically limited to the control, modulation, demodulation, and isolation electronics. The microprocessor provides access and control of the MODEM and also allows ease of testing and revision. It also provides communication with the host computer's keyboard and video display. The function of the UART is to provide serial-parallel and parallel-serial conversion so that communication between the microprocessor and MODEM is possible. The UART also performs parity bit checking which is necessary since the MODEM will function using serial asynchronous data with start, stop, and parity bits. The general block diagram of the design is shown in Figure 1.

The carrier medium is a voice-grade public telephone line and therefore additional design considerations are incorporated due to isolation and answer/receive acknowledgements. Once speeds over 600 bps are desired then synchronous and

phase-shift-keying are necessary.

Figure 1



FSK modulation is a term given to the process of converting binary or digital information into an analog signal with specific frequencies which represent a logic 1 and logic 0. The analog equivalent is Mark and Space, respectfully. FSK demodulation works in the exact opposite manner. FSK is generally voltage-frequency conversion and should not be confused with A/D or D/A conversion. The later deals with scaled voltage conversion not voltage-frequency conversion.

PSK modulation requires synchronous data flow since the angle sampled from the incoming analog signal is what determines the digital output. This is called phase-voltage conversion and is inherently faster and more complicated then FSK.

For the 300 baud FSK MODEM the term bits per second(bps) and baud can be used interchangeable since one transmitted data bit corresponds to one binary data bit. This is not true for PSK. This is because PSK sends two dibits per every binary bit. So, for the 1200 baud PSK MODEM only 600 bps are actually sent and in comparison is only twice as fast as a 300 baud FSK MODEM.

The main reason for under taking this project was to gain knowledge and experience in the fields of digital and analog design. The MODEM is a unique design project since it incorporates both types of design. To this end I am using a project approach similar to that of industry. In industry, prior to layout, the design is tested in various ways to proved validation and confirmation of design.

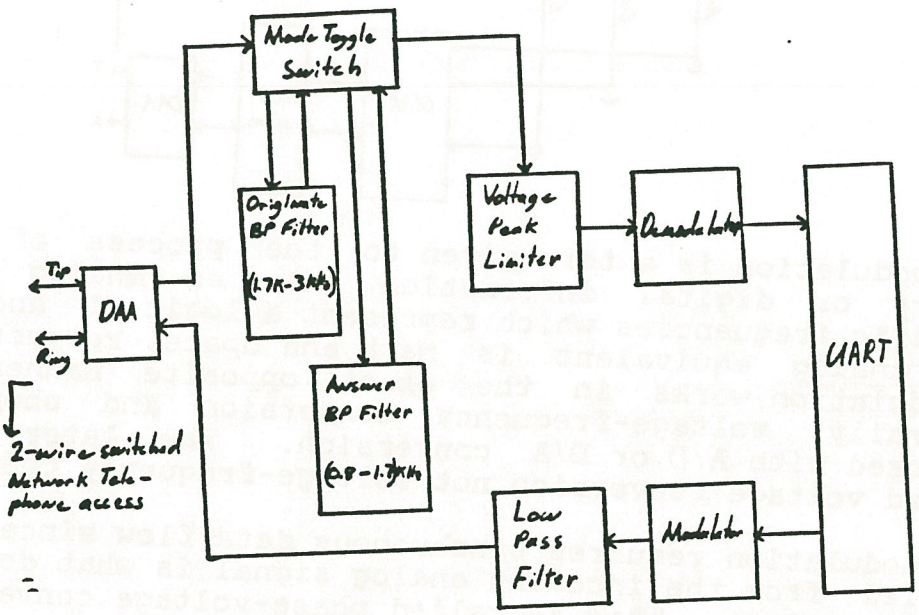
EXPERIMENTAL

The basic approach of this project is to research the function and specifications of a 300 baud MODEM To learn the fundamentals of modulator/demodulator operation as it applies

to MODEM design. Through this enhanced understanding of serial communication then design, acquire the necessary discrete components, build and test. This approach, though extremely general, is always in a state of flux as more of the design is known until the design is working as desired.

The specific block diagram for the MODEM is given in Figure 2. The electronic design is relatively straight forward once the logic design is completed. This however does not include the control logic and handshaking logic. This portion of the design is handled by the microprocessor and UART.

Figure 2

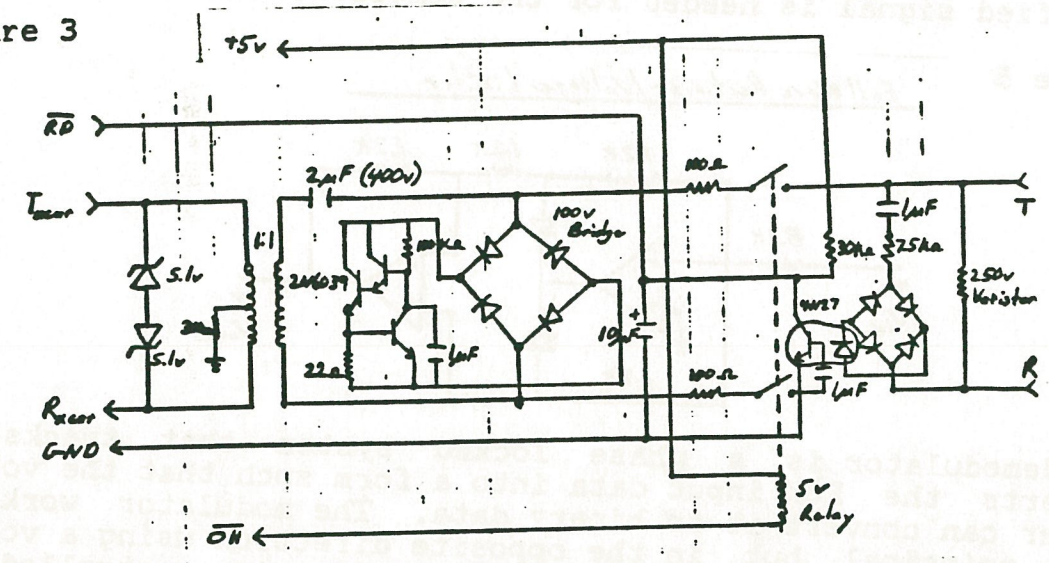


The public telephone lines are called voice-grade because the range of frequencies transmitted is 300 Hz to 3000 Hz which is the mid range of of the human voice. Due to this frequency band the theoretical rate of transmittion is 9600 bps, but 2400 bps is the practical limit. The public telephone lines uses a DC current of approximately 30 mA to determine when a telephone is off-hook due to a DC impedance of 200 ohms or less. Ringing is produced by a 60 - 150 AC voltage voltage across a matching impedance of 600 ohms. These voltages and currents must be isolated from the MODEM electronics along with the possibility of lightning potential. The need for isolation also is required to prevent excessive voltage from the MODEM to the telephone line. The isolation necessary for connection to public telephone lines is regulated by the FCC and the circuit must be registered with them prior to use.

The isolation circuit used in this design is shown in Figure 3. The bridge rectifier and photo-isolator combination is only activated by an AC voltage, as when ringing, then the Ring Detect line is forced low. When the Ring Detect is detected low the the Off Hook line is then forced low causing the relay to close and thereby provides access to and from the MODEM. The second bridge and circuitry provide a current sink so that

the transformer will not become saturated. The center tapped transformer has half the intrinsic impedance so as to allow both transmit and receive at the same. This is called full duplex operation.

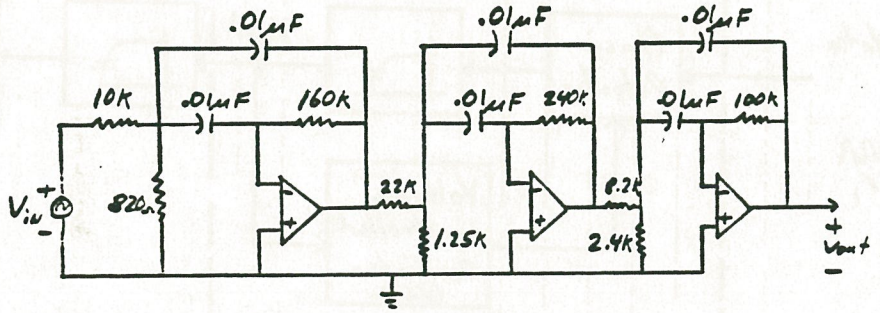
Figure 3



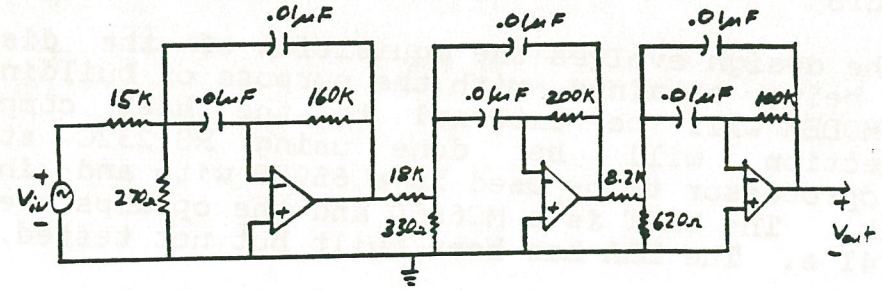
Since the same line is being used to send and receive a bandpass filter is needed such that only the incoming signal is being read and not the transmitted signal. The active RC filters are given in Figure 4. The frequency plot of the filters verses the voltage transfer is given in the APPENDIX along with the method of calculation.

Figure 4 -

Answer Bandpass Filter/Amplifier

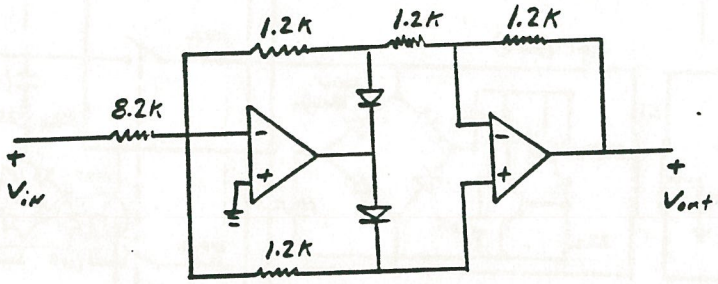


Originate Bandpass Filter/Amplifier



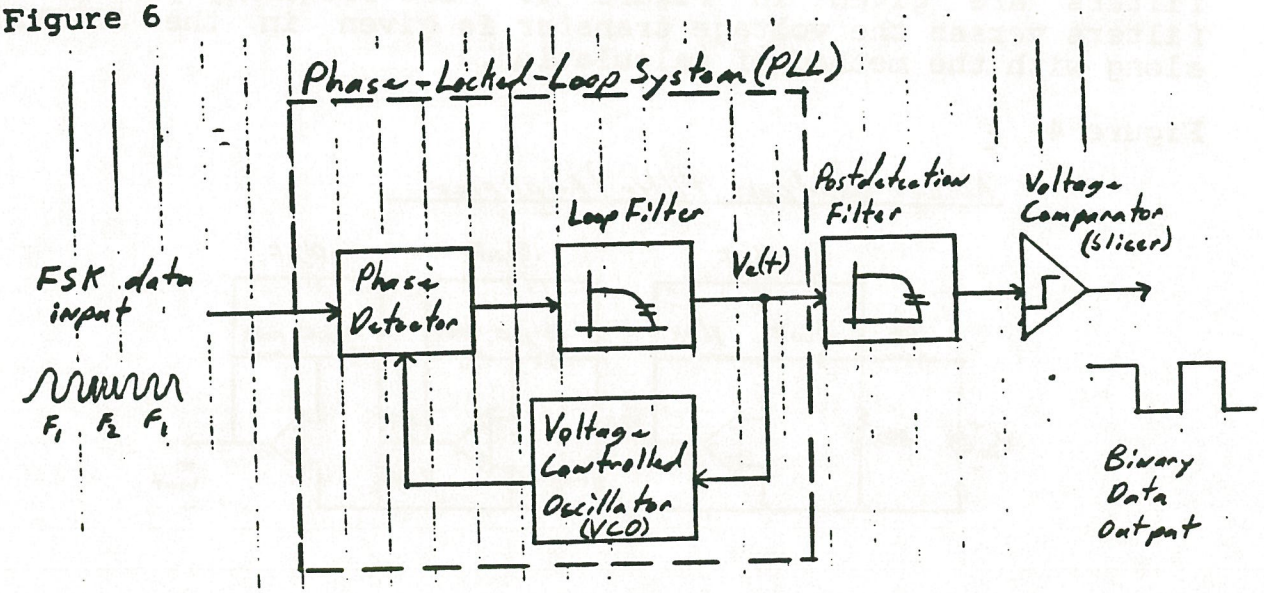
The bandpass filters are also amplifying the signal therefore a voltage limiter is needed. The circuit shown in Figure 5 reduces the incoming signal by approximately a factor of seven and it also performs full wave positive rectification. The rectified signal is needed for the demodulator section.

Figure 5 Full Wave Rectifier/Voltage Limiter



The demodulator is a phase locked system that tracks and converts the FSK input data into a form such that the voltage slicer can convert it to binary data. The modulator works on same principal but in the opposite direction using a voltage controlled oscillator where the timing is controlled by division of the system clock. The demodulator logic diagram is shown in Figure 6.

Figure 6



RESULTS

As the design evolves the aquisition of the discrete devices are being obtained with the purpose of building and testing. The MODEM will be external to the host computer and the connection will be done using RS-232C standards. The microprocessor to be used is a 6502B with and internal 3 MHz clock. The UART is a MC6850 and the op-amps are quad packages of 741's. The DAA has been built but not tested.

To communicate with the microprocessor a keypad and display was designed using a ROM keypad detect program with seven segment LED displays. The keypad is hexadecimal with control switches.

CONCLUSIONS

Once the design has been built, tested, and if needed, revised then the MODEM can be used to communicate using the public telephone lines. The MODEM is a unique electronic device due to both analog and digital design considerations. Due to this dual nature the knowledge gained can be applied to any analog or digital electronic design.

ACKNOWLEDGEMENTS

Darrel Joesph - ADD Electronics
Victor, NY

Dr. Salem - Electrical Engineering Faculty
RIT

Mike Jackson - Microelectronic Engineering Faculty