PMOS STANDARD CELL LIBRARY

by

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ABSTRACT

To allow for a quicker, more efficient design process, a PMOS standard cell library has been designed. The cells designed include; NAND, AND, OR, NOR and Exclusive OR gates, Output Pad Driver, RS Flip-Flop, D-type Flip-Flop, Shift Register, Up-Down Counter, Multiplexor, Decoder, Encoder, Inverter, and a Serial Adder. These cells were all simulated using SPICE, and laid out with ten micron metal gate PMOS design rules.

INTRODUCTION

The four levels of PMOS fabrication make the process quick, simple, and the device characteristics very repeatable. The four masking layers of the process are the diffusion, gate oxide, contact cut, and metal. It is a logical advancement to design and layout a standard cell library for this well established process.

In the past, each time a student wanted to design and fabricate a circuit, he would start from scratch and design, simulate, and layout each gate. This required a significant amount of ground work before a larger circuit could be designed. Not only was this method of design much more time consuming, but it also leads to inefficient or none functional basic gates. By repeatedly simulating each gate, the optimum pull-up and pull-down gate dimensions were determined. There were two basic criteria which were used to define the optimal ratios. First, the logic high and logic low voltage levels must be within acceptable ranges. Second, the pull-up and pull-down times must be approximately equal. In the past, such simulation iterations were often too time consuming to be practical. Thus larger designs may not of functioned due to simple gate malfunctions. By using standard cells, the designer can spend more time doing the circuit design, and be certain that the basic cells being used are functional.

The designs were all laid out with RIT's ten micron metal gate PMOS design rules. To facilitate ease of layout, certain criteria were upheld while designing the cells. The basic gate cells were all made the same height to allow for easy

placement. Larger cells were made to be multiples of this standard height. Power and ground ports are available at the top and bottom, while signal ports are available on both sides of the cell. These criteria make the chip much easier to layout, and also make for a more dense design. The cells were laid out on ICE integrated circuit editor. The minimum feature size is ten microns, with a gate overlap of ten microns, minimum metal and diffusion width of 30 microns, and minimum contact size of ten microns square.

EXPERIMENTAL

The majority of the development time was spent thoroughly simulating each of the designed cells. The schematics were done on a Mentor Graphics CAD Design station, and consequent simulations performed using MSPICE. The transistor model used for simulation was derived from transistors previously fabricated in the labs at RIT. The simulations model used is as follows:

Substrate doping	= 3.81E14 /CC
Surface Mobility	= 80.77 cm**2/V-S
Zero Bias Threshold Voltage	= -2.0 volts
Channel Length Modulation	= .0145 1/V
Source and Drain Resistance	= 60.0
Transconductance	= 4.83E-6 A/V**2
Surface State Density	= 8.0E11 /cm**2
Oxide Thickness	= 580 angstroms
Junction Depth	= 1.17 uM
Gate to Source Capacitance	= 560 pF
Gate to Drain Capacitance	= 560 pF

Each of the simulations was performed at twenty-seven degrees centigrade.

RESULTS/DISCUSSION

The simulation of the cells gave very favorable results. A NOR gate has a rise time of approximately one micro-second, when simulated at fifteen volt supply rails. An exclusive OR gate has a rise time of approximately two micro-seconds. To achieve suitable logic high and logic low output voltage levels, and achieve symmetrical rise and fall times the length to width ratio of the pull-up and pull-down transistors must be made unequal. Each transistor is characterized by its length to width ratio, and a gate is characterized by the ratio of the pull-up to pull-down transistors. The optimum ratio of an inverter was found to be 20:1, 4:1 for a NAND gate, and 12:1 for a NOR gate. Figure 1 shows the schematic of a NOR gate, a NAND gate, and an Inverter. All of the more complicated cells designed were made up of these three gates.

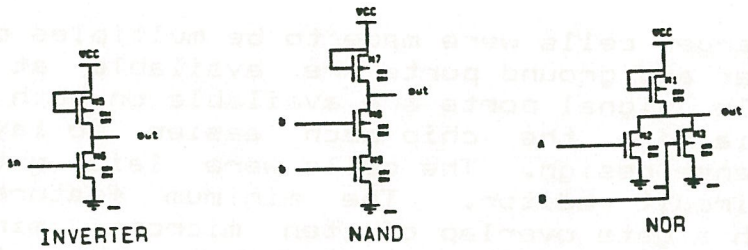

Figure 1. Schematic Representation of the basic gates

The simulation of an inverter yields a logic low output of -.6 volts, and a logic high output of -14.0 volts. These voltages are well within acceptable ranges to control later stages. Figure 2 is an example of a library data sheet, which contains the schematic, and a selected simulation result.

The basic gate height was 140 microns. All of the basic gates were stretched to be this height. The power and ground ports come out the top and bottom, while the signal ports come out each side. The larger gates were all laid out to be multiples of this standard height. Attached is an example of a library data sheet. It contains the cell name, the pmos implementation schematic, and the results from a simulation.

CONCLUSION

A PMOS standard cell library was designed and laid out with 10uM metal gate design rules. The cells designed include; NAND, AND, OR, NOR and Exclusive OR gates, Output Pad Driver, RS Flip-Flop, D-type Flip-Flop, Shift Register, Up-Down Counter, Multiplexor, Decoder, Encoder, Inverter, and a Serial Adder. These cells were all simulated using SPICE, and laid out with ICE integrated circuit editor.

REFERENCES

1) Millman, Jacob, "Microelectronics", McGraw-Hill Books, New York, 1979.

2) Taub, Herbert, "Digital Integrated Electronics", McGraw-Hill Books, New York, 1979.

LIBRARY DATA SHEET EXAMPLE

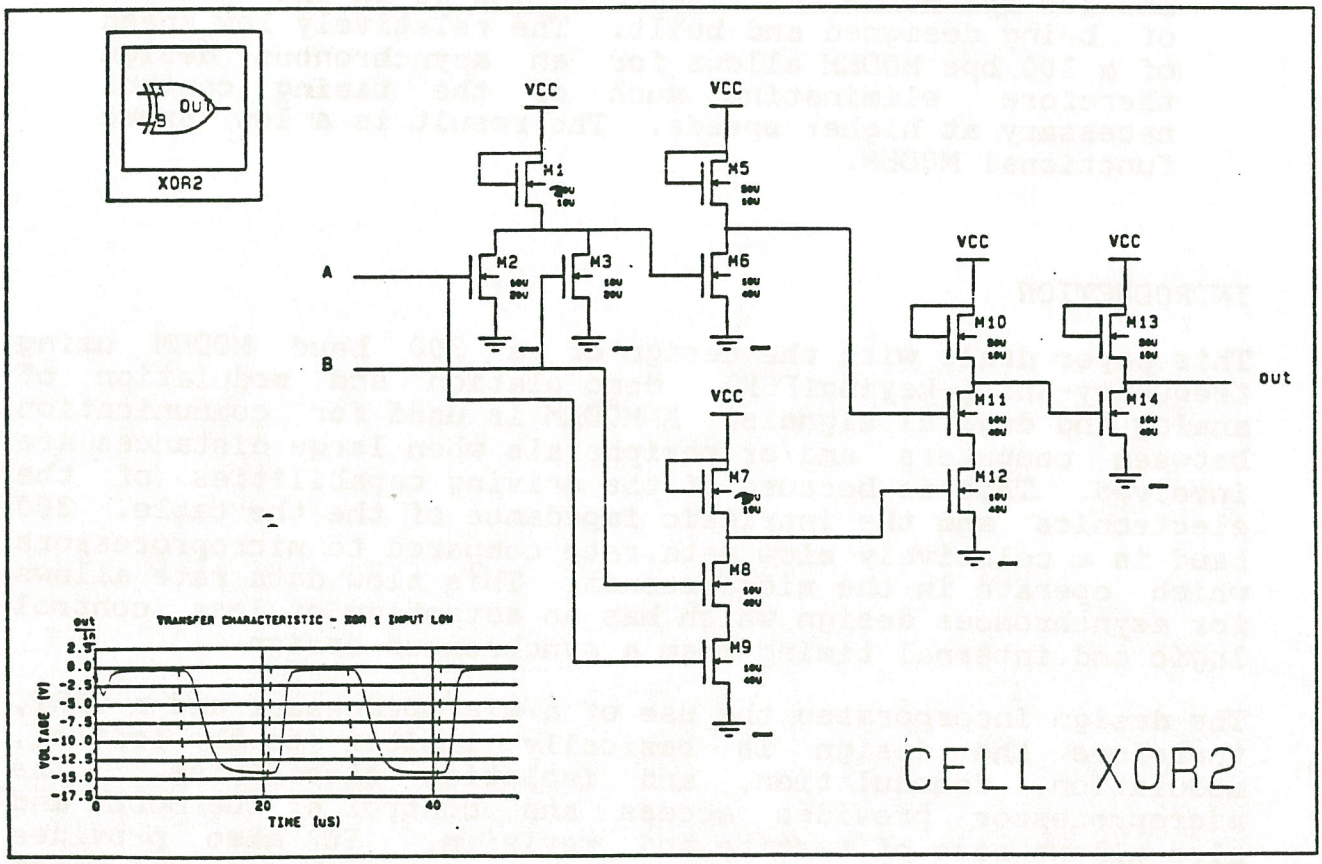

Figure 2