PMOS OPERATIONAL AMPLIFIER EVALUATION

BY

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ABSTRACT

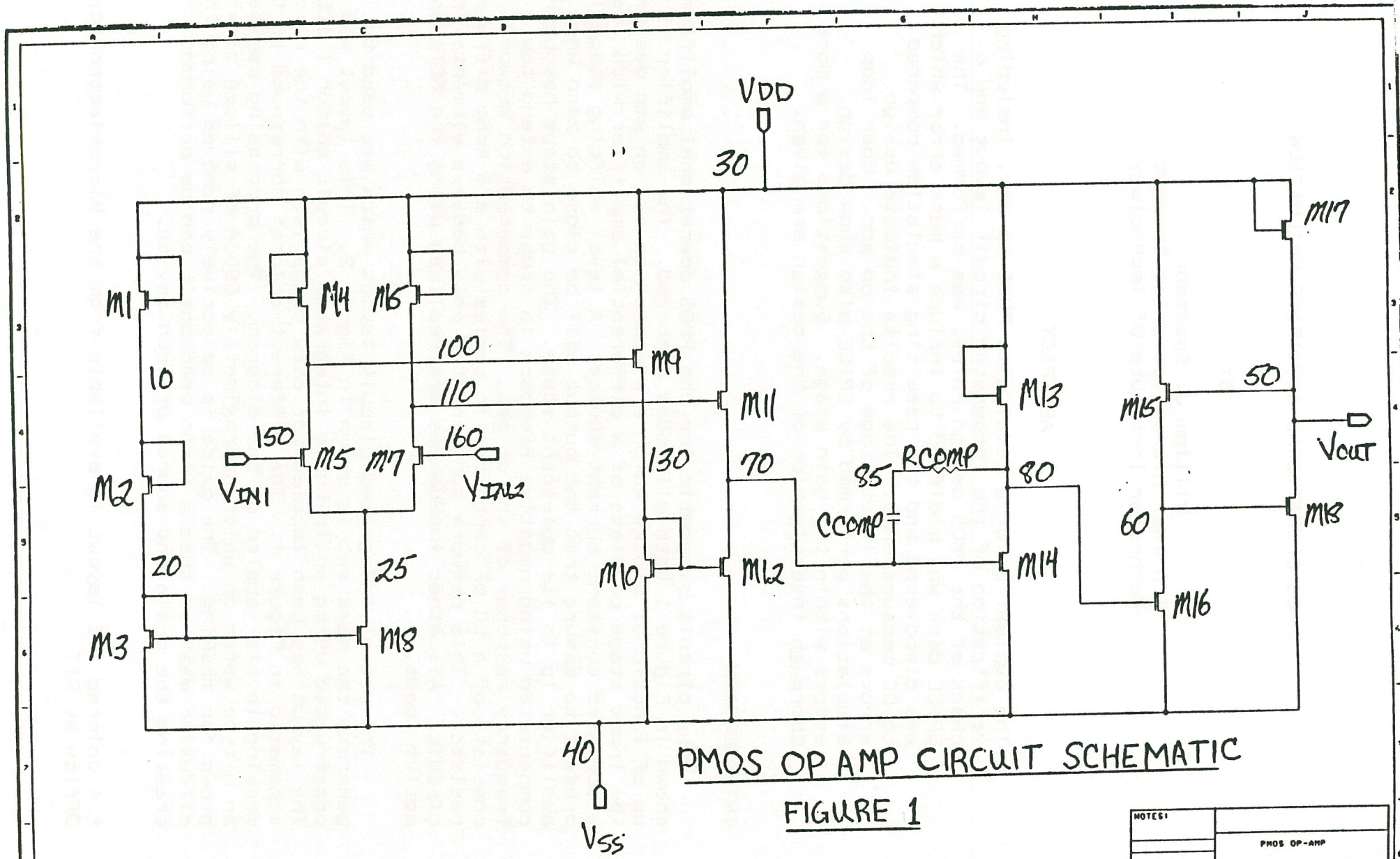
The evaluation of a metal gate PMOS op amp, including verification of the integrated circuit layout and a check of the PMOS design rules, was performed. The SPICE deck was modified to include a mask error which was discovered and the resulting simulation compared to DC measurements. The results indicate design errors at the input stage of the op amp. Open loop simulations performed by SPICE also show design errors within the gain stage. Suggestions for a more thorough investigation of the design are given.

INTRODUCTION

The circuit schematic for the PMOS operational amplifier is shown in Figure 1 with all nodes numbered. The amplifier is made up of functional blocks which are common to all op amp designs. The input stage consists of a differential amplifier with its associated constant current source. A level shifting stage is present to assure that the output will be close to zero when the amplifier is in its quiescent state. The gain stage has been compensated using negative feedback in order to extend the frequency response of the op amp. The compensation network consists of a 50 pF capacitor in series with a 6 kohm diffused resistor. This network contains the only passive elements in the circuit. All other impedances are realized using the FETs as active loads.

The actual integrated circuit layout which was used to generate the mask set is shown in Figure 2. This layout was constructed using an in-house integrated circuit editor (ICE). The layout has been labeled for easy comparison with the circuit schematic in Figure 1. The different colors* correspond to the masking levels labeled on the diagram. The processing begins with an n-type wafer on which approximately 6000A of silicon dioxide is grown for masking. The oxide is selectively removed using the diffusion mask so that a boron predeposit can be performed creating the drain and source of each device.

* A colored ICE layout is available from the Microelectronics Office at RIT

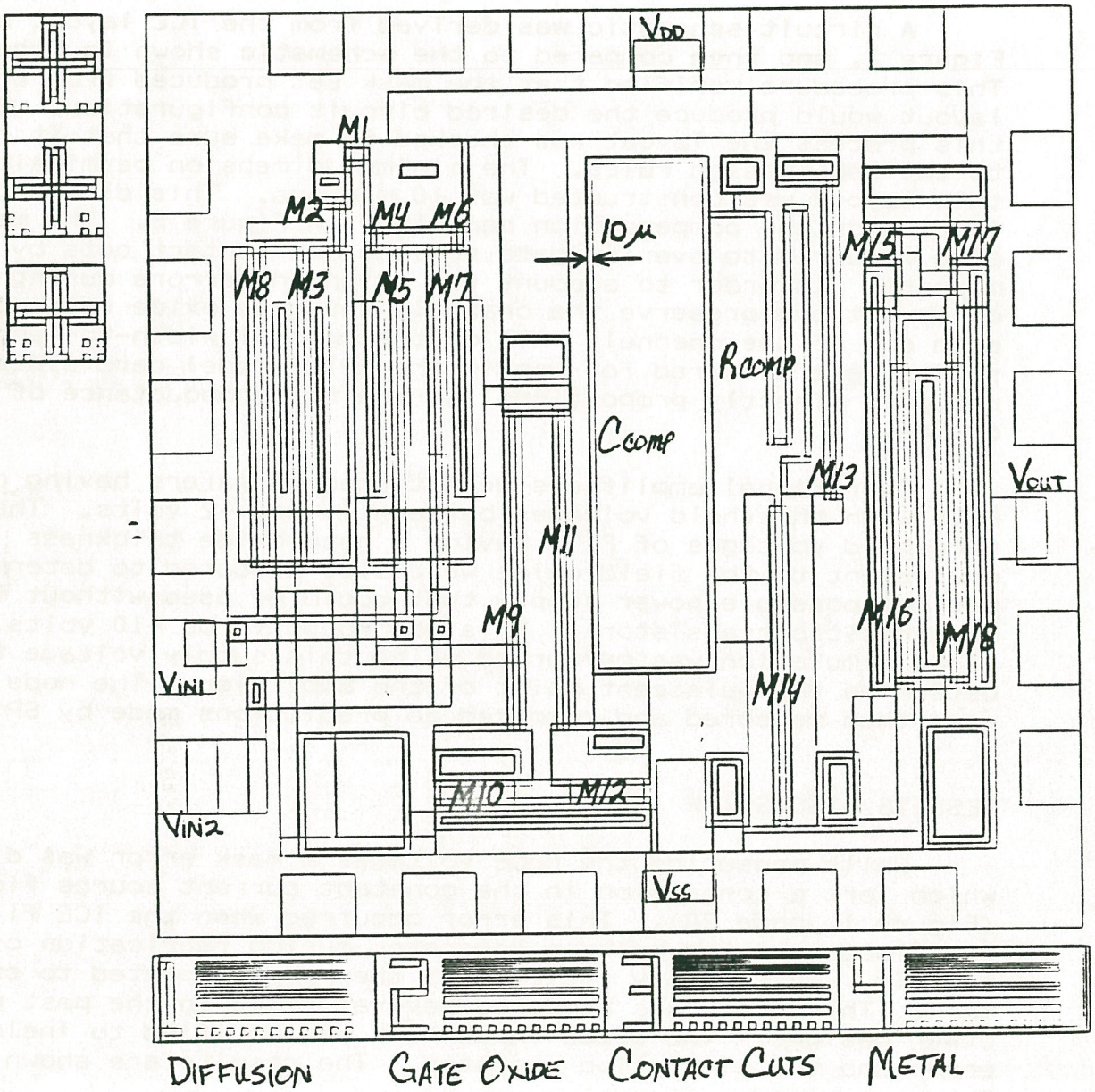


PMOS OP AMP CIRCUIT SCHEMATIC

FIGURE 1

NOTES:	
	PMOS OP-AMP
	J. ERWIN 4/18/05
	SHEET 1 OF 1 REV

* ALL TRANSISTORS ARE PMOS ENHANCEMENT MODE DEVICES



PMOS OPERATIONAL AMPLIFIER ICE LAYOUT

FIGURE 2

This predeposit also forms the 6 kohm resistor. The remaining oxide is removed following the predeposit, and the boron is driven in while the field oxide is grown (approximately 6000A). This field oxide is removed from the intended gate regions using the gate oxide mask, and about 500A of gate oxide is grown. The contact cut mask is used to cut through the field oxide in order to make electrical contacts to the diffused areas. Finally the entire wafer is coated with aluminum and the interconnections are defined using the metal mask.

EXPERIMENT

A circuit schematic was derived from the ICE layout shown in Figure 2, and then compared to the schematic shown in Figure 1. This procedure verified that the mask set produced from the ICE layout would produce the desired circuit configuration. During this process the layout was checked to make sure that it conformed to the PMOS design rules. The minimum dimension permissible when this layout was constructed was 10 microns. This dimension is labeled on the compensation capacitor in Figure 2. The metal was also required to overlap gate regions and contact cuts by 10 microns. In order to account for alignment errors during the gate oxide cut and preserve the channel, the gate oxide was indented at each end of the channel. All of the channel width-to-length ratios were measured for use in the SPICE model card since this ratio is directly proportional to the transconductance of each device.

Operational amplifiers were tested on wafers having discreet FETs with threshold voltages between -1 and -2 volts. The threshold voltages of FETs having a gate oxide thickness equivalent to the field oxide were also measured to determine the maximum possible power supply that could be used without turning on parasitic transistors. This was found to be -10 volts. A SPICE simulation was performed using this supply voltage to determine the quiescent point of the amplifier. The node voltages were then measured and compared to predictions made by SPICE.

RESULTS/DISCUSSION

While measuring the node voltages a mask error was discovered which left a connection in the constant current source floating (Figure 1, node 20). This error occurred when the ICE file was down-loaded to the pattern generator during fabrication of the reticle. This faulty reticle was then photorepeated to create the mask. This error has happened several times in the past with other designs. The SPICE input deck was modified to include this error and the simulation repeated. The results are shown in Table I.

Table I
Comparison of Predicted and Measured Node Voltages

Node	SPICE (v)	Measured (v)
10	-1.03	-1.43
20	0	+3.32
21 *	+4.99	+3.70
25	+4.82	+3.66
30 (VDD)	-5.00	-5.00
40 (VSS)	+5.00	+5.00
50 (VOUT)	+0.44	+0.92
60	+2.65	+3.87
70	+5.00	+5.00
80	+2.88	+3.58
85	+2.88	+3.56
100	+4.72	+4.64
110	+4.72	+4.56
130	+5.00	+5.00
150 (VIN1)	0	+2.55
160 (VIN2)	0	+3.94

* Floating node at the gates of M3 and M8

The measured voltages agree quite well with SPICE's predictions with the exception of the voltages at the inputs and at node 20 in the constant current source. These deviations indicate design flaws within the differential amplifier and the constant current source. No other measurements could be performed, but SPICE was used to simulate the open loop response of the amplifier. A DC gain of one was predicted which rolled off significantly at one kilohertz. This data indicates further design errors within the compensated gain stage.

CONCLUSION

The evaluation of the PMOS operational amplifier is by no means complete. The circuit deserves a more in-depth analysis. This analysis would be greatly facilitated by breaking the circuit up into the functional blocks. Each block could then be simulated, fabricated, and tested seperately to give more insight into the operation of the amplifier as a whole. Once the individual performance of these blocks has been optimized, they can be reassembled to complete the design, and testing of the complete circuit may be resumed.

ACKNOWLEDGEMENTS

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