A FIVE MICRON, SELF-ALIGNED, POLYSILICON GATE CMOS PROCESS DESIGN

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ABSTRACT

The design of a five micron, polysilicon gate, CMOS process is discussed. A p-well approach was used with a <100> oriented n-type substrate as the starting material. Calculations of the threshold adjustment dose and desired doping level of the p-well were based on a desired threshold voltage of -0.8 volts for the p-channel transistor and 0.8 volts for the n-channel device. The desired doping levels of the sources and drains were based on minimizing the parasitic resistances and capacitances associated with a MOS transistor. SUPREM II was used to determine the implant/drive cycles necessary to obtain the required doping profiles and to simulate the oxide growths, sheet resistances, and junction depths of the various levels. Simulation of the electrical characteristics of the NMOS and PMOS devices and the CMOS inverter was done using SPICE.

INTRODUCTION

First introduced in 1963 by Wanlass and Sah [1], CMOS provides both n-channel and p-channel MOSFETs on the same chip. Presently, CMOS is the dominant VLSI technology in the semiconductor industry due mainly to its low power consumption. In addition, CMOS processes have been simplified so that NMOS and CMOS technologies are now comparable in complexity. In fact, modern complex CMOS circuits are designed with more NMOS than PMOS devices so as to enhance the effective speed of the circuit. Another desirable quality of CMOS circuits is the lower susceptibility to noise since the output voltage makes a full swing between the positive supply and ground. However, CMOS is not without its disadvantages. CMOS circuits are vulnerable to latchup and, when compared to NMOS, are slower in speed.

Latchup is a condition where high currents are conducted between the positive voltage supply and ground causing the CMOS circuit to cease functioning. The CMOS inverter structure produces parasitic lateral pnp as well as lateral and vertical npn transistors. The collectors of each of these bipolar transistors feed each others' bases and together make up a thyristor (pnpn device). A crossection of a CMOS inverter along with a model of the thyristor is shown in Figure 1. If the thyristor becomes biased appropriately, an undesireable effect occurs in the CMOS circuit. The collector current of the pnp supplies base current

to the npn, and vice versa in a positive feedback arrangement. A sustained current then exists between the terminals of the thyristor. That is, the current becomes latched. This latchup can only be terminated if the power to the thyristor is interrupted.

The work reported here is the design of a seven level, 5um CMOS process that requires ion implantation and chemical vapor deposition (CVD) capabilities. A p-well approach was used for two reasons. First, it provides balanced performance of the p-channel and n-channel devices because of two opposing factors. The n-channel transistors have higher conductivity than the p-channel transistors. However, this is compensated for by the heavy doping of the p-well as compared to the n-type substrate. Second, the p-well method allows for easier threshold voltage adjustments. Polysilicon was used as the gate material since it is compatible with high temperature (>600 C) process steps as opposed to the commonly used aluminum. In addition, polysilicon allows the use of a self-aligned gate process which, in effect, reduces the overlap capacitances. The process also includes p+ and n+ guard rings which serve as channel stops. These guard rings also prevent latchup by diverting minority carriers from creating the lateral IR drops needed to bias the thyristor. Threshold voltages of 0.8 volts and -0.8 volts for the n-channel and p-channel devices, respectively, are desired. These low threshold voltages allow the circuit to be operated at relatively low voltage supplies and provide a higher drain current for a given drain voltage.

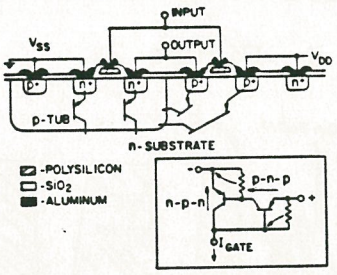

Figure 1. Structures to illustrate lachup in CMOS [1].

EXPERIMENT

The main objective in the design of a CMOS process is to match the threshold voltages (magnitudes) and transconductance parameters of the n- and p-channel devices. This allows for optimum switching characteristics and low power consumption in the circuit. The doping level of the p-well determines the threshold voltage of the n-channel transistor, while the threshold adjust implant dose determines the threshold voltage of the p-channel device. Threshold voltages of 0.8 volts for the NMOSFET and -0.8 volts for the PMOSFET were used to determine the desired p-well doping level and threshold adjust implant dose, respectively. The doping levels of the sources and drains were based on minimizing the parasitic resistances and capacitances

associated with a MOS device. Process modeling was carried out using SUPREM II. This involved determining the implant/drive cycles necessary to obtain the required doping profiles and simulating the oxide growths, sheet resistances, and junction depths of the various levels.

Listed below are the design rules of the 5um CMOS process. Actual mask dimensions should be designed to compensate for predicted undercutting from the various isotropic etch process steps and forecasted impurity redistribution during the various drive cycles. Source and drain dimensions were made relatively large to allow the use of 5x5 contacts. All values are in microns.

- P-Well: L=60, W=30
- All Contacts: L=5, W=5
- Channel Length (NMOS and PMOS): L=5
- Channel Width of PMOS = 1.8 x Channel Width of NMOS
  Actual channel widths can be varied.
- P+ and N+ Source/Drain: L=10, W=10
- P+ and N+ Guard Rings: L=10
  Guard rings are moats that surround the NMOS and PMOS devices. Therefore, the following spacing criteria are specified.
- P+ Guard Ring to N+ Source Spacing: L=5
  The spacing width is defined by the p-well since the P+ guard rings should lay along the edge of the p-well.
- N+ Drain to P+ Guard Ring Spacing: L=10
- P+ Guard Ring to N+ Guard Ring Spacing: L=10
- N+ Guard Ring to P+ Drain Spacing: L=10, W=5
- P+ Source to N+ Guard Ring: L=5, W=5

See device crossection in Figure 2.

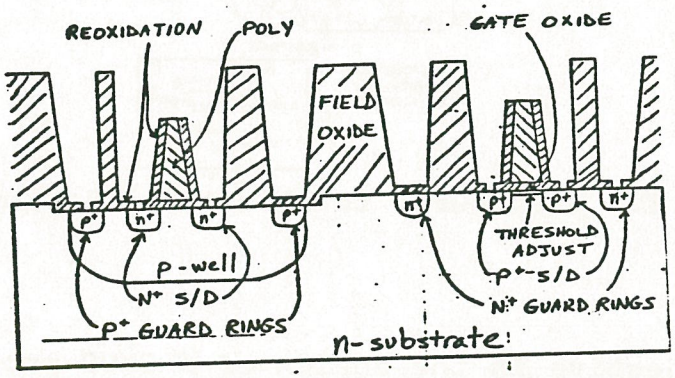

Figure 2. Crossection of final device.

RESULTS

An outline of the 5um, p-well CMOS process is listed below and a crossection of the final device is shown in Figure 2. The process modeling was based on an assumed oxide charge density of 5.0E11 /cm2 and a desired threshold voltage magnitude of 0.8 volts for each transistor. Since the CVD equipment has not yet

been qualified, the polysilicon deposition parameters needed to obtain the desired 0.5um film have not been defined. The same is true for the polysilicon/gate oxide etch. In addition, the desired beam currents for the various ion implantations need to be determined once the implanter is ready for use. The beam current should not be so high as to cause charring of the masking photoresist.

The major process steps are:

1. Obtain 3-5 ohm-cm, (100) orientation, n-type wafers.
2. Grow 500 Ang. well oxide. Use wet O2 for 25 min. at 900 C.
3. Coat, softbake, develop, and hardbake resist. (LEVEL 1)
4. Ion implant 2.5E13 ions/cm2 of Boron at 150 keV. (P-WELL)
5. Etch well oxide in p-well region. Then strip resist.
6. Drive in p-well: Do a dry oxidation for 60 min. at 1150 C. Switch to nitrogen for 430 min. Switch to wet O2 for 50 min. to grow a total of 6500 Ang. field oxide.
7. Coat, softbake, develop, and hardbake resist. (LEVEL 2)
8. Etch field oxide until wafer pulls dry. (~13 min.)
9. Strip resist.
10. Grow gate oxide. Use dry O2 for 50 min. at 1000 C. Switch to nitrogen and anneal for 20 min.
11. Ion implant 6.1E11 ions/cm2 of Boron at 30 keV. (Threshold Adjustment)
12. Do a 5000 Ang. CVD deposition of polysilicon.
13. Coat, softbake, develop, and hardbake resist. (LEVEL 3)
14. Etch polysilicon and gate oxide. (preferably anisotropic)
15. Strip resist.
16. Do a reoxidation in dry O2 for 50 min. at 1000 C.
17. Coat, softbake, develop, and hardbake resist. (LEVEL 4)
18. Ion implant 1.0E15 ions/cm2 of Boron at 30 keV. (P+ Source/Drain and Guard Ring)
19. Strip resist.
20. Coat, softbake, develop, and hardbake resist. (LEVEL 5)
21. Ion implant 8.0E15 ions/cm2 of Arsenic at 160 keV. (N+ Source/Drain, Guard Ring, and Poly Doping)
22. Strip resist.
23. Activation/Anneal in nitrogen at 1000 C for 30 min.
24. Coat, softbake, develop, and hardbake resist. (LEVEL 6)
25. Etch contacts in Buffered HF for ~1 min. Strip resist.
26. Evaporate ~3000 to 5000 Ang. of Aluminum on front side.
27. Coat, softbake, develop, and hardbake resist. (LEVEL 7)
28. Etch Aluminum in wet Al etch at 39 C for 2 to 4 min.
29. Strip resist.
30. Sinter wafer at 450 C in forming gas for 30 min.

The data obtained from SUPREM II is listed Table 1. The predicted junction depth of the N+ source and drain is about half that of the P+ source and drain for two reasons. First, the p-well is doped more heavily than the n-substrate. That is, the background concentration for the N+ source and drain is higher than that for the P+ source and drain. Second, arsenic has a lower diffusivity than boron and, therefore, is not driven as deep as boron for a constant anneal time and temperature. In addition, the sheet resistance of the P+ regions is much higher

than that of the N+ regions because the N+ doping level is a factor of six higher than that of the P+ level.

It is more likely than not that the assumed oxide charge density of 5.0E11 /cm2 is not totally accurate. Therefore, the graphs in Figures 3 and 4 were generated to allow for easy adjustment of p-well doping and threshold implant based on the actual charge density and a threshold voltage magnitude of 0.8 volts.

SPICE was used to model the electrical characteristics of NMOS and PMOS transistors and the CMOS inverter. Among the characteristics investigated were the rise and fall times of the output voltage signal and the current coming out of the 5 volt supply. All the data obtained from SPICE is listed in the appendix along with the SPICE input decks and calculations of SPICE input parameters.

SUPREM II DATA FOR 5um CMOS PROCESS

REGION	SURFACE CONC. (cm-3)	Xj (um)	SHEET RHO (ohm/sq)	OXIDE DATA TYPE	OXIDE DATA THICKNESS (Ang.)
P-WELL	8.04E16	5.00	956	WELL	508
THRESHOLD ADJUST	2.70E16	0.38	29,710	FIELD	6517
P+ SOURCE/ DRAIN	3.79E19	0.68	123		
P+ GUARD RING	3.79E19	0.55	113	GATE	488
N+ SOURCE/ DRAIN	2.30E20	0.32	24.2	REOX	488
N+ GUARD RING	2.30E20	0.34	24.1		

TABLE 1

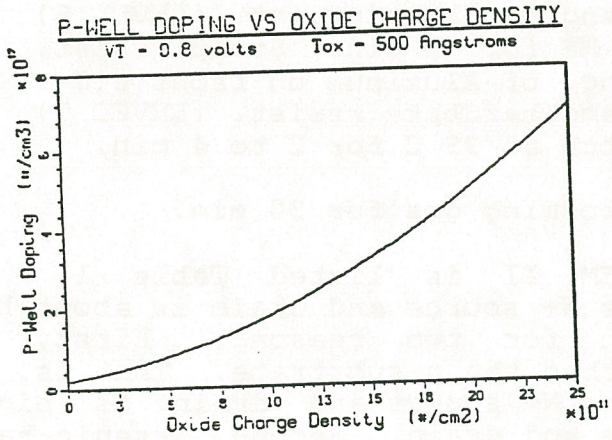

Figure 3

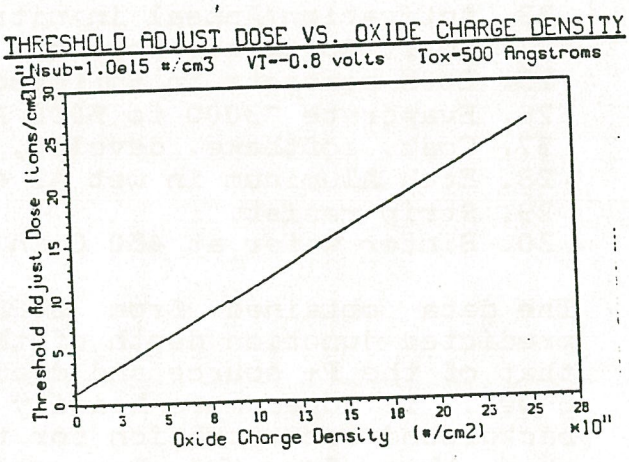

Figure 4

CONCLUSION

A seven level, 5um CMOS process has been designed using an n-substrate/p-well structure. Process modeling was carried out using SUPREM II and SPICE was used for electrical simulations. Because no devices were fabricated, an assumption of oxide charge density was necessary. However, the process can easily be adjusted to account for any level of oxide charge density by adjusting the p-well doping and threshold adjustment implant dose accordingly.

ACKNOWLEDGEMENTS

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REFERENCE

[1] Sze, S. M., VLSI Technology, McGraw-Hill Book Company, New York, 1983.