PROCESS DEVELOPMENT FOR A MULTI-LEVEL METAL PROCESS

By

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ABSTRACT

Preliminary work on multi-level metal processes using photosensitive polyimide, Kodak 820 resist, Shipley 1400-27 resist, Pyralin polyimide, spin-on glass and evaporated silicon monoxide was reviewed. The results of this analysis yielded some problem areas which were the foundation for this work. Results from an aluminum/spin-on glass/aluminum process show that spin-on glass is a viable dielectric material and that some work is needed to optimize the process.

INTRODUCTION

Cost efficiency is an important ingredient in the business world including the semiconductor industry. Production costs of an integrated circuit are directly related to the packing density obtainable in the process. Processes have evolved to manufacture devices with micron dimensions yet the metallization techniques lagged behind, causing a limitation in the packing density when single level metal was used. To solve this problem, multi-level metals were introduced which allowed for a major increase in packing density. This is illustrated in Figure 1 below which compares the same circuit with single level metal to a two level metal design. The two level metal layout consumes approximately forty percent less area than the single level design

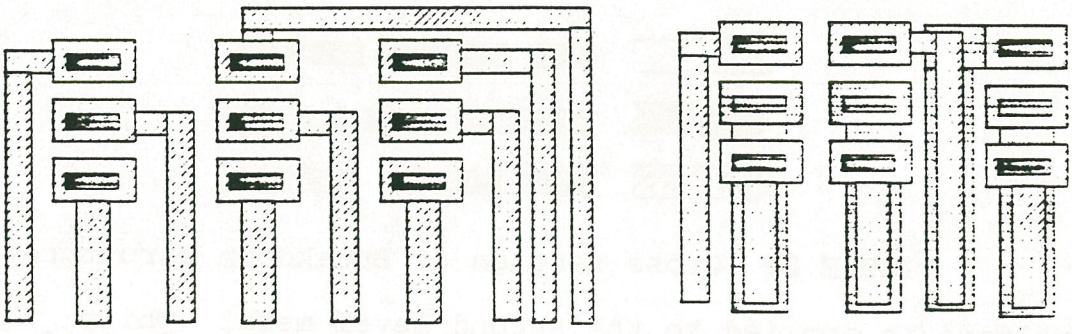


FIGURE 1: Comparison showing savings in chip real estate for single level vs. 2-level metal.

An added benefit is the increase in circuit performance with regards to the time constant involved. A single-level metal involves the routing of metal traces through long stretches in order to make all connections without crossing paths. With the advent of mutli-level metal, traces were decreased in length which decreased the response time of the circuit [1]. This is shown below in Equation 1:

$$RC = (rho * L * K) / T \qquad (1)$$

where rho is the sheet resistivity of the metal trace, L is the length of the metal trace, K is the dielectric constant and T is the dielectric thickness.

In order to use a multi-level metal process, glasses and resists were utilized as the dielectric layer. The properties of these dielectrics also affects the performance of the circuit. For example, the breakdown voltage of the insulator must be able to withstand the voltages required to operate the device. The ability to etch via contacts through the dielectric so that connections can be made reproducibly is also important. Other important parameters include step coverage and the uniformity of the insulator across the wafer and adhesion of the dielectric to the substrate and first layer metal.

Test structures are crucial in the evaluation of a new process and its usefulness. Two parameters of interest are dielectric breakdown and via resistance. This meant that test structures had to be included which would test these properties In order to accomplish this, the breakdown of the dielectric will be tested using the device cross-section shown in Figure 2.

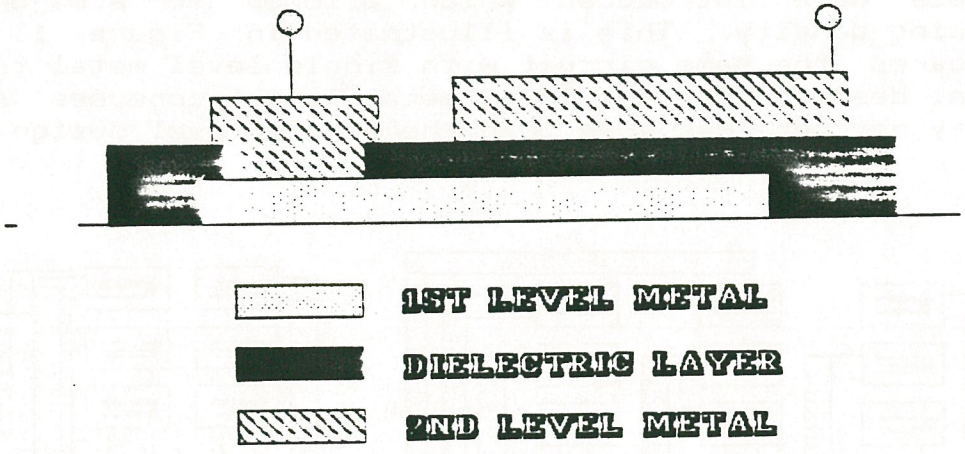


FIGURE 2: Cross section of Breakdown structure.

A voltage is applied to the second level metal while the first level metal is connected to a ammeter. When a predetermined current is measured in the circuit, this indicates the dielectric breakdown voltage which is equivalent to the applied voltage to the second level metal.

A second property is the ability to etch via contacts into the dielectric layer to allow interconnection between the two levels of metal. To test vias incorporates the use of a via chain. A via chain consists of alternating first and second level metal runs connected through vias. A via chain cross-section is shown in Figure 3 below:

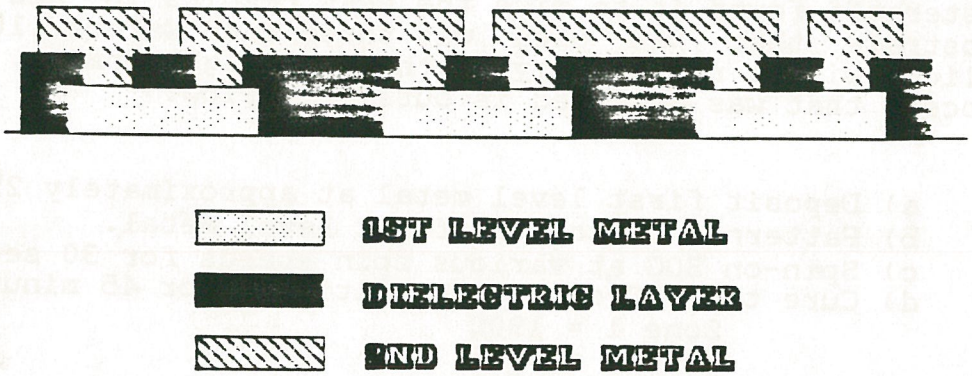


FIGURE 3: Cross section of Via Resistance structure.

By connecting enough of these vias into a chain formation, the resistance can be measured. It can be assumed that the resistance is mainly due to the vias and therefore can determine the single via resistance by dividing the total resistance by the number of vias. The use of different size vias will result in a change in the via resistance of the chain if all other parameters remain the same. The via resistance of the single via can be used to minimize the voltage loss through the via. For example, if the 8um via offers a resistance ten times higher than the 12um via, it would be wise to design 12um vias to minimize the voltage loss.

Previous work was performed by other RIT students to determine a two-level metal process [2,3]. The work was beneficial since they do indicate problem areas which were encountered by these students. Chris Knaus incorporated photosensitive polyimide as the dielectric layer. This process resulted in vias with extremely high resistance which would nullify their practical use in a multi-level design. Eric Westerhoff attempted to compare various dielectric materials to determine which one worked the best. The experimental work uncovered many problem areas with the main one being adhesion failures of the dielectric material during second level metal deposition.

EXPERIMENTAL

The process design involved much consideration as to the decision of which dielectric material to use. The final two candidates were ACCUGLASS Spin-on Glass 103 [4,5] and Kodak 820 Resist [6]. The final decision was to use the Spin-on Glass since Eric Westerhoff found it to give the best results in his work. The substrate that was used was three inch wafers (100) of n-type silicon with a resistivity of three to eight ohm-cm. The basic process that was utilized is outlined below:

a) Deposit first level metal at approximately 2500A.
b) Pattern and etch the first level metal.
c) Spin-on SOG at various spin speeds for 30 seconds.
d) Cure the SOG on 3-zone belt oven for 45 minutes at:
   Zone 1 = 190C
   Zone 2 = 300C
   Zone 3 = 190C
e) Pattern and HF etch the vias.
f) Deposit second level metal at approximately 2500A.
g) Pattern and etch the second level metal.

The spin-on glass was coated at five different spin speeds in order to investigate the effect of dielectric thickness vs. breakdown voltage. The spin speeds used are given below in Table 1 with the approximate thickness obtained from the data sheets [5].

Spin Speed (rpm)	Thickness (Angstroms)
1000	2000
2000	1680
3000	1350
4000	1150
5000	1020

TABLE 1: Spin speeds used to coat SOG layer.

The test design consisted of nine breakdown structures and four via chains with 600 vias per chain. The dimensions of the structures are given below in Table 2.

Via Chain Dimensions	Breakdown Dimensions	
5 um	5 um	15 um
8 um	8 um	20 um
10 um	10 um	30 um
12 um	12 um	40 um
		50 um

TABLE 2: Dimensions of the test structures.

RESULTS

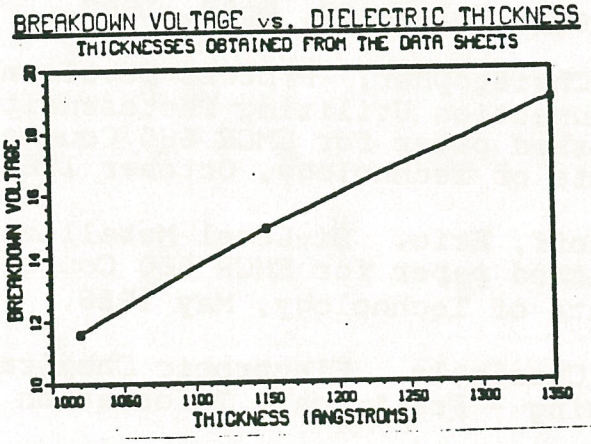
Final test of the devices produced mixed results. The via chains were tested and the resistances were in the five megohm region. This can be attributed to the fact that the first level metal was deposited onto the silicon substrate therefore providing the large resistance measured. The original process should have included a oxidation step so that the first level metal is insulated from the silicon substrate.

The breakdown voltage structures produced results that were expected from the start. Of the five different spin speeds, two of them (1000 and 2000 rpms) did not work. This can be attributed to the fact that very low spin speeds typically result in nonuniform film coating which would pose a problem with step coverage in a two level metal process. The other three spin speeds provided adequate coverage and allowed for the measurement of the breakdown voltage. The measured data is given below in Table 3:

Breakdown Structure Dimension	Spin speed (rpms) 3000	4000	5000
50 um	21.0 V	15.6 V	12.8 V
40 um	16.4 V	14.4 V	14.0 V
30 um	17.4 V	18.0 V	11.4 V
10 um	21.4 V	11.6 V	8.2 V
Average	19.0	14.9	11.6

TABLE 3: Breakdown voltage data.

The breakdown voltages listed above are plotted below in Graph 1:



GRAPH 1: Breakdown voltage vs. dielectric thickness

Many problems were encountered during the production of the mask set. The third mask that was used had some major problems in that it was yellow, the geometries did not fully resolve and some

geometries were missing due to a pattern generator problem. To compensate for this, it was necessary to overexpose and overdevelop the third level imaging resist in order to produce the needed geometries.

CONCLUSIONS

Overall, the spin-on glass is a potentially useful dielectric material for a multi-level process. Further work should include the study of:

a) Different curing methods to improve breakdown voltages.
b) Via chain analysis using an oxide layer on the silicon.
c) Thicker metal to decrease the resistance in a via chain.

ACKNOWLEDGEMENTS

I would like to thank my instructor, Mike Jackson, for all of his help throughout the project. I also thank Rob Pearson for his technical assistance, Scott Blondell for upkeep of the equipment and especially to Gary Hinnenkamp for help in the mask making process.

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