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**COMPACT MODELING OF THIN-FILM
SILICON TRANSISTORS FABRICATED ON GLASS**

by

CHRISTOPHER JAMES NASSAR

A DISSERTATION

Submitted in partial fulfillment of the requirements
For the degree of Doctor of Philosophy
in
Microsystems Engineering
at the
Rochester Institute of Technology
February 2011

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Compact Modeling of Thin-Film Silicon Transistors Fabricated on Glass

by

CHRISTOPHER JAMES NASSAR

Submitted by Christopher James Nassar in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microsystems Engineering and accepted on behalf of the Rochester Institute of Technology by the dissertation committee.

We, the undersigned members of the Faculty of the Rochester Institute of Technology, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

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MICROSYSTEMS ENGINEERING PROGRAM
ROCHESTER INSTITUTE OF TECHNOLOGY
FEBRUARY 2011

ABSTRACT

Kate Gleason College of Engineering
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Degree: Doctor of Philosophy

Program: Microsystems Engineering

Name of Candidate: Christopher J. Nassar

Title: Compact Modeling of Thin-Film Silicon Transistors Fabricated on Glass

The semiconductor industry, now entering its seventh decade, continues to innovate and evolve at a breakneck pace. E. O. Wilson, the famous Harvard biologist who is an expert on ants, estimates that there are 10^{17} ants on earth. The semiconductor industry is now shipping 100 transistors per ant every year [1]. In addition, the pace of growth means we are building more electronics in a year than existed on January 1st of that year!

A major driver for this growth in recent years is the portable consumer electronics market which includes cell phones, personal digital assistants, and tablets. The focus of this dissertation is centered on a new thin-film silicon technology on glass introduced by Corning Inc., and targeted to meet the needs of the portable product display market.

The work presented in this dissertation revolves around a new technology developed by Corning Inc. known as Silicon on Glass or SiOG which permits the transfer of a thin single-crystal silicon film to a glass substrate. This technology coupled with a low-temperature CMOS process has the potential to create devices with performance characteristics rivaling those developed using conventional bulk CMOS processes. These higher performing devices permit an increased level of circuit integration directly on the glass substrate and have the potential to enable new display technologies such as OLED (Organic Light Emitting Diode).

The SiOG CMOS devices are distinctly different from traditional thin-film, silicon-on-insulator, and bulk CMOS devices in that they rely on both surface and bulk conduction. Furthermore, their current-voltage characteristics are heavily influenced by fringing electric fields in the glass substrate.

This dissertation presents an overview of display technology as well as a review of computer-aided design tools for integrated circuit development with a focus on compact modeling. In addition, some early work on developing advanced OLED display driver circuits using SiOG technology is presented. The bulk of this dissertation is focused on the development of compact models which properly describe the electrical characteristics of SiOG CMOS devices.

For all but the most trivial cases, the set of coupled nonlinear partial differential equations that describe semiconductor device behavior has not been solved analytically. Even when the semiconductor equations that represent current flow, charge distribution, and potential distribution are decoupled and device-specific simplifications are applied, analytic solutions remain elusive. Two different methods for developing compact models for the SiOG CMOS devices are presented with distinct methods for developing approximate solutions. In addition, a model for the fringing electric field is developed using conformal mapping techniques, and its effect on drain current is explored.

Finally, a new technique for solving the nonlinear semiconductor equations is explored. The application of a new mathematical technique known as the Homotopy Analysis Method (HAM) is presented as it relates to the general Poisson's equation for semiconductor devices.

Abstract Approval:

Committee Chair _____

Program Director _____

Dean KGCOE _____

Acknowledgments

I'd like to extend my sincerest appreciation to everyone who has helped me in some way to complete this dissertation and to those who have made my graduate experience one that I will treasure forever.

I'd like to thank my advisor, Dr. Bowman whose dedication, knowledge, and guidance are unmatched. I have been amazingly lucky to have an advisor who had enough confidence in me to allow me to explore topics on my own, but also to put me back on the right path when I strayed too far. Dr. Bowman has always been there for me, and often times he will drop what he is doing just to talk. In addition, he has taught me how to formulate my thoughts and to be a better communicator. I would be hard pressed to find a better advisor.

A very special thanks goes out to Dr. Revelli (Joe), whose contagious enthusiasm for science and mathematics has infected the entire lab. I will never forget the numerous mornings when Joe arrived in the lab and shouted, "I got it..." or "I was thinking about that problem last night..." and then proceeded to tell us about his solution (right or wrong) to the problem of the day. I'd also like to thank him for his patience with my never ending barrage of math and physics questions. In addition, I'd like to give him a slap on the wrist for wasting so much of my precious time on political discussions (just kidding) and ask him how the college Tea Party meeting went.

I'd like to acknowledge Corning, Inc., and particularly Carlo Kosik Williams, Greg Couillard, and Dave Dawson-Elli. Without them, silicon-on-glass and this research effort would not have been possible. I'd also like to thank Carestream Health Inc. for their direction and support.

I'd like to thank my committee, Dr. Hirschman, Dr. Moon, Dr. Rommel, and Dr. Tutt for their instruction, support and quality suggestions. I'd like to give a special thanks to Dr. Moon for painstakingly reviewing this Dissertation. I can only strive to one day match his dedication, patience, and attention to detail.

I'd like to thank Team Eagle also known as the Hirshman Research group, Robert Manley, Andrew McCabe, Ryan Rettmann, Chris Shea, Patricia Meller, and Dr. Hirschman for their help with fabrication and processing. I'd especially like to thank Dr. Hirschman and Rob Manley for their enlightening discussions on device physics and simulation.

I'd like to thank my parents for their love and support, but also for teaching me how to learn and how to be a good student. I thank them for forcing me to do my homework even though my first grade teacher was going to make my brain explode. Most of all, I thank them for instilling in me the quality of perseverance which has enabled me to complete my graduate studies.

I'd like to thank Annie for her dedication and support even when I was consumed by my studies, as well as for reading this entire dissertation! I hope you learned something about transistors. I can't wait to see how the Spanish translation comes out.

Finally I'd like to say thanks to all my friends who have provided me with support, motivation or in some way improved my quality of life along the way including but not limited to...Christopher Urban, Hans-Christian Rotmann, Murtuza Quaizar, Matt Paluch, Steve Marshall, Jeff Abbott, Virag Chaware, Matt Lipschutz, Eric Bohannon and Chris Fisher.

*He helps you to understand,
He does everything he can,
Doctor Robert...*

—Lennon and McCartney

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Nomenclature

| | |
|--------------------|---|
| Δ_L | Parameter related to the effective channel length in the fringing field model |
| F | Auxillary parameter used in HAM |
| η_f | Fitting parameter used in SOI DIBL model |
| κ | Subthreshold slope parameter |
| λ | Embedding parameter used in HAM |
| μ | Electron or Hole mobility |
| μ_n | Electron mobility |
| μ_o | Empirical parameter related to effective mobility |
| μ_p | Hole mobility |
| ϕ_f | Fermi potential |
| ϕ_t | Thermal voltage kT/q |
| ψ_o | Potential at the center of the silicon film in a DG MOSFET |
| ψ_s | Surface potential |
| ψ_{sa} | Top (silicon-oxide interface) surface potential |
| ψ_{sb} | Bottom (silicon-glass interface) surface potential |
| τ_{GC} | Charge associated with silicon-glass interface |
| ε_s | Permittivity of silicon |
| ε_{ox} | Permittivity of silicon dioxide |
| ξ | Constant related to physical parameters in blending model |
| C_{ox} | Oxide capacitance per unit area |
| D_n | Coefficient of electron diffusivity |

| | |
|------------|--|
| D_p | Coefficient of hole diffusivity |
| d_L | Length of the left hand electrode used in fringing field model |
| d_R | Length of the right hand electrode used in fringing field model |
| E_o | Empirical parameter related to effective mobility |
| E_{FF} | Fringing electric field |
| E_{sa} | Top (silicon-oxide interface) surface electric field |
| E_{sb} | Bottom (silicon-glass interface) surface electric field |
| G_n | Rate of electron generation |
| G_p | Rate of hole generation |
| I_{DS} | Drain to source current |
| J_n | Electron current density |
| J_p | Hole current density |
| k | Boltzmann's constant |
| k' | Transconductance parameter |
| L | Transistor length |
| l_A | Channel length modulation parameter |
| L_E | Effective channel length used in fringing field model |
| l_F | Fringing Field parameter |
| n | Electron concentration |
| N_A | Concentration of acceptor atoms |
| N_D | Concentration of donor atoms |
| N_i | Intrinsic carrier concentration |
| OS_{VD} | Parameter to control the offset of output resistance blending function |
| OS_{VGn} | Parameter to control the offset of the channel length modulation blending function |
| OS_{VG} | Parameter to control the offset of the effective gate voltage blending function |
| p | Hole concentration |

| | |
|----------------------|--|
| $P_{\Delta V_{FBA}}$ | Parameter to control the severity of the channel length modulation blending function |
| P_{VD} | Parameter to control the severity of the output resistance blending function |
| P_{VG} | Parameter to control the severity of the effective gate voltage blending function |
| Q | Integrated mobile charge |
| q | Magnitude of electronic charge |
| Q_C | Total charge associated with the channel |
| Q_D | Total charge associated with the drain |
| Q_e | Integrated mobile electron charge |
| Q_G | Total charge associated with the gate |
| Q_h | Integrated mobile hole charge |
| Q_S | Total charge associated with the source |
| Q_{hD} | Integrated hole charge calculated at the drain |
| Q_{hS} | Integrated hole charge calculated at the source |
| Q_{sa} | Charge associated with silicon-oxide interface |
| Q_{sb} | Charge associated with silicon-glass interface |
| R_n | Rate of electron recombination |
| R_p | Rate of hole recombination |
| v | Empirical parameter related to effective mobility |
| V_T | Threshold voltage |
| V_z | Empirical parameter related to effective mobility |
| V_{BE} | Effective body voltage used in fringing field model |
| V_{bi} | Built-in junction potential |
| V_{ch} | Channel potential |
| V_{DE} | Effective drain voltage used in fringing field model |
| V_{DS} | Drain to source potential |
| V_D | Drain potential |

| | |
|-------------|--|
| V_{FB} | Flatband voltage |
| V_{GEFF} | Effective gate to source voltage |
| V_{GF} | Gate to source voltage minus flatband voltage |
| V_{GS} | Gate to source potential |
| V_G | Gate potential |
| V_L | Potential on left-hand electrode used in fringing field model |
| V_{OV} | Overdrive Voltage |
| V_P | Programming Voltage |
| V_R | Potential on right-hand electrode used in fringing field model |
| V_{SE} | Effective source voltage used in fringing field model |
| V_S | Source potential |
| V_T | Threshold Voltage |
| W | Transistor width |
| x_{glass} | Glass substrate thickness |
| x_{ox} | Gate oxide thickness |
| x_{SDE} | Effective source/drain length used in fringing field model |
| x_{SD} | Source/Drain length used in fringing field model |
| x_{si} | Silicon film thickness |

Chapter 1

Introduction

Mobile telephones, personal navigation systems, and ultra-portable video and music players have become an integral part of the modern lifestyle. In recent years, there has been rapid growth in the mobile device market. To illustrate this trend, Figure 1.1 plots the number of mobile phones sold worldwide since 1997 [2]. Over

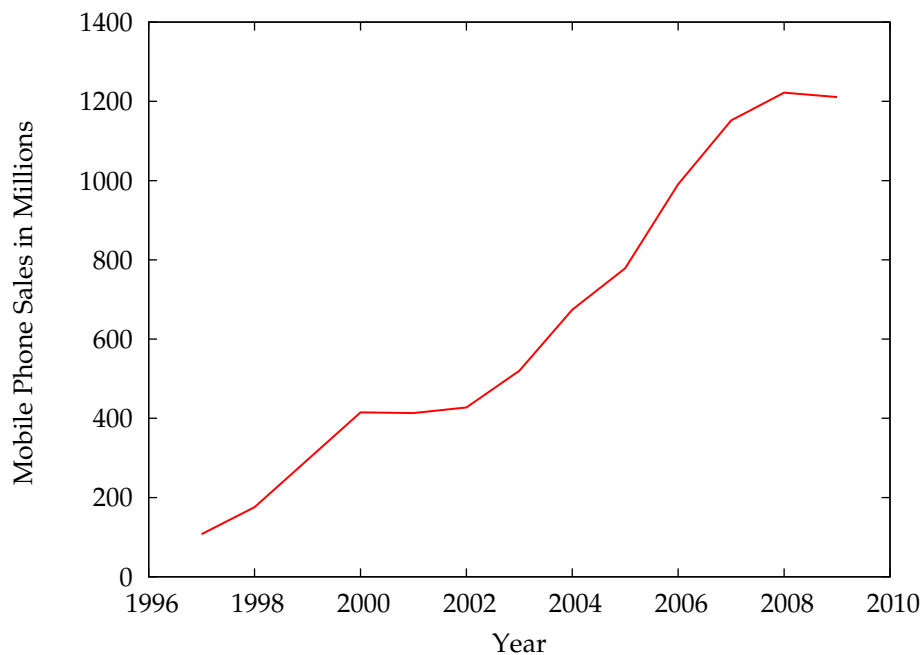


Figure 1.1: Worldwide mobile phone sales since 1997

the past twelve years, mobile phone sales have increased ten-fold. In 2009 alone, 1.2 billion cellular telephones were sold worldwide, which is the equivalent of thirty-one phones being sold every second. Today, most of these portable electronic devices rely on small-format displays for their graphical user interfaces and their ability to display multimedia content. In addition to being used strictly as an output device, many displays implement touchscreen technology allowing for both input and output. The high demand for mobile technology has created fierce competition in the field and is driving researchers in industry and academia to continuously strive for new low-power, high-resolution, high-contrast ratio, and ultra-thin display architectures.

Typically, flat panel displays are made up of an m by n grid of pixels. Early flat panel displays used what is known as passive matrix technology to control the color level of each pixel. Passive matrix displays are made by employing m row and n column parallel metal bus-bars extended across the display with the display medium sandwiched in between. For example, all of the row bus-bars would be patterned on top of the display medium, while the column bus-bars would be patterned on the bottom. To set the brightness level of a particular pixel, an external circuit places a voltage on the column and a ground on the row which intersects the pixel of interest. Since there are no active switching elements, the pixel must maintain its state until it is refreshed. Although passive matrix displays are simple and inexpensive, they are plagued by slow response times and cross talk between pixels [3]. To alleviate the problems associated with the passive matrix scheme, active matrix addressing was introduced. Active matrix displays are characterized by the use of active elements, usually thin-film transistors (TFTs), to hold the state of each pixel on the display while all the other pixels are being updated. The use of TFTs at the pixel site allow for the row and column lines to be fabricated on one side of the display, while the other side is made to be a ground plane. The advent

of active matrix technology was the first time electronics were integrated directly on a glass substrate.

The integration of electronic components, and in particular the fulfillment of Moore's Law [4], has characterized the semiconductor industry for the past half-century. Moore's Law states that the number of transistors that can be inexpensively placed on an integrated circuit doubles about every two years. As the size of individual transistors is rapidly reduced in compliance with Moore's Law, devices operate faster and consume less power. The current digital age where powerful computers and other electronic devices are readily available is a direct result of the continued scaling of devices. The realization of Moore's Law has created the ability to cram larger and larger numbers of transistors into one place, but that place has been for the most part limited to the surface of single-crystalline silicon chips. Applications such as flat panel displays which require electronic devices to be fabricated on large area or transparent substrates have not seen that level of integration.

Integration of complex electronics on alternative substrates has been limited by current TFT technologies [5]. The two most pervasive TFT technologies in use today are amorphous silicon and low-temperature polycrystalline silicon (LTPS). For over 25 years, amorphous TFT technology has been the dominant thin-film transistor technology in the display industry. Amorphous devices enabled the rise of the flat panel display industry, but the performance of these devices is dismal when compared to their traditional monolithic counterparts. The average electron mobility exhibited by amorphous TFTs is 600 times lower than that of monolithic silicon [6]. More recently, LTPS devices were introduced which have notably higher mobilities, around one third of monolithic silicon, but suffer from severe non-uniformity due to the presence of crystal grain boundaries in the active region of the transistor [7].

1.1 System-on-a-Panel

Typical active matrix displays rely heavily on driver electronics to convert a digital signal into an image. A high-level diagram of the electronics needed to drive an active matrix display is depicted in Figure 1.2 (adapted from [8]).

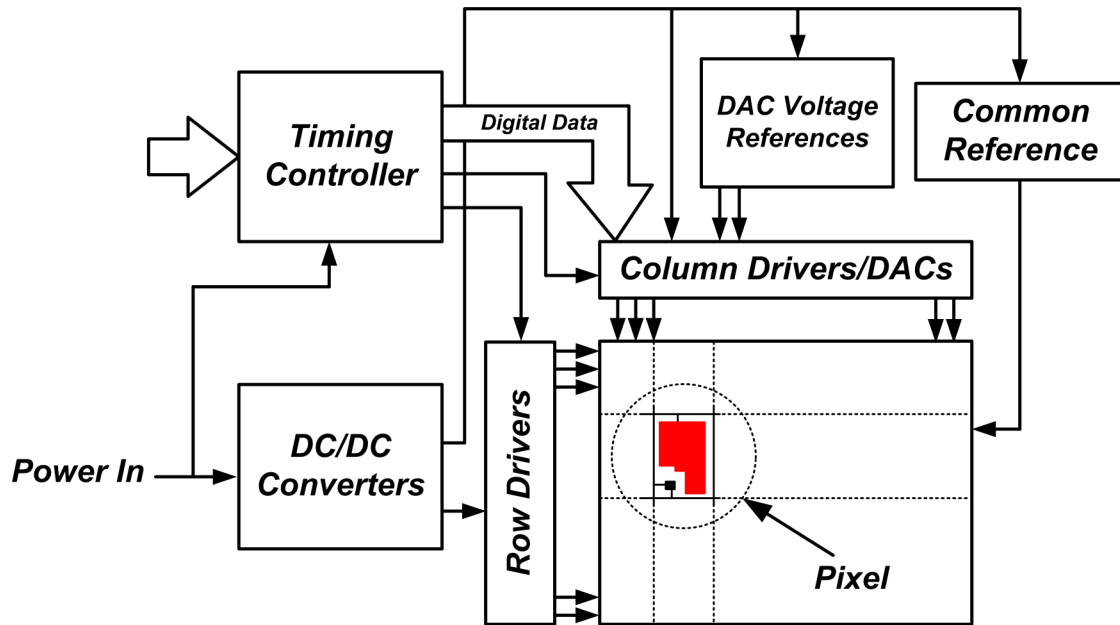


Figure 1.2: Display Driver Electronics

The electronics for a typical display consist of pixel circuits, row drivers, column drivers, DC to DC converters, and timing controllers. As briefly described above, active matrix displays are arranged in a row-column format. Both a pixel and a pixel circuit are located at each intersection of each row and column. The color of a particular pixel is set by activating the pixel's row and transmitting data representing the color to be displayed by the pixel to the pixel circuit via the column line as an analog current or voltage. The pixel circuit then stores the analog value and drives the pixel so that it displays the proper color until it is necessary to reprogram it. The row drivers are used to activate a row of pixels for programming and generally consist of a series of D-type flip-flops and output buffers. The column drivers generate an analog signal representing the color to display from a digital word and

direct it to the proper column. Column drivers are composed of digital to analog converters (DACs), multiplexers, and buffers. The timing controller receives the digital signal from the graphics processor and repackages it, retimes it, and sends it to the column drivers. It also generates the proper timing signals for the rest of the display and is generally made up of high-speed digital components. The DC-DC converter takes in a single supply voltage and generates the appropriate voltage levels to run the display.

To compensate for the poor quality of TFTs, electronic components that make up modern small-format active matrix displays have classically been fabricated using a blend of both traditional silicon complementary metal-oxide-semiconductor (CMOS) chips and TFTs, placed directly on the glass surface. Traditionally, only pixel circuits were fabricated on the glass surface due to the poor performance of amorphous silicon TFTs, but more recently a limited number of circuits have been integrated on the glass surface using LTPS. Only circuits which do not require high performance or high precision such as row drivers have been integrated on the glass surface using LTPS devices. Circuitry which requires high-performance or high-precision devices is fabricated on bulk silicon chips. The traditional silicon CMOS chips are independently fabricated and then bonded to the glass to realize an entire display system. An example of a display utilizing this blend of fabrication processes can be seen in Figure 1.3 [9].

Despite the limited amount of circuit integration on the glass surface today, there is already a push to integrate a greater number of circuits directly on the glass surface. The ultimate goal is to integrate all of the electronics required to drive the display directly on the glass surface, eliminating the need for silicon chips bonded to the glass. This level of integration is known as system-on-a-panel or SOP. SOP technology holds the promise of ultimately thin displays.

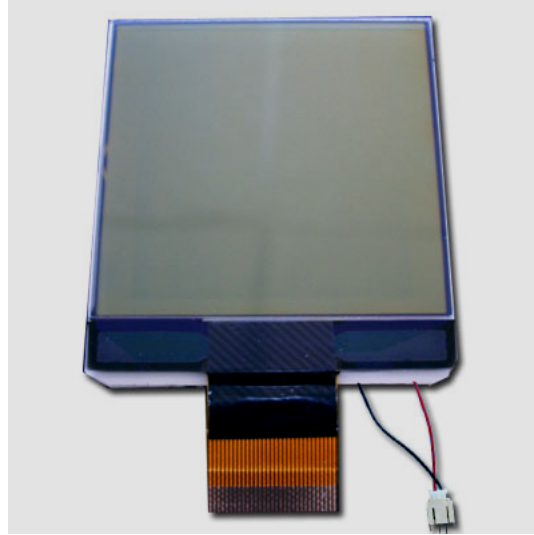


Figure 1.3: Example of Chip-on-Glass Technology

1.2 Silicon on Glass

With the realization of SOP in mind and to overcome the problems associated with current TFT technology, Corning Inc. has developed a new process which enables the transfer of a single-crystal silicon film to a glass substrate [10]. In addition to the substrate material, a low-temperature CMOS process is currently being jointly developed by Corning Inc., Kyung Hee University, and The Rochester Institute of Technology promising TFT device performance which rivals monolithic CMOS. The new single crystal substrate together with the CMOS process have been named Silicon on Glass or SiOG.

1.2.1 Silicon on Glass Substrate

The details of the technology developed by Corning Inc. to transfer single-crystal silicon to a glass substrate are proprietary, but the basic steps are outlined in Figure 1.4.

The creation of an SiOG substrate begins with a prime grade bulk silicon wafer. Hydrogen is implanted into the bulk substrate to aid in the exfoliation of the bulk

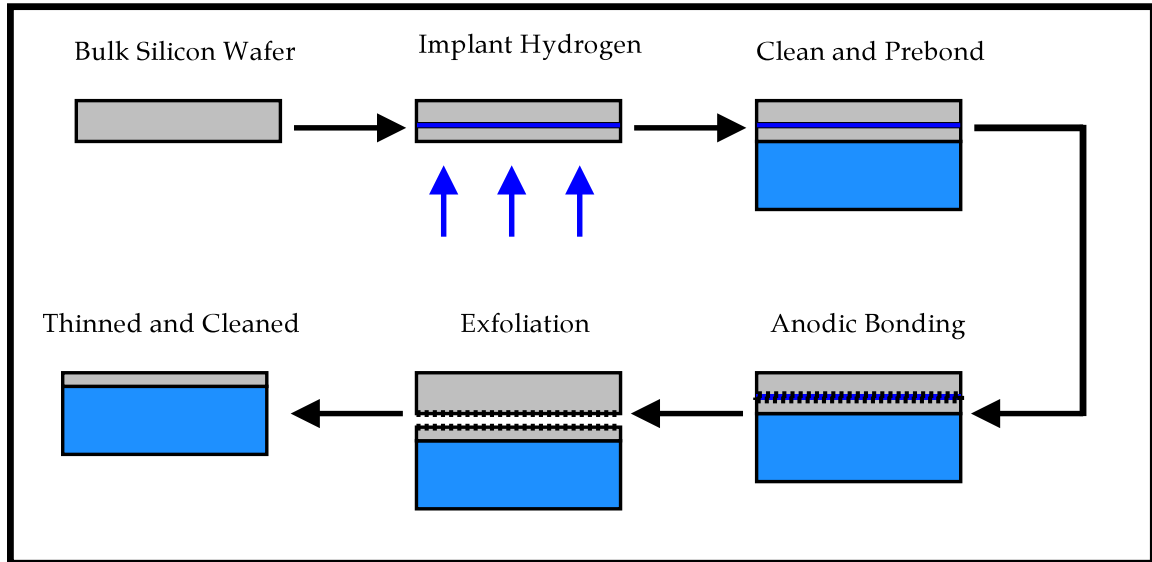


Figure 1.4: Silicon-on-Glass Substrate Creation

silicon wafer later in the process. The silicon wafer and the glass substrate are cleaned and prebonded together through van der Waals forces. The silicon and the glass are then anodically bonded through the application of heat and high voltage. The bulk silicon wafer is exfoliated from the glass leaving a thin layer of silicon on the glass. The remaining layer of silicon is then further thinned and polished, resulting in a finished SiOG substrate ready for device formation. A typical generation-two SiOG substrate created with this process is shown in Figure 1.5.

1.2.2 Silicon on Glass CMOS Process

The low-temperature CMOS fabrication process for SiOG substrates was designed to be compatible with the glass substrate and the display industry's semiconductor manufacturing equipment. The critical difference between the SiOG process and a traditional CMOS bulk process is that all of the processing steps must remain under 600°C , the melting temperature of the glass. Another difference between SiOG and a traditional process is that SiOG has been designed to minimize the number of mask layers and process steps to reduce cost and optimize display panel

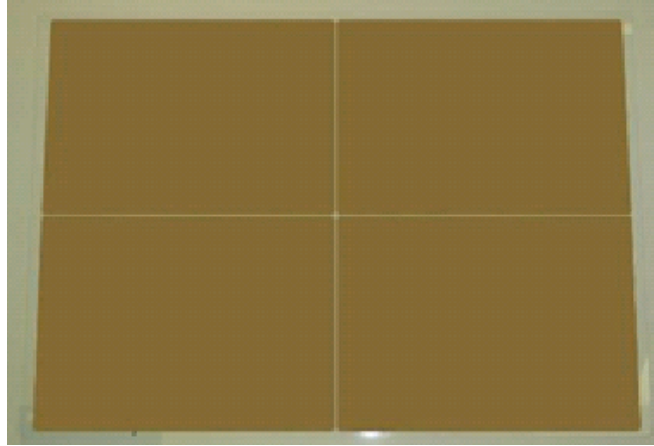


Figure 1.5: Generation Two SiOG Substrate

yield. These design constraints resulted in a single-Fermi-level CMOS technology leading to devices which operate in a rather unconventional manner. The CMOS device operation is described in Section 1.2.3, and the steps used to fabricate the devices will be outlined below. A more complete description of the CMOS process can be found in [11] [12].

Before processing begins, the SiOG substrate is cleaned in a piranha bath consisting of a 50 : 1 $\text{H}_2\text{O} : \text{H}_2\text{SO}_4$ mix to remove unwanted organic material and metal contaminants. Lithography is used to define the location of the mesas of thin-film silicon where each individual transistor will be located. All of the silicon between the mesas is then etched away using a DC plasma with SF_6 chemistry. The SiOG substrate is then cleaned again, first with the piranha bath then with a 5 : 1 : 1 $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{HCl}$ bath. The second bath is targeted specifically at metals and other inorganic material that may be on the surface of the silicon. Next a 50 nm gate oxide is deposited using low pressure chemical vapor deposition (LPCVD). To form the gates of the transistors, a molybdenum film is deposited over the gate oxide by RF sputtering. Another lithography step is done to define the location of the molybdenum gates and interconnect metal. The excess metal is etched away using

a reactive ion etch, RIE. The use of molybdenum as the gate metal allows for a self-aligned process as it blocks the source and drain implants from the channel region. The source and drain regions of the n -type device are implanted with a $4 \times 10^{15} \text{cm}^{-2}$ dose of phosphorus. The phosphorus amorphizes the silicon, allowing for dopant activation at low temperatures [13]. Since boron atoms do not have enough mass to cause significant damage to the silicon lattice, the source and drain regions of the PFET are pre-amorphized using ^{19}F with a dose of $3 \times 10^{15} \text{cm}^{-2}$ at 70 keV. Then ^{11}B is implanted with a dose of $4 \times 10^{15} \text{cm}^{-2}$ at 35 keV. After the formation of the $n+$ and $p+$ regions, an LPCVD SiO_2 inter-level dielectric, ILD, is deposited, followed by an anneal at 600°C for two hours in an N_2 ambient to help activate the source and drain as well as improve the insulating characteristics of the ILD. Contact holes are then patterned and etched followed by aluminum deposition, pattern and etch. The last step is a fifteen minute sinter at 425°C in a forming gas (5% H_2 in N_2). A pictorial representation of the finished devices is shown in Figure 1.6.

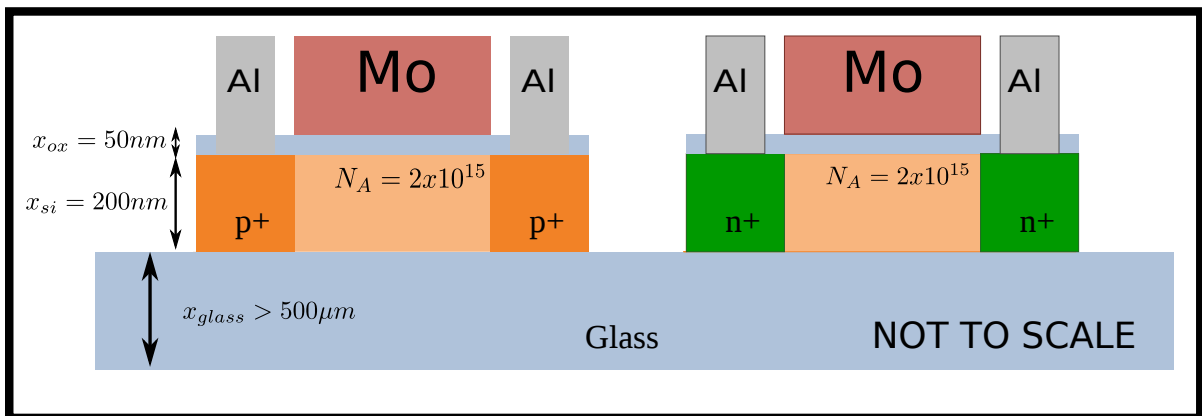


Figure 1.6: SiOG CMOS Devices

1.2.3 Silicon on Glass Device Operation

To better understand the nature of the devices, the operation of the SiOG devices will be described in a qualitative way below, although it is assumed that the reader

has some knowledge of semiconductor devices. Examining Figure 1.6, it is seen that both of the devices are built in a p -type substrate, and the device structures are exactly the same except for differing source and drain dopant types. The technology can be described as a single-Fermi-level CMOS process technology in that the complementary FET devices are fabricated in a thin-film substrate of the same doping type. To date, all devices have been built in a p -type substrate, but theoretically, devices built in an n -type film are possible. Since the bodies of the devices are exactly the same, the response of the mobile carriers in the channel to an applied gate voltage will be the same in both device. It is the differing source and drain regions that allow for complementary device operation.

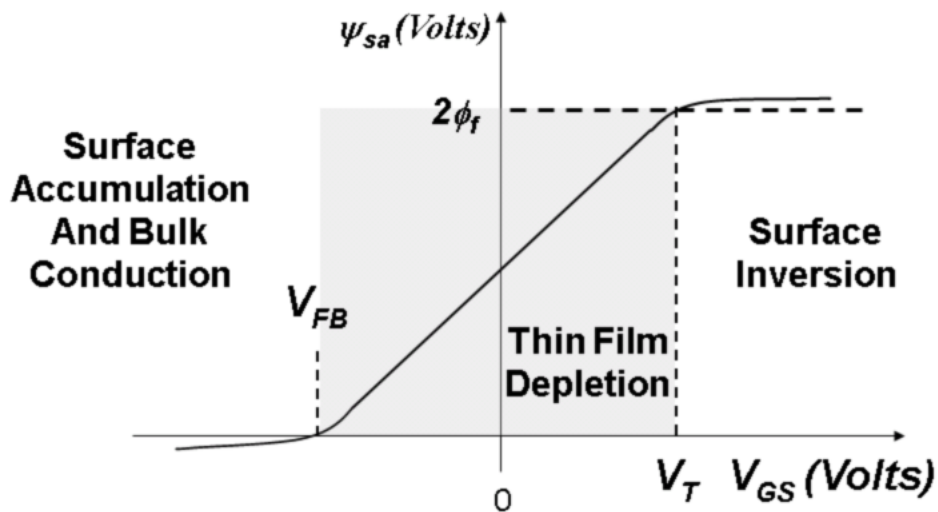


Figure 1.7: Surface Potential Versus Gate Voltage

In its unperturbed natural state, p -type silicon has an equal number of holes and acceptor ions. The presence of the gate structure in CMOS devices upsets this natural state. Since the energy levels of the carriers in each material are different, charge carriers will move from one material to the other. In this system, negative charges (electrons) leave the molybdenum gate and enter the p -type silicon, while positive charges (holes) leave the p -type silicon and enter the gate. This movement

of charge is analogous to a positive voltage source being placed between the gate and the channel. The voltage difference can be quantified by taking the difference between the vacuum energy levels, also called work functions, of the metal and semiconductor materials. The SiOG CMOS devices have been carefully designed so that the movement of charge leaves the silicon film devoid of mobile carriers with zero volts applied between the gate and the source. In this state, the devices are said to be depleted or operating in depletion. Because there are no mobile carriers in the channel, the devices cannot support current conduction and are said to be operating in the off state. Figure 1.7 is a plot of the top surface potential, ψ_s , in an SiOG device versus the applied gate-to-source voltage, V_{GS} . In this first state, V_{GS} is zero while the surface potential is positive due to the metal-semiconductor work function difference. The positive surface potential can be thought of as pushing the native holes out of thin-film region under the gate.

If a small positive voltage is applied between the gate and source, negative electrons will leave the gate and enter the silicon film. Since there are no more positive holes to neutralize, excess electrons build up in the silicon film. These extra electrons form a layer at the silicon-oxide interface as they are attracted to the positive gate. There are now mobile carriers (electrons) in channel, allowing for current conduction in the n -type device. This mode of operation is called weak inversion and corresponds to the gray area to the right of the vertical axis in Figure 1.7. No current flows in the p -type device since the layer of electrons in the channel form back to back p-n junctions (one junction is always reverse biased) with the $p+$ source and drain regions. If the gate-to-source voltage is made even more positive, a thick layer of electrons forms at the surface of the device and a conducting channel is formed between the source and drain. This region of operation is known as strong inversion, and a large amount of current can flow in the n -type device. The gate-to-source voltage at which the device is on the cusp of strong inversion is called the

threshold voltage, V_T (Although more exact definitions for V_T exist, this definition is sufficient for the current discussion) . The p -type device remains off again due to the reverse biased p-n junctions.

If a small negative voltage is placed between the gate and source of the p -type device, holes begin to return to the silicon film. In this region of operation, the small negative applied gate voltage is not enough to overcome the metal semiconductor work function difference, and therefore the surface potential is still positive. Although the surface potential is still positive, the magnitude of the surface potential is now smaller. The devices are now unable to push all of the holes out of the silicon film, and the holes return to the device starting from the back surface. The mobile holes in the channel allow for conduction to occur in the p -type device. This mode of operation is called weak depletion and corresponds to the gray region in Figure 1.7 to the left of the vertical axis. No current flows in the n -type device since the holes in the channel form back-to-back p-n junctions (one junction is always reverse biased) with the $n+$ source and drain regions. If the magnitude of the gate-to-source voltage is to equal the difference between the metal and the semiconductor work functions, the silicon film is now acting as if it is in an unperturbed state. The silicon will now have an equal number of holes and acceptor ions and the holes will be uniformly distributed throughout the silicon film. Since these devices do not have a body terminal and any body charging phenomenon is a third-order effect, the source-to-body voltage is zero. With the source-to-body voltage equal to zero, the gate-to-source voltage required to reach this state is simply the flatband voltage, V_{FB} . In this state, current flows throughout the body of the p -type device and is at the boundary between the weak depletion and accumulation regions. If the applied gate-to-source potential is made even more negative and the metal-to-semiconductor work function difference is overcome even more

holes enter the channel. Since the potential between the gate and channel is negative, holes will be attracted to the gate and a thick layer of holes will form at the surface. In this state, the p -type device is said to be conducting and is operating in the strong accumulation region. Current in the p -type device flows at the surface and in the thin-film of the device.

The n -type device operates in a similar manner to traditional SOI and bulk devices where conduction occurs in an inversion layer at the silicon-oxide interface. The p -type device is different from traditional devices in that it is operated in accumulation and conduction occurs both at the surface and in the thin-film of the device. Although the fully depleted enhancement mode p -channel transistor operated in accumulation or PACC is not new [14] [15], they have not been studied to the extent that the classical inversion mode MOS transistor has.

The study and development of SiOG devices and circuits could not be done without the aid of computers. The complexity of modern circuits can be staggering, and engineers must rely on computers for the rapid simulation of semiconductor devices and the integrated circuits of which they are a part. The bulk of this dissertation is dedicated to one aspect of computer simulation, compact device modeling. The use of computer simulation in the design of integrated circuits is described in the next section, highlighting the role and importance of compact device modeling.

1.3 Simulation of Integrated Circuits

Compute-aided simulation and modeling have become a crucial part of the integrated circuit development cycle. Figure 1.8, adapted from [16], shows each distinct area of simulation and also highlights the feedback between them. During the feedback process, knowledge gained through one step is used to optimize the system as a whole, leading to higher quality products while minimizing design

time. Each block in Figure 1.8 will be described below.

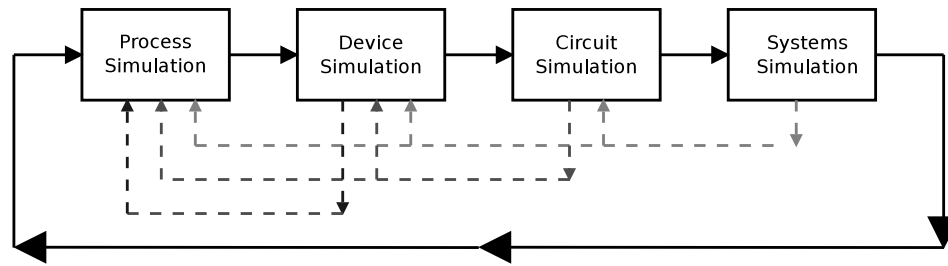


Figure 1.8: Computer Simulation of Integrated Circuit Fabrication

Process simulation is used by device physicists and processing engineers to predict the outcome of the various physical and chemical processes required to create an integrated circuit. Typical processes that would be modeled include ion implantation, annealing (diffusion and dopant activation), etching, deposition, oxidation, and epitaxy. The simulation of these processes is done in a serial fashion, using the result of one process as the starting point for the next. In this way, one can simulate the entire fabrication of a device. These processes are often modeled by complicated partial differential equations such as Fick's diffusion laws. Since closed-form solutions to these equations are not easily obtainable, numerical techniques such as finite difference, finite element, and Monte Carlo methods are used to solve the equations. The result of process simulation is a file containing a one-dimensional, two-dimensional or three-dimensional representation of a semiconductor device which can be fed into the device simulator. Some commonly used process simulation tools include Stanford University Process Modeling (SUPREM) and Silvaco's Athena.

The device simulator either takes the structure created from the process simulation or a simplified version of it and rigorously analyzes the response of the structure to applied electric potentials. Device simulators solve the fundamental equations describing the electrical and thermal behavior of semiconductors in two or

three dimensions. These equations are coupled nonlinear partial differential equations which must be solved numerically [17, pp 513-514]. These device simulations can be highly accurate, but the accuracy comes at the cost of computation time. Modern device simulators include GNU Archimedes, Synopsis's Taurus Medici, and Silvaco's Atlas.

Circuits are built from individual devices to form complicated electrical systems. Modern circuits can contain thousands or even billions of elements. Circuit simulation programs rely on iterative numerical techniques such as Newton's method to solve Kirchhoff's circuit laws for node voltages and branch currents. Thus computation time for each element must be kept to a minimum. It is for this reason that circuit simulators cannot use the same approach to modeling semiconductor devices as the device simulator. Compact models which describe the behavior of the device in a succinct, computationally-efficient form are used instead. Although the term compact model is not rigidly defined, the spirit of compact modeling was best described by Gildenblat when he wrote, "Models of circuit elements which are sufficiently simple to be incorporated in circuit simulators and are sufficiently accurate to make the outcome useful to circuit designers are called compact. The conflicting objectives of model simplicity and accuracy make the compact modeling field an exciting and challenging research area for device physicists, electronic engineers and applied mathematicians." [18] The focus of this work is on compact modeling, and therefore it will be described in detail in the following section. Circuit simulation programs include SPICE (Simulation Program with Integrated Circuit Emphasis), Cadence Spectre, and Silvaco's SmartSpice. All of those simulators use standard compact models such as BSIM (Berkeley Short-channel IGFET Model), and the PSP Model.

Today's products rarely consist of a single integrated circuit. Often times they are coupled together with many other integrated circuits, mechanical and optical

devices. Systems simulation is a set of techniques for using computers to simulate the interactions between all of these components. Often, multi-purpose packages such as Matlab or Simulink are used for this purpose.

1.4 Compact MOSFET Modeling

As briefly mentioned in the previous section, the electrical behavior of semiconductor devices is described by a set of coupled nonlinear partial differential equations (PDEs). Specifically, the equations are Poisson's equation

$$\nabla^2 \psi = \frac{-q}{\epsilon_s} (p - n + N_D - N_A) \quad (1.1)$$

and the current continuity equations for carrier distribution

$$\frac{\partial n}{\partial t} = \nabla \cdot J_n + G_n - R_n \quad (1.2)$$

$$\frac{\partial p}{\partial t} = -\nabla \cdot J_p + G_p - R_p \quad (1.3)$$

where

$$J_n = q\mu_n n E + qD_n \nabla n \quad (1.4)$$

$$J_p = q\mu_p p E - qD_p \nabla p \quad (1.5)$$

representing the electron and hole current density, respectively. In equation (1.1), ψ is the electric potential, q is the charge of an electron, ϵ_s is the permittivity of silicon, p is the hole concentration, n is the electron concentration, N_D is the donor concentration, and N_A is the acceptor concentration. In equations (1.2) and (1.3), J_n and J_p are the electron and hole current densities. G_n and G_p are the electron and hole generation rates, and R_n and R_p are the electron and hole recombination rates.

In equations (1.4) and (1.5) μ_n and μ_p are the electron and hole mobilities. D_n and D_p are the electron and hole diffusivities, and E is the electric field.

For all but the most trivial cases, these equations have no closed-form solution. General purpose semiconductor device simulators solve the set of coupled non-linear PDEs using numerical methods. Most semiconductor devices can be simulated with reasonable accuracy using these methods, at the cost of computation time. Since the governing equations do not lend themselves to closed-form computationally efficient solutions, compact models must be developed using device-specific simplifications at the cost of generality.

1.4.1 Compact Modeling History

In the early days of semiconductors, high-speed digital computers were not readily available. Numerical solutions to the governing semiconductor equations were too costly computationally. It was in this climate that the start of compact Field Effect Transistor (FET) modeling began. In 1952 Shockley introduced an important simplification to the complex semiconductor equations known as the Gradual Channel Approximation (GCA) [19]. Under this approximation, the rate of change of the vertical electric field (from gate to substrate) is considered to be much greater than the rate of change of the lateral field set up by the source and drain. Applying this simplification leads to the decoupling of the x and y dimensions, breaking the problem up into two 1-D problems. The first equation is the 1-D Poisson's equation which governs the number of carriers in the channel and the second equation describes how the carriers flow from the source to the drain. The complete theory based on the GCA for MOSFETS was developed by H.C. Pao and C.T. Sah in 1966 [20]. The Pao-Sah model shown below in (1.6) and (1.7) is recognized as a benchmark for

compact models since it is based on a limited number of assumptions.

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{-q}{\epsilon_s} (p - n + N_D - N_A) \quad (1.6)$$

$$I_{DS} = \mu \frac{W}{L} \int_{V_S}^{V_D} Q dV_{ch} \quad (1.7)$$

In (1.7), W is the width of the transistor, L is the length of the transistor, V_s is the source voltage, V_D is the drain voltage, Q is the integrated mobile charge, and V_{ch} is the channel potential. The Pao-Sah model considers both drift and diffusion as carrier transport mechanisms. It is based on the total mobile charge Q by integrating the mobile carrier concentration from gate to substrate with the only approximation being the GCA.

Despite the major simplifications introduced by the GCA, users of the Pao-Sah model generally must solve for Q numerically, reducing its utility as a compact model. To reduce the amount of computation required by the Pao-Sah model, J.R Brews introduced the charge sheet model in 1972 [21]. The charge sheet model further reduced the complexity of the computation by introducing the following approximations: The inversion charge in the channel is located in an infinitesimally thin layer at the Si – SiO₂ interface and to estimate the bulk charge under the inversion layer, the depletion approximation is valid. The depletion approximation states that the carrier concentrations n and p will be negligible in comparison to the impurity concentration in depleted regions of the device. Because of its simplicity, the charge sheet model used in conjunction with the GCA form a common platform for all compact models currently available for use as shown in Figure 1.9.

Compact models are classified by the variables that make up the expression for current. For example, the expression for drain current in surface-potential-based models is a function of the surface potentials at the source and drain, while in a

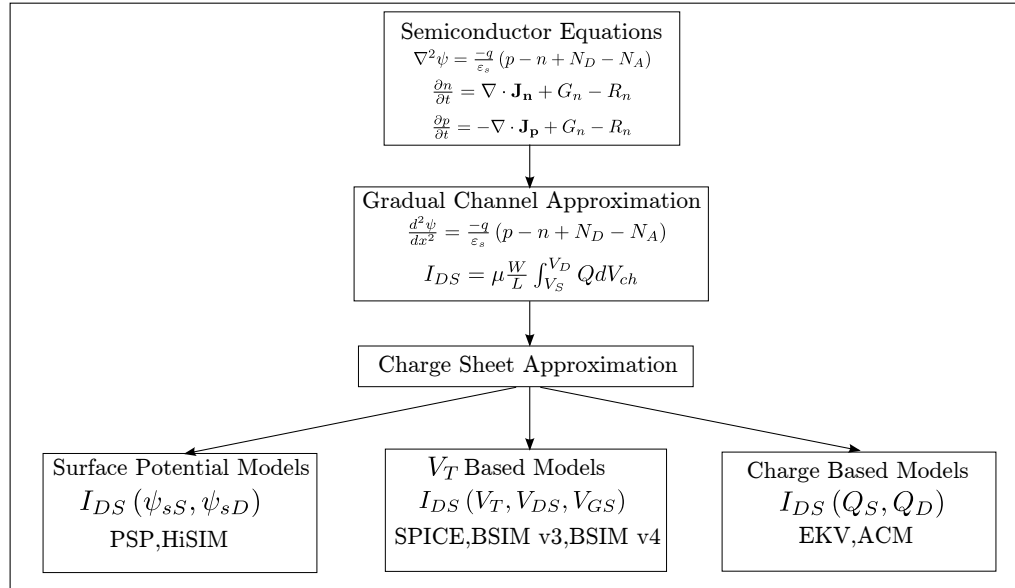


Figure 1.9: Compact Modeling Breakdown

charge-based model the current expression is a function of the total integrated mobile charge at the source and drain.

1.4.2 Characteristics of a Good Compact Model

The elements of a good compact model have been covered extensively in the literature [22] [23] [17], but will be summarized for the reader below.

Obviously, reasonable accuracy in current-voltage and capacitance-voltage characteristics are important, but other requirements must be imposed for proper circuit simulation. As stated above, modern circuits can contain thousands of elements, and circuit simulation programs use iterative techniques like Newton's method to solve for node voltages and branch currents. Thus, the computation time for each element must be kept to a minimum. The use of Newton's method demands that the model expressions be continuous and continuous in the first derivative for the

system to converge. Today both accuracy and continuity are desired in all derivatives to accurately predict nuances in I - V characteristics and to make use of advanced numerical techniques. Functions which satisfy this constraint are called C - ∞ functions. In addition, the model formulation and parameters should be as physical as possible, and the model should exhibit physically realizable behavior. Models should strive to properly predict the behavior of the device over temperature and geometry. The model should not cause numerical problems for the simulator outside of the normal operating range.

Development of a compact model that meets all of these criteria is a difficult challenge. Even industry standard models such as BSIM and PSP do not completely satisfy all of these criteria and there is always an ongoing effort in industry and academia to improve the current compact models.

1.5 The Need for Compact SiOG Device Models

Wanting to demonstrate the superior performance of SiOG, Corning became interested in developing advanced circuit architectures using SiOG for system-on-a-panel or SOP displays. To study the use of SiOG for SOP displays, Corning partnered with the Analog Devices Integrated Microsystems Laboratory (ADIML) at RIT. Initially the ADIML focused on developing the circuit elements necessary for creating a complete SOP active matrix liquid crystal display (AMLCD), but soon decided to work on the newer active matrix organic light emitting diode displays (AMOLED) since properly driving AMOLED displays begs for the higher performing SiOG devices. The work presented in this dissertation began under a partnership with Corning to study the use of SiOG for SOP applications. Some of this early work on SOP circuits is presented in Chapter 2.

Before the design community, or even students in the ADIML, would be able to

design the circuit blocks needed to realize an SOP display in SiOG, compact device models of the SiOG transistors were needed for circuit simulation.

Initially models from the AMI 0.5 μm process were used until measured data from SiOG devices became available. As measured data arrived from the fabrication group, the AMI 0.5 μm models were no longer used. Instead, a SPICE level 3 model was used with the model parameters chosen to best match the measured data. The SPICE model was initially a good choice since the parameter count is low, and the parameter extraction techniques are straight forward. For a particular device geometry, parameters could be extracted which allowed for a fairly accurate description of the on-state characteristics of the SiOG devices. Despite its ease of use, the SPICE model had many issues when applied to SiOG. The SPICE level 3 model is unable to capture subthreshold and leakage behavior, the capacitance characteristics are not accurately reproduced, the parameters had little physical meaning, and the model did not scale properly with geometry.

The need for new device models to replace the inadequate SPICE 3 models was apparent. Initially it was thought that the SiOG devices would resemble SOI (Silicon-on-Insulator) devices in both physics and operation, but the SiOG devices were unique. Models such as BSIM-SOI and PSP-SOI were not adequate to capture the physics of the SiOG devices. All commercial and downloadable compact models are based on Brew's charge sheet approximation which does not accurately describe the surface and bulk conduction inherent to the p -type device operated in accumulation. In addition, the available models did not account for effects caused by the glass substrate.

Although there is currently no ready-to-use model for the PACC device, some work is available in the literature. Previously, the behavior of PACCs has been approximated by a surface channel in parallel with a JFET bulk channel [24]. Although it provides insight into the device operation, this model is not continuous

and does not accurately predict the drain current in the low current depletion region. Iniguez et al. [25] and Su and Kuo [26] modeled the PACC device in all regions of operation, but the resulting models rely on complicated regional partitioning schemes. The low current region has been modeled before [27] [28], however the models do not explicitly show the relationship between film thickness and doping levels on drain current. Analytical models for the intrinsic thin-film case do not accurately predict the effects of dopants on PACC devices [29] [30]. Liu et al. [31] introduced a non-charge-sheet model for the doped symmetric double gate MOS-FETs which utilized the fixed-point method to develop an approximate solution to Poisson's equation. Their solution to Poisson's equation is able to handle both inversion and accumulation regions, but the complete model (drain current) has not yet been extended to accumulation devices. In addition, Liu's model is developed strictly using the zero-field boundary condition at the center of the device which is not valid for PACC devices with fixed charge at the silicon-glass interface.

The modeling of the PACC device was sufficiently new and interesting enough to become the bulk of this work.

1.6 Dissertation Overview

The organization of the rest of this dissertation is as follows: Chapter 2 describes some of the initial work done on SiOG Circuit development. Chapters 3 and 4 describe compact models developed for the SiOG Accumulation PFET device. Chapter 5 describes the effect of the fringing electric field on SiOG device characteristics. Chapter 6 focuses on the application of a new mathematical technique, the Homotopy Analysis Method, to the Poisson's equation for semiconductor devices. Chapter 7 outlines a path for future work.

Chapter 2

System-on-a-Panel Circuits

As stated in Chapter 1, the work presented in this dissertation began as part of an effort to study the use of SiOG for system-on-a-panel (SOP) applications. Initially the focus of the research was on developing advanced circuit architectures in SiOG with the overall goal of developing all of the components necessary to drive small format AMLCDs (Active Matrix Liquid Crystal Displays). Shortly after beginning work on liquid crystal based displays, it became apparent that the industry was moving towards a new type of emissive display, AMOLED (Active Matrix Organic Light Emitting Diode). OLED devices depend on careful control of current to adjust luminance. Circuit techniques for precise control of current depend on the use of current mirrors and matched MOSFET devices in terms of their threshold voltage and intrinsic transconductance. SiOG devices promised to offer better matching in devices and, hence, more uniform displays. As the need for SiOG device models became apparent, the focus of this work again shifted, this time from circuit design to device modeling. Despite the shift to device modeling, a significant amount of circuit work was completed. Three different AMOLED driver circuits have been devised and prototyped. Although the circuit work was not pursued, it has lead to two patents [32,33] and is described below.

2.1 AMOLED Technology

The small format display industry is moving towards AMOLED displays because of their many excellent attributes. OLEDs are thin, lightweight, low power, and emissive while providing good contrast, high resolution, broad color gamut, and wide viewing angle. They have the potential to become the next dominant flat panel technology [34]. OLEDs have acquired a significant portion of the small format display market, and are poised to overtake the large format display market in the coming years [35]. Despite their excellent attributes, OLEDs have been plagued by poor device stability, short lifetime, poor yield, and low emission efficiency, limiting their adoption. Circuit-based solutions to the problems associated with the OLED devices have been stifled by the use of amorphous and polysilicon thin-film transistors which are also plagued by instability and non-uniformity. It is surmised that SiOG will overcome the problems associated with amorphous and polysilicon-based TFTs to allow for circuit solutions which enable AMOLED displays.

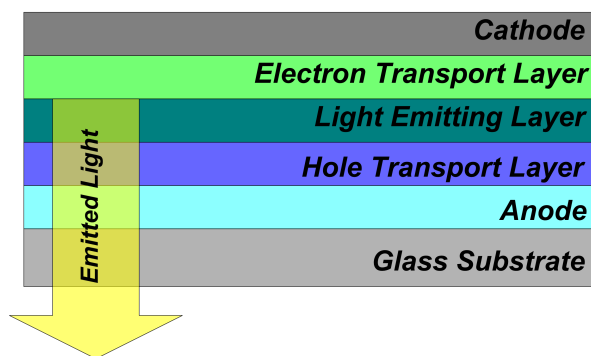


Figure 2.1: Bottom Emitting OLED Device

OLED devices are made by depositing layers of organic materials between two electrodes. A simple bottom emission OLED structure is shown in Figure 2.1. OLED devices consists of an electron injecting cathode, an electron transport layer (ETL), a light-emitting layer (ELM), a hole transport layer (HTL), and a transparent hole injecting anode. When a forward bias is applied between the anode and cathode,

electrons travel from the cathode to the anode, while holes are traveling from the anode to the cathode. The two charge-carrying species recombine in the ELM and produce a photon with a wavelength corresponding to the difference in energy between the ETL and HTL.

The first practical OLED devices were developed by C.W. Tang and S.A. VanSlyke [36] at the Eastman Kodak Research Laboratories in Rochester, NY in the late 1980s. Earlier attempts to create organic light-emitting devices suffered from unreasonably high turn-on voltages. These early devices were built by sandwiching a single organic material between two carrier injecting materials. Tang and VanSlyke's device was different in that it consisted of a double layer of organic thin films where one layer was only capable of monopolar transport. In addition to the double layer of organics, the use of a low-work-function alloy for efficient electron injection was introduced.

Two other interesting observations were noted in the original paper by Tang and VanSlyke. The first one is that the light output from the device is linearly proportional to the current input. The second observation was that the devices degraded quickly. In order to maintain a constant current through the device, the voltage across the OLED needed to be increased from 7 V to 14 V in the one hundred hour test. Through the use of new materials, the efficiency and lifetime of OLED devices has been steadily increasing since the original work by Tang and VanSlyke was published. Voltage shifts for modern OLED structures is now less than 0.3 mV/hr [37].

There is still no industry standard for OLED materials or structure. Depending on the order of the materials composing the OLED, a device may be either classified as either a top-side or a bottom-side emitting structure. Bottom-side emission displays are easier to manufacture, but the light output must shine through the same glass on which the display electronics are built, reducing the aperture ratio of the

display. The industry is moving toward top-side emission displays which can use the entire pixel area for emission and allow for complex circuitry underneath.

Additional organic layers can be added in tandem forming multiple-stack OLED devices [37] which offer an increase in luminance efficiency, improved color gamut, and extended OLED lifetime. The current-voltage characteristic of a double stack

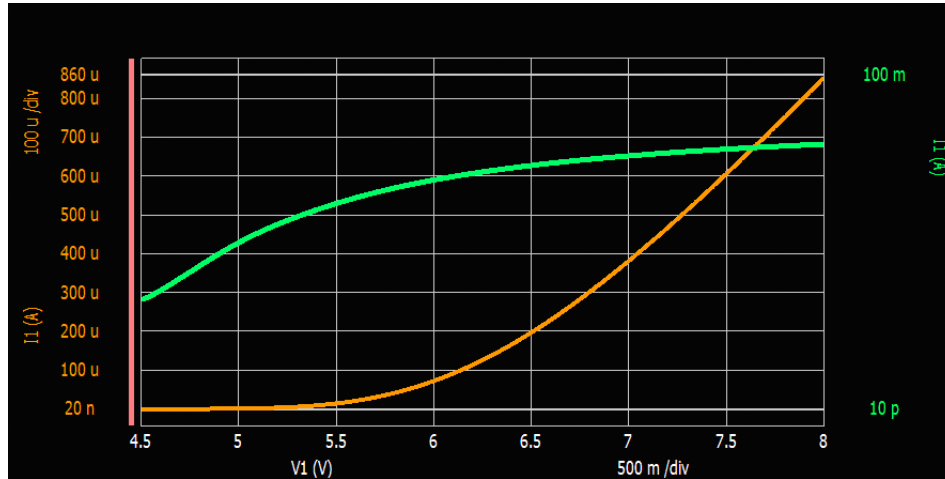


Figure 2.2: OLED IV Characteristics

OLED resembles that of a semiconductor diode as shown in Figure 2.2. The threshold voltage to stimulate emission is roughly 2 V for each organic stack in the OLED device. OLED luminance is very linear with applied forward current density over a range of four decades with an operational upper limit of 100 mA/cm² as shown in Figure 2.3.

2.2 Driving OLED Displays

As previously mentioned, the single OLED pixel can be viewed as a circuit element that resembles a silicon diode in its current voltage behavior and the luminescence of an OLED varies linearly with current. As the OLED ages, the voltage across the OLED needed to achieve a specific current will shift, but the luminescence is always directly proportional to current density.

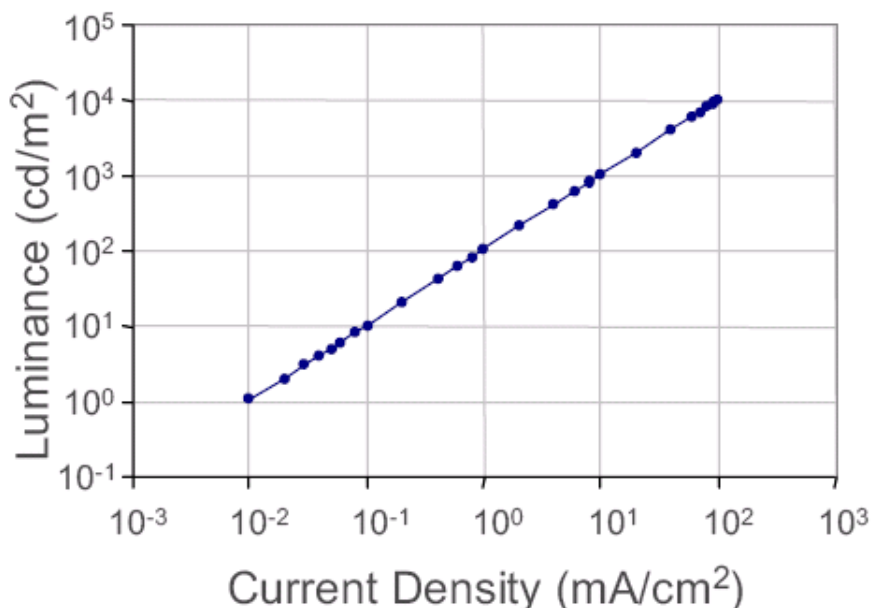


Figure 2.3: OLED Luminance vs. Current Density (Data provided by Kodak)

The work in this chapter is aimed at improving small-format OLED displays with minimum display resolutions of 320 X 240 tri-color pixels which corresponds to QVGA. The active current density range to drive small format display OLED pixels can be estimated from the area of the OLED pixel and the luminance plot in Figure 2.3. A typical pixel size is 150 x 50 microns. For 10-bit gray scale illumination a current range of 0-7.5 μA results with a least significant bit of 7.5 nA. Clearly, at these current drive levels leakage currents must be managed carefully and CMOS device operation must include the subthreshold/low current region of operation. Since industry tends to resist change, an effort should be made to keep the display architecture as similar to AMLCD technology as possible.

The light output of an OLED pixel is always directly proportional to the current flowing through the device, and therefore OLEDs must be driven with a good current source if uniformity is desired. OLED pixel drivers fall into two main categories, voltage-programmed and current-programmed. Voltage-programmed

pixel drivers utilize TFTs as transconductors to create voltage-controlled current sources, while current-programmed pixel drivers use TFTs in the current mirror configuration to realize current-controlled current sources.

Voltage-programmed techniques are now the dominant methods for driving OLED pixels because the industry is reluctant to switch from known voltage-based LCD programming/driving techniques. Another reason the industry has been reluctant to switch is because current-programming based drive techniques pose settling time issues.

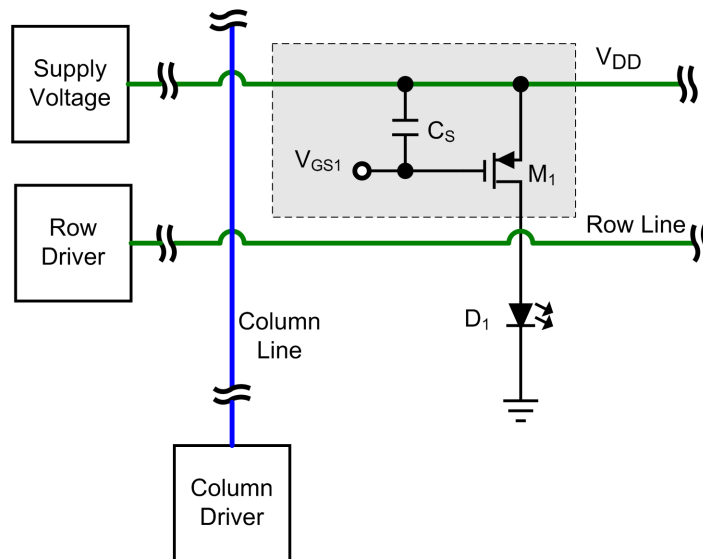


Figure 2.4: OLED Pixel Site

The region in the gray box shown in Figure 2.4 represents a generic circuit for driving OLED device D_1 . D_1 's luminance is proportional to its current density and p -type MOSFET M_1 acts as a voltage-controlled current source to drive D_1 . M_1 also provides a means of storing the pixel drive current value through gate-to-source voltage V_{GS1} . The assorted circuit driving schemes for OLED devices use this generic circuit as the starting point. The V_{DD} line is the power source for the OLED current. Row scan logic selects the row of the pixel site at the exact time the column line is active with the luminance control parameter, either current or voltage, for the

pixel. As the row is deselected, the programmed gate voltage corresponding to the desired OED current is stored at V_{GS1} .

The static and dynamic performance issues with either OLED current-programmed or voltage-programmed pixel circuits stem from the way the gate voltage V_{GS1} is developed and retained and also the equivalent network of the column line. Figure 2.5 illustrates a simple distributed element network model for a column line used in a small format displays. If the column line is driven with a current source, the speed

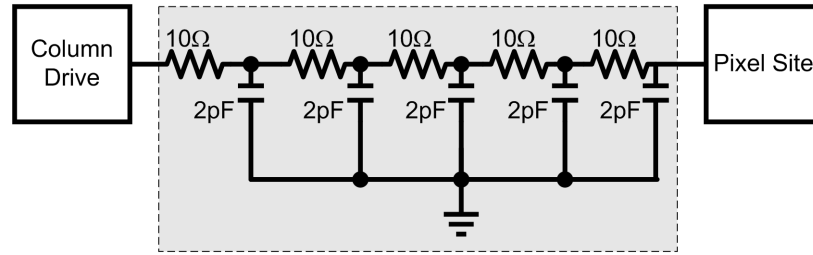


Figure 2.5: Column Line

is governed by the slew rate

$$\frac{I}{C} = \frac{\Delta V}{\Delta t} \quad (2.1)$$

where I is the drive current, C is the total capacitance and $\frac{\Delta V}{\Delta t}$ is the change in voltage with respect to time. The slowest switching time occurs when switching a pixel from completely on, or full scale, to just one bit of luminance. This corresponds to about $7.5 \mu\text{A}$ to 7.5nA of current for a small format display. For a typical PACC device, this leads to about a 1 V change in the gate to source voltage.

$$\frac{7.5 * 10^{-9}}{10^{-11}} = \frac{1}{\Delta t} \quad (2.2)$$

$$\Delta t = 1.33 \text{ ms} \quad (2.3)$$

A small format QVGA display has a resolution of 320x240 operating at 30 Hz. Therefore the entire display must be updated in

$$\Delta t_{Display} = \frac{1}{30} = 33.33 \text{ ms} \quad (2.4)$$

which leaves

$$\Delta t_{Row} = \frac{1}{30 * 240} = 139 \text{ } \mu s \quad (2.5)$$

for each row. Hence, if every pixel in a row was driven simultaneously, the pixel sites would not have enough time to settle.

It can easily be proven that voltage-programmed pixels will settle in the allotted time. Using the open-circuit time constant approach [38], the time needed to settle a pixel site using a voltage source can be determined.

$$\tau = RC * \sum_{k=0}^n k = RC \left(\frac{n(n+1)}{2} \right) \quad (2.6)$$

In Equation (2.6), n is the total number of resistors in the network, R is the resistance of a single resistor and C is the capacitance of a single capacitor. From Figure 2.5, $R = 10 \text{ } \Omega$, $C = 2 \text{ pF}$, and $n = 5$.

$$\tau = (10) (2 * 10^{-12}) \left(\frac{5(6)}{2} \right) = 300 \text{ ps} \quad (2.7)$$

To settle the voltage at the pixel site to within 0.1% of its final value, seven time constants are needed or

$$\Delta t = 7\tau = 2.1 \text{ ns.} \quad (2.8)$$

Using a voltage source to drive the column line is two orders of magnitude faster than using a current source and provides the ability to settle the voltage at the pixel site in a time that meets the refresh rate requirements.

The simplest voltage drive OLED pixel circuit consists of two transistors and a capacitor (2T-1C) shown in Figure 2.6.

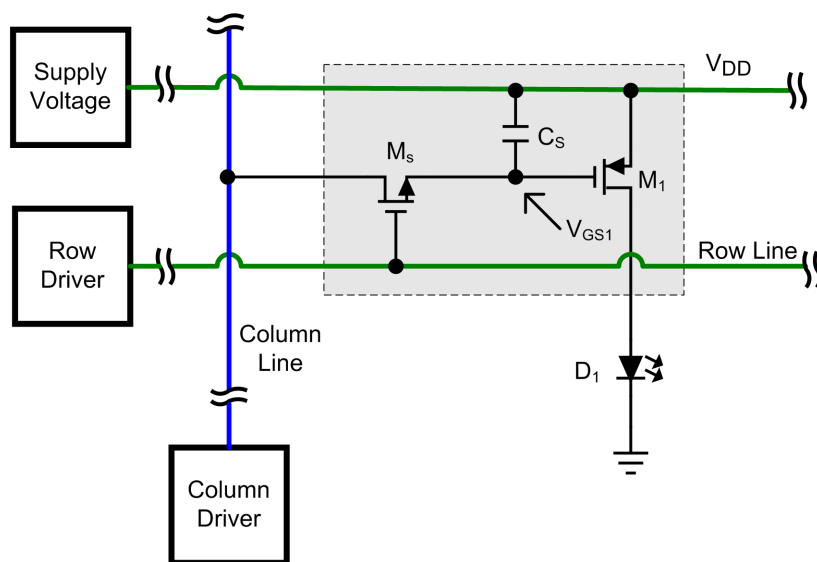


Figure 2.6: 2T1C Pixel Circuit

In the 2T1C circuit, the column driver places a voltage on the column line that corresponds to the exact voltage drive V_{GS1} required for M1 to deliver OLED drive current according to the MOSFET square law equation.

$$I_{DS} = \frac{k'}{2} \frac{W}{L} (V_{GS1} - V_{T1})^2 \quad (2.9)$$

In (2.9), k' is the transconductance parameter and V_{GS1} and V_{T1} are the gate-to-source voltage and threshold voltage of transistor M1, respectively. By comparison, in the current-mirror-based circuit, Figure 2.7, the column driver sinks the appropriate current down the column line and diode-connected transistor M2 generates the drive voltage V_{GS1} required for M1 to deliver the appropriate current to the OLED.

Despite its speed and simplicity, the 2T1C circuit is not able to maintain uniformity across the display. In the 2T1C circuit, the drive voltage V_{GS1} is developed somewhere far away on the display panel or perhaps on an external chip. Due to

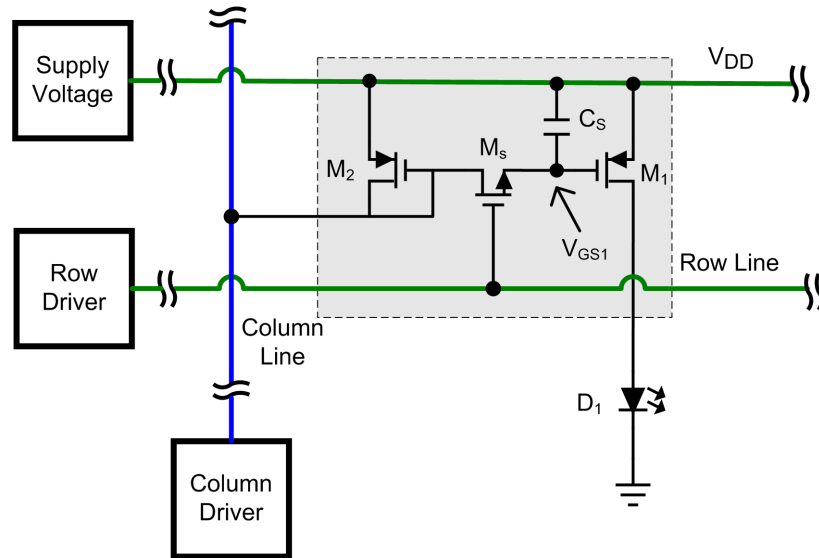


Figure 2.7: Current Mirror Pixel Circuit

the process gradients and non-uniformities inherent with amorphous and polysilicon TFTs, each drive transistor responds with a different amount of drain current to the same applied V_{GS1} . In the current mirror circuit, V_{GS1} is developed at the pixel site, using a device which, in theory, closely matches the drive transistor, reducing the amount of mismatch. Current-programmed pixel circuits therefore provide a higher level of uniformity at the cost of speed [39].

Many different pixel drive schemes have been developed to compensate for the mismatch issues associated with voltage drive circuits, while still maintaining an acceptable settling time [40]. These circuits are mostly based on a technique where the threshold voltage of the drive transistor is generated and the programming voltage from the column driver is added to it in some fashion. Figure 2.8 illustrates a popular circuit architecture implementing this technique. During the first cycle, Scan $n - 1$, capacitor C_s is pulled down to V_{reset} . On the next cycle, M1 is diode connected and its source is set to the programming voltage V_P from the column driver, see Figure 2.9. During this stage, the capacitor C_s will discharge through M1 until

$$V_{GS} = V_T \quad (2.10)$$

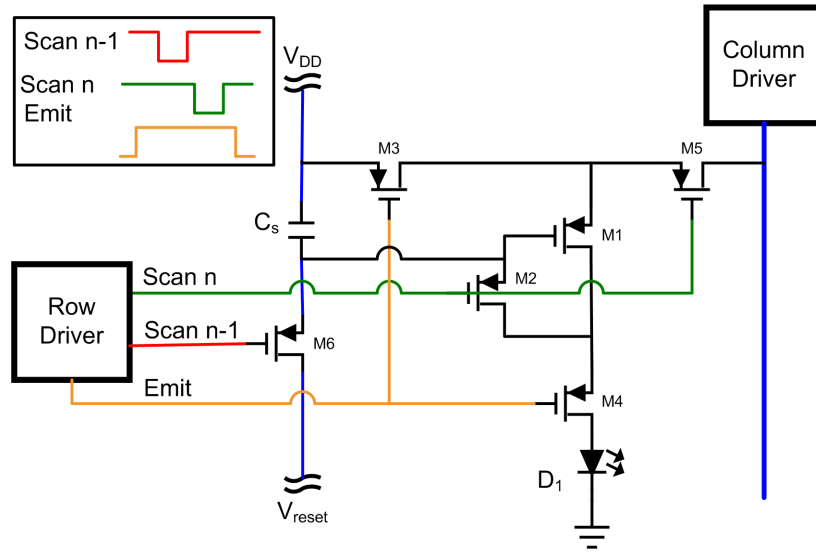


Figure 2.8: 6T1C Pixel Circuit

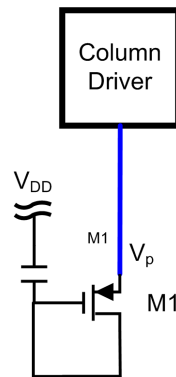


Figure 2.9: 6T1C Programming Equivalent Circuit

at which point the current through M1 will equal zero and

$$V_G - V_S = V_T \quad (2.11)$$

$$V_G = V_S + V_T = V_P + V_T \quad (2.12)$$

the gate voltage is equal to the programming voltage, V_P , plus the threshold voltage. Now, the emit line is activated and the OLED is illuminated.

Drive schemes like the one above still suffer from non-uniformities due to mobility mismatch and imperfect threshold voltage compensation. For perfect compensation, the current through M1 should be zero at the end of the V_T capture cycle. Since the amount of settling time for a pixel is limited, the current is never zero. This can lead to a percent error in the OLED current of well over 3% for conservative choices of circuit parameters.

Hybrid voltage-current drive schemes have been proposed as well. Ryu *et al.* [41] developed a system in which a pixel circuit was driven first with a voltage source, and then trimmed with a current source. Settling times of 20 μs were achieved.

More exotic techniques based on in-line optical feed back [42] and MEMs-based switches [43], have been proposed. While interesting, these techniques rely on costly fabrication steps that the flat panel display industry would be reluctant to adopt.

Feedback circuits have been proposed as a method for decreasing the settling time of current-based OLED drivers. In 2006 Ashtiani *et al.* [44] developed a feedback circuit based on a simple OLED driver. The pixel settling time was only decreased to 70 μs , and an extra feedback line had to be added, decreasing the space available for pixel circuitry. At the International Solid State Circuits Conference in 2008 another feedback-based OLED current driver was presented [45]. This work

reduced the settling time to 11 μs , but still relied on an extra feedback line and an adjustable compensation scheme based on current drive to maintain stability.

2.3 Proposed OLED Driver Architectures

2.3.1 Scale up/Scale down

The speed of circuits being driven with current is directly related to the slew rate.

$$\frac{I}{C} = \frac{\Delta V}{\Delta t} \quad (2.13)$$

Since the capacitance, C , is generally a fixed value, one must increase the current, I , to achieve better settling times. In OLED driver circuits, a simple way to accomplish this is by using scale-up and scale-down current mirrors which are illustrated in Figure 2.10. The local reference cell scales up the current by a factor of K by using ratioed geometry MOSFETs. The precision current mirror transmits the scaled up current to the remote current drive cell. At the remote current drive cell, the current is again scaled down to the desired OLED current.

The benefits of this circuit are that it is simple to implement and based entirely on local matching. This scheme is rather difficult to implement without a good understanding of how the output current of the TFT devices change with geometry. Another pitfall of this architecture is that the estimated improvement in settling time is not enough to meet the requirements. Another technique to boost the performance will most likely be needed.

2.3.2 Derivative Sampling Driver

One idea for decreasing the settling time of current-programmed OLED drivers is based on a derivative sampling technique. A schematic diagram of this method

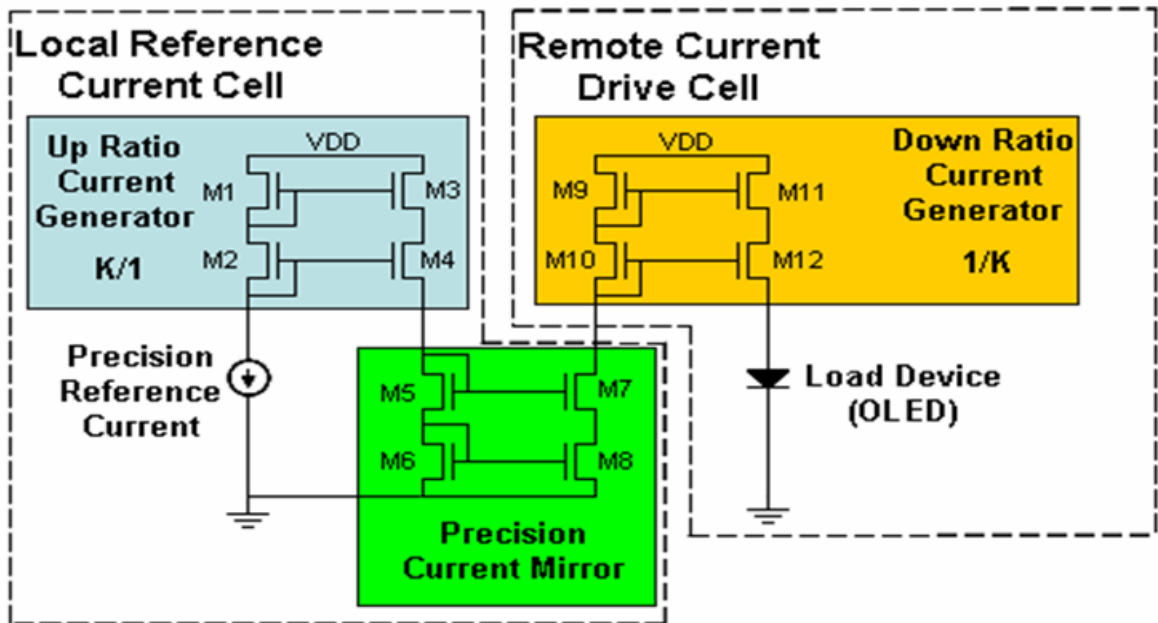


Figure 2.10: Scale up/Scale down OLED Driver

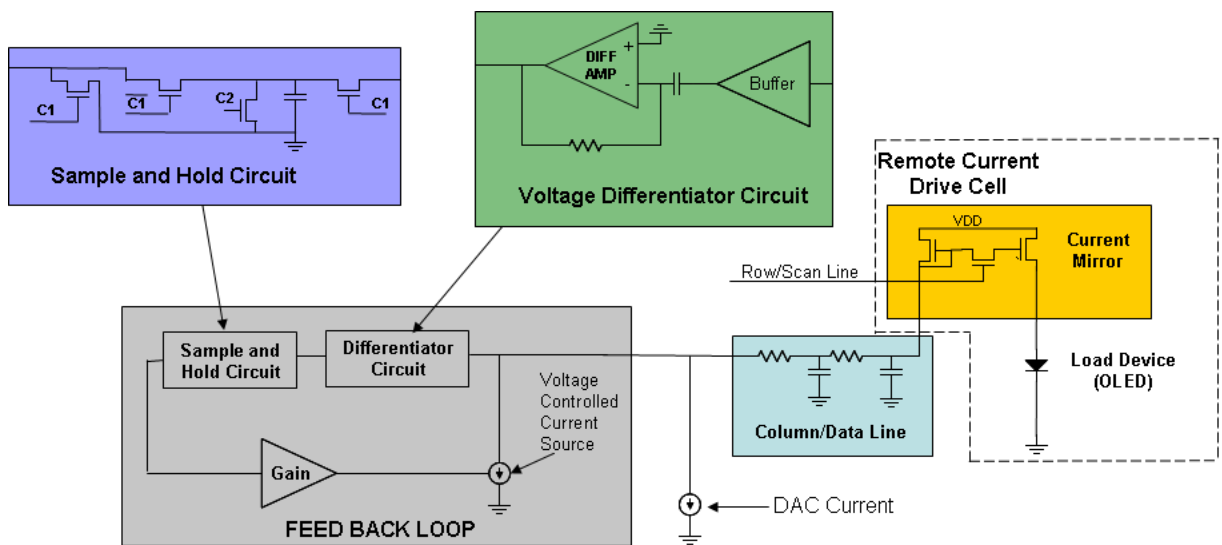


Figure 2.11: Fast Derivative Action

can be seen in Figure 2.11. The circuit operation will be described in the following text. Initially a DAC in the column driver begins sinking a current proportional to the desired light output from the OLED down the column line. At the same time, an analog differentiator circuit is continuously watching the column line and outputting a voltage proportional to the change in voltage on the column line. A sample and hold circuit captures the output from the differentiator. The value stored by the sample and hold circuit is appropriately gained, and the signal is sent to a voltage-controlled current source. The voltage-controlled current source hits the column line with a pulse of current proportional to the change in current that was sensed by the differentiator and stored by the sample-and-hold circuit. The current pulse rapidly changes the voltage on the column line, quickly bringing the system closer to its steady-state value. Next, the voltage-controlled current source is turned off and the output of the differentiator is again captured by the sample and hold circuit. The change in voltage should be less this time since the circuit is closer to settling. The voltage-controlled current source again hits the column line with a pulse of current, but smaller in magnitude than the first time. This cycle continues until the differentiator output is zero, which signals that the circuit is in steady state and the voltage at the pixel site has settled. The derivative sampling technique has been tested in Cadence VirtuosoTM using ideal components. The circuit is able to decrease the settling time for low drive currents to a very acceptable value, but insuring the stability of this circuit under all conditions will be a major challenge. Since the operation of the circuit is very non-linear, traditional control theory does not apply. Also, a fast and precise differentiator is not easy to build.

2.3.3 Binary Search Driver

Another possible circuit architecture for driving OLED displays is based on the binary search algorithm. In computer science, the binary search is a method for

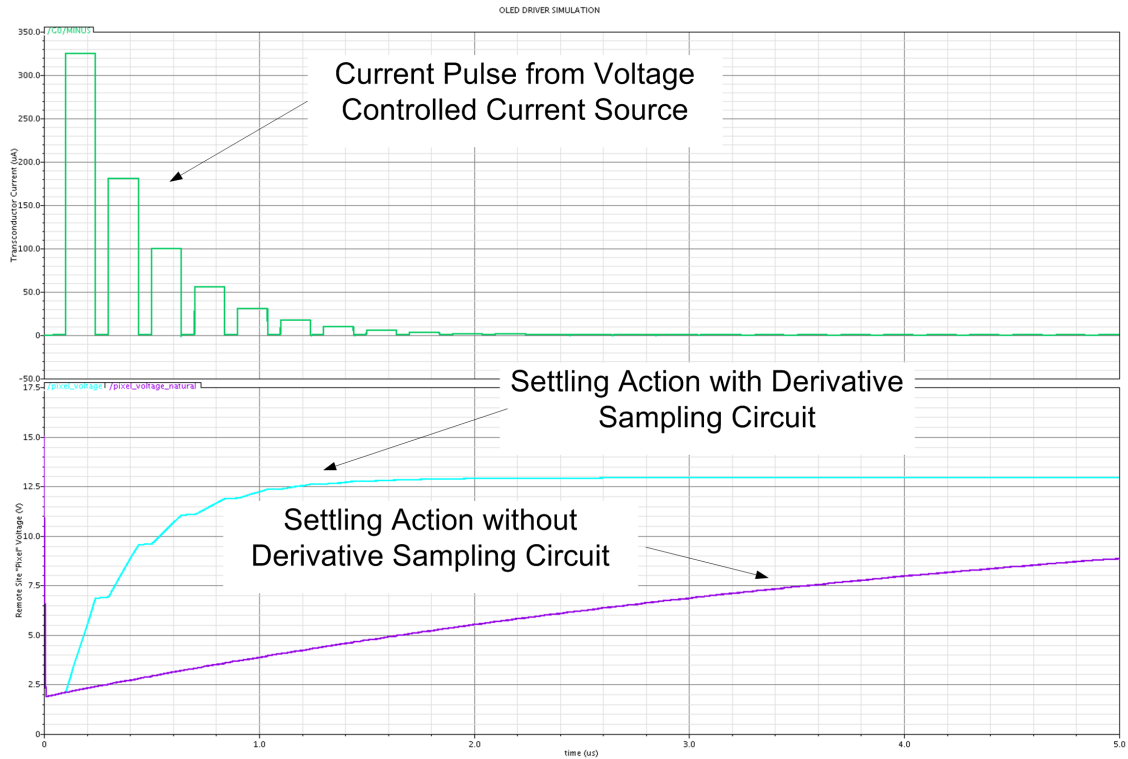


Figure 2.12: Fast Derivative Action OLED Driver

finding a particular value in a sorted list. The algorithm works by making progressively better guesses and homes in on the desired value by selecting the median element in a list and comparing it to the target value and determining if the selected value is greater than, less than, or equal to the target value. A guess that is too high becomes the new upper bound for subsequent guesses, and a guess that is too low becomes the new lower bound of future guesses.

When driving OLEDs, one does not know the gate-to-source voltage of the pixel drive transistor that corresponds to the desired current. One can still deduce whether a voltage on the drive transistor is greater than, less than, or equal to the desired voltage in the following way. Initially, a DAC in the column driver begins sinking a current proportional to the desired light output from the OLED down the column line. At the same time, the voltage on the column line is set to a test voltage value and then released. If the voltage on the column line then moves up from the

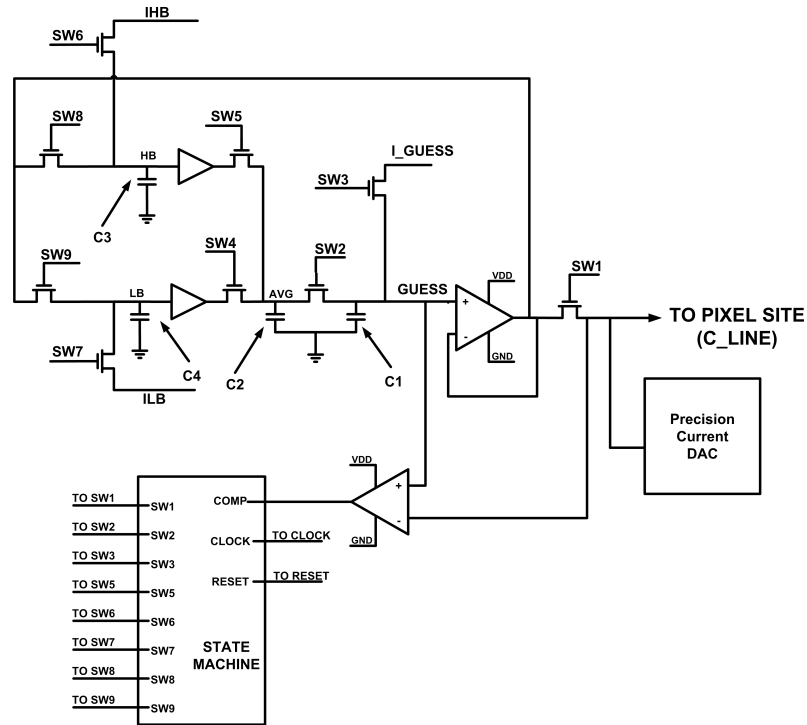


Figure 2.13: Binary Search Circuit

test value, the test voltage was too low. If the voltage on the column line moves down, the test voltage was too high, and if the column line stays at the test voltage then the test voltage is equal to the proper value. In this way, the binary search algorithm can be implemented. A circuit architecture implementing this idea has been developed, and consists of a drive buffer, averaging circuit, comparator, and a state machine. A schematic of the circuit can be seen in Figure 2.13. A block diagram outlining the algorithm can be seen in Figure 2.14. The circuit has been tested in Cadence using mostly ideal components to quickly implement the architecture. The column line and pixel circuit were modeled with real devices. Results from a Cadence simulation can be seen in Figure 2.15. The circuit was simulated using an OLED current of 6 nA and the guess voltage is plotted as a function of time as the circuit homes in on the final value. The circuit promises to be able to accurately settle the voltage on the pixel circuit quickly, and unlike the derivative sampling circuit, stability is not an issue. The performance of the circuit will depend on having

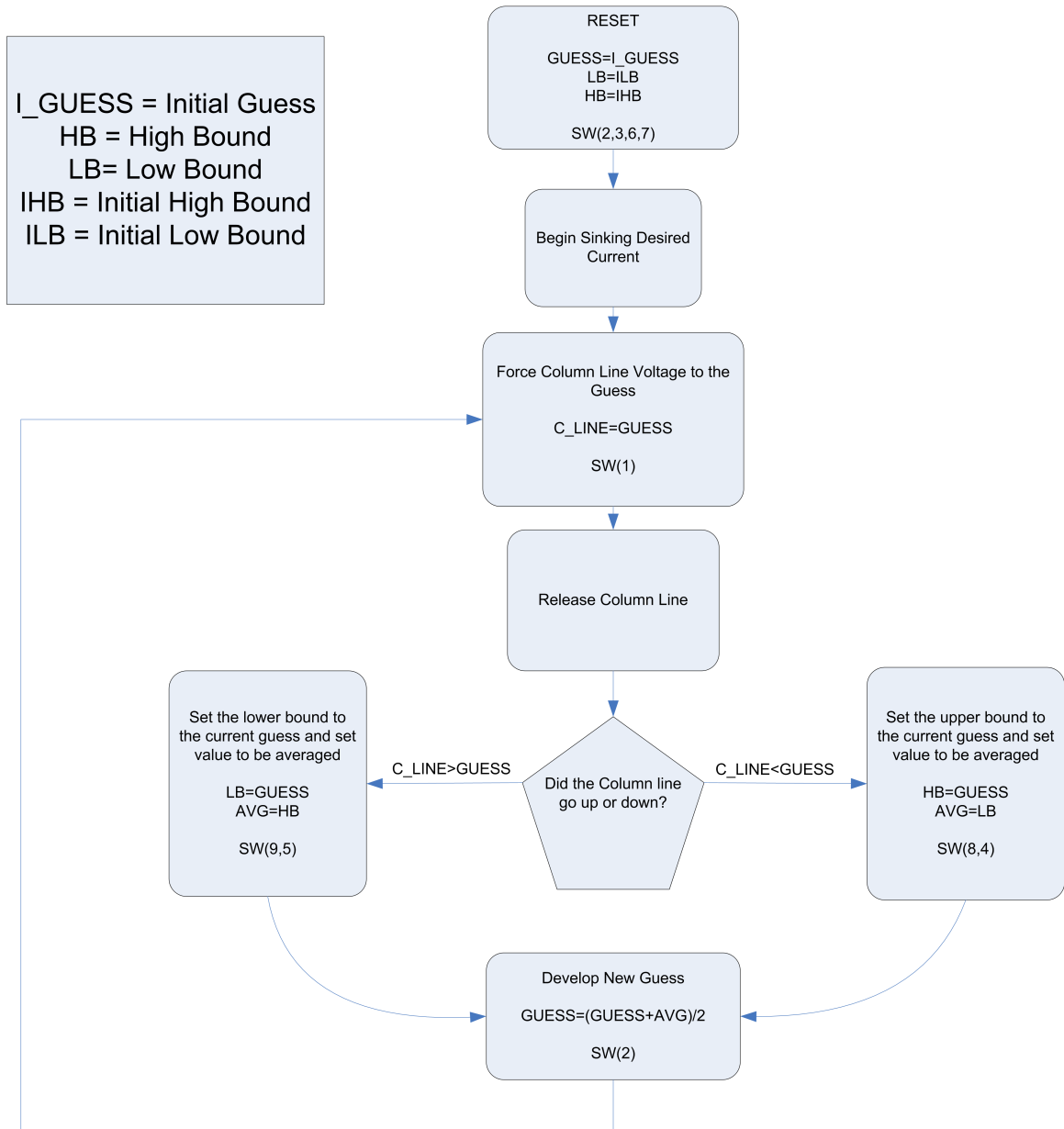
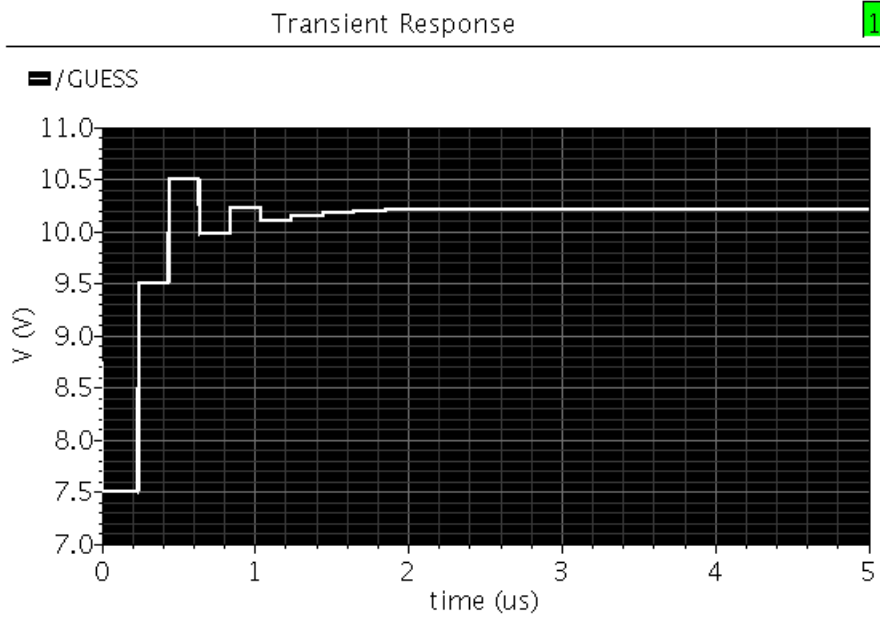


Figure 2.14: Binary Search Algorithm



a fast, precise comparator and a good output buffer.

2.4 Conclusion

In this chapter, a description of OLED devices and the issues associated with driving them has been described. In addition, three new methods of quickly and uniformly driving OLEDs have been outlined including a scale-up/scale-down driver, derivative sampled driver and a binary search based driver.

Chapter 3

Blended Compact Device Model

SiOG CMOS consists of an n -type MOSFET device relying on channel inversion to create a conducting path between the source and drain whose operation strongly resembles a traditional SOI MOSFET, and a thin-film p -type MOSFET which must be operated in accumulation to create a conducting channel. The p -type MOSFET, or PACC, has a number of unique physical features (See Chapter 1), including bulk conduction, which are not captured by industry standard compact models. In order to develop complex circuit architectures in SiOG, accurate compact device models for the SiOG PACC are needed.

This chapter describes the first of two methods of modeling the PACC device which are developed in this dissertation. In the approach described below, physically derived expressions are presented for drain current in the accumulation and depletion regions which include the correct dependence on drain voltage, film thickness, and doping level. A continuous model is realized from cutoff to accumulation by interpolating the drain current around the flatband voltage and merging the regional equations together using blending functions based on the hyperbolic tangent. The complete device model shows excellent agreement with measured results for output and transfer characteristics. The work presented in this chapter

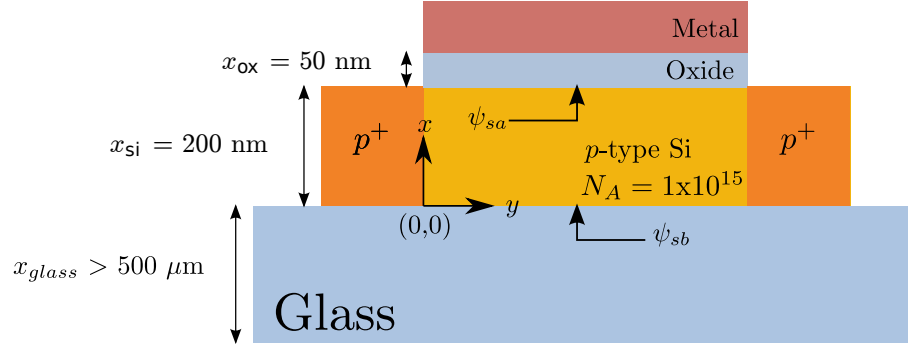


Figure 3.1: Schematic Drawing of Accumulation p -type MOSFET (PACC)

was initially published in the *IEEE Transactions on Electron Devices* [46].

3.1 Drain Current Model

Figure 3.1 shows a cross section of a SiOG PACC. The backside oxide x_{glass} is the glass substrate thickness and is many orders of magnitude larger than the top gate oxide x_{ox} . Values of film thickness x_{si} and doping concentration N_A produce a fully depleted film region for $V_{GS} = 0$ V. ψ_{sa} and ψ_{sb} represent the surface potential in the silicon film at the top and backside interfaces, respectively.

As noted in Chapter 1, it is very difficult to directly solve the multidimensional semiconductor equations analytically, therefore any attempt to develop a compact model must rely on simplifying approximations. To begin modeling this device, the gradual channel approximation (GCA) is applied (Chapter 1). Specifically, the Pao-Sah model (3.1) and (3.2) is used directly without invoking Brew's charge sheet approximation in order to model current flow in both the surface and the bulk of the device.

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{-q}{\epsilon_s} (p - n + N_D - N_A) \quad (3.1)$$

$$I_{DS} = \mu_p \frac{W}{L} \int_{V_S}^{V_D} Q_h dV_{ch} \quad (3.2)$$

The equations for the Pao-Sah model given in (1.6) and (1.7), have been updated to better represent the PACC device and are shown in (3.1) and (3.2). In (3.1), Q has been replaced with Q_h representing the total intergrated hole charge. Under the gradual channel approximation, the x and y dimensions are decoupled, breaking the 2-D problem up into two 1-D problems. The first equation is the 1-D Poisson's equation which governs the number of carriers in the channel and the second equation describes how the carriers flow from source to drain.

Since the electron concentration is negligible during normal PACC operation and never contributes to current conduction, and no donor atoms are introduced in the channel region, Equation (3.1) can be reduced to

$$\frac{\partial\psi}{\partial x} = \frac{-q}{\varepsilon_s} (p - N_A). \quad (3.3)$$

The hole concentration is given by Boltzmann statistics:

$$p = N_A e^{\frac{-\psi + V_{ch}}{\phi_t}} \quad (3.4)$$

where ϕ_t is the thermal voltage (kT/q). Combining equations (3.4) and (3.3) yields:

$$\frac{d^2\psi}{dx^2} = \frac{-q}{\varepsilon_s} \left[N_A e^{\frac{-\psi + V_{ch}}{\phi_t}} - N_A \right]. \quad (3.5)$$

There is no known solution to Equation (3.5) for this geometry. In this modeling effort, a regional approach is taken where solutions to (3.3) are found for the limiting cases of depletion and accumulation.

3.1.1 Thin-Film Depletion (Low-Current) Region

For negative values of $(-\psi + V_{ch})$, p is much smaller than fixed acceptor atom concentration, N_A , therefore the potential distribution in the silicon film is dominated

by the influence of fixed acceptor atoms. One can now simplify Poisson's equation for this case to:

$$\frac{d^2\psi}{dx^2} = \frac{qN_A}{\epsilon_s}. \quad (3.6)$$

The electric field at the silicon glass interface E_{sb} is given by the division of the silicon glass surface potential, ψ_{sb} and the glass thickness, x_{glass} . Since the glass substrate is very thick, the electric field at the back interface E_{sb} can be considered negligible.

$$E_{sb} = -\frac{\epsilon_{ox}}{\epsilon_s} \frac{\psi_{sb}}{x_{glass}} \approx 0 \quad (3.7)$$

The field at the top surface can be defined as

$$E_{sa} = -\left(\frac{\epsilon_{ox}}{\epsilon_s}\right) \left(\frac{V_{GF} - \psi_{sa}}{x_{ox}}\right) \quad (3.8)$$

where ϵ_{ox} is the permittivity of silicon dioxide and V_{GF} is equal to $V_{GS} - V_{FB}$.

$$V_{GF} = V_{GS} - V_{FB}. \quad (3.9)$$

The solution to (3.6) is then given by:

$$\psi = \frac{qN_A}{2\epsilon_s}x^2 + k_1x + k_2 \quad (3.10)$$

where k_1 and k_2 are constants that can be found by applying (3.7) and noting that ψ evaluated at $x=0$ is ψ_{sb} . This leads to,

$$\psi = \frac{qN_A}{2\epsilon_s}x^2 + \psi_{sb} \quad (3.11)$$

where ψ_{sb} can be related to the gate voltage through

$$\psi_{sb} = V_{GF} - \frac{qN_A}{C_{ox}}x_{si} - \frac{qN_A}{2\epsilon_s}x_{si}^2 \quad (3.12)$$

and C_{ox} is given by $\frac{\epsilon_{ox}}{x_{ox}}$. The depletion region drain current can then be found from the potential using the Pao-Sah double integral formula as shown below:

$$I_{DDR} = q\mu_p \frac{W}{L} \int_{V_S}^{V_D} \int_0^{x_{si}} p(x, y) dx dV_{ch}. \quad (3.13)$$

Substituting (3.4), (3.11) and (3.12) into (3.13) and evaluating the integral leads to the equation for drain current in the thin-film depletion region which is given by:

$$I_{DDR} = \xi (e^{V_D} - e^{V_S}) e^{\frac{-\psi_{sb}}{\phi_t}} \quad (3.14)$$

where ξ is given by

$$\xi = \left(\frac{W}{L} \right) \left(q\mu_p \phi_t^{\frac{3}{2}} \right) \sqrt{\frac{\epsilon_s \pi N_A}{2q}} \operatorname{erf} \left(\sqrt{\frac{N_A q}{2\epsilon_s \phi_t}} x_{si} \right). \quad (3.15)$$

3.1.2 Accumulation Region

In the accumulation region, holes dominate the shape of the potential distribution in the x -direction as:

$$\frac{d^2\psi}{dx^2} = -\frac{qN_A}{\epsilon_s} e^{-\frac{\psi - V_{ch}}{\phi_t}}. \quad (3.16)$$

Multiplying by $\frac{2d\psi}{dx}$ and integrating from the front surface to the back surface yields:

$$E_{sa}^2 - E_{sb}^2 = -\left(\frac{2qN_A\phi_t}{\epsilon_s} \right) e^{\frac{V_{ch}}{\phi_t}} \left[e^{\frac{-\psi_{sa}}{\phi_t}} - e^{\frac{-\psi_{sb}}{\phi_t}} \right]. \quad (3.17)$$

Once again, the electric field normal to the back surface is assumed to be negligible. In accumulation, the magnitude of the back gate potential is small compared to the top-gate potential; therefore, the second term in the brackets can be ignored, leading to,

$$E_{sa} = \sqrt{\frac{2qN_A\phi_t}{\epsilon_s} e^{\frac{V_{ch}}{\phi_t}}} \sqrt{e^{\frac{-\psi_{sa}}{\phi_t}}}. \quad (3.18)$$

The electric field at the front gate is again given by:

$$E_{sa} = \frac{-(V_{GF} - \psi_{sa}) \varepsilon_{ox}}{x_{ox} \varepsilon_s}. \quad (3.19)$$

Combining equations (3.18) and (3.19) and simplifying leads to

$$(\psi_{sa} - V_{GF}) C_{ox} = \sqrt{2qN_A \phi_t \varepsilon_s e^{\frac{V_{ch}}{\phi_t}}} \sqrt{e^{-\frac{\psi_{sa}}{\phi_t}}} \quad (3.20)$$

It would be favorable to solve equation (3.20) for the surface potential, ψ_{sa} , but (3.20) is transcendental and one finds that it cannot be solved for in terms of standard functions. The solution is given in terms of the Lambert W function which is defined as the solution to

$$W(x)e^{W(x)} = x \quad (3.21)$$

and has already been used to describe the surface potential of undoped double-gate MOSFETs [47] and has been implemented in some circuit simulation tools. Solving (3.20) in terms of Lambert W function yields:

$$\psi_{sa} = V_{GF} + 2\phi_t W \left(e^{\frac{V_{ch} - V_{GF}}{2\phi_t}} \frac{\sqrt{2qN_A \varepsilon_s \phi_t}}{2\phi_t C_{ox}} \right). \quad (3.22)$$

At the source end of the device, the surface potential becomes

$$\psi_{sas} = V_{GF} + 2\phi_t W \left(e^{\frac{-V_{GF}}{2\phi_t}} \frac{\sqrt{2qN_A \varepsilon_s \phi_t}}{2\phi_t C_{ox}} \right) \quad (3.23)$$

and at the drain end is given by

$$\psi_{sad} = V_{GF} + 2\phi_t W \left(e^{\frac{V_{DS} - V_{GF}}{2\phi_t}} \frac{\sqrt{2qN_A \varepsilon_s \phi_t}}{2\phi_t C_{ox}} \right). \quad (3.24)$$

Since holes dominate the potential distribution, the solution for the undoped-film symmetric double-gate MOSFET [30] can accurately describe the drain current in the accumulation region. If the expression is adjusted for a single gate geometry, the accumulation region drain current, I_{DAR} , is given by

$$\begin{aligned}
 I_{DAR} = & -\frac{W}{L}\mu_p C_{ox} \cdot \\
 & \left[(V_G(\psi_{sad} - \psi_{sas}) - \frac{1}{2}(\psi_{sad}^2 - \psi_{sas}^2) \right. \\
 & + 2\phi_t(\psi_{sad} - \psi_{sas})) \\
 & \left. + 2\phi_t n_i x_{si} \left[e^{\frac{\psi_{sbd} - V_{DS}}{\phi_t}} - e^{\frac{\psi_{sbs} - V_{DS}}{\phi_t}} \right] \right] \quad (3.25)
 \end{aligned}$$

Although I_{DAR} is continuous in all regions of operation, it is only accurate in the accumulation region where the influence of the acceptor atoms is negligible.

3.2 Compact Device Model

In order to create a complete compact device model for simulation from the two regional expressions for drain current derived above, a number of additions to the model must be made. In the previous section, two independent current equations were developed for the thin-film depletion and accumulation regions. Neither the accumulation nor depletion region current equation is accurate when the device is operating around flatband. An expression must be developed that accurately represents the drain current around flatband, and the three regional expressions must be blended together continuously. In addition, expressions representing second-order physical effects which have not been considered from the base theory must be added to the model. Finally the model must be instantiated inside a circuit simulator which has been accomplished by coding the model in Verilog-A.

3.2.1 Interpolating and Blending

In order to develop an accurate expression for current around flatband, the following interpolating function was developed

$$I_{DINT} = \frac{-1}{1 + e^{-(aV_{GS}^3 + bV_{GS}^2 + cV_{GS} + d)}}. \quad (3.26)$$

I_{DINT} is infinitely differentiable and is bounded for large values of V_{GS} . An incremental voltage ΔV (on the order of $\pm 0.25V$) around the flatband voltage is chosen as the region of interpolation to ensure that the endpoints lie on the known functions. The coefficients a , b , c , and d are found from the two boundary points and their derivatives.

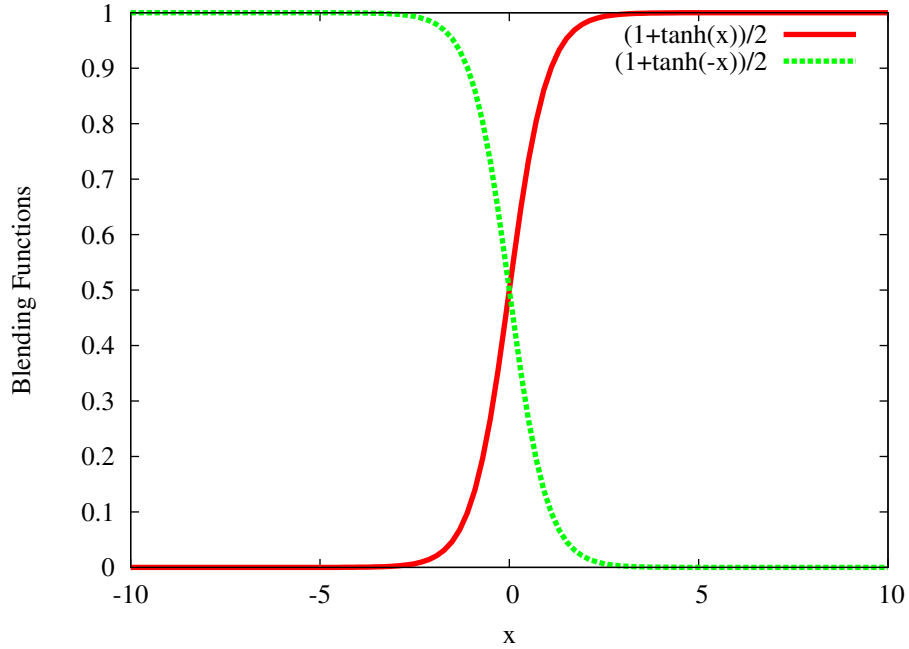


Figure 3.2: Example Blending Functions

In coding the compact model, conditional statements can be avoided [23] and continuity maintained by linking the two known regions and the interpolating expression with a hyperbolic tangent (\tanh) blending function [48]. The hyperbolic

tangent is part of a class of functions called sigmoid functions which have an S shape. $\tanh(x)$ approaches 1 as x goes to infinity and -1 as x approaches minus infinity. Therefore $(1 + \tanh(x))/2$ saturates at values of 1 and 0 as x approaches plus and minus infinity. The function $(1 + \tanh(x))/2$ and its mirror image $(1 - \tanh(x))/2$ are called blending functions and are plotted in Figure 3.2. Since the blending functions have the property that in the region where they saturate one of them is 0 and the other is 1, and in between the saturation regions there is a smooth transition, they can be used to continuously link two functions.

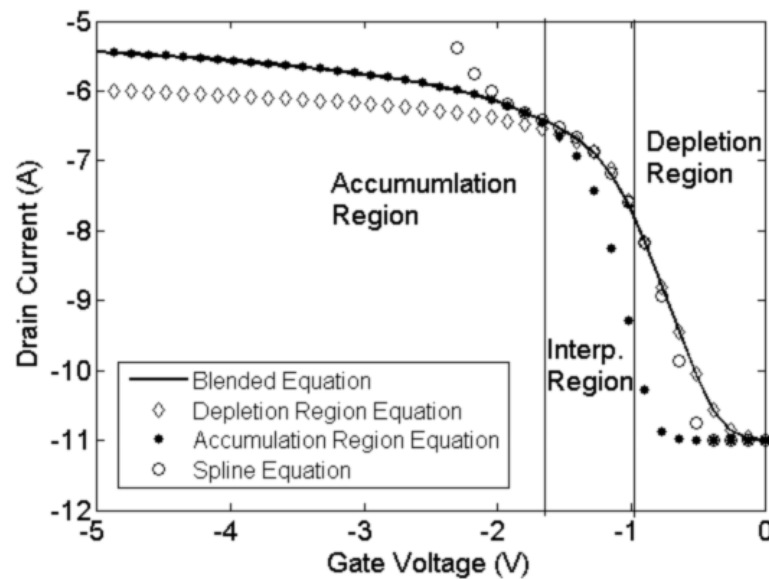


Figure 3.3: Semilog plot of drain current versus gate voltage depicting the range of operation for each of the developed regional equations.

Here they are used to link the three regional drain current expressions, as shown in Figure 3.3. The following unified expressions result from blending the accumulation region (3.27) and the interpolating function (3.26). An offset voltage, ΔV (on the order of ± 0.25 V) around flatband is chosen to ensure that the endpoints lie on

known functions and to minimize the interpolated region.

$$I_{DA} = I_{DAR} \frac{1}{2} [1 - \tanh(z(V_{GS} - (V_{FB} - \Delta V)))] + I_{DINT} \frac{1}{2} [1 + \tanh(z(V_{GS} - (V_{FB} - \Delta V)))] \quad (3.27)$$

By blending in the depletion region with (3.27), the complete PACC drain-current behavior from cutoff to accumulation results in

$$I_D = I_{DA} \frac{1}{2} [1 - \tanh(z(V_{GS} - (V_{FB} - \Delta V)))] + I_{DDR} \frac{1}{2} [1 + \tanh(z(V_{GS} - (V_{FB} - \Delta V)))] \quad (3.28)$$

In (3.27) and (3.28), z defines the shape of the transition region and is experimentally found to be any number larger than 20. Using this method to link the three equations ensures a continuous drain current expression which is essential for circuit simulation.

3.2.2 Second Order Effects

To predict drain current behavior accurately, the influence of traps, channel-length modulation, fringing field induced barrier lowering (FFIBL, see Chapter 5), and mobility degradation must be included in the model.

The presence of interface traps in the PACC device alters the slope in the low-current region. A subthreshold slope parameter κ has been added to (3.14) to account for this change. The updated equation is shown below.

$$I_{DDR} = \xi (e^{V_D} - e^{V_S}) e^{\frac{-\psi_{sb}}{\kappa \phi_t}} \quad (3.29)$$

Channel length modulation for long channel PACC devices can be modeled with the Early voltage fitting parameter l_A and a \tanh function to gradually introduce the

effect in the saturation region.

$$I_{DCM} = I_D \left[-1 + \frac{1}{2} (V_{DS} l_A) (1 + \tanh(-A (V_{DS} - (V_{GS} - V_{FB})))) \right] \quad (3.30)$$

I_{DCM} is the drain current with the addition of channel length modulation and A determines the curvature in the transition for the linear region to the saturation region.

An empirical expression [49] that represents the mobility degradation in MOS-FETs and has been found to work well for SiOG CMOS devices is given by:

$$\mu = \frac{\mu_o}{1 + \left(\frac{E_{EFF}}{E_o} \right)^v} \quad (3.31)$$

where μ_o , E_o , and v are fitting parameters. The form of E_{EFF} has been taken from [49], but modified for the PACC devices since the turn-on voltage for the PACC device is V_{FB} and not V_T .

$$E_{EFF} = \frac{\text{abs}(V_G - V_{FB})}{6x_{ox}} + \frac{\text{abs}(V_{FB} - V_z)}{3x_{ox}} \quad (3.32)$$

3.3 Results

Measurements were conducted with a $6 \mu m \times 6 \mu m$ SiOG PACC device with a silicon film thickness of 2000 and a top gate oxide thickness of 500 . Current-Voltage characteristics were measured using an Agilent B1500A semiconductor parameter analyser and an R&K 680 Probe Station. The compact model was implemented in both MATLAB and Cadence Spectre using Verilog-A.

The measured results are depicted with discrete data points, and the modelled results are shown as a continuous line. Figure 3.4 shows the I-V transfer characteristics with $V_{DS} = -0.1V$ and $V_{DS} = -5.1V$. The modeled linear $I-V$ characteristics

in Figure 3.4 accurately show the measured data including the effects of mobility degradation. The output characteristics also show good agreement with measured results including the effects of high drain voltage.

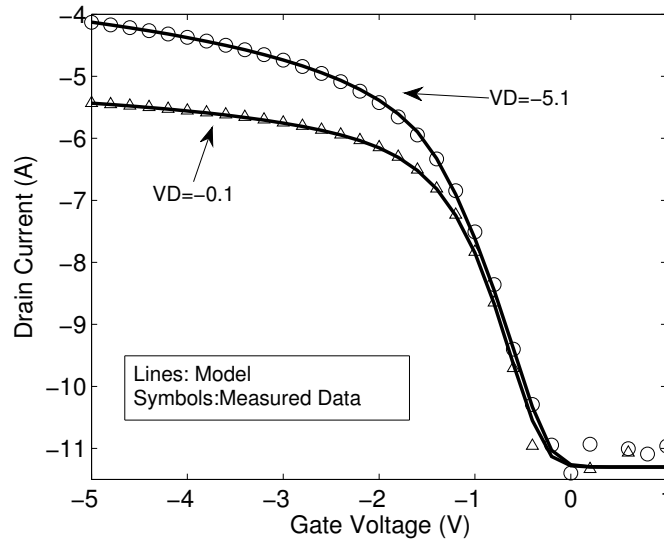


Figure 3.4: Semi-Log plot of Drain Current versus Gate Voltage with the Source Voltage set to 0 V

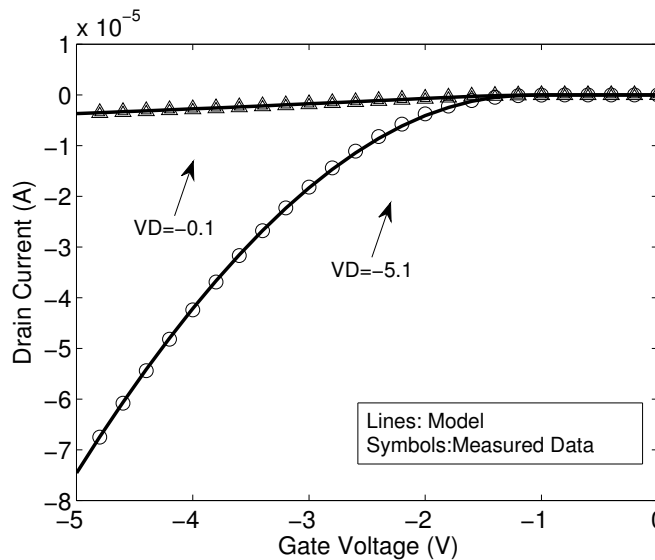


Figure 3.5: Plot of Drain Current versus Gate Voltage with the Source Voltage set to 0 V

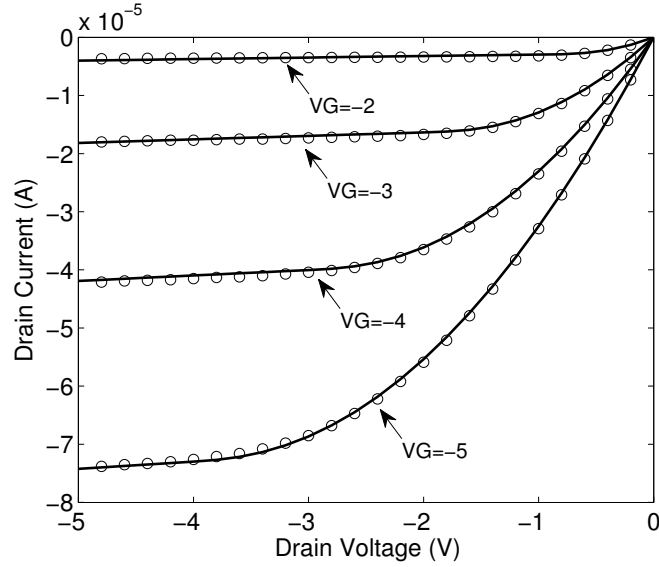


Figure 3.6: Plot of Drain Current versus Drain Voltage with the Source Voltage set to 0 V

3.4 Continuing Efforts

Although the model developed in this chapter accurately predicts the current voltage characteristics for SiOG PACC devices, it is not perfect. After extensive testing of the model, a number of problems associated with the use of the interpolating function, Equation (3.26), to link the two physical expressions together have come up. The accuracy of the equation is highly dependent on where the end-points for the physical expressions are chosen. In addition, the monotonicity of the interpolating function is not guaranteed, sometimes leading to anomalies in the current voltage characteristics which are not physically realizable. Although both of these problems can be mitigated through the use of complicated parameter extraction routines, new methods for modeling the device were explored. This exploration lead to the charge-based modeling technique for SiOG CMOS devices described in the next chapter. This approach results in a single expression for drain current valid in all regions of operation which does not suffer from the problems associated with interpolating functions.

Chapter 4

Charge-Based Model

In Chapter 3, the DC characteristics of a SiOG PACC device were successfully modeled, but relied on complex interpolating and blending functions to link the equations representing the strong accumulation region to the equations representing the depletion region. This chapter describes a new compact modeling methodology that eliminates the need to apply blending functions to regional solutions for drain current. The modeling method is based directly on the Pao-Sah equation and the 1-D Gauss' law in a similar manner to other recent charge-based models such as BSIM5 [50]. The equations are formulated such that the need for an exact solution to Poisson's equation is limited. Poisson's equation is used to describe the relationship between the majority carrier concentration at the surface of the device to the total majority carrier charge in the device. This relationship is closely approximated through the use of a simple rational polynomial, circumventing the need for an exact solution to Poisson's equation. The resulting models are comprised of single C^∞ expressions for drain current accurately modeling both surface and bulk conduction valid in all regions of operation. In this way, a single-piece model is created without the need for blending functions. We begin by developing the methodology and deriving the core long-channel DC drain current equation for

the PACC device.

The development of the charge-based modeling technique has been an on-going effort. The initial work was presented at the *Second International Workshop on Compact Thin-Film Transistor Modeling for Circuit Simulation* in London [51]. That initial work was expanded on and published in an article in the *IEEE Journal of Display Technology* [52]. Methods for simplifying the model equations and making the resulting expressions more robust, as well as a method of extending the model to inversion mode devices, were presented at the 218th *Meeting of the Electrochemical Society* in Las Vegas [53].

The second part of this chapter focuses on additions to the core model making it more useful for circuit designers. A compact model must include more than just the equations describing the long channel current-voltage characteristics of the p -type device. A model for the n -type device must also be included. Secondary effects such channeling-length modulation, fringing-field-induced barrier lowering, and mobility degradation must be added to the model. In order to allow for transient and small signal simulation, the AC characteristics of the device must also be modeled. Finally, the entire model should be instantiated inside a circuit simulator so that the model can be utilized by engineers.

4.1 Long-Channel Model

4.1.1 Problem Setup

The derivation of the charge-based PACC model begins with the Pao-Sah double integral equation for drain current, shown in (4.1), which models the influence of both surface and bulk conduction over all regions of operation.

$$I_{DS} = q\mu_p \frac{W}{L} \int_{V_S}^{V_D} \int_0^{x_{si}} p(x, y) dx dV_{ch} \quad (4.1)$$

The inside integral, equation (4.2), sums up the total hole charge per area in a slice of the device and will be defined as Q_h for convenience. All Q terms are per area unless otherwise stated.

$$Q_h = q \int_0^{x_{si}} p(x, y) dx \quad (4.2)$$

Substituting equation (4.2) into (4.1) results in the single integral expression for drain current,

$$I_{DS} = \mu_p \frac{W}{L} \int_{V_S}^{V_D} Q_h dV_{ch}. \quad (4.3)$$

Since it is difficult to find the function $Q_h(V_{ch})$ to directly compute the integral in equation (4.3), the equation is reformulated by changing the integration variable to Q_h . This leads to the following expression for drain current

$$I_{DS} = \mu_p \frac{W}{L} \int_{Q_{hS}}^{Q_{hD}} Q_h \left(\frac{dV_{ch}}{dQ_h} \right) dQ_h. \quad (4.4)$$

Thus the problem is transformed to one of finding an expression for dV_{ch}/dQ_h in terms of Q_h . This expression can be found through the application of the 1-D Gauss' Law,

$$E_{sa} - E_{sb} = \frac{Q_h + Q_f}{\epsilon_s} \quad (4.5)$$

which states that the electric flux density at the top surface minus the electrical flux density at the back surface is equal to the total charge enclosed by the two surfaces. In (4.5), Q_f is the charge due to the fixed acceptor atoms in the silicon film. The electric field at the top surface (silicon-oxide interface), E_{sa} is given by,

$$E_{sa} = - \left(\frac{V_{GF} - \psi_{sa}}{x_{ox}} \right) \left(\frac{\epsilon_{ox}}{\epsilon_s} \right) - \frac{Q_{sa}}{\epsilon_s} \quad (4.6)$$

and the electric field at the back surface (silicon-glass interface), E_{sb} is described by,

$$E_{sb} = \frac{Q_{sb}}{\varepsilon_s}. \quad (4.7)$$

In (4.6) and (4.7) Q_{sa} and Q_{sb} represent fixed charge at the silicon-oxide and silicon-glass interfaces, respectively. If the silicon-glass interface was ideal (no interface charge), then the field at that boundary would be approximately equal to 0 (See Chapter 3). Real devices have a non-negligible amount of fixed charge at the silicon-glass interface leading to the electrostatic boundary condition in (4.7). Combining equations (4.5), (4.6), (4.7) yields:

$$V_{GF} = \psi_{sa} - \left(\frac{1}{C_{ox}} \right) (Q_h + Q_f + Q_{sa} + Q_{sb}) \quad (4.8)$$

where C_{ox} is given by ε_{ox}/x_{ox} . The surface potential can be related to the hole concentration at the silicon-oxide interface through Boltzmann statistics,

$$\psi_{sa} = V_{ch} - \phi_t \ln \left(\frac{p_{sa}}{N_A} \right) \quad (4.9)$$

where p_{sa} is the hole concentration at the silicon oxide interface. Combining (4.8) and (4.9) yields the results the following expression for V_{ch} :

$$V_{ch} = V_{GF} + \phi_t \ln \left(\frac{p_{sa}}{N_A} \right) + \frac{Q_h + Q_f + Q_{sa} + Q_{sb}}{C_{ox}}. \quad (4.10)$$

To find dV_{ch}/dQ_h , one must first express (4.10) in terms of only Q_h and then differentiate with respect to Q_h . In short, p_{sa} must be expressed in terms of Q_h .

The hole concentration at the top surface, p_{sa} , can be expressed as a function of the total hole charge, Q_h by solving the 1-D Poisson's equation for the PACC device

shown below:

$$\frac{d^2\psi}{dx^2} = \frac{-q}{\varepsilon_s} \left[N_A e^{\frac{-\psi(x)+V_{ch}}{\phi_t}} - N_A \right]. \quad (4.11)$$

Since there is no known analytical solution to (4.11), an approximate expression for the hole concentration at the surface must be used.

4.1.2 Approximating $p_{sa}(Q_h)$

To better understand how p_{sa} varies as a function of Q_h , the limiting behavior of the solution in separate regions will be investigated.

For negative values of $-\psi(x) + V_{ch}$, $p(x, y)$ is much smaller than fixed acceptor atom concentration, N_A , therefore the potential distribution in the silicon film is dominated by the influence of fixed acceptor atoms. Under this condition, the device is said to be operating in depletion. One can now rewrite Poisson's equation for this case as

$$\frac{d^2\psi}{dx^2} = \frac{qN_A}{\varepsilon_s}. \quad (4.12)$$

Using the potentials and (4.7) as boundary conditions, the solution to (4.12) is given by:

$$\psi(x) = \frac{qN_A}{2\varepsilon_s}x^2 - \frac{qN_A}{2\varepsilon_s}x_{si}^2 - \frac{Q_{sb}}{\varepsilon_s}x + \frac{Q_{sb}}{\varepsilon_s}x_{si} + \psi_{sa}. \quad (4.13)$$

From (4.13), the total mobile hole charge in the depletion region, Q_{hdep} can be found by integrating the mobile holes from the bottom of the silicon to the top:

$$Q_{hdep} = \int_0^{x_{si}} qN_A e^{-\left(\frac{\psi(x)-V_{ch}}{\phi_t}\right)} dx. \quad (4.14)$$

Computing the integral results in,

$$Q_{hdep} = p_{sad}C_1. \quad (4.15)$$

The first term in (4.15), p_{sad} is the hole concentration at the silicon-oxide interface when the device is operating under depletion, and C_1 is a constant based entirely on process parameters equal to

$$C_1 = \left[e^{\frac{(Q_{sb} - qN_A x_{si})^2}{2\varepsilon_s q N_A \phi_t}} \sqrt{\frac{q\varepsilon_s \pi \phi_t}{2N_A}} \right] \left[\operatorname{erf} \left(\frac{Q_{sb}}{\sqrt{2\varepsilon_s q N_A \phi_t}} \right) - \operatorname{erf} \left(\frac{Q_{sb} - qN_A x_{si}}{\sqrt{2\varepsilon_s q N_A \phi_t}} \right) \right]. \quad (4.16)$$

It can be seen that the expression for the hole concentration at the top surface in depletion is a linear function of the total mobile hole charge given by:

$$p_{sad} = \frac{Q_{hdep}}{C_1}. \quad (4.17)$$

In the accumulation region, holes dominate the shape of the potential distribution in the x -direction. Writing Poisson's equation for this case leads to the following expression:

$$\frac{d^2\psi}{dx^2} = -\frac{qN_A}{\varepsilon_s} e^{\frac{(-\psi(x) + V_{ch})}{\phi_t}}. \quad (4.18)$$

Multiplying by $\frac{2d\psi}{dx}$ and integrating from the front surface to the back surface yields:

$$E_{sa}^2 - E_{sb}^2 = \frac{-2qN_A\phi_t}{\varepsilon_s} e^{\frac{V_{ch}}{\phi_t}} \left[e^{-\frac{\psi_{sa}}{\phi_t}} - e^{-\frac{\psi_{sb}}{\phi_t}} \right]. \quad (4.19)$$

E_{sb} is assumed to be small compared to E_{sa} in this region and can be neglected. Furthermore, in accumulation the magnitude of $e^{-\frac{\psi_{sb}}{\phi_t}}$ is small compared to $e^{-\frac{\psi_{sa}}{\phi_t}}$. Accordingly, equation (4.19) reduces to

$$E_{sa} = \sqrt{\frac{2q\phi_t}{\varepsilon_s}} \sqrt{N_A e^{-\frac{\psi_{sa} - V_{ch}}{\phi_t}}}. \quad (4.20)$$

Using Gauss' law and noting that the last term in (4.20) is the hole concentration at the top surface, it is seen that

$$p_{saa} = \frac{Q_h^2}{C_2}, \quad (4.21)$$

where C_2 is given by

$$C_2 = 2q\varepsilon_s\phi_t. \quad (4.22)$$

From equations (4.21) and (4.17) it can be seen that the hole concentration at the surface varies from a linear to a quadratic function of the total integrated hole charge as the device varies from depletion to strong accumulation. The function should vary smoothly over the region between the two extremes. This behavior can be approximated by a rational polynomial of the form:

$$p_{sa} = \frac{a + bQ_h + cQ_h^2 + dQ_h^3 + rgQ_h^4}{1 + fQ_h + gQ_h^2} \quad (4.23)$$

where the coefficients remain to be determined.

From physical considerations, it is known that if Q_h is zero, then p_{sa} must also be zero; therefore a is zero. In the limit of small Q_h (4.23) becomes

$$p_{sa} \approx bQ_h. \quad (4.24)$$

Comparing (4.24) to (4.17), one can see that

$$b = \frac{1}{C_1}. \quad (4.25)$$

In the limit of large Q_h (4.23) becomes

$$p_{sa} \approx rQ_h^2, \quad (4.26)$$

and from (4.22) it can be seen that

$$r \approx \frac{1}{C_2}. \quad (4.27)$$

The remaining four coefficients c , d , f , and g could be determined by solving the system of four equations and four unknowns using data points from (4.21) and (4.17). However, this approach can generate singularities in the final expression for the region of interest. Instead, only three data points are used to express the c , d , and g in terms of f . One of the data points is chosen in the depletion region and is generated with (4.17) and another data point is chosen in the quadratic region and is generated with (4.21). The third point can be chosen to be in either region, or if a higher degree of accuracy is desired, it can be chosen around the flatband region using a numeric or series solution to (4.11). Expressing the coefficients g , c , and d in terms of the variable f yields the results

$$\begin{aligned} g &= \alpha_1 f + \beta_1 \\ c &= \alpha_2 f + \beta_2 \\ d &= \alpha_3 f + \beta_3 \end{aligned} \tag{4.28}$$

where (α_i, β_i) ($i=1,2,3$) are constants determined from the three data points mentioned previously.

In order to avoid singularities, the roots of the denominator of (4.23) must be forced to be either negative or imaginary. Negative roots were chosen to simplify number representation. The roots of the denominator of (4.23) are given by

$$1 + fQ_h + gQ_h^2 = 0. \tag{4.29}$$

The solutions of (4.29) are found by applying the quadratic formula:

$$p_{sroots} = \frac{-f \pm \sqrt{f^2 - 4g}}{2}. \tag{4.30}$$

To make both roots negative, the following inequality must hold:

$$0 > -f \pm \sqrt{f^2 - 4g}. \quad (4.31)$$

It has been found empirically that f can be any large number greater than zero with little effect on the final behavior of the function. If the condition $f > 0$ is stipulated then the inequality (4.31) has two cases, one where the sign of the square root is positive, and one where the sign square root is negative. The case where the sign of the square root is positive is shown below.

$$0 > -f + \sqrt{f^2 - 4g} \quad (4.32)$$

Adding f to both sides and squaring shows that

$$g > 0. \quad (4.33)$$

Now looking at the other case

$$0 > -f - \sqrt{f^2 - 4g} \quad (4.34)$$

and adding f to both sides results in

$$f > -\sqrt{f^2 - 4g}. \quad (4.35)$$

Since it has been stipulated that $f > 0$, (4.35) is always true. The final result is that if f is forced to be positive, then g must also be positive to avoid singularities. It follows from (4.28) that if f is a large positive number (it will be shown below that it is advantageous to let $f \rightarrow +\infty$) and it is required that $g > 0$ then β_1 can be ignored, and therefore α_1 must also be positive to avoid singularities. To enforce this

condition, α_1 must be replaced by $|\alpha_1|$. It has been found empirically that replacing α_1 by $|\alpha_1|$ not only avoids singularities, but also gives a good fit to the data.

Substituting (4.28) into (4.23) results in

$$p_{sa} = \frac{bQ_h + (\alpha_2 f + \beta_2) Q_h^2 + (\alpha_3 f + \beta_3) Q_h^3 + r(|\alpha_1 f| + \beta_1) Q_h^4}{1 + fQ_h + (|\alpha_1|f + \beta_1) Q_h^2}. \quad (4.36)$$

Dividing top and bottom by f yields:

$$p_{sa} = \frac{\frac{b}{f}Q_h + \left(\alpha_2 + \frac{\beta_2}{f}\right) Q_h^2 + \left(\alpha_3 + \frac{\beta_3}{f}\right) Q_h^3 + r\left(|\alpha_1| + \frac{\beta_1}{f}\right) Q_h^4}{\frac{1}{f} + Q_h + \left(|\alpha_1| + \frac{\beta_1}{f}\right) Q_h^2}. \quad (4.37)$$

Because f can be any large positive number, let $f \rightarrow +\infty$. Letting $f \rightarrow \infty$ in (4.37) results in the simplified expression

$$p_{sa} = \frac{\alpha_2 Q_h + \alpha_3 Q_h^2 + r|\alpha_1| Q_h^3}{1 + |\alpha_1| Q_h}. \quad (4.38)$$

Dividing through by α_1 yields

$$p_{sa} = \frac{\frac{\alpha_2}{|\alpha_1|} Q_h + \frac{\alpha_3}{|\alpha_1|} Q_h^2 + rQ_h^3}{\frac{1}{|\alpha_1|} + Q_h}. \quad (4.39)$$

The final form of the rational polynomial approximation given by:

$$p_{sa} = \frac{CQ_h + DQ_h^2 + rQ_h^3}{F + Q_h} \quad (4.40)$$

where $C \equiv \alpha_2/|\alpha_1|$, $D \equiv \alpha_3/|\alpha_1|$, and $F \equiv 1/|\alpha_1|$. Although it might be tempting to start with this simplified rational polynomial, a direct method for solving for the coefficients while simultaneously controlling the location of the pole has not been found.

4.1.3 Drain Current Derivation

Once the coefficients in (4.40) have been determined, all of the information needed to evaluate the drain current is known. Substituting (4.40) into (4.10) yields:

$$V_{ch} = V_{GF} + \phi_t \ln \left(\frac{CQ_h + DQ_h^2 + rQ_h^3}{N_A(F + Q_h)} \right) + \frac{Q_h + Q_f + Q_{sa} + Q_{sb}}{C_{ox}}. \quad (4.41)$$

Differentiating (4.41) with respect to Q_h results in

$$\frac{dV_{ch}}{dQ_h} = \frac{1}{C_{ox}} + \frac{\phi_t}{Q_h} \left(\frac{F}{F + Q_h} + \frac{DQ_h + 2rQ_h^2}{C + DQ_h + rQ_h^2} \right). \quad (4.42)$$

Substituting the derivative into (4.4) and integrating with respect to Q_h leads to the following expression for drain current:

$$I_{DS} = \mu_p \frac{W}{L} \phi_t (I_f [Q_{hD}] - (I_f [Q_{hS}])) \quad (4.43)$$

where the function I_f is given by

$$I_f [Q_h] = \left[2Q_h + \frac{Q_h^2}{2\phi_t C_{ox}} + \frac{(D^2 - 4Cr) \arctan \left(\frac{D+2rQ_h}{\sqrt{-D^2+4Cr}} \right)}{r\sqrt{-D^2+4Cr}} \right] + \left[F \ln (F + Q_h) - \frac{D}{2r} \ln (C + DQ_h + rQ_h^2) \right]. \quad (4.44)$$

Q_{hD} and Q_{hS} represent the total mobile hole charge at the source and at the drain, respectively. Q_{hS} and Q_{hD} can be found in terms of the terminal voltages by solving (4.41) at $y = 0, V_{ch} = V_S$ and $y = L, V_{ch} = V_{DS}$, respectively, using numerical methods. The exact algorithm used for the efficient solution of (4.41) is described in Section 4.2.3 where the Verilog-A implementation is discussed.

4.2 Compact Model

The focus of this section is to describe the effort needed to turn the equations derived above into a useful model for circuit designers. A number of important additions to the model are described below including the addition of secondary effects and capacitance equations. In addition, the model is extended to n -type devices and the method of instantiating the model in the circuit simulator is described.

4.2.1 Secondary Effects

To predict drain current behavior accurately, the influence of traps, channel-length modulation, fringing field induced barrier lowering (FFIBL, see Chapter 5), and mobility degradation must be included in the model.

All of the secondary effects except mobility degradation are introduced into the model through an effective gate voltage. V_{GF} in equation (4.41) is replaced with V_{GEFF} ,

$$V_{ch} = V_{GEFF} + \phi_t \ln \left(\frac{CQ_h + DQ_h^2 + rQ_h^3}{N_A(F + Q_h)} \right) + \frac{Q_h + Q_f + Q_{sa} + Q_{sb}}{C_{ox}} \quad (4.45)$$

where V_{GEFF} is given by

$$V_{GEFF} = V_{G\kappa} + \Delta_{VFBL}. \quad (4.46)$$

V_{GEFF} consists of $V_{G\kappa}$ which modifies the gate voltage to account for the subthreshold slope degradation, and Δ_{VFBL} , which is an offset factor used to account for both FFIBL and channel length modulation. $V_{G\kappa}$ is constructed using blending functions

similar to those introduced in Chapter 3 to link the regional current expressions together and is given by:

$$\begin{aligned}
 V_{G\kappa} &= \frac{V_{GF}}{2} (1 + \tanh[-P_{VG}(V_{GF} - OS_{VG})]) \\
 &+ \frac{V_{GF}}{2\kappa} (1 + \tanh[P_{VG}(V_{GF} - OS_{VG})]). \quad (4.47)
 \end{aligned}$$

In (4.47), the blending functions are used to divide the gate voltage down by the subthreshold slope parameter, κ , in the depletion region, but not in the accumulation region with a smooth transition in between. P_{VG} controls how quickly the transition is made, while OS_{VG} is an offset describing where the middle of the transition occurs. P_{VG} and OS_{VG} must be found empirically.

The term Δ_{VFBT} also uses sigmoid blending functions to transition between the value needed for the accumulation region due to channel length modulation, and the value needed for FFIBL in the depletion region. In this case, the sigmoid blending functions are of the form $\frac{x}{\sqrt{1+x^2}}$ which was empirically found to match the data better than the previously used hyperbolic blending functions. Δ_{VFBT} is shown below

$$\begin{aligned}
 \Delta_{VFBT} &= \frac{\Delta_{VFBA}}{2} \left(1 + \frac{-P_{\Delta VFBT}(V_{G\kappa} - OS_{VD})}{\sqrt{1 + [P_{\Delta VFBT}(V_{G\kappa} - OS_{VD})]^2}} \right) \\
 &+ \frac{\Delta_{VFBD}}{2} \left(1 + \frac{P_{\Delta VFBT}(V_{G\kappa} - OS_{VD})}{\sqrt{1 + [P_{\Delta VFBT}(V_{G\kappa} - OS_{VD})]^2}} \right) \quad (4.48)
 \end{aligned}$$

where Δ_{VFBA} and Δ_{VFBD} are the values of the offset factor in accumulation and depletion, respectively. $P_{\Delta VFBT}$ controls how quickly the transition is made from Δ_{VFBA} to Δ_{VFBD} , while OS_{VD} is an offset describing where the middle of the transition occurs.

Δ_{VFBA} is the factor which describes channel length modulation and is described

empirically by

$$\Delta_{VFBA} = (V_{DS} - V_{G\kappa}) \frac{l_A}{10^4 L} (1 + \tanh[-P_{\Delta_{VFBA}} (V_{DS} + OS_{V_{G\kappa}})]) \quad (4.49)$$

while Δ_{VFBD} is a factor which describes the influence of FFIBL

$$\Delta_{VFBD} = V_{DS} l_F \quad (4.50)$$

where l_F describes the severity of the FFIBL effect.

Mobility degradation is introduced into the model by allowing mobility to be a function of the gate voltage. The expression for drain current is then given by

$$I_{DS} = \mu [V_{GEFF}] \frac{W}{L} \phi_t (I_f [Q_{hD}] - (I_f [Q_{hS}])) \quad (4.51)$$

where the I_f function is given by (4.44). An empirical expression [49] that represents the mobility degradation in MOSFETs and has been found to work well for SiOG CMOS devices is given by:

$$\mu (V_{GEFF}) = \frac{\mu_o}{1 + \left(\frac{E_{EFF}}{E_o}\right)^v} \quad (4.52)$$

where μ_o , E_o , and v are fitting parameters. The form of E_{EFF} has been taken from [49], but modified for the PACC devices since the turn on voltage for the PACC device is V_{FB} and not V_T .

$$E_{EFF} = \frac{\text{abs}(V_{GEFF} - V_{FB})}{6x_{ox}} + \frac{\text{abs}(\Delta_{VFBD} - V_z)}{3x_{ox}} \quad (4.53)$$

Using the above equations, the secondary effects can be added to the long channel model. Although the equations shown above allow the long channel model to

match measured data, a method for adding secondary effects based on the integrated charges Q_{hS} and Q_{hD} at the source and drain rather than the terminal voltages would be a cleaner implementation, and perhaps be the basis for future work.

4.2.2 Capacitance Model

One advantage of a charge-based modeling technique is that it leads directly to a model for the intrinsic capacitances associated with the SiOG transistors. Including a capacitance model in the compact model enables both transient and AC simulation.

The method used for developing a charge conserving capacitance model is based on the work first presented by Ward and Dutton [54]. For any region of space, the current is related to the time derivative of charge as

$$i = \frac{dQ}{dt} \quad (4.54)$$

where i is the net current flowing into the region and Q is the total charge contained in the region. Hence, the AC current flowing into the gate is given by

$$i_G = \frac{dQ_G}{dt}, \quad (4.55)$$

while the current flowing in the source and drain is equal to

$$i_{(S+D)} = \frac{d(Q_S + Q_D)}{dt}. \quad (4.56)$$

In reality, computing the above derivatives is very difficult because Q is a complex function of time. The problem can be greatly simplified by assuming that the charge is at any time determined by the terminal voltages. Another way of expressing this idea is to say that the charge responds instantly to applied voltages. This

simplification of the actual physics is called the quasi-static approximation and is not accurate for high frequency signals, but it is sufficient for this model. Under the quasi-static approximation, Q can be determined from the steady-state conditions. Since Q is a fundamental variable in the charge-based model, the calculations are simplified.

The model derivation begins with a statement of the conservation of charge given by equation (4.57). The charge on the gate, Q_G , is equal and opposite to the charge in the channel Q_C . In addition, the channel charge can be broken up into two parts: the charge at the source, Q_S , and the charge at the drain Q_D .

$$Q_C = Q_S + Q_D = -Q_G \quad (4.57)$$

The total charge in the channel can be found by integrating Q_h along the length of the channel, and is given by:

$$Q_C = -Q_G = W \int_0^L Q_h dy. \quad (4.58)$$

Since Q_h is not expressed in terms of y , the integral in (4.58) can not be evaluated in its present form. An expression for dy can be found from the differential form of the Pao-Sah model given by

$$I_{DS} = W \mu Q_h \frac{dV_{ch}}{dy}. \quad (4.59)$$

Solving for dy and substituting (4.59) into (4.58) yields:

$$Q_C = \frac{W^2 \mu}{I_{DS}} \int_0^L Q_h^2 dV_{ch}. \quad (4.60)$$

Changing variables, as was done in the derivation of the charge-based model drain

current expression, results in

$$Q_C = \frac{W^2 \mu}{I_{DS}} \int_0^L Q_h^2 \left(\frac{dV_{ch}}{dQ_h} \right) dQ_h. \quad (4.61)$$

Equation (4.61) can be evaluated by substituting (4.42) into (4.61) and integrating, but this leads to a rather complex expression. Techniques for making (4.61) yield less complicated expressions will be described below, but first the expression for the source and drain charge will be derived for completeness.

The charges associated with the source and drain are not as well defined as the gate charge and must be obtained by arbitrarily partitioning the channel. In accordance with the treatment in [17], the following approach has been shown to be experimentally correct:

$$Q_D = W \int_0^L \frac{y}{L} Q_h dy \quad (4.62)$$

$$Q_S = W \int_0^L \left(1 - \frac{y}{L} \right) Q_h dy = Q_C - Q_D. \quad (4.63)$$

Since Q_S can be found in terms of Q_C and Q_D , one only needs to evaluate the expressions for Q_c and Q_D . As done above, (4.59) can be substituted into (4.62) and a change of variables from V_{ch} to Q_h results in

$$Q_D = \int_0^L \frac{W^2 \mu}{I_{DS}} \frac{y}{L} Q_h^2 \left(\frac{dV_{ch}}{dQ_h} \right) dQ_h \quad (4.64)$$

where an expression for y can be found from (4.59) and is given by

$$y = \frac{W \mu}{I_{DS}} \int_{Q_S}^{Q_h} Q_h \left(\frac{dV_{ch}}{dQ_h} \right) dQ_h. \quad (4.65)$$

Evaluating (4.64) is very difficult using the complete expression for dV_{ch}/dQ_h , and results in extremely complex equations. It has been found that since the capacitance values in the depletion region are often smaller than the parasitic capacitances, a

good approximation can be made by assuming the device is operating in accumulation. In accumulation (4.41) becomes

$$V_{ch} = V_{GEFF} + \phi_t \ln \left(\frac{Q_h^2}{C_2 N_A} \right) + \frac{Q_h + Q_f + Q_{sa} + Q_{sb}}{C_{ox}}. \quad (4.66)$$

Therefore, dV_{ch}/dQ_h is given by

$$\frac{dV_{ch}}{dQ_h} = \frac{1}{C_{ox}} + \frac{2\phi_t}{Q_h}. \quad (4.67)$$

The expression for drain current in accumulation can be found by inserting (4.67) into (4.4) and integrating

$$I_{DS} = \frac{\mu_p W}{2C_{ox} L} (Q_{hD} - Q_{hS}) (4C_{ox} \phi_t + Q_{hD} + Q_{hS}). \quad (4.68)$$

Substituting (4.67) and (4.68) into (4.61) results in the following expression for Q_C :

$$Q_C = \frac{2LW (Q_{hD}^2 + Q_{hD}Q_{hS} + Q_{hS}^2 + 3C_{ox}\phi_t(Q_{hD} + Q_{hS}))}{3(4C_{ox}\phi_t + Q_{hD} + Q_{hS})}. \quad (4.69)$$

The drain charge expression Q_D is broken up into two parts

$$Q_D = \frac{Q_{DN}}{Q_{DD}} \quad (4.70)$$

where Q_{DN} represents the numerator of the expression and Q_{DD} represents the denominator of the expression.

$$Q_{DN} = WL(6Q_{hD}^3 + 12Q_{hD}^2Q_{hS} + 8Q_{hD}Q_{hS}^2 + 4Q_{hS}^3) \quad (4.71)$$

$$+ 40C_{ox}^2\phi_t^2(2Q_{hD} + Q_{hS}) \quad (4.72)$$

$$+ 5C_{ox}\phi_t(9Q_{hD}^2 + 10Q_{hD}Q_{hS} + 5Q_{hS}^2) \quad (4.73)$$

$$Q_{DD} = 15 (4C_{ox}\phi_t + Q_{hD} + Q_{hS})^2 \quad (4.74)$$

and Q_S is equal to the subtraction of Q_C and Q_D .

4.2.3 Verilog-A Model

In order to instantiate the model inside the circuit simulator, the model presented above was coded in Verilog-A. The program will be described below using pieces of code to aid in understanding.

The Verilog-A model begins by including the standard libraries and setting up the three ports of the PACC device using the following code:

```
...
#include "constants.vams"
#include "disciplines.vams"

module SimDoG( source, drain, gate );
inout source, drain, gate;
electrical source, drain, gate;
...
```

The constants library includes a number of physical constants such as pi and the Boltzmann constant for ease of use. The disciplines library includes the information necessary to define different types of physical models. Each discipline defines a different potential and flow. For electrical systems the potential is voltage and the flow is current, while in a mechanical system the potential is position and the flow is force.

The next block of lines declares the module and sets up the ports. Modules are the fundamental user-defined primitives in Verilog-A. Modules define the interfaces and the behavior of components. In this case, the module name is SimDoG and it has ports source, drain and gate. The *inout* statement says that all of the ports are input/output ports and *electrical* line says that each port has a voltage and current associated with it.

Next, all of the user-defined parameters are defined and given default values. An example of parameter setup and definition is given as:

```
...  
parameter real W = 24e-4;  
parameter real L = 12e-4;  
parameter real Vfb = 1.32701;  
...
```

Things defined as parameters can be changed by the user in the Cadence properties menu. The most important user-defined parameters are shown above, W and L and the flat band voltage V_{FB} .

Next all of the global variables are declared.

```
...  
real VGEFF;  
integer mcd;  
integer swap;  
...
```

Floating point numbers such as the effective gate voltage are declared as real, while whole numbers are declared as integers.

Next in the code are two functions, QHGUESS and QHNEWTONITERATION, which are used to solve (4.41) for the integrated hole concentration from the terminal voltages. These two functions will be described in detail after the main program is defined.

The main program loop is initiated with the call:

```
...  
analog begin  
CODE  
...
```

The first thing that occurs in the program is that parameters are calculated from the more basic user-defined parameters, for example:

```
...
Qf = ( q * Na * Xsi );
Cox = ( Eox / Xox );
...
```

which calculates the fixed charge due to acceptor atoms and the oxide capacitance per unit area.

Since the SiOG devices are symmetric about the source and drain, the source and drain are interchangeable. The next block of code calculates V_{GS} and V_{DS} accounting for the possibility of the drain and source being swapped.

```
swap = 0 ;
Vds = V(drain) - V(source);
Vgs = (V(gate) - V(source)) ;
if ( Vds >= 0 ) begin
swap=1;
Vds = -1*Vds;
Vgs = (V(gate) - V(drain));
end
```

If the source and drain are swapped, a flag (swap) is set so that the current is given the proper polarity in the model. Next the effective gate voltage is determined by evaluating equations (4.46) through (4.50).

Next, values for Q_{hD} and Q_{hS} are calculated. This is done by solving (4.41) numerically using Newton's method. Good starting guesses for Newton's method reduce the number of iterations required for convergence. The function QHGUESS provides those guesses. It turns out that good starting guesses can be found by solving (4.41) in the depletion or accumulation regions.

A simplified version of (4.41) valid only in the depletion region can be developed by substituting equation (4.17) in for $p_{sa}(Q_h)$. The equation reads as

$$V_{ch} = V_{GF} + \phi_t \ln \left(\frac{Q_{hdep}}{C_1 N_A} \right) + \frac{Q_{hdep} + Q_f + Q_{sa} + Q_{sb}}{C_{ox}}. \quad (4.75)$$

This expression can be solved for the Q_{hdep} in terms of the Lambert W function described in Chapter 3.

$$Q_{hdep} = C_{ox}\phi_t W \left[\left(\frac{C_1 N_A}{C_{ox}\phi_t} \right) e^{\frac{-Q_f - Q_{sb} - Q_{sa}}{C_{ox}\phi_t} + \frac{V_{ch}}{\phi_t} - \frac{V_{GFEFF}}{\phi_t}} \right] \quad (4.76)$$

Using the same technique, a similar expression can be found in the accumulation region.

$$V_{ch} = V_{GF} + \phi_t \ln \left(\frac{Q_{hacc}^2}{C_2 N_A} \right) + \frac{Q_{hacc} + Q_f + Q_{sa} + Q_{sb}}{C_{ox}} \quad (4.77)$$

$$Q_{hacc} = 2C_{ox}\phi_t W \left[\frac{1}{2} \sqrt{\left(\frac{C_2 N_A}{C_{ox}^2 \phi_t^2} \right) e^{\frac{-Q_f - Q_{sb} - Q_{sa}}{C_{ox}\phi_t} + \frac{V_{ch}}{\phi_t} - \frac{V_{GFEFF}}{\phi_t}}} \right] \quad (4.78)$$

Since both (4.76) and (4.78) provide good enough guesses, the simpler depletion region expression was chosen for the compact model. The Lambert W function is not native to Verilog-A and is usually solved for using numerical methods. Instead of directly implementing the complete Lambert W function, approximations are used since it is only employed to provide a guess anyway. If the argument of the Lambert W function is greater than 3, the following truncated asymptotic expansion [55] is used

$$W[x] \approx L_1 - L_2 + \frac{L_2}{L_1} + \frac{L_2(-2 + L_2)}{2L_1^2} + \frac{L_2(6 - 9L_2 + 2L_2^2)}{6L_1^3} \quad (4.79)$$

where

$$L_1 = \ln[x] \quad (4.80)$$

$$L_2 = \ln[\ln[x]]. \quad (4.81)$$

Otherwise the (3,3) Pade Approximant is used

$$W[x] \approx \frac{x + \frac{228}{85}x^2 + \frac{451}{340}x^3}{1 + \frac{331}{85}x + \frac{1193}{340}x^2 + \frac{133}{204}x^3}. \quad (4.82)$$

Another problem results from Verilog-A's poor handling of very small and very large numbers. If $V_{GEFF} - V_{ch}$ is greater than about 4, Q_{hD} becomes too small for Verilog-A to handle. If $V_{GEFF} - V_{ch}$ exceeds 4, the code pins the value to 4 with no detriment to the model. The code for the function GHGUESS can be seen in the appendix.

The starting value produced by QHGUESS is used by QHNEWTONITERATION to solve for Q_h from the terminal voltages. QHNEWTONITERATION directly implements Newton's Method

$$x_1 = x_0 - \frac{f[x_0]}{f'[x_0]} \quad (4.83)$$

where x_0 is the initial guess and x_1 is a closer approximation to the answer. Q_h is found to converge in less than 3 iterations to an acceptable value.

After both Q_{hS} and Q_{hD} have been found, the charge model equations are evaluated leading to expressions for $Q_G, Q_S,$ and Q_D .

The value for the effective mobility is calculated and finally the DC drain current is determined. The drain-to-source current is set using the following code:

```

if (swap == 0 ) begin
I( drain, source ) <+ curr;
end else begin
I( drain, source ) <+ -1*curr;
end

//AC Current
I( drain, gate ) <+ ddt(Qdrain);
I( source, gate ) <+ ddt(Qsource);

end

```

where *curr* is the calculated DC current. The DC current is set by using the contribution operator $< +$ with an if statement used to correct the polarity if the source and drain are swapped. The AC current is also set by using a contribution operator in conjunction with the time derivative of Q_D and Q_S .

The complete code listing for the most current version of the Verilog-A model can be found in the appendix.

4.2.4 *n*-type Device

The *n*-type inversion device can be modeled in a similar manner to the accumulation device, noting that the current-carrying species changes from holes to electrons. For example, Q_h , the integrated mobile hole charge, is replaced by $-Q_e$, the mobile electron charge. p_{sa} , the number of holes at the silicon-oxide interface, is changed to n_{sa} , the number of electrons at the silicon-oxide interface. Based on these changes the Pao-Sah equation becomes:

$$I_{DS} = -\mu_n \frac{W}{L} \int_{V_S}^{V_D} Q_e dV_{ch}. \quad (4.84)$$

The result of the application of the 1-D Gauss' law becomes:

$$V_{GF} = \psi_{sa} - \frac{1}{C_{ox}} (-Q_e - Q_f + Q_{sa} + Q_{sb}) \quad (4.85)$$

and Poisson's equation changes to

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_s} [N_A e^{\psi - V_{ch} - 2\phi_f} + N_A] \quad (4.86)$$

where ϕ_f is the Fermi-level in the silicon-film. Developing the solution in a similar manner to the accumulation mode *p*-type model, one finds that the *n*-type inversion devices can be described by:

$$V_{ch} = V_{GF} - 2\phi_f - \phi_t \ln \left[\frac{CQ_e + DQ_e^2 + rQ_e^3}{N_A(F + Q_e)} \right] + \frac{-Q_e - Q_f + Q_{sa} + Q_{sb}}{C_{ox}} \quad (4.87)$$

and (4.87) can then be differentiated to find dV_{ch}/dQ_e . Substituting the derivative into (4.84) and integrating with respect to Q_e leads to the following expression for drain current.

$$I_{DS} = \mu_n \frac{W}{L} \phi_t (I_f [Q_{eD}] - (I_f [Q_{eS}])) \quad (4.88)$$

where the function I_f is given by

$$I_f [Q_e] = \left[2Q_e + \frac{Q_e^2}{2\phi_t C_{ox}} + \frac{(D^2 - 4Cr) \arctan\left(\frac{D+2rQ_e}{\sqrt{-D^2+4Cr}}\right)}{r\sqrt{-D^2+4Cr}} \right] + \left[F \ln(F + Q_e) - \frac{D}{2r} \ln(C + DQ_e + rQ_e^2) \right]. \quad (4.89)$$

and Q_{eS} and Q_{eD} represent the total mobile electron charge at the source and drain respectively. Q_{eS} and Q_{eD} can be solved for in terms of the terminal voltages by solving (4.84) at $y = 0$ and $y = L$, respectively, using numerical methods as done above.

4.2.5 Results

Initially, the long channel model for the p -type accumulation device was compared to two-dimensional numerical simulation using Silvaco's Atlas. The device structure shown in Figure 4.1 was developed to be similar to the devices fabricated in the laboratory, but also to have long channel characteristics. The silicon film has a thickness of 200 nm, and was doped $N_A = 2 \times 10^{15} \text{ cm}^{-3}$. The top gate oxide, x_{ox} is 50 nm. In order to suppress short channel effects and maintain long channel characteristics, a number of things were done: the channel length was made to be 200 μm , the glass substrate was made to be very thin, and the size of the source and drain regions was reduced to 0.5 μm . The thin glass substrate and small source and drain regions reduced the effects of fringing fields. In addition, a constant mobility model was used in the Silvaco Atlas.

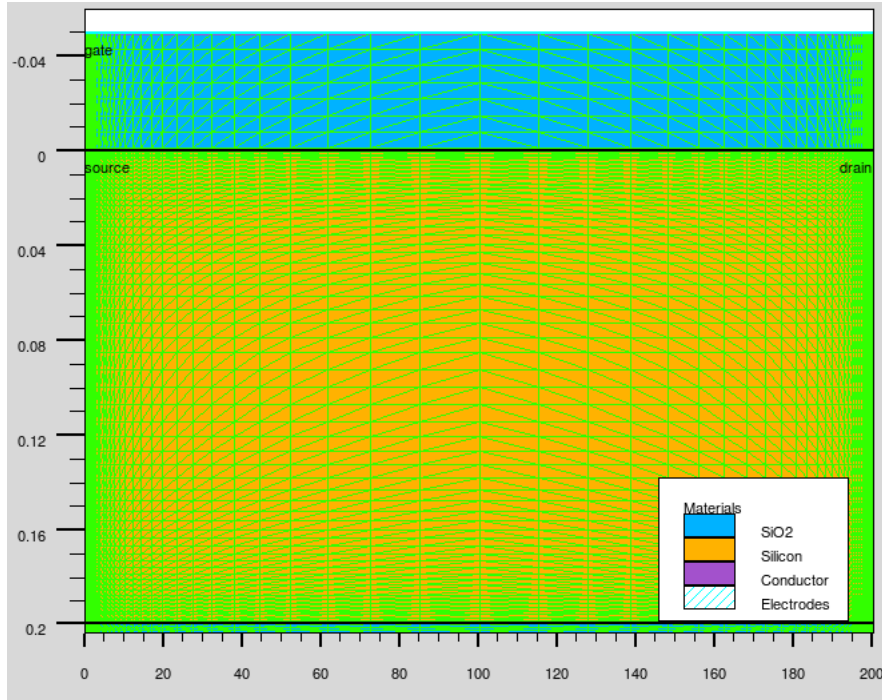


Figure 4.1: Long-Channel Structure in Silvaco Atlas

In order to verify the approach used to develop the core model equations, the use of the rational polynomial approximation to represent the mobile surface charge p_{sa} as a function of the total integrated mobile charge Q_h is verified in Figure 4.2. Figure 4.2 shows good correspondence between the rational polynomial approximation and the values obtained through numerical simulation in Atlas. The simulation was conducted using both the structure described above, and also a similar structure where the silicon film thickness was reduced to 50 nm.

Figure 4.3 shows a plot of I_{DS} versus V_{GS} comparing the long channel model to numerical simulation, while Figure 4.4 plots the same data on a semi-log graph. One can see excellent correspondence between the numerical simulation and the compact model. Figure 4.5 plots I_{DS} versus V_{DS} which also shows good correspondence between the numerical simulation and the compact model. If Figure 4.5 is examined closely one notices that the numerical simulation shows hints of channel length modulation, but since the channel length is so long the effect is hardly

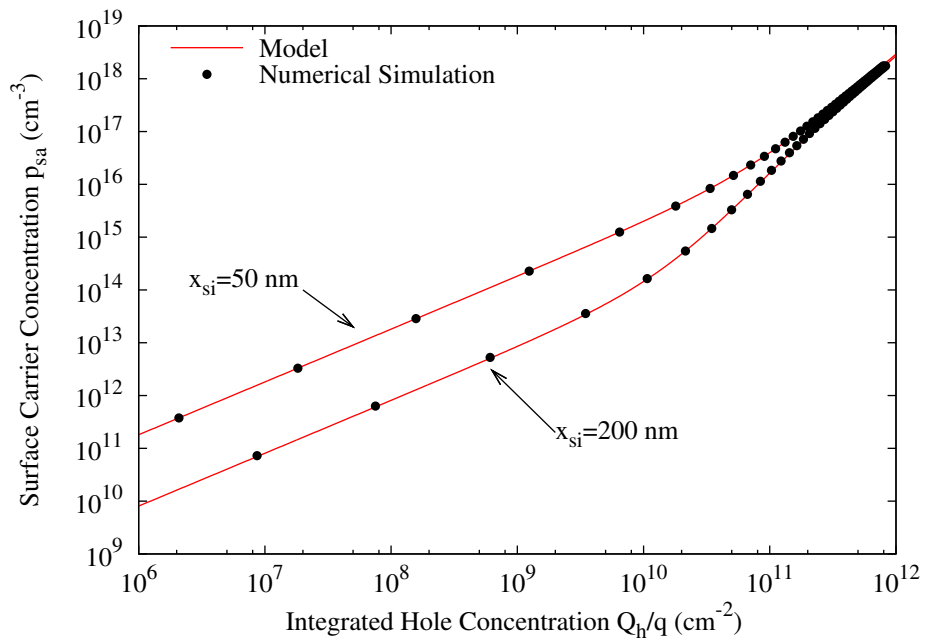


Figure 4.2: A plot of p_{sa} versus Q_h/q

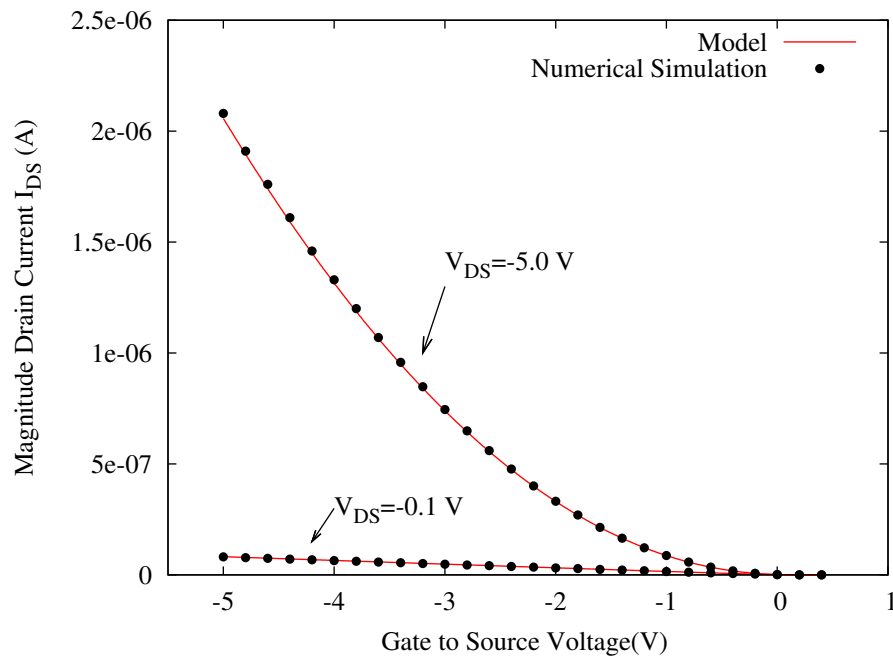


Figure 4.3: A plot of drain current versus gate to source voltage for a $L = 200 \mu\text{m}$ $W = 1 \mu\text{m}$ PACC device. This plot compares the core model to numerical simulation.

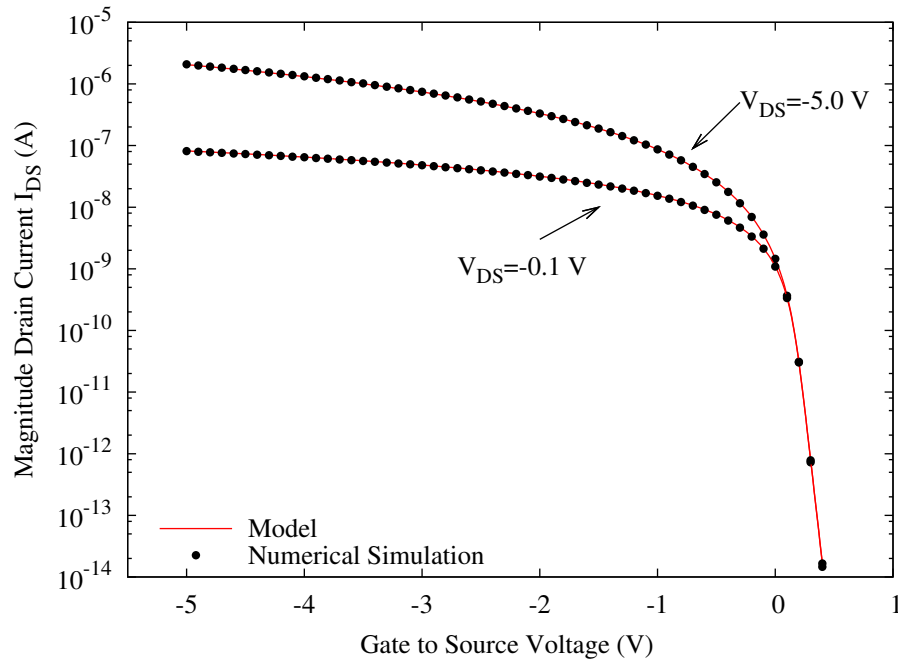


Figure 4.4: A semi-log plot of drain current versus gate to source voltage for a $L = 200 \mu\text{m}$ $W = 1 \mu\text{m}$ PACC device. This plot compares the core model to numerical simulation.

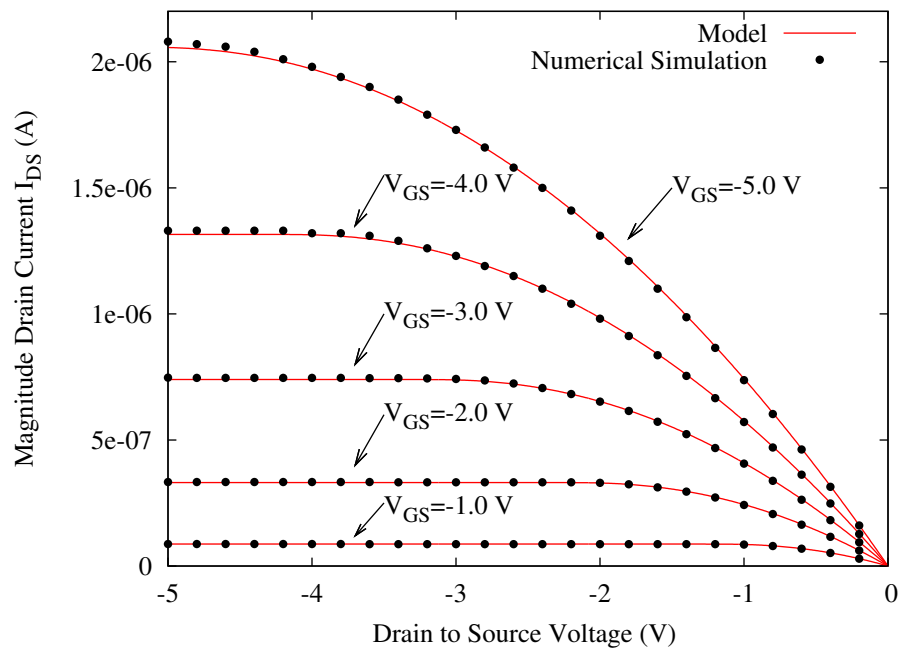


Figure 4.5: A plot of drain current versus drain to source voltage for a $L=200 \mu\text{m}$ $W=1 \mu\text{m}$ PACC device. This plot compares the core model to numerical simulation.

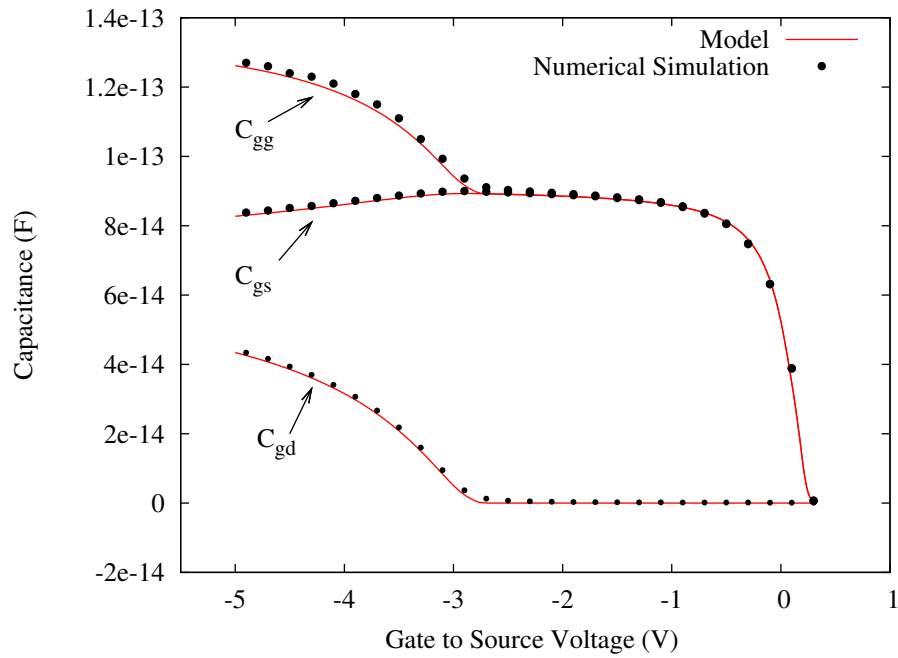


Figure 4.6: A plot of the magnitude of small signal capacitances (C_{gg} , C_{gd} , C_{gs}) versus V_{GS} , for $V_{DS} = -3.0$ V

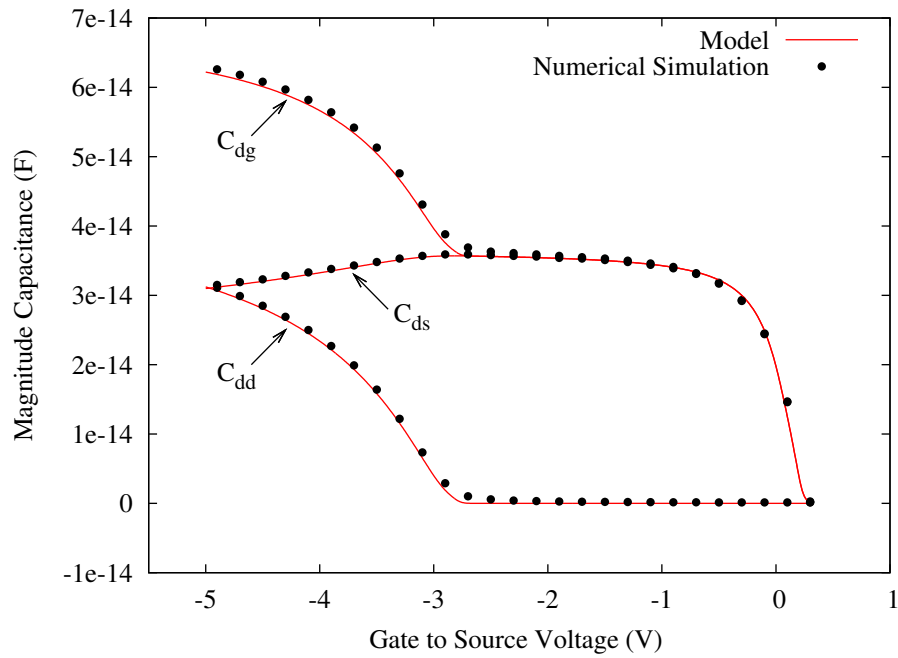


Figure 4.7: A plot of the magnitude of small signal capacitances (C_{dg} , C_{dd} , C_{ds}) versus V_{GS} , for $V_{DS} = -3.0$ V

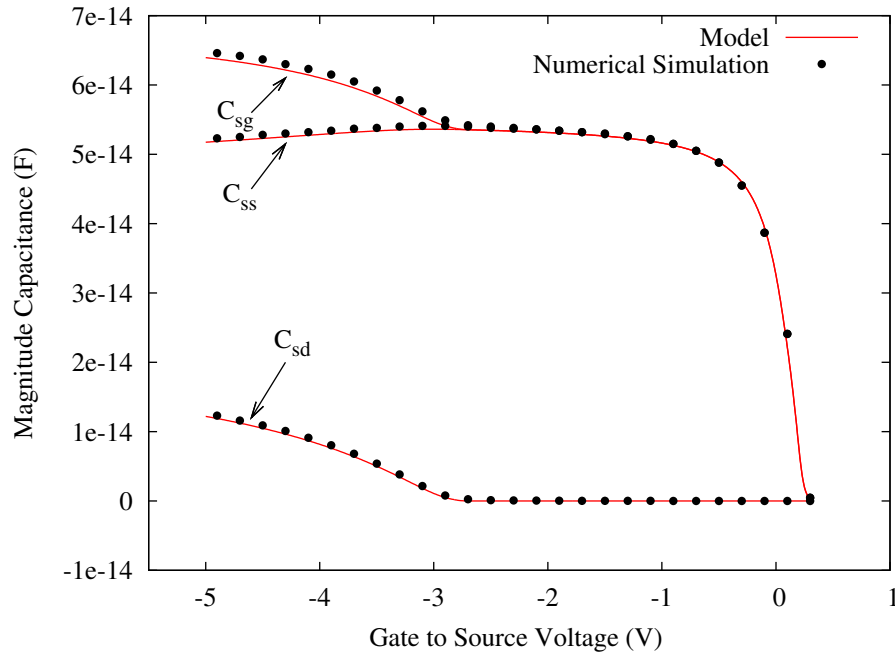


Figure 4.8: A plot of the magnitude of small signal capacitances (C_{sg} , C_{sd} , C_{ss}) versus V_{GS} , for $V_{DS} = -3.0$ V

noticeable.

Figures 4.6 through 4.8 plot the magnitude of all nine small signal capacitances versus V_{GS} . The model matches the numerical simulation very closely.

Next, data presented at the 2010 Electrochemical Society Meeting is shown where the model is compared against numerical simulation again, but with channel lengths of $6 \mu m$. The rest of the device dimensions are the same as above. In addition, the modeling method is applied to both the inversion n -type device and the accumulation p -type device.

Figure 4.9 plots the mobile surface charge versus integrated mobile charge comparing the compact model to 2-D simulation for both the inversion device and the accumulation device. It is interesting to note that for a given value of surface charge, the accumulation device has a higher level of total integrated charge. This can be understood by noting that the accumulation device supports mobile charge at both the surface and in the body of the device, while the inversion device only supports

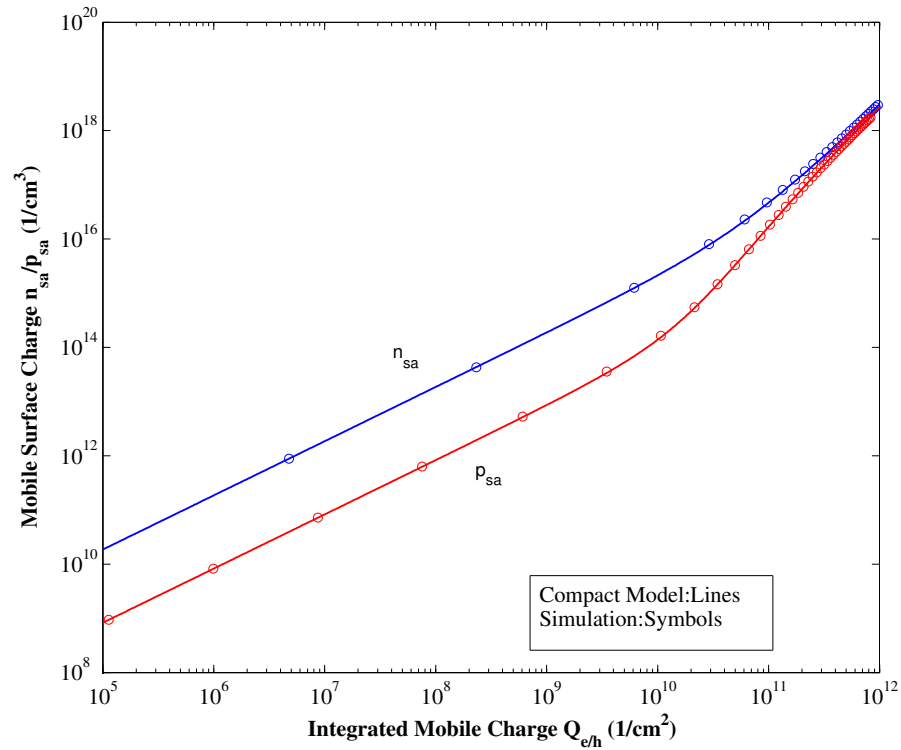


Figure 4.9: A plot of mobile surface charge versus integrated mobile charge comparing the compact model to 2-D simulation. The surface electron charge n_{sa} versus the integrated mobile electron charge Q_e in the inversion n -type device is plotted in blue. The surface hole charge p_{sa} versus the integrated mobile hole charge Q_h in the accumulation p -type device is plotted in red.

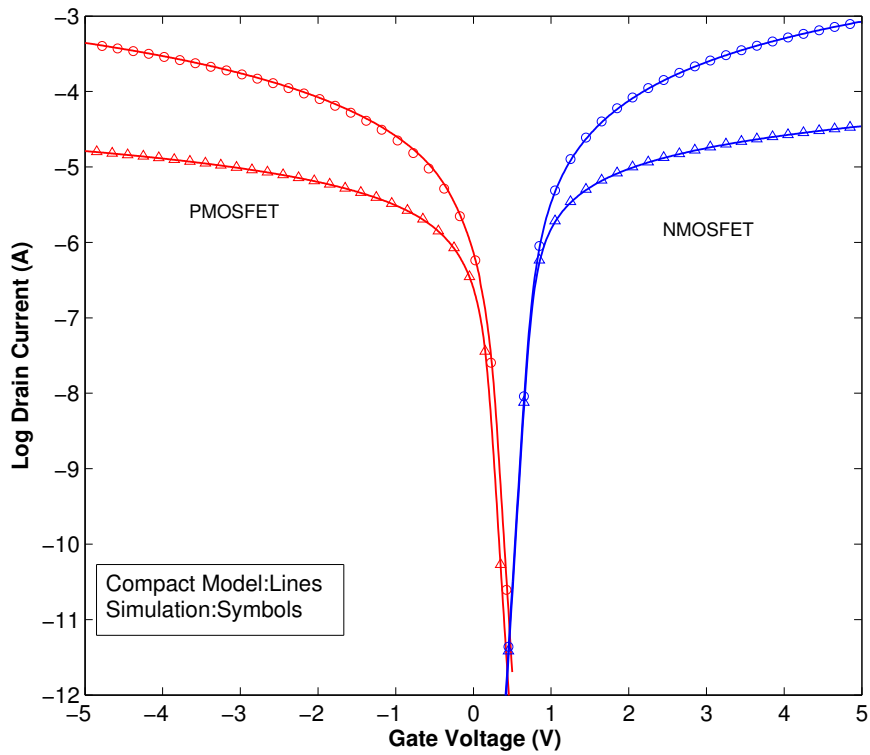


Figure 4.10: A plot of drain current versus gate voltage comparing the compact model to 2-D simulation for $1 \mu\text{m} \times 6 \mu\text{m}$ inversion NMOSFET (blue) and accumulation PMOSFET (red). Drain to source biases of ± 5.0 V (circles) and ± 0.1 V (triangles) were used.

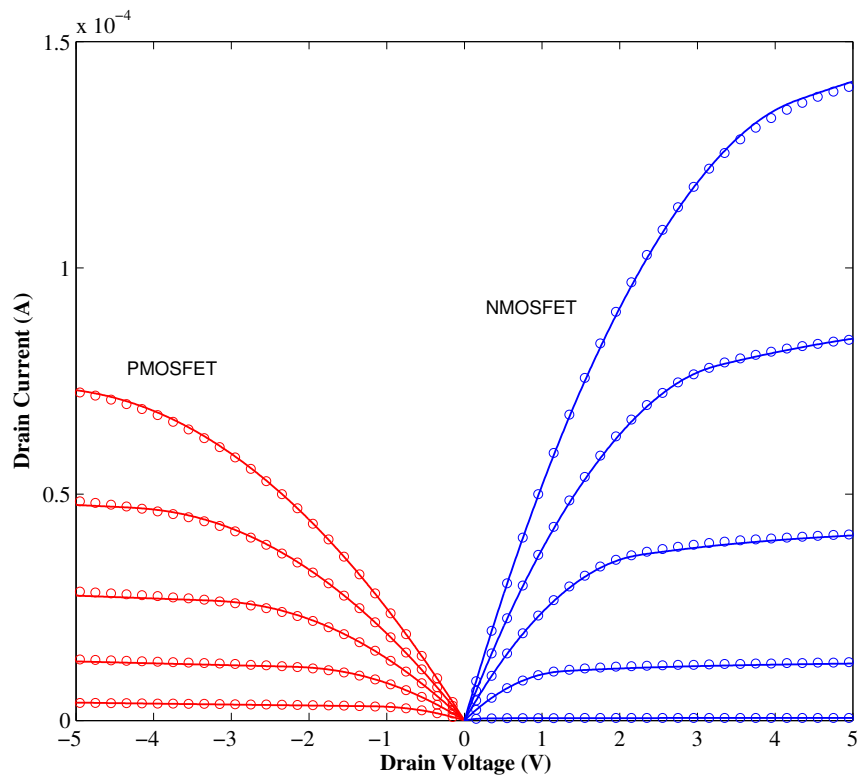


Figure 4.11: A plot of drain current versus drain voltage comparing the compact model to 2-D simulation for $1 \mu\text{m} \times 6 \mu\text{m}$ inversion NMOSFET (blue) and accumulation PMOSFET (red). Gate to source biases of ± 1.0 V through ± 5.0 V were used.

mobile charge at the surface. For very high values of the surface charge density the curves overlap because most of the charge in the accumulation device now resides at the surface, and the mobile charge in the body only represents a small fraction of the overall charge.

Figure 4.10 plots the I_{DS} versus V_{GS} curves on a semi-log graph for both the n -type and p -type devices. Figure 4.11 plots the I_{DS} versus V_{DS} curves. The model shows good correspondence with measured data over the entire operating range.

The complete model is shown against measured data from a PACC device with a length of $12 \mu\text{m}$ and a width of $24 \mu\text{m}$. The rest of the device dimensions are the same as those used in simulation. Figure 4.12 depicts the linear $I - V$ transfer characteristics with $V_{DS} = -0.1$ and $V_{DS} = -5.0$ including the effect of mobility degradation. Figure 4.13 shows the semi-log $I - V$ characteristics, highlighting the matching of the model to the measured data over all regions of operation. Finally, output characteristics are plotted in Figure 4.14.

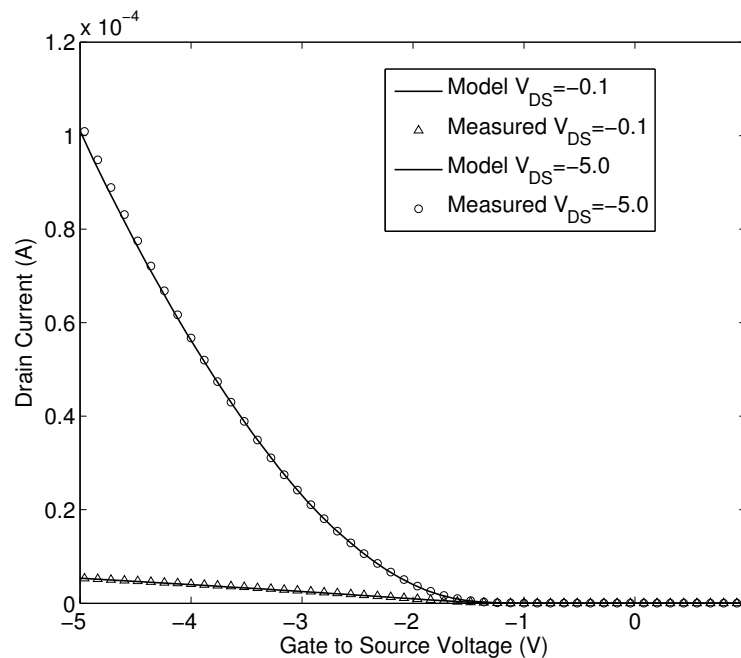


Figure 4.12: A plot of drain current versus gate to source voltage for a $W = 12 \mu\text{m}$, $L = 24 \mu\text{m}$ accumulation p -type device.

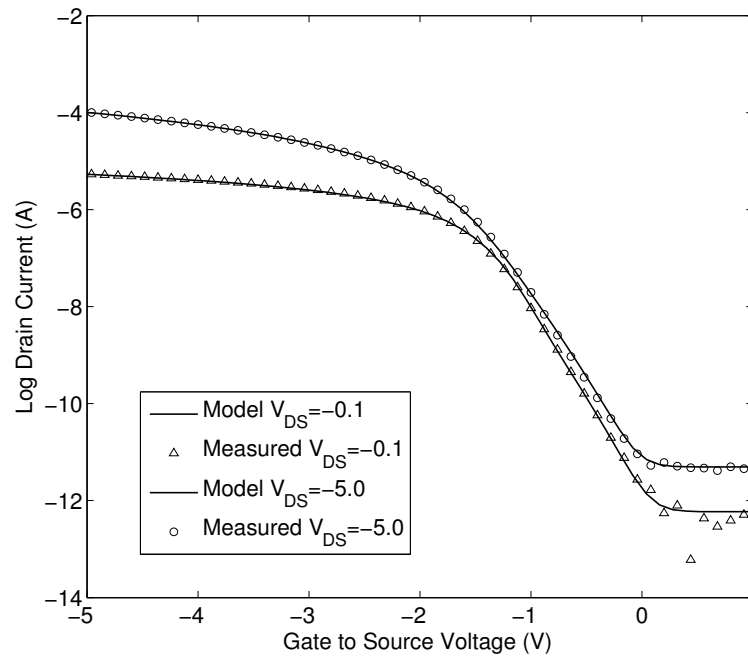


Figure 4.13: A semi-log plot of drain current versus gate to source voltage for a $W = 12 \mu\text{m}$ $L = 24 \mu\text{m}$ accumulation p -type device.

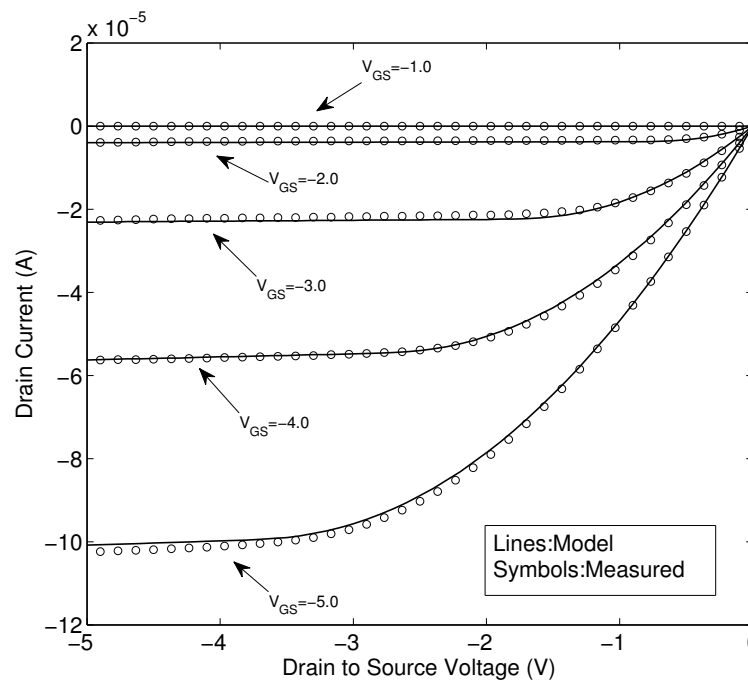


Figure 4.14: A semi-log plot of drain current versus gate to source voltage for a $W = 12 \mu\text{m}$ $L = 24 \mu\text{m}$ accumulation p -type device.

4.3 Conclusions

This chapter described a new compact modeling technique for SiOG CMOS devices. The modeling method is based directly on the Pao-Sah equation and the 1-D Gauss' law. The equations have been formulated such that the need for an exact solution to Poisson's equation is minimal. The solution of Poisson's equation is only needed to derive the relationship between the majority mobile carrier concentration at the silicon-oxide interface to the total majority carrier charge in the device. That relationship was approximated using a rational polynomial avoiding the complexity introduced by Poisson's equation. The completed model is comprised of a single continuous expression valid in all regions of operation.

The basic model was then augmented with effects that are not captured by the basic model equations, including channel-length modulation, fringing field induced barrier lowering, and mobility degradation. A charge model was derived to allow for transient and AC simulation. In addition, the model was extended to n -type inversion devices.

The model shows good correspondence with both 2-D numerical simulation and measured data.

Chapter 5

Fringing Field Effects

Unlike traditional silicon-on-insulator devices, SiOG devices are built on thick insulating substrates and are targeted at large area display applications. Typically, SiOG devices are patterned using contact lithography, ultimately limiting the minimum possible feature size to a few microns. At these dimensions, traditional short channel effects such as drain-induced barrier lowering (DIBL) are almost nonexistent. The fringing electric field at the silicon-glass interface due to the source and drain electrodes is the dominant two-dimensional effect in SiOG devices as shown in Figure 5.1. This is in contrast to SOI devices where there is a silicon substrate on which field lines from the source and drain can terminate. The lack of silicon substrate forces most of the field lines to terminate on the body of the transistor, altering its conduction properties, even for relatively long channel devices ($L > 10\mu m$). The fringing field leads to a shift in flatband or threshold voltage which manifests itself in the device's current-voltage characteristics in a similar manner to DIBL. In SOI devices, this shift in threshold voltage has been labeled drain-induced virtual substrate biasing (DIVSB) [56]. To distinguish this work from the previous SOI models, the effect of the fringing field on the drain current in SiOG devices is referred to as fringing-field-induced barrier lowering (FFIBL).

Initially the FFIBL effect was accounted for in the long channel SiOG compact models through the use of a simple empirical scaling factor, similar to the way DI-VSB has been handled in many device models [57] [58]. However, since the scale factor is based on empirical observation, it does not predict the correct value of the fringing field over all device geometries.

Ernst *et al.* [59] have developed a model for the fringing field in short channel SOI devices based on a Schwarz-Christoffel conformal mapping. The conformal map and surrounding model were chosen to accommodate the silicon substrate which does not exist in SiOG devices. As a consequence, the Ernst model is not able to capture the effect of finite source/drain dimensions on the fringing field.

In this chapter, a model is developed which shows the relationship between the fringing field and the subthreshold drain current in SiOG PACC devices. In addition, a physically based model for the fringing field in SiOG is presented utilizing a very simple bilinear conformal mapping targeted at devices on thick insulating substrates. This mapping captures the dependence on both channel length and the size of the source and drain electrodes. The work described in this chapter was first published in the *IEEE Journal of Display Technology* [60].

5.1 FFIBL's EFFECT on PACC Drain Current

In this section, an expression for the subthreshold drain current for a SiOG PACC device is derived. To maintain consistency with the complex variable notation used in the conformal mapping for developing the fringing field model, the y -axis in this chapter is taken to be in the vertical direction. $y = 0$ is taken to be at the silicon-glass interface and $y = y_{si}$ is located at the silicon-oxide interface.

To accurately model the drain current in a thin-film bulk conduction device, the carrier concentrations must be known throughout the film. The hole concentration

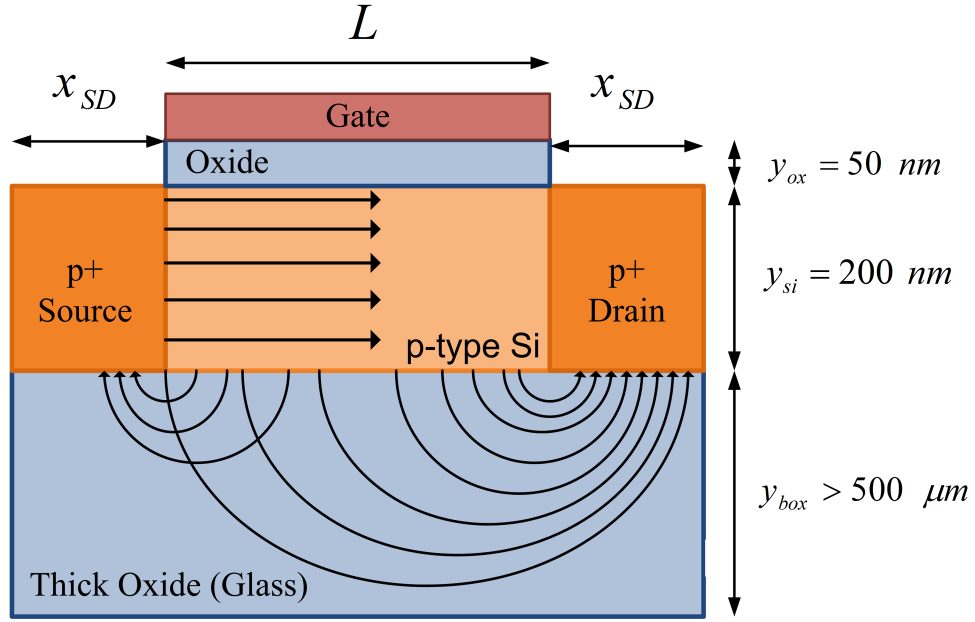


Figure 5.1: SiOG PFET operated in accumulation, illustrating the fringing electric field.

is related to the localized potential through the expression:

$$p(x, y) = N_A e^{\frac{-\psi + V_{ch}}{\phi_t}}. \quad (5.1)$$

Invoking the gradual channel approximation, the potential distribution, ψ , in the y direction is given by

$$\frac{d^2\psi}{dy^2} = \frac{-q}{\epsilon_s} \left[N_A e^{\frac{-(\psi - V_{ch})}{\phi_t}} - N_A \right] \quad (5.2)$$

where the symbols have their usual meaning.

The FFIBL effect is most apparent in the subthreshold region where the potential distribution in the silicon film is dominated by the influence of fixed acceptor atoms.

Simplifying (5.3) for this case leads to:

$$\frac{d^2\psi}{dy^2} = \frac{q}{\epsilon_s} N_A. \quad (5.3)$$

Since the oxide is thick, the electric field at the silicon-glass interface E_{sb} is simply

the fringing field E_{FF} and is given by:

$$E_{sb} = E_{FF} \frac{\varepsilon_{ox}}{\varepsilon_s}. \quad (5.4)$$

The top surface boundary condition E_{sa} is defined as:

$$E_{sa} = -\frac{(V_{GF} - \psi_{sa})C_{ox}}{\varepsilon_s}. \quad (5.5)$$

Integrating (5.3) twice with respect to y and applying the boundary conditions given by (5.4) and (5.5) leads to the following equation for ψ :

$$\psi = \frac{N_A q}{2\varepsilon_s} y^2 - \frac{E_{FF} \varepsilon_{ox}}{\varepsilon_s} y + \psi_{sb} \quad (5.6)$$

where ψ_{sb} is

$$\psi_{sb} = V_{GF} - \frac{qN_A}{C_{ox}} y_{si} - \frac{qN_A}{2\varepsilon_s} y_{si}^2 + \frac{E_{FF} \varepsilon_{ox}}{C_{ox}} + \frac{E_{FF} \varepsilon_{ox}}{\varepsilon_s} y_{si}. \quad (5.7)$$

The subthreshold drain current I_{DS} can be found from the Pao-Sah double integral formula given as:

$$I_{DS} = \frac{W}{L} q \mu_p \int_{V_S}^{V_D} \int_0^{y_{si}} p(x, y) dy dV_{ch}. \quad (5.8)$$

Substituting (5.1) and (5.6) into (5.8) and evaluating the double integral leads to the equation for the drain current in the subthreshold region including fringing field effects:

$$I_{DS} = \frac{W}{L} q \mu_p \phi_t^{\frac{3}{2}} \sqrt{\frac{\varepsilon_s \pi N_A}{2q}} \left(e^{\frac{E_{FF}^2 \varepsilon_{ox}^2}{2q N_A \phi_t \varepsilon_s}} \right) \left(e^{\frac{V_D}{\phi_t}} - e^{\frac{V_S}{\phi_t}} \right) \left(e^{\frac{-\psi_{sb}}{\phi_t}} \right) \cdot \left(\operatorname{erf} \left[\frac{E_{FF} \varepsilon_{ox}}{\sqrt{2\varepsilon_s q N_A \phi_t}} \right] - \operatorname{erf} \left[\frac{E_{FF} \varepsilon_{ox} - q N_A y_{si}}{\sqrt{2\varepsilon_s q N_A \phi_t}} \right] \right). \quad (5.9)$$

The fringing field E_{FF} in (5.9), (5.6), and (5.7) must be evaluated at the maximum

potential barrier (located at x_o), which controls carrier flow into the channel, and it is derived for fully depleted SOI MOSFETS in [61]:

$$x_o = \frac{L}{2} - \frac{l}{2} \ln \left(\frac{V_{bi} - \psi_{saL} + V_{DS}}{V_{bi} - \psi_{saL}} \right) \quad (5.10)$$

where l is the characteristic length given by

$$l = \sqrt{\frac{\varepsilon_s x_{ox} x_{si}}{\varepsilon_{ox} \eta_f}}. \quad (5.11)$$

In (5.11), η_f is a fitting parameter. From (5.10) and (5.11) it can be shown that for long channel devices ($L > 2\mu m$), the location of the potential barrier can be approximated as $L/2$.

5.2 Fringing Field Model

To evaluate the drain current in (5.9), a model for the fringing field must be developed. Since the two-dimensional fringing field is inherently a complex problem, many simplifications must be made in order to keep the math tractable and maintain a computationally efficient form. The fringing field model derivation begins by assuming that the potential at the silicon-glass interface is constant in the x -direction (a good assumption for long channel devices). The silicon can then be modeled as three coplanar metal electrodes with effective potentials V_{SE} , V_{BE} , and V_{DE} :

$$V_{SE} = V_S + V_{bi} \quad (5.12)$$

$$V_{DE} = V_D + V_{bi}$$

$$V_{BE} = \psi_{sb}.$$

Since there is no net charge in the glass, the fringing field obeys Laplace's equation. Laplace's equation is linear, therefore it can be broken up into the superposition of three cases. Each case consists of applying a voltage to one of the electrodes and grounding the other two electrodes as shown in Figure 5.2. It is easy to see that in

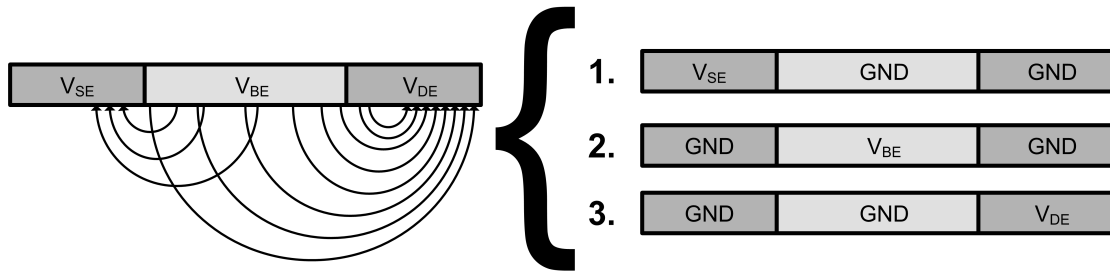


Figure 5.2: Superposition of Laplace's Equation

the first case and in the last case that when a voltage is applied to the drain or source and the other electrodes are grounded that these cases can be modeled as asymmetric coplanar electrodes. The remaining case in which a potential is applied to the middle electrode and the outer two electrodes are grounded is a more difficult problem. It has been found through numerical simulation that a good approximation to case two is obtained by eliminating one of the two ground electrodes and multiplying the resulting fringing field by a factor of 2. As shown in Figure 5.3, this approximation modifies case two in such a way that it can also be modeled as asymmetric coplanar electrodes.

The asymmetric coplanar electrode problem has been solved exactly using the Schwarz-Christoffel transformation [62]. The resulting solution is in terms of the inverse Jacobian Elliptic function and is not suited for compact modeling. A more computationally efficient model can be derived by starting with infinite symmetric coplanar electrodes and applying a simple bilinear conformal map to realize the asymmetric case with finite contacts.

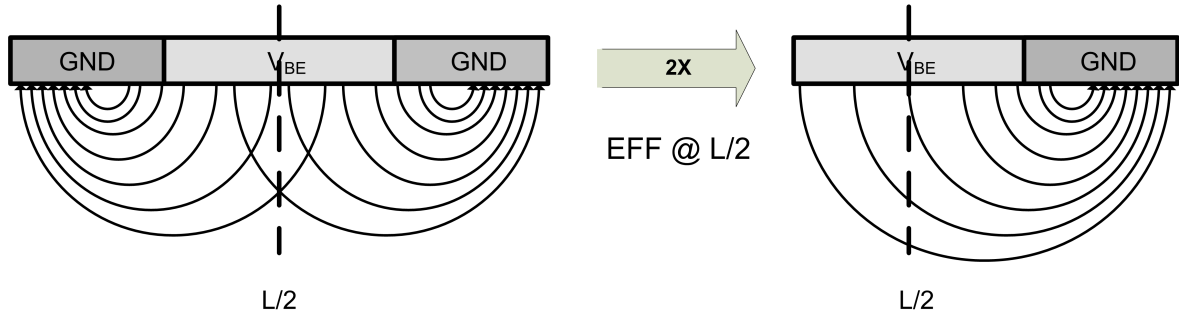


Figure 5.3: Pictorial representation of approximation for case two

5.3 Infinite Symmetric Coplanar Electrodes

Infinite symmetric coplanar electrodes separated by an infinitesimal insulator located at the origin, as shown in Figure 5.4, can be modeled by expressing Laplace's equation in cylindrical coordinates and assuming the potential only varies as a function of the angle between the electrodes, ϕ . Laplace's equation in cylindrical coordinates is given by:

$$\nabla^2 V = \frac{1}{r^2} \frac{\partial^2 V}{\partial \phi^2} = 0 \quad (5.13)$$

where r is the radius and V is potential. The solution of (5.13) is given by:

$$V = C_1 \phi + C_2 \quad (5.14)$$

where the coefficients C_1 and C_2 can be found by applying the following boundary conditions

$$V(0) = V_R \quad (5.15)$$

$$V(\pi) = V_L.$$

In (5.15) V_R and V_L refer to the potentials on the right and left hand side of the origin, respectively. The application of the boundary conditions in (5.15) leads to

the follow expression for V :

$$V = \frac{(V_L - V_R)\phi}{\pi} + V_R. \quad (5.16)$$

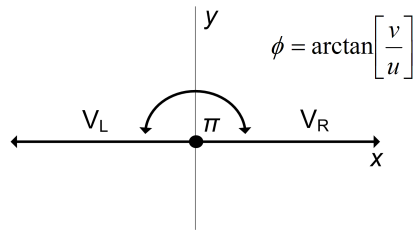


Figure 5.4: Symmetric Coplanar Electrode Schematic

5.4 Asymmetric Coplanar Electrodes

By applying the bilinear conformal mapping (5.17), as depicted in Figure 5.5

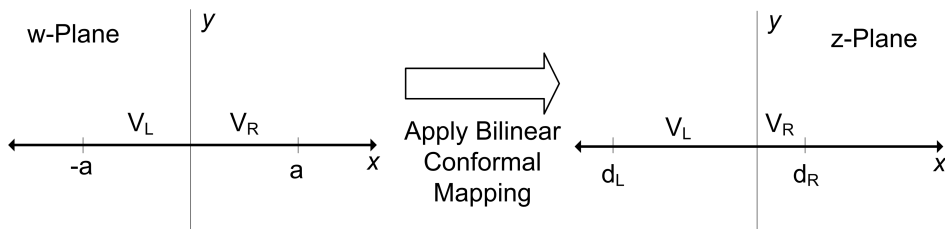


Figure 5.5: Bilinear Conformal Mapping

$$z = \frac{w}{C_a w + C_b} \quad (5.17)$$

one can transform the symmetric coplanar electrode system into the corresponding asymmetric system.

In (5.17) $w = u + jv$ refers to the complex plane in which the electrodes are symmetric and $z = x + jy$ refers to the corresponding transformed complex plane

where they are asymmetric. The coefficients C_a and C_b can be determined by requiring that:

$$u = -a \rightarrow x = d_L \quad (5.18)$$

$$u = a \rightarrow x = d_R$$

where d_L, d_R , and a are defined in Figure 5.5. Since a can be taken to be any value, a is chosen to be at infinity, converting the infinite conductors in the w plane to finite ones in the z plane. Solving (5.17) and (5.18) for C_a and C_b yields:

$$z = \frac{2d_L d_R w}{a(d_L - d_R) + (d_L + d_R)w}. \quad (5.19)$$

Since it is necessary to convert points on the z plane to points on the w plane, (5.19) must be inverted,

$$w = \frac{az(d_L - d_R)}{2d_L d_R - d_L z - d_R z}. \quad (5.20)$$

Plugging (5.19) into (5.16), noting that the angle of the imaginary part of w over the real part yields ϕ :

$$V(x, y) = \frac{(V_L - V_R) \arctan \left[\frac{v(x, y)}{u(x, y)} \right]}{\pi} + V_R \quad (5.21)$$

$$V(x, y) = \frac{(V_L - V_R) \arctan \left[\frac{2d_L d_R y}{(2d_L d_R x - (x^2 + y^2)(d_L + d_R))} \right]}{\pi} + V_R. \quad (5.22)$$

Differentiating (5.23) with respect to y leads to the electric field in the asymmetric coplanar conductor system:

$$E_y = \frac{-2d_L d_R (V_L - V_R) [2d_L d_R x - (d_L + d_R) x^2 + (d_L + d_R) y^2]}{\pi (x^2 + y^2) [(-2d_L d_R + (d_L + d_R) x)^2 + (d_L + d_R)^2 y^2]}. \quad (5.23)$$

Since, in general one is only interested in the field at the silicon glass interface, $y = 0$, one can further simplify the expression for the field as:

$$E_y = \frac{-2d_L d_R (V_L - V_R) [2d_L d_R x - (d_L + d_R) x^2]}{\pi (x^2) [(-2d_L d_R + (d_L + d_R) x)^2]}. \quad (5.24)$$

(5.24) can then be evaluated for each of the three superposition cases and summed together to yield the complete fringing field at the silicon-glass interface

$$\text{Case 1 : } V_L = V_{SE}; V_R = 0; d_L = -x_{SDE}; d_R = x_{SDE} + L_E \quad (5.25)$$

$$\text{Case 2 : } V_L = V_0; V_R = V_{BE}; d_L = -x_{SDE}; d_R = L_E$$

$$\text{Case 3 : } V_L = V_0; V_R = V_{DE}; d_L = -x_{SDE} - L_E; d_R = x_{SDE}$$

where L_E is the effective channel length given by

$$L_E = L - \Delta L \quad (5.26)$$

and x_{SDE} is the effective length of the source and drain regions defined as

$$x_{SDE} = x_{SD} + \Delta L. \quad (5.27)$$

ΔL is a parameter which is determined empirically to account for the non-uniform potential distribution in the channel region. In practice, the value of ΔL can be chosen to find the best fit of the model to measured plots of ΔV_{FB} versus L .

5.5 Results

Since one can not directly measure the fringing field in SiOG devices, the model was compared against the commercial device simulator Silvaco Atlas.

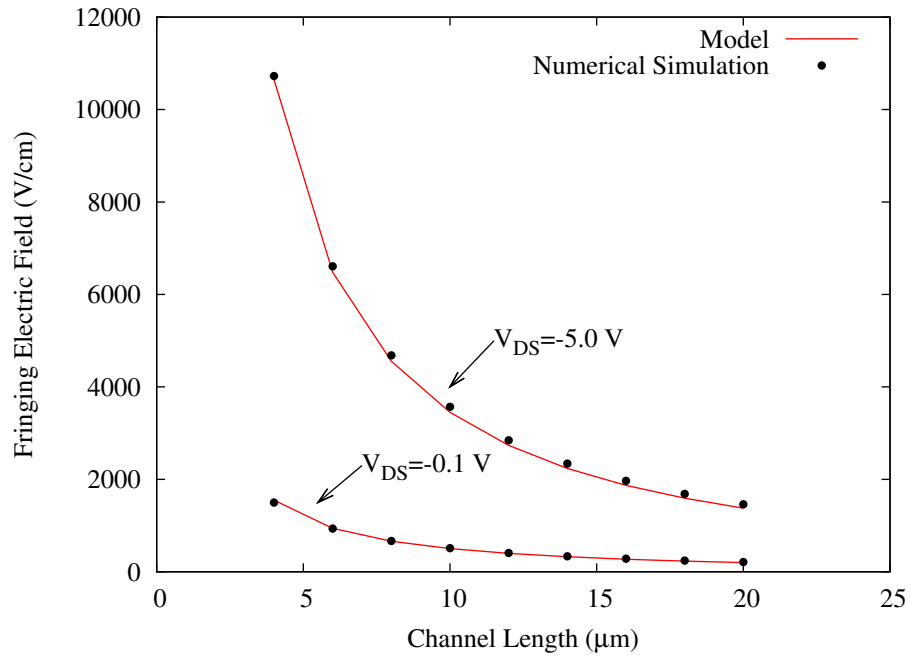


Figure 5.6: A plot of the fringing electric field versus channel length in micrometers.

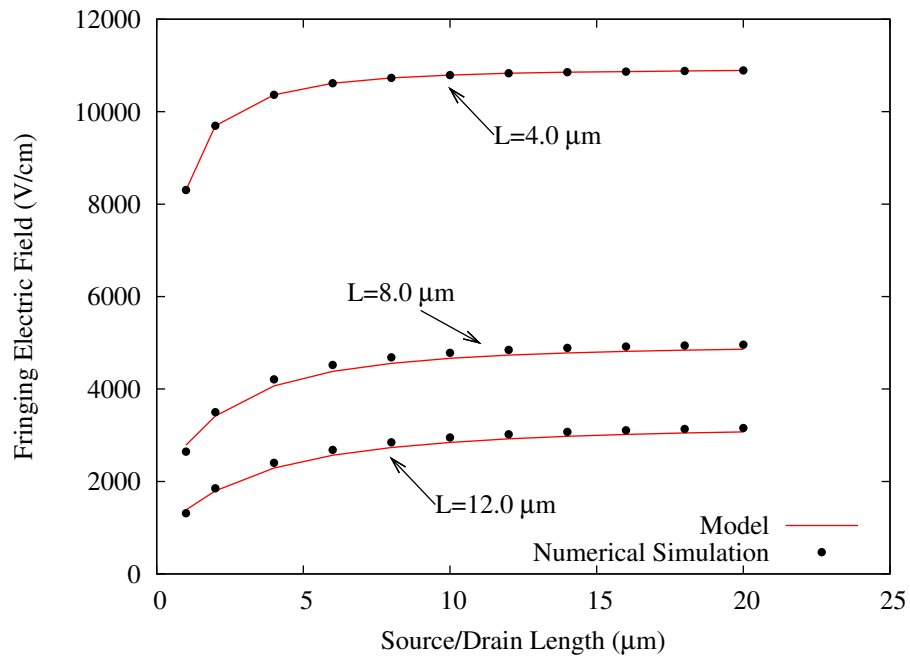


Figure 5.7: A plot of the fringing electric field versus source/drain length for $V_{GS} = 0.3$ V and $V_{DS} = -5.0$ V.

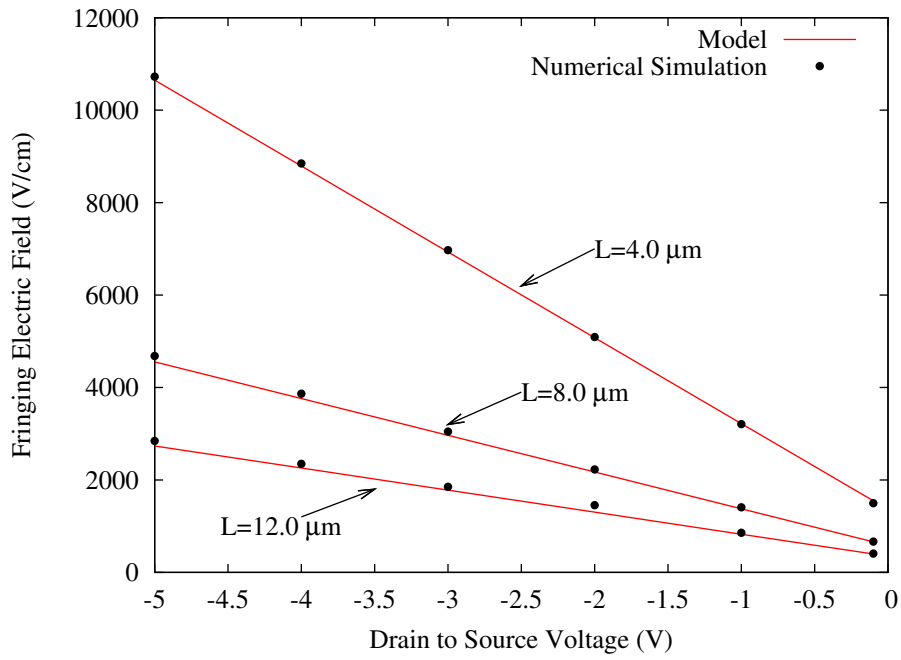


Figure 5.8: A plot of the fringing electric field versus the drain voltage with $V_{GS} = 0.3$ V.

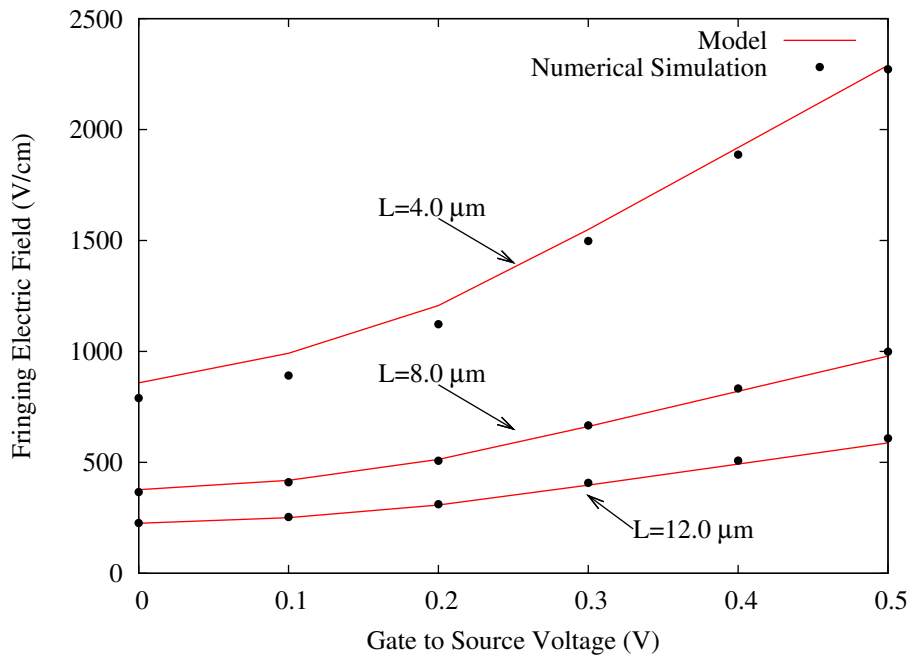


Figure 5.9: A plot of the fringing electric field versus gate to source voltage for $V_{DS} = -0.1$ V.

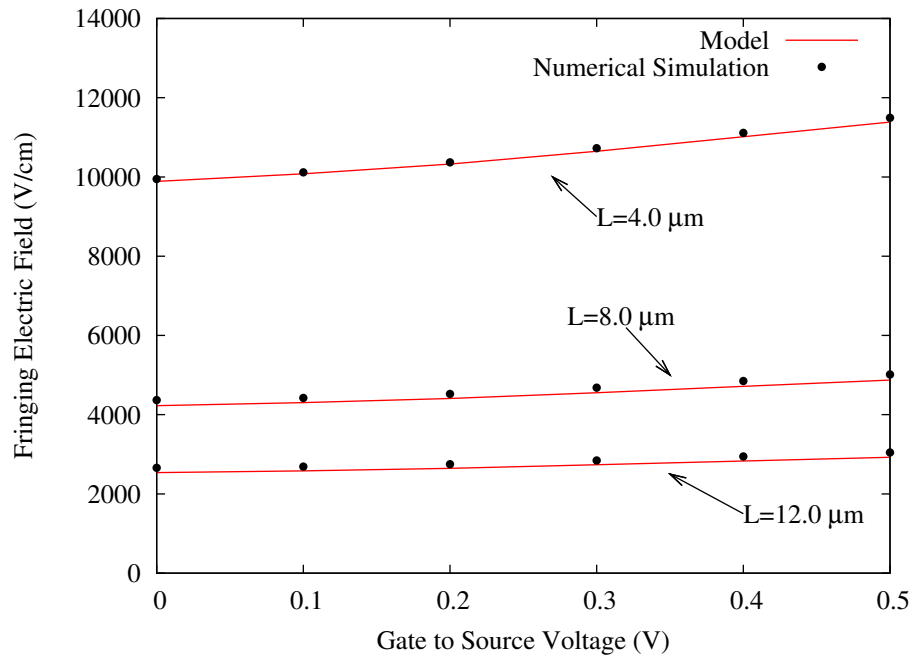


Figure 5.10: A plot of the fringing electric field versus gate to source voltage for $V_{DS} = -5.0$ V.

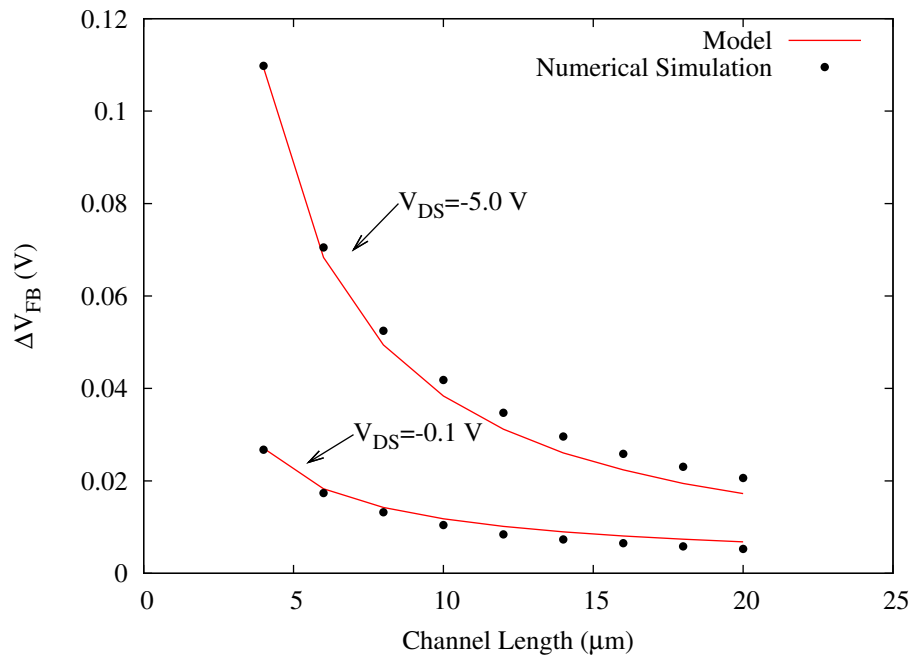


Figure 5.11: A plot of the shift in the flatband voltage versus channel length due to the fringing electric field for $V_{GS} = 0.3$ V.

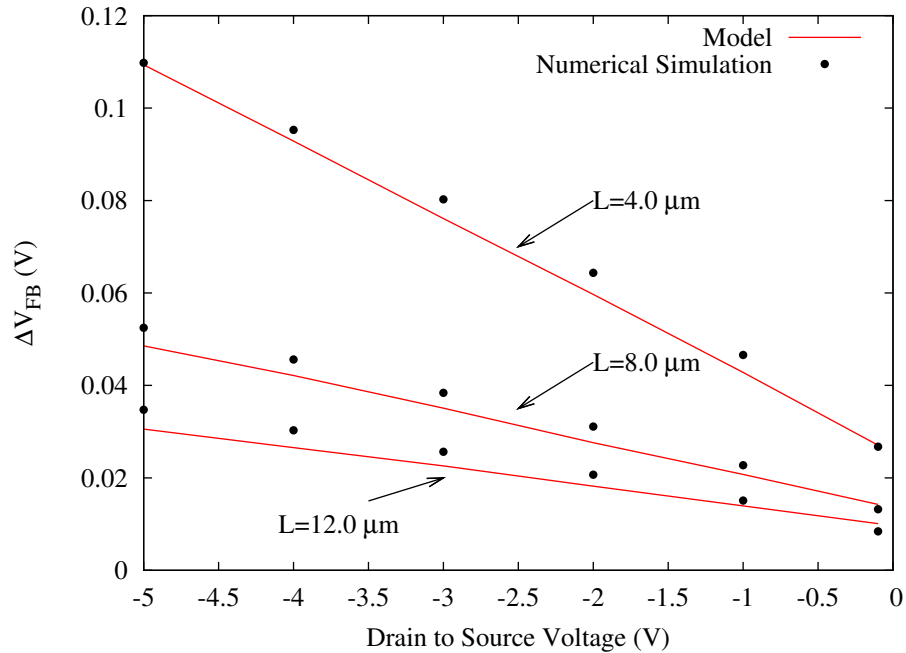


Figure 5.12: A plot of the shift in flatband voltage versus drain voltage due to the fringing electric field for $V_{GS} = 0.3$ V.

Two-dimensional simulations were conducted using standard SiOG PACC specifications: silicon film ($N_A = 2 \times 10^{15}$) thickness equal to 200 nm and a top gate oxide of 50 nm. The flatband voltage was set to zero volts for simplicity; $8 \mu\text{m}$ was used as the length of the source and drain in all calculations unless otherwise specified, and the length of the conducting channel is given in each plot. The glass thickness was set to $40 \mu\text{m}$ in simulation, and a constant mobility model was used for simplicity. In all plots, ΔL was determined to be $0.8 \mu\text{m}$.

In Figures 5.6-5.10, the value of the fringing field is plotted against different parameters. In these plots, the fringing field was evaluated at $L/2$ and the values of V_{SE} , V_{DE} , and V_{BE} used in the compact model were taken from the Silvaco Atlas simulation. Figures 5.6 and 5.7 show the effect of channel length and source drain length on the fringing electric field. Figure 5.8 plots the fringing field versus V_{DS} for $V_{GS} = 0.3$ V placing the device in subthreshold operation. Figures 5.9 and

5.10 chart the fringing field versus gate voltage for low ($V_{DS} = -0.1$ V) and high ($V_{DS} = -5.0$ V) drain voltages, respectively.

Figures 5.11 and 5.12 show the shift in flatband voltage versus channel length and drain voltage. The shift was calculated by solving for the required gate voltage to generate $1 \frac{nA}{W/L}$ of drain current, similar to the traditional threshold voltage technique, but ensuring subthreshold operation.

5.6 Conclusion

In this chapter, a compact model describing the fringing field in SiOG devices was developed using a simple conformal map. In addition, an expression relating the fringing field in the subthreshold to the drain current in the device was developed. Good correspondence was found between the 2D numerical simulation and the compact model.

Chapter 6

Homotopy Analysis Method

6.1 Introduction

For all but the most trivial cases, the set of coupled nonlinear partial differential equations that describe semiconductor device behavior has not been solved analytically (See Chapter 1). Specialized commercial [63–65] packages are available to compute numerical solutions to the semiconductor equations based on finite difference or finite element techniques, and generic math packages such as Mathematica can compute numeric solutions using Runge-Kutta methods, but finding analytic solutions has been very challenging. In fact, even when the semiconductor equations that represent current flow, charge distribution, and potential distribution are decoupled and device specific simplifications are applied, analytic solutions remain elusive. In this chapter, a new solution technique, the Homotopy Analysis Method, or HAM [66–68], is for the first time applied to semiconductor device problems. In general, the HAM technique can be used to solve nonlinear ODEs and PDEs. Here it is applied to the complete 1-D Poisson equation for the doped Symmetric Double-Gate MOSFET. The work described in this chapter was first published in the *Journal of Communications in Nonlinear Science and Numerical Simulation* [69].

6.2 Problem Statement

The potential distribution in a 1-D silicon semiconductor device is described by a variant of the nonlinear Poisson-Boltzmann equation,

$$\frac{d^2\psi}{dx^2} = \frac{-q}{\varepsilon_s} \left[N_A e^{\frac{-\psi}{\phi_t}} - N_A - \frac{N_i^2}{N_A} e^{\frac{\psi}{\phi_t}} + \frac{N_i^2}{N_A} \right] \quad (6.1)$$

where ψ is the electric potential, x is distance, N_A is the doping concentration in the silicon film, N_i is the intrinsic carrier concentration, q is the charge of an electron, ε_s is the permittivity of silicon, and ϕ_t is the thermal voltage. By applying different boundary conditions, a wide range of semiconductor devices can be modeled. This chapter focuses on a large class of devices known as Double-Gate MOSFETs which are described by the following boundary conditions,

$$\left. \frac{d\psi}{dx} \right|_{x=0} = 0 \quad (6.2)$$

$$\psi|_{x=0} = \psi_o. \quad (6.3)$$

where $x = 0$ is the center of the body that is bounded by the two gates. Two particular devices that have seen a lot of attention lately are the Symmetric Double Gate MOSFET [70–75] as it is one of several technologies promising to extend Moore's Law [4], and the thin-film MOSFET on a thick insulating substrate [46, 51, 76, 77], which is the class of devices of which SiOG devices are a part. Both of these devices can be modeled by applying boundary conditions (6.2) and (6.3) to (6.1).

6.3 HAM Description

Developed in 1992 by Liao [66,67], HAM is a general analytic technique for generating series solutions to various kinds of nonlinear problems in science and engineering. Many problems have already been solved using HAM including nonlinear oscillations [78,79,79–81], boundary layer flows [79,82,83], heat transfer [83,84], nonlinear water waves [81,85], the Thomas-Fermi [86,87] equation, and many more. Unlike perturbation methods, the range of validity of the HAM solution is not limited to problems with small or large parameters. HAM provides a simple way to ensure the convergence of the series solution and is therefore valid for strongly nonlinear problems. Most importantly, HAM provides the freedom to choose the proper basis functions which are specific to each particular nonlinear problem. Along with the basis functions, the user of HAM must also choose other parameters and functions including the initial approximation, the auxiliary linear operator, the auxiliary function, and the auxiliary parameter. These user-specified parameters and functions will be discussed in Section 6.4. Although Liao provides some general rules for choosing these parameters, currently there are no specific rules governing these choices. The user must employ a “trial and error” approach in order to obtain parameters and functions that lead to a rapidly converging series solution.

6.4 An Overview of HAM

Consider the following differential equation

$$\mathcal{A}[u(t)] = 0 \tag{6.4}$$

where \mathcal{A} is a nonlinear operator, t is the independent variable, and $u(t)$ is an unknown function. Let $u_o(t)$ be an initial approximation of $u(t)$. HAM is based on a

mapping from $u(t) \Rightarrow \Phi(t; \lambda)$ such that as λ , the so-called embedding parameter, goes from 0 to 1, and $\Phi(t; \lambda)$ varies from the initial guess $u_o(t)$ to the exact solution $u(t)$. This mapping is generated by the *zero-order deformation equation* which is expressed as

$$(1 - \lambda)\mathcal{L}[\Phi(t; \lambda) - u_o(t)] = \lambda F H(t)\mathcal{A}[\Phi(t; \lambda)] \quad (6.5)$$

where $\Phi(t; \lambda)$ is subject to the initial boundary conditions and where $F \neq 0$ is the auxiliary parameter, $H(t) \neq 0$ is the auxiliary function, and \mathcal{L} is the auxiliary linear operator.

For now, assume that F , $H(t)$, $u_o(t)$, and \mathcal{L} are chosen such that the solution $\Phi(t; \lambda)$ to the zero-order deformation equation exists as do all derivatives with respect to λ . Then let

$$u_o^{[k]}(t) \equiv \left. \frac{\partial^k \Phi(t; \lambda)}{\partial \lambda^k} \right|_{\lambda=0} \quad (6.6)$$

where $u_o^{[k]}$ is called the *kth-order deformation derivative*. Now define

$$u_k(t) \equiv \frac{1}{k!} \left. \frac{\partial^k \Phi(t; \lambda)}{\partial \lambda^k} \right|_{\lambda=0} = \frac{1}{k!} u_o^{[k]}(t). \quad (6.7)$$

To develop HAM, Liao expands $\Phi(t; \lambda)$ in a power series of λ

$$\Phi(t; \lambda) = \Phi(t; 0) + \sum_{k=1}^{\infty} \frac{1}{k!} \left. \frac{\partial^k \Phi(t; \lambda)}{\partial \lambda^k} \right|_{\lambda=0} \lambda^k \quad (6.8)$$

or

$$\Phi(t; \lambda) = u_o(t) + \sum_{k=1}^{\infty} u_k(t) \lambda^k. \quad (6.9)$$

From (6.9) it can be seen that when $\lambda = 1$, then

$$u(t) = u_o(t) + \sum_{k=1}^{\infty} u_k(t) \quad (6.10)$$

where $u_o(t)$ satisfies the stated boundary conditions and each $u_k(t)$ has zero boundary values. The K^{th} order HAM approximation of $u(t)$ is defined as

$$u(t) \approx \sum_{k=0}^K u_k(t). \quad (6.11)$$

It can be seen that (6.10) provides a relationship between the exact solution, $u(t)$, and the initial approximation, $u_o(t)$, by means of the series of terms $u_k(t)$ providing:

1. the solution of (6.5) exists for all $\lambda \in [0, 1]$
2. the deformation derivative, $u_o^{[k]}$, exists for all k
3. the power series (6.9) converges at $\lambda = 1$.

It remains now to find each u_k . This is accomplished by first defining the vector

$$\mathbf{u}_{k-1} = [u_o(t), u_1(t), u_2(t) \dots u_{k-1}(t)]. \quad (6.12)$$

Differentiating the zero-order deformation equation, (6.5), with respect to λ , setting $\lambda = 0$, and dividing by $k!$ gives

$$\mathcal{L}[u_k(t) - \chi_k u_{k-1}] = FH(t)R_k(\mathbf{u}_{k-1}) \quad (6.13)$$

where

$$R_k(\mathbf{u}_{k-1}) = \frac{1}{(k-1)!} \left. \frac{\partial^{k-1} \mathcal{A}[\Phi(t; \lambda)]}{\partial \lambda^{k-1}} \right|_{\lambda=0} \quad (6.14)$$

$$\chi_k = \begin{cases} 0 & \text{when } k \leq 1 \\ 1 & \text{otherwise} \end{cases} \quad (6.15)$$

Equation (6.13) is known as the k^{th} order deformation equation. According to (6.13) every u_k can be found with a recursion relation.

As mentioned previously in Section 6.3, in order to apply HAM the user must specify:

1. a set of basis functions

$$\mathbf{P} = \{e_n(t) | n = 0, 1, 2, 3, \dots\} \quad (6.16)$$

2. an initial guess, $u_o(t)$, which satisfies the stated boundary conditions
3. an auxiliary linear operator, \mathcal{L}
4. an auxiliary function, $H(t)$
5. an auxiliary convergence parameter F .

These functions and parameters cannot be chosen arbitrarily in that they must satisfy three rules; namely, the *rule of solution expression*, the *rule of coefficient ergodicity*, and the *rule of solution existence*.

The rule of solution expression states that the basis set must be chosen such that

$$u(t) = \sum_{n=0}^{\infty} c_n e_n(t), \quad (6.17)$$

which implies that $u_o(t)$ as well as all $u_k(t)$ are in the space spanned by \mathbf{P} . Furthermore, \mathbf{P} must be closed under the operators \mathcal{L} , \mathcal{A} , and $H(t)R_k(\mathbf{u}_{k-1})$. Consequently, it follows immediately that the so-called special solution, $u_k^*(t)$, of the high-order deformation equation, (6.13), must be given by

$$u_k^*(t) = \mathcal{L}^{-1} [F H(t) R_k(\mathbf{u}_{k-1})] + \chi_k u_{k-1} = \sum_{n=0}^{M(k)} a_n e_n(t) \quad (6.18)$$

where a_n is a coefficient and \mathcal{L}^{-1} is the inverse of the auxiliary linear operator.

The rule of coefficient ergodicity requires that as n approaches infinity in (6.17), all basis functions in \mathbf{P} must appear in the final solution; that is, the final solution expression should be complete with respect to the set \mathbf{P} . The rule of coefficient ergodicity along with the rule of solution expression insure that the auxiliary function, $H(t)$, can be determined once the basis set, the initial guess, and the auxiliary linear operator are chosen.

The rule of solution existence is perhaps the most important of the three rules in that it specifies the means for determining values of the parameter F for which the solution series (6.10) is convergent. It turns out that the Homotopy Analysis Method generates a family of convergent series, one for each value of F within a convergence range of values. Furthermore, the rate of convergence of the series depends on the particular value of F within this range. Typically, there is an optimum value of F for which the solution series (6.10) converges with the fewest number of terms. As will be shown, the convergence range can be determined from so-called F -curves. It should be emphasized that in addition to the value of F , the rate of convergence is significantly influenced by the choices of basis set, initial guess, and auxiliary linear operator.

6.5 Equation Transformation and Setup

Although the form of (6.1) is written such that it is recognizable to the semiconductor community, it is useful to transform this equation to a form that is more convenient for the application of the Homotopy Analysis Method. According to (6.4), the nonlinear operator \mathcal{A} is given by

$$\mathcal{A}[\psi(x)] = \frac{d^2\psi}{dx^2} + \frac{q}{\varepsilon_s} \left[N_A e^{-\frac{\psi}{\phi_i}} - N_A - \frac{N_i^2}{N_A} e^{\frac{\psi}{\phi_i}} + \frac{N_i^2}{N_A} \right]. \quad (6.19)$$

The exponential terms in (6.19) can be eliminated by creating the new variable, p , which is given by:

$$p = N_A e^{-\frac{\psi}{\phi_t}}. \quad (6.20)$$

This variable is recognizable as the hole concentration in the silicon film. Equation (6.19) can be rewritten in terms of p as

$$pp'' - (p')^2 - \frac{qN_A}{\varepsilon_s \phi_t} \left[\frac{p^3}{N_A} - \left(1 - \frac{N_i^2}{N_A^2} \right) p^2 - \frac{N_i^2}{N_A} p \right] = 0 \quad (6.21)$$

subject to the boundary conditions

$$p'(0) = 0 \quad (6.22)$$

$$p(0) = p_o \quad (6.23)$$

where p' and p'' indicate the first and second derivatives with respect to x , respectively. Equation (6.21) is further transformed by normalizing x with respect to the silicon film thickness, x_{si} , and p with respect to its initial value, p_o . Setting

$$y = \frac{x}{x_{si}} \quad (6.24)$$

and

$$\frac{p(x)}{p_o} = u(y) \quad (6.25)$$

leads to the normalized expression:

$$uu'' - (u')^2 - \alpha u^3 + \beta u^2 + \gamma u = 0 \quad (6.26)$$

where

$$\alpha = \frac{qx_{si}^2 p_o}{\varepsilon_s \phi_t} \quad (6.27)$$

$$\beta = \frac{qx_{si}^2}{\varepsilon_s \phi_t} \left(N_A - \frac{N_i^2}{N_A} \right) \quad (6.28)$$

$$\gamma = \frac{qx_{si}^2}{\varepsilon_s \phi_t} \left(\frac{Ni^2}{p_o} \right) \quad (6.29)$$

subject to the boundary conditions

$$u'(0) = 0 \quad (6.30)$$

$$u(0) = 1. \quad (6.31)$$

It was determined empirically that the rate of convergence could be improved by transforming (6.26) to the variable $\zeta = \frac{1}{u}$ which yields:

$$\zeta \zeta'' - (\zeta')^2 + \alpha \zeta - \beta \zeta^2 - \gamma \zeta^3 = 0 \quad (6.32)$$

Furthermore, it is known that the solution $p(x)$ appears to increase hyper-exponentially with respect to x . This suggests that the transformation $\eta = e^y$ and $\zeta(y) = w(\eta)$ should be made. Applying this transform to (6.32) yields

$$w (w'' \eta^2 + w' \eta) - (w')^2 \eta^2 + \alpha w - \beta w^2 - \gamma w^3 = 0. \quad (6.33)$$

According to (6.24), $y \in [0, 1]$ which implies $\eta \in [1, e]$. The final transformation shifts the η axis back to zero by letting $z = \eta - 1$ and $v(z) = w(\eta)$:

$$vv''(z+1)^2 + vv'(z+1) - (v')^2(z+1)^2 + \alpha v - \beta v^2 - \gamma v^3 = 0 \quad (6.34)$$

$$v'|_{z=0} = 0 \quad (6.35)$$

$$v|_{z=0} = 1. \quad (6.36)$$

The variable v in (6.34) is related to the potential ψ by

$$\psi = -\phi_t \ln \left(\frac{p_o}{v(z)N_A} \right) = \psi_o + \phi_t \ln v \quad (6.37)$$

where $\psi_o = \psi(x = 0)$ and

$$x = x_{si} \ln(z + 1) \quad (6.38)$$

where $z \in [0, e - 1]$.

6.6 Application of HAM

6.6.1 Basis Set

Several attempts were made to apply HAM to (6.26) and (6.32) using a variety of basis sets including power series in y , exponential series in y , and even products of polynomials and exponentials in y . Unfortunately, none of the solutions converged even when the computations were carried out to order $K > 25$. The reason for the failure to converge was that the trial basis functions lacked sufficient power to express the observed hyper-exponential behavior of the variable p . It was realized that the transform $\eta = e^y$, converts an exponential series in η to a hyper-exponential series in y :

$$u(\eta) = \sum_n c_n e^{n\eta} = \sum_n c_n e^{ne^y}. \quad (6.39)$$

On the other hand, it can be seen from (6.33) that the basis (6.39) violates the rule of solution expression since (6.33) contains terms like η and η^2 . However, a basis set for (6.34) that both satisfies the rule of solution expression and includes the exponential behavior is given by

$$v(z) = \sum_m \sum_n c_{mn} z^m e^{-nz}. \quad (6.40)$$

6.6.2 Linear Operator

According to HAM, the highest order of the auxiliary linear operator must be the same as that of the nonlinear operator. The simplest auxiliary linear operator that satisfies this condition is

$$\mathcal{L}[\Phi] = \frac{d^2\Phi}{dz^2}. \quad (6.41)$$

Associated with this linear operator are two arbitrary constants, C_1 and C_2 , which are coefficients of the two “homogeneous” solutions of this operator:

$$\mathcal{L}[C_1 + C_2z] = 0. \quad (6.42)$$

It is important to realize that these homogeneous solutions must be added to the special solutions $u_k^*(z)$, equation (6.18), for each order k .

6.6.3 Initial Guess

The initial guess must satisfy the boundary conditions (6.35) and (6.36) and must be one of the basis functions given in (6.40). The simplest function that satisfies these conditions is

$$v_o = 1. \quad (6.43)$$

This particular choice has the advantage that it reduces the computational complexity in determining each v_k , thereby making it possible to compute a higher order series approximation.

6.6.4 Auxiliary Function

In order to comply with the rules of ergodicity and solution expression, the auxiliary function must be of the form:

$$H(z) = e^{-z}. \quad (6.44)$$

This is true since no exponential terms appear in the nonlinear operator nor are they introduced in the chosen auxiliary linear operator or the chosen initial guess.

6.7 Evaluation of R_k

According to (6.14), the quantity $R_k(v_{k-1})$ is obtained by evaluating the $(k-1)^{th}$ partial derivative of $\mathcal{A}[\Phi(z; \lambda)]$ with respect to λ at $\lambda = 0$. From (6.34) it can be seen that $\mathcal{A}[\Phi(z; \lambda)]$ contains six terms, five of which are nonlinear in Φ . Application of Liebnitz's rule for derivatives of products to the five nonlinear terms and using the definition (6.7) for $v_k(z)$ yields the following expressions where Q_m is the m^{th} term as shown in (6.51):

$$Q_1 \equiv \frac{1}{(k-1)!} \left. \frac{\partial^{k-1} [\Phi \Phi'']}{\partial \lambda^{k-1}} \right|_{\lambda=0} = \sum_{j=0}^{k-1} v_j v''_{k-1-j} \quad (6.45)$$

$$Q_2 \equiv \frac{1}{(k-1)!} \left. \frac{\partial^{k-1} [\Phi \Phi']}{\partial \lambda^{k-1}} \right|_{\lambda=0} = \sum_{j=0}^{k-1} v_j v'_{k-1-j} \quad (6.46)$$

$$Q_3 \equiv \frac{1}{(k-1)!} \left. \frac{\partial^{k-1} [(\Phi')^2]}{\partial \lambda^{k-1}} \right|_{\lambda=0} = \sum_{j=0}^{k-1} v'_j v'_{k-1-j} \quad (6.47)$$

$$Q_5 \equiv \frac{1}{(k-1)!} \left. \frac{\partial^{k-1} [\Phi^2]}{\partial \lambda^{k-1}} \right|_{\lambda=0} = \sum_{j=0}^{k-1} v_j v_{k-1-j} \quad (6.48)$$

and

$$Q_6 \equiv \frac{1}{(k-1)!} \left. \frac{\partial^{k-1} [\Phi^3]}{\partial \lambda^{k-1}} \right|_{\lambda=0} = \sum_{j=0}^{k-1} \sum_{r=0}^{k-1-j} v_j v_r v_{k-1-j-r}. \quad (6.49)$$

The remaining linear term yields

$$Q_4 \equiv \frac{1}{(k-1)!} \left. \frac{\partial^{k-1} [\Phi]}{\partial \lambda^{k-1}} \right|_{\lambda=0} = v_{k-1}. \quad (6.50)$$

The k th order deformation (6.13) therefore can be rewritten as

$$\begin{aligned} \frac{\partial^2}{\partial z^2} [v_k(z) - \chi_k v_{k-1}(z)] &= F e^{-z} [(z+1)^2 Q_1] \\ &+ F e^{-z} [(z+1) Q_2 - (z+1)^2 Q_3] \\ &+ F e^{-z} [\alpha Q_4 - \beta Q_5 - \gamma Q_6]. \end{aligned} \quad (6.51)$$

6.8 Computation

Equation (6.51) can be processed either symbolically using computer algebra systems such as Mathematica or Maxima [88] or numerically using C or MATLAB. In either case, computation is made more efficient if (6.51) is carried out in parallel using matrix operations. Each v_k can be expressed as a linear combination of basis functions

$$v_k(z) = \sum_{m=0}^M \sum_{n=0}^N c_{mn}^k z^m e^{-nz} \quad (6.52)$$

where the indexes M and N are also assumed to be functions of k . The coefficients c_{mn}^k in (6.52) can be represented as a matrix \mathbf{V}_k where the columns correspond to

different exponential terms and the rows correspond to different powers of z :

$$\mathbf{V}_k \equiv \begin{bmatrix} c_{00}^k & c_{01}^k & \cdots & c_{0N}^k \\ c_{10}^k & c_{11}^k & \cdots & c_{1N}^k \\ \vdots & \vdots & \vdots & \vdots \\ c_{M0}^k & c_{M1}^k & \cdots & c_{MN}^k \end{bmatrix}. \quad (6.53)$$

Similarly, the argument of the linear operator on the left hand side of (6.51) can be represented by the matrix \mathbf{A}_k

$$v_k(z) - \chi^k v(z)_{k-1} \rightarrow \mathbf{A}_k \equiv [a_{mn}^k] \quad (6.54)$$

and the right hand side of (6.51) can be represented by the \mathbf{R}_k

$$F H(z) R_k(\mathbf{v}_{k-1}) \rightarrow F \mathbf{R}_k = F [r_{mn}^k]. \quad (6.55)$$

It is straightforward to show from (6.51) that the matrix \mathbf{R}_k is equal to the sum of six separate matrices: one representing each of the six components Q_j defined in (6.45) through (6.50):

$$\mathbf{R}_k = \sum_{j=1}^6 \mathbf{R}_k^j \quad (6.56)$$

where

$$\mathbf{R}_k^1 = \mathbf{H} \otimes \mathbf{F}^2 \otimes \sum_{j=0}^{k-1} \mathbf{V}_j \otimes \mathbf{V}_{k-1-j}'' \quad (6.57)$$

$$\mathbf{R}_k^2 = \mathbf{H} \otimes \mathbf{F} \otimes \sum_{j=0}^{k-1} \mathbf{V}_j \otimes \mathbf{V}_{k-1-j}' \quad (6.58)$$

$$\mathbf{R}_k^3 = -\mathbf{H} \otimes \mathbf{F}^2 \otimes \sum_{j=0}^{k-1} \mathbf{V}_j' \otimes \mathbf{V}_{k-1-j}' \quad (6.59)$$

$$\mathbf{R}_k^4 = \alpha \mathbf{H} \otimes \mathbf{V}_{k-1} \quad (6.60)$$

$$\mathbf{R}_k^5 = -\beta \mathbf{H} \otimes \sum_{j=0}^{k-1} \mathbf{V}_j \otimes \mathbf{V}_{k-1-j} \quad (6.61)$$

and

$$\mathbf{R}_k^6 = -\gamma \mathbf{H} \otimes \sum_{j=0}^{k-1} \sum_{r=0}^{k-1-j} \mathbf{V}_j \otimes \mathbf{V}_r \otimes \mathbf{V}_{k-1-j-r}. \quad (6.62)$$

The matrix $\mathbf{H} = [\delta_{m0}\delta_{n1}]$, where δ_{pq} is the Kronecker delta function, corresponds to the coefficient matrix of $H(z) = e^{-z}$ and the matrix $\mathbf{F} = [\delta_{m0}\delta_{n0} + \delta_{m1}\delta_{n0}]$ corresponds to the coefficient matrix of $f(z) = 1 + z$. The matrices \mathbf{V}'_j and \mathbf{V}''_j represent the coefficient matrices of $\frac{dv_j}{dz}$ and $\frac{d^2v_j}{dz^2}$, respectively, and the symbol \otimes represents 2D matrix convolution. The first derivative of v_k is given by

$$\frac{dv_k}{dz} = \sum_{m=0}^M \sum_{n=0}^N c_{mn}^k [mz^{m-1} - nz^m] e^{-nz}. \quad (6.63)$$

This operation is equivalent to replacing each column vector \mathbf{c}_n^k in \mathbf{V}_k by the column vector $\mathbf{D}_n^1 \mathbf{c}_n^k$, where the $(M+1) \times (M+1)$ matrix \mathbf{D}_n^1 is given by

$$\mathbf{D}_n^1 = \begin{bmatrix} -n & 1 & 0 & \dots & 0 & 0 & 0 \\ 0 & -n & 2 & \dots & 0 & 0 & 0 \\ 0 & 0 & -n & \dots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \dots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & -n & (M-1) & 0 \\ 0 & 0 & 0 & \dots & 0 & -n & M \\ 0 & 0 & 0 & \dots & 0 & 0 & -n \end{bmatrix}. \quad (6.64)$$

Similarly, the second derivative of v_k can be represented by replacing each column vector \mathbf{c}_n^k by the column vector $\mathbf{D}_n^2 \mathbf{c}_n^k$, where \mathbf{D}_n^2 is given by

$$\mathbf{D}_n^2 = \begin{bmatrix} n^2 & -2n & 2 & \dots & 0 & 0 & 0 \\ 0 & n^2 & -4n & \dots & 0 & 0 & 0 \\ 0 & 0 & n^2 & \dots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \dots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & \dots & n^2 & -2n(M-1) & M(M-1) \\ 0 & 0 & 0 & \dots & 0 & n^2 & -2nM \\ 0 & 0 & 0 & \dots & 0 & 0 & n^2 \end{bmatrix}. \quad (6.65)$$

Equation (6.51) can now be represented by the matrix equation

$$\mathbf{D}_n^2 \mathbf{a}_n^k = F \mathbf{r}_n^k \quad (6.66)$$

where \mathbf{a}_n^k and \mathbf{r}_n^k are vectors corresponding to column n of the matrices \mathbf{A}_k and \mathbf{R}_k , respectively. The elements of matrix \mathbf{R}_k are known since $\mathbf{V}_{k-1}, \mathbf{V}_{k-2}$, etc., are obtained recursively from the initial guess $\mathbf{V}_0 = [\delta_{m0} \delta_{n0}]$. Equation (6.66) can be inverted for each value of $n \neq 0$ to yield

$$\mathbf{a}_n^k = F (\mathbf{D}_n^2)^{-1} \mathbf{r}_n^k \quad n \neq 0 \quad (6.67)$$

where $(\mathbf{D}_n^2)^{-1}$ is the inverse of the matrix \mathbf{D}_n^2 . If $n = 0$, the inverse \mathbf{D}_0^2 can not be found since the determinant of this matrix is equal to zero. The reason why $|\mathbf{D}_n^2| = 0$ is that the first two columns of \mathbf{D}_0^2 are zeros. This is a direct consequence of the fact that C_1 and C_2 are homogeneous solutions of the linear operator \mathcal{L} , as was noted in (6.42). This difficulty can be overcome by solving for the coefficients $\hat{\mathbf{a}}_0^k = \{a_{m0}^k | m = 2, 3, \dots, M\}$ in terms of the coefficients $\hat{\mathbf{r}}_0^k = \{r_{m0}^k | m = 0, 1, 2, \dots, M-2\}$ from the matrix

equation

$$\hat{\mathbf{a}}_0^k = F \left(\hat{\mathbf{D}}_n^2 \right)^{-1} \hat{\mathbf{r}}_0^k \quad (6.68)$$

where the matrix $\hat{\mathbf{D}}_0^2$ is obtained from \mathbf{D}_0^2 by eliminating the first two columns and the last two rows. The solution matrix \mathbf{A}_k can be expressed as

$$\mathbf{A}_k = \begin{bmatrix} C_1 & a_{01}^k & a_{02}^k & \cdots & a_{0N}^k \\ C_2 & a_{11}^k & a_{12}^k & \cdots & a_{1N}^k \\ a_{20}^k & a_{21}^k & a_{22}^k & \cdots & a_{2N}^k \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ a_{M0}^k & a_{M1}^k & a_{M2}^k & \cdots & a_{MN}^k \end{bmatrix}. \quad (6.69)$$

and the solution matrix \mathbf{V}_k is given by

$$\mathbf{V}_k = \mathbf{A}_k + \chi_k \mathbf{V}_{k-1}. \quad (6.70)$$

The constants C_1 and C_2 are determined from the boundary conditions (6.35) and (6.36) and are given by

$$C_1 = - \sum_{n=1}^N a_{0n}^k. \quad (6.71)$$

and

$$C_2 = - \sum_{n=1}^N b_{0n}^k. \quad (6.72)$$

where b_{0n}^k can be obtained from the first row of the matrix obtained by applying the first derivative matrix, \mathbf{D}_n^1 , to matrix \mathbf{V}_k given in (6.70).

As mentioned previously, $v_0(z) = 1$, $H(z) = e^{-z}$, and $\mathcal{L}\Phi = \frac{d^2\Phi}{dz^2}$ were selected as the user-defined functions and linear operator, respectively, for the HAM process. It turns out that these choices lead to nearly triangular $\mathbf{V}_k = [c_{mn}^k]$ matrices of dimension $M \times N \approx 2k \times k$. For the sake of computational convenience, all \mathbf{V}_k matrices were zero-padded to yield square matrices of dimension $(2K + 1) \times (2K + 1)$,

where K is the highest order to be computed. Matrices \mathbf{R}_k^j obtained as a result of 2-D convolutions ((6.57)-(6.62)) are re-sized to $(2K + 1) \times (2K + 1)$ following the convolutions.

6.9 Series Convergence

The HAM process yields a family of solutions of the nonlinear differential equation (6.51)

$$v(z, F) = \lim_{K \rightarrow \infty} \sum_{k=0}^K v_k(z, F). \quad (6.73)$$

This series is not convergent for all values of F . In general there is a limited range of values for which convergence is realized. Liao's convergence theorem [67] states that as long as the series (6.73) is convergent, it must be a solution to the associated nonlinear differential equation (6.51). This theorem implies that the family of functions given in (6.73) must all yield the same exact solution for $\{F | F \in (F_1, F_2)\}$ so that if one were to plot $v(z_o, F)$ or $\left. \frac{d^n v(z, F)}{dz^n} \right|_{z=z_o}$ ($n = 1, 2, 3, \dots$) as a function of F , one should observe a horizontal line F in this range. Figure 6.1 shows plots of three derivatives of $v(z, F)$ for $z = z_o = 0$ for the 20th order approximation. It can be seen from the figure that the boundaries for the region of convergence are $F_1 \approx -1.4$ and $F_2 \approx -0.6$.

It should be emphasized that although (6.73) converges for $\{F | F \in (F_1, F_2)\}$, the rate of convergence depends critically on the value of F . Specifically, there is a value $F = F_o$ for which the rate of convergence is optimum, that is, the series converges for the lowest value of K . Liao has found that F_o can be determined by minimizing the following integral

$$\varepsilon(F) \equiv \int_0^{e-1} |\mathcal{A}[v(z, F)]| dz \quad (6.74)$$

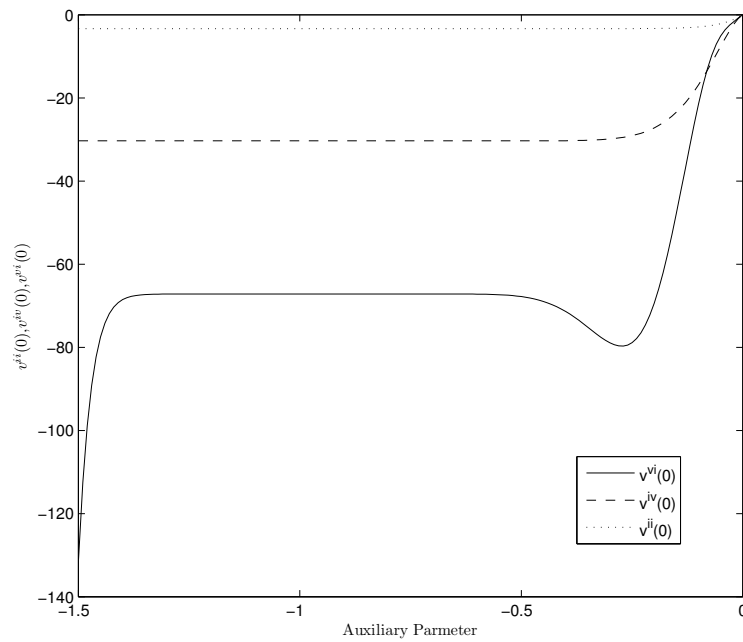


Figure 6.1: Plots of the second, fourth, and sixth derivatives of v evaluated at $z = 0$ as function of F . These derivatives were computed with $\alpha = 8.1035$, $\beta = 4.7667$, and $\gamma = 1.473 \times 10^{-10}$ for $K = 20$. Note that $v''(0)$ and $v^{iv}(0)$ also deviate from horizontal lines, but the deviation is outside the range of the F -axis.

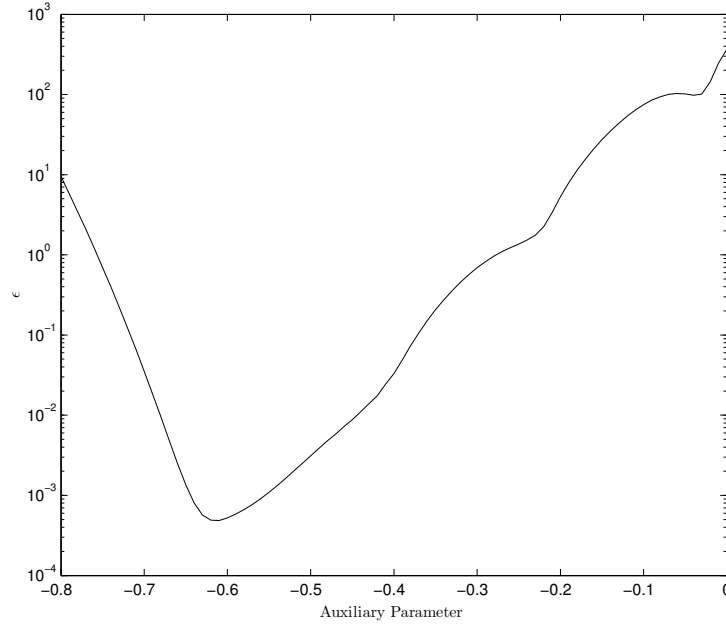


Figure 6.2: Plot of $\varepsilon(F)$ in the convergence region. The minimum value of this function occurs at $F_o = -0.61$. This curve was computed with $\alpha = 8.1035$, $\beta = 4.7667$, and $\gamma = 1.4733 * 10^{-10}$ for $K = 20$.

with respect to F [89]. Since it is rather computationally expensive to calculate (6.74), a discrete version is used in practice:

$$\varepsilon(F) \approx \sum_{k=0}^{10} |\mathcal{A}[v(k/10, F)]|. \quad (6.75)$$

The function $\varepsilon(F)$ was computed for several values of F using (6.75) in the convergence region and a plot of this function is shown in Figure 6.2 for $\psi_o = -0.0137$. As can be seen from the figure, the minimum value of the function occurs at $F_o = -0.61$. Since $\varepsilon(F)$ was computed using an approximate expression, the F_o computed was not exact. In addition, only $K = 20$ terms were used when computing the best F for each different ψ_o . It turns out that for $K = 20$, different values of ψ_o all produce similar values of F , but that is not always the case for $K > 20$. In particular it was found that $F = -0.4$ converged faster for $\psi_o = 0.5819$ while for

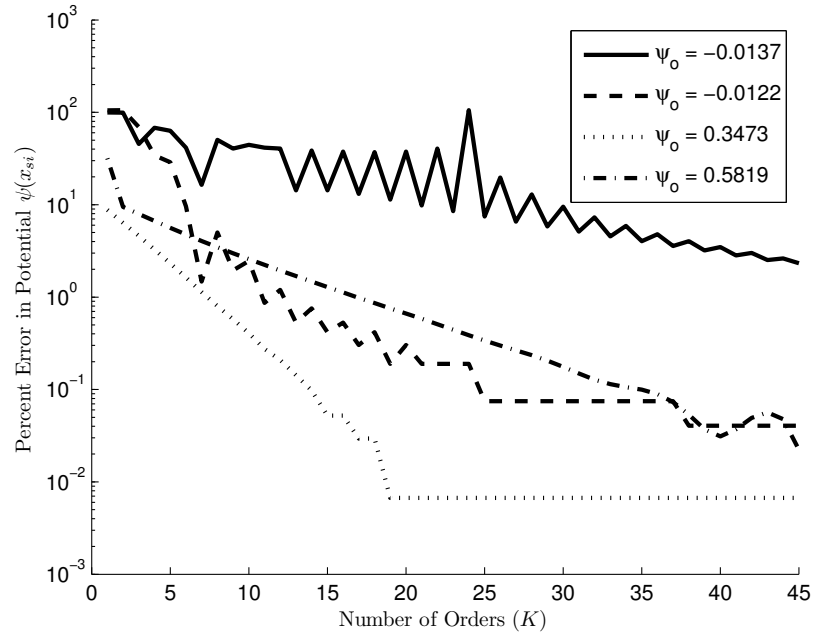


Figure 6.3: Plot of percent error in $\psi(x_{si})$ obtained using HAM compared to the Runge-Kutta algorithm at $\psi_{x_{si}}$ for different values of ψ_o . $\psi_o = -0.0137$ corresponds to $\alpha = 8.1035$, $\beta = 4.7667$, $\gamma = 1.4738 * 10^{-10}$ and $F = -0.63$. $\psi_o = -0.0122$ corresponds to $\alpha = 7.6268$, $\beta = 4.7667$, $\gamma = 1.5659 * 10^{-10}$ and $F = -0.63$. $\psi_o = 0.3473$ corresponds to $\alpha = 7.150 * 10^{-6}$, $\beta = 4.7667$, $\gamma = 1.670 * 10^{-4}$ and $F = -0.63$. $\psi_o = 0.5819$ corresponds to $\alpha = 8.34 * 10^{-10}$, $\beta = 4.7667$, $\gamma = 1.4317$ and $F = -0.4$.

other values of ψ_o , $F = -0.63$ seemed to converge the fastest.

The rate of convergence is also found to depend heavily on the values of α , β , and γ . To illustrate this difference, the HAM solution was compared to the solution obtained by Mathematica's NDSolve function using the Runge-Kutta method. The percent error in $\psi(x_{si})$ (the value of potential at which the largest error was observed) was plotted in Figure 6.3 as a function of order K for four different values of ψ_o . The values of ψ_o were chosen to represent typical operating ranges of real MOSFETs.

The value $\psi_o = -0.0137$ showed the slowest convergence rate with approximately 2.3 percent error for $K = 45$.

6.10 Results

Figures 6.4 and 6.5 compare plots of $\psi(\frac{x}{x_{csi}})$ computed using the HAM process with the same function computed using NDSolve and the Runge-Kutta algorithm in Mathematica. These curves were computed for four different initial values, ψ_0 .

As can be seen, the HAM curves agree with the Runge-Kutta results over a wide range of boundary values (which corresponds to a wide range in the values of α and γ).

6.11 Conclusion

It has been shown that the application of the Homotopy Analysis Method can be used to obtain extremely good analytical approximations to the solution of the complete 1-D nonlinear Poisson-Boltzmann for semiconductor devices. To the author's knowledge, this is the first time that such an analytical solution approximation has been obtained for this equation. HAM has the advantage that it can be extended to a wide range of nonlinear electrostatic potential distribution problems that heretofore have been difficult to solve analytically. In addition to solving for potential distributions arising in standard semiconductor devices, HAM can also be used to find approximate analytical solutions to more complicated forms of (6.1) which include the influence of defects and trap states. In contrast to numerical methods such as the Runge-Kutta algorithm, HAM provides an analytical function of position that can be differentiated continuously with respect to x . This attribute is very important when applying the solution function for semiconductor device models where derivative action on the function is always required.

The order required for the HAM approximation to converge can be quite high. Convergence requiring values of K in the range of 20 to 50, depending on the degree on non-linearity, is not uncommon. Unfortunately, for a given order K , each

coefficient in \mathbf{V}_k depends on all of the coefficients of all \mathbf{V}_k for $k < K$. If the computation is carried out symbolically, this results in an exponential growth in storage requirements as K increases. For example, symbolic processing leads to 4 gigabytes of data for K as low as 13 for the problem presented in this paper. On the other hand, if the computation is carried out numerically, extremely high precision must be used since truncation errors accumulate with each successive order computed. This latter problem can be overcome by representing numbers as exact rationals or multi-precision floating point numbers and avoiding the use of standard double precision floating point numbers. In addition, it is quite possible that convergence for smaller values of K might be possible for different choices of initial guess, auxiliary linear operator, and auxiliary function. We have not exhausted all of the possible ways of applying HAM.

In addition to increasing the rate of convergence, there is still much fertile ground to explore when applying HAM to semiconductor problems. The solution to the potential distribution in other devices could be studied by modifying (6.1) or changing the boundary conditions, as well as extending the current and future applications of HAM to semiconductor problems into two dimensions.

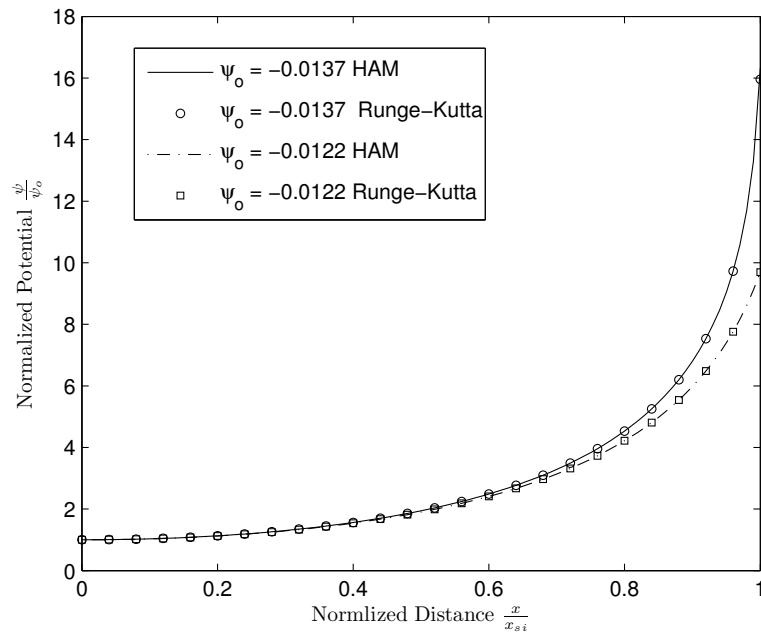


Figure 6.4: Comparison of plots of $\psi(\frac{x}{x_{si}})$ using the HAM process (lines) with plots obtained using the Runge-Kutta algorithm (symbols). The solid curve is for $\alpha = 8.1035$ and $\gamma = 1.473844 * 10^{-10}$. The dashed curve is for $\alpha = 7.6268$ and $\gamma = 1.5659 * 10^{-10}$. These curves were both computed for the 45th order approximation and with the same value of $F_o = -0.63$. The value $\beta = 4.7668$ was used for both cases.

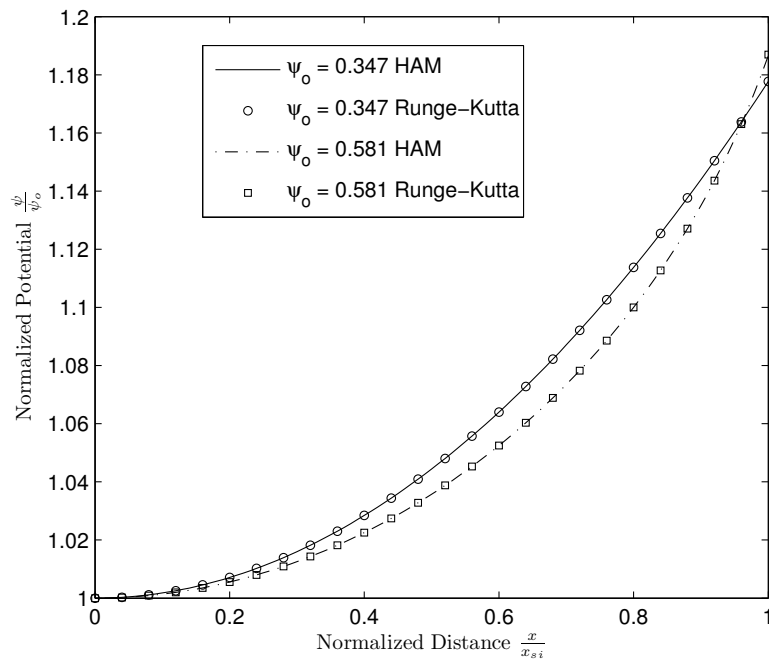


Figure 6.5: Comparison of $\psi(\frac{x}{x_{si}})$ using the HAM process (line) with plots obtained using the Runge-Kutta algorithm (symbol). The solid curve is for $\psi_0 = 0.3473$ corresponding to $\alpha = 7.150 \times 10^{-6}$, $\beta = 4.7667$, $\gamma = 1.670 \times 10^{-4}$ and $F = -0.63$. The dashed line is for $\psi_0 = 0.5819$ corresponding to $\alpha = 8.34 \times 10^{-10}$, $\beta = 4.7667$, $\gamma = 1.4317$ and $F = -0.4$. The HAM curve was computed using the 45th order approximation.

Chapter 7

Future Work

As with all engineering and scientific explorations, there is always more work to be done. The adoption of the SiOG Technology by circuit design community will not occur until accurate device models are readily available within commercial circuit simulation environments. Therefore the ultimate goal of this project is to provide the community with a compact model for circuit simulation. Development of the complete compact model for circuit simulation has begun and is named SimDOG (Simulation of Devices on Glass).

The work presented in this dissertation is a good start towards that goal, but developing a useful compact model is not a trivial undertaking and requires the cooperation of many people. The complete development of compact model includes much more than just a set of equations which describe the device behavior and the initial development of a Verilog-A model. The development of a quality compact model, like any large software project, requires source code and revision control, testing, documentation, release procedures, and ongoing enhancements and maintenance.

A model is only as good as the values of the parameters used. Software must be developed which can quickly and accurately extract the best value of the model

parameters to match measured data. This software would ideally be included with the public release of the compact model.

In addition to releasing the model, there is always room to improve the core model equations. There are a number of known effects that have yet to be implemented including self-heating, breakdown, and gate-induced drain leakage.

New mathematical techniques for solving differential equations are always being developed, some of which may greatly improve compact modeling efforts. The application of new solution or approximation techniques to the fundamental semiconductor equations could lead to a more physical, accurate and or a more computationally efficient model. Another area for improvement is the methods and equations used for describing and or adding secondary effects to the core model equations. These equations can always be improved, yielding more accurate solutions with easier parameter extraction.

Although challenges still remain, the development of accurate process, device, and circuit models of technologies in the semiconductor industry has been shown to be indispensable in its evolution. These models not only simply our understanding of this microscopic world today but suggest what can be tomorrow. Likewise, the acceptance of SiOG as a viable technology will also depend on the development and availability of good models. Hopefully, this work has taken us one small step down that path.

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Appendix A

Verilog-A Model

```
'include "constants.vams"
'include "disciplines.vams"

module PACC( source, drain, gate );
inout source, drain, gate;

electrical source, drain, gate;

//Physical Constants
parameter real W = 4e-4;
parameter real L = 4e-4;
parameter real Vfb = 1.327;

//RDS
parameter real rmin=1000e9;

parameter real Eox = 3.45E-13;
parameter real Xox = 500E-8;
parameter real PhiT = ( 300 * 8.617343E-5 );
parameter real Na = 2E15;
parameter real q = 1.602E-19;
parameter real Xsi = 2000E-8;
parameter real Es = 1.04E-12;

//Extracted Parameters
parameter real C1 = 3.87235E-8;
parameter real c = 9.41262E14;
parameter real d = 3.80034E23;
parameter real f = 1.82246E-8;

//CLM Parameters
parameter real Pvfbt = 2;
parameter real Pvfba = 10;
parameter real OSvd = 2;
parameter real LAMBDA_ACC = 0.24;
parameter real LAMBDA_DEC = 0.005;

//Effective Vg Parameters
parameter real n = 3.353;
parameter real OSvg = -0.03;
parameter real Pvg = 1.6222;
```

```

//Mobility
parameter real mu = 124;
parameter real Eo = 2.2e6;
parameter real v = 1.2;
parameter real Vz = 0.2;

//Variables
real Qf; //Fixed Charge
real Cox; //Oxide Capacitance
real C2;
real R;
real EFF;

// Terminal Voltages
real Vgs;
real Vds;

//Other variables

real QASSLambertWInput;
real QOLambertWInput;
real QALambertWInput;
real QASSLambertWApprox;
real QOLambertWApprox;
real QALambertWApprox;
real QASSApprox;
real QAApprox;
real QAS;
real QAD;
real Qgate;
real Qgate_num;
real Qgate_den;
real Qdrain;
real Qdrain_num;
real Qdrain_den;
real Qsource;
real SQQAS;
real SQQAD;
real CUQAS;
real CUQAD;
real tempCurr1;
real tempCurr2;
real tempsqrt;
real curr;
real mur;
real DELVFBA;
real DELVFBD;
real DELVFBT;
real VGEFF_temp;
real VGEFF;
real Qtemp;
real Qdraint;
real Qsourcet;
real Vgd;

integer mcd;
integer swap;

//This function provides an initial guess for the charge in the device
analog function real QAGUESS;
input Vch, Vg, Qf, Cox;
real Vch, Vg, Qf, Cox;
real x,y;
real temp1;
real temp2;
real temp3;
real tempvch;

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real L1;
real L2;
integer overflowControl;

begin

tempvch=Vch;

// y is the value inside the exponential inside the LambertW function
y = ( ( Qf / ( Cox * PhiT ) ) +
      ( ( tempvch ) / PhiT ) - ( ( Vg ) / PhiT ) );

//If y is small use rational approximation to the LambertW function
if (y < 6) begin

x= C1 * exp(y) / ( Cox * PhiT );
temp1 = ( x + ( (228.0/85.0) * pow( x, 2.0 ) ) +
          ( (451.0/340.0) * pow( x, 3.0 ) ) );

overflowControl = log( temp1 ); //Because the variable is an integer, this will take on
                               //the value of the power to which temp 1 is raised to within 1
                               //(the decimal representing the exact value is rounded off)
                               //This is used to avoid overflow

//This is done to avoid overflow
temp1 = ( temp1 / pow( 10, overflowControl ) );

temp2 = ( 1.0 + ( (313.0/85.0) * x ) +
          ( (1193.0/340.0) * pow( x, 2.0 ) ) +
          ( (133.0/204.0) * pow( x, 3.0 ) ) );

//This is done to avoid overflow
temp2 = ( temp2 / pow( 10, overflowControl ) );

//If y is large use an asymptotic series from Wolfram.com
end else begin
L1 = y + ln(C1) - ln( Cox * PhiT );
L2 = ln(L1);

temp1 = L1 - L2 + L2*(-2.0+L2)/(2*pow(L1,2)) +L2*(6-9*L2+2*pow(L2,2))/(6*pow(L1,3));
temp2 = 1;
end

temp3 = temp1/temp2;

QAGUESS = temp3;

end

endfunction
//Function running Newton's Method on the approximate value of Qh to
//more accurately approximate it

analog function real QhNewtonIteration;
input Qh, Vch, Vg, Cox, R, Qf;
real Qh, Vch, Vg, Cox, R, Qf;
integer mcd;

// f(Qh)
real fx;

// f'(Qh)
real dfx;
real temp;
real temp2;

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real temp3;
real temp4;

begin

temp = c*Qh + d*pow(Qh,2.0) + R*pow(Qh,3.0);
temp2 = ( Na * ( f + Qh ) );
temp3 = temp / temp2;

if (temp3 < pow(10,-37)) begin
temp3 = pow(10,-37);
end

fx = ( Vg - Vch + PhiT * ( ln( temp3 ) ) + ( ( Qh - Qf ) / Cox ) );

dfx = ( 1 / Cox ) + ( PhiT / Qh ) * ( ( f / ( f + Qh ) ) + (Qh*(d + 2 * Qh * R))/(c+(Qh*(d+Qh*R))) );

temp4 = Qh - ( fx/dfx );

QhNewtonIteration = temp4;

end

endfunction

//The beginning of the actual program

analog begin

//Calculate Parameters

Qf = ( q * Na * Xsi );
Cox = ( Eox / Xox );
C2 = ( 2 * q * Es * PhiT * Na );
R = ( 1 / ( C2 / Na ) );
R = 1.05e32;

//If Vds>0 swap the source and drain

swap = 0 ;
Vds = V(drain) - V(source);
Vgs = (V(gate) - V(source)) ;
Vgd = (V(gate) - V(drain)) ;
if ( Vds >= 0 ) begin
swap=1;

Vds = -1*Vds;
Vgs = (V(gate) - V(drain));
Vgd = (V(gate) - V(source)) ;
end

//Calculate Effective Gate Voltage

Vgs = Vgs + Vfb;

VGEFF_temp = Vgs * ( 1 + tanh(-1 * ( Vgs + OSvg ) * Pvg ) ) / 2 +
( Vgs / n ) * ( 1 + tanh(1 * ( Vgs + OSvg ) * Pvg ) ) / 2;

//Calculate CLM+DIBL Parameters

DELVFBA = ((Vds-VGEFF_temp) * LAMBDA_ACC / ( L * pow(10,4) )) *
(tanh(-1*(Vds-VGEFF_temp)*Pvfba)+1)/2;
DELVFBD = Vds * LAMBDA_DEC;
DELVFBT = DELVFBA * ( -1 * Pvfbt * (VGEFF_temp + OSvd) /
sqrt ( 1 + pow ( Pvfbt * VGEFF_temp + Pvfbt * OSvd ,2) ) + 1 ) /2
+ DELVFBD * ( Pvfbt * (VGEFF_temp + OSvd) /

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sqrt ( 1 + pow ( Pvfbt * VGEFF_temp + Pvfbt * OSvd ,2)) +1 ) /2 ;

VGEFF = VGEFF_temp+DELVFBT;

// Value being input into the Lambert W Function approximation to find a
// starting value to run Newton's Method to approximate Qh for Vch = 0.

QASSLambertWApprox = QAGUESS( 0.0, ( VGEFF ), Qf, Cox );
QASSApprox = ( QASSLambertWApprox * Cox * PhiT );

if (QASSApprox < pow(10,-35)) begin
QASSApprox = pow(10,-35);
end

//Repeating the above process for Vch = Vds
QALambertWApprox = QAGUESS( Vds, ( VGEFF ), Qf, Cox );
QAApprox = ( QALambertWApprox * Cox * PhiT );

//Using iteration of Newton's Method to approximate Qh(source) and Qh(drain) more accurately

repeat (3) begin
QASSApprox = QhNewtonIteration( QASSApprox, 0.0, ( VGEFF ), Cox, R, Qf );
QAApprox = QhNewtonIteration( QAApprox, ( Vds ), ( VGEFF ), Cox, R, Qf);
end

//Charge Model
QAS = QASSApprox;
QAD = QAApprox;

SQQAS = pow(QAS, 2);
SQQAD = pow(QAD ,2);
CUQAS = pow(QAS,3);
CUQAD = pow(QAD,3);

Qgate_num = 2 * L * ( SQQAD + QAD*QAS + SQQAS + 3 * Cox * PhiT * (QAD+QAS))*W;
Qgate_den = 3 * ( 4 * Cox * PhiT + QAD + QAS);
Qgate = Qgate_num / Qgate_den;

Qdrain_num = ( L * ( 6 * CUQAD + 12 * SQQAD * QAS + 8 * QAD * SQQAS + 4 * CUQAS
+ 40 * pow (Cox * PhiT,2) * ( 2 * QAD + QAS) + 5 * Cox * PhiT *
( 9 * SQQAD + 10 * QAD * QAS + 5 * SQQAS )) * W );

Qdrain_den = (15 * pow((4 * Cox * PhiT + QAD + QAS ),2) );

Qdrain = Qdrain_num / Qdrain_den;
Qsource = Qgate - Qdrain;

//Mobility Reduction

EFF = ( abs (VGEFF) / (6 * Xox ) ) + ( abs ( VGEFF - Vz ) / (3 * Xox ) );
mur = mu / (1 + pow ( (EFF / Eo) , v ));

//mur=487.3;

tempsqrt = sqrt(d)*sqrt(-d+(4*c*R/d));

tempCurr1 = 2*PhiT*QAS+SQQAS/(2*Cox)-(PhiT/R)*tempsqrt*atan((d+2*QAS*R)/tempsqrt)
+f*PhiT*ln(f+QAS)-((d*PhiT)/(2*R))*ln (c + QAS * (d + QAS*R));

tempCurr2 = 2*PhiT*QAD+SQQAD/(2*Cox)-(PhiT/R)*tempsqrt*atan((d+2*QAD*R)/tempsqrt)
+f*PhiT*ln(f+QAD)-((d*PhiT)/(2*R))*ln (c + QAD * (d + QAD*R));

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curr = ( W / L ) * mur * ( tempCurr2 - tempCurr1 );

if (swap == 0 ) begin
I( drain, source ) <+ curr+ V(drain,source)/rmin;

end else begin
I( drain, source ) <+ -1 * (curr )+ V(drain,source)/rmin;
Qtemp=Qdrain;
Qdrain=Qsource;
Qsource=Qtemp;
end

I( drain, gate ) <+ ddt(Qdrain) + 10e-9*Cox*ddt(V(drain,gate)) ;
I( source, gate ) <+ ddt(Qsource) + 10e-9*Cox*ddt(V(source,gate)) ;
I( drain, source ) <+ 1e-21*ddt(V(drain,source));

end

endmodule
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