Electro-Static-Discharge (ESD) Protection in Touch and Display Driver Integrated (TDDI) Systems

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***Abstract*— This project evaluated the implications of system level electro-static discharge (ESD) on a touch and display driver integrated (TDDI) architecture component. Due to the components unique location in the system, typical component level ESD standards (JEDEC Human Body Model and Charged Device Model) were unable to adequately represent the ESD stresses seen by the integrated circuit (IC) during system level ESD testing (IEC 61000-4-2). An alternative stimulus, transmission line pulse (TLP), has been purposed as a better metric to model the devices performance under system level ESD testing and ESD devices were optimized to this stimulus.**

I. Introduction

ELECTROSTATIC discharge (ESD) has long been a concern in integrated circuit (IC) manufacturing. Although many types of ESD devices and protection schemes have become well understood, ever shrinking process nodes coupled with higher consumer expectations have kept ESD performance a constant concern in consumer electronics. The miniaturization of many types of consumer electronics, specifically cellular phones, has only made the problem more challenging. As the market drives the size of cellular phones down and the size and complexity of displays up, new architectures are being developed to optimize the performance of modern touch screens. A touch screen for a cellular phone traditionally consists of four major components, a liquid crystal display (LCD), a display driver IC (DDIC), a capacitive touch sensor, and a touch controller.

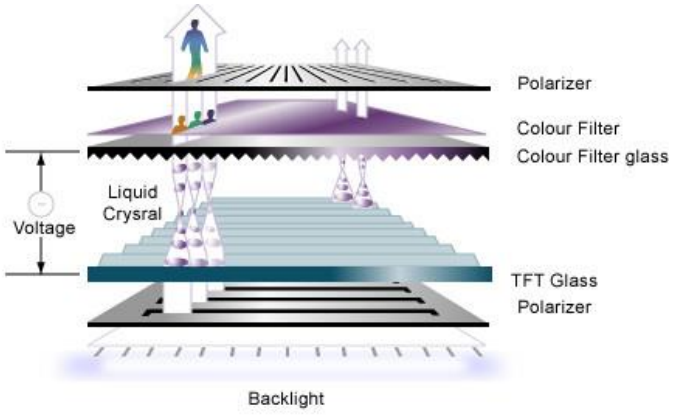

Fig. 1. Example of the layer stack present in a typical LCD panel. The thin-film transistor (TFT) glass portion of the LCD contains the devices responsible controlling the liquid crystal material. [1]

A. Display Drivers

A display driver is the component responsible for taking an image transmitted digitally from a host central processing unit (CPU) and converting that data into a series of analog voltages applied to the liquid crystal material. Display drivers are directly mounted the LCD substrate and control and array of thin-film transistors (TFTs) to apply the correct voltage to the correct sub-pixel at the correct time. The display driver receives the data through a flexible printed circuit (FPC) connect to the cell phones main board.

B. Capacitive Touch Controllers

A capacitive touch controller is responsible for other major aspect of a touch screens operation, the ability to sense an object adjacent to the display. Using a series of electrodes in the touch sensor, the touch controller monitors the electric field around the display so that if an object is placed in close proximity it detects the change and sends the location information to the host CPU. The touch controller traditionally exists on a separate FPC utilizing a second connection to the main board to communicate with the host.

C. TDDI Architecture

While a classic touch screen consists of the four components separately, cutting edge developments seek to reduce the complexity of the touch screen. Efforts have been made to incorporate the capacitive touch sensor into the LCD utilizing the same TFTs. Doing so removes the requirement for two separate FPCs and connectors on the main board. Further advances have merged the functions of the DDIC and the touch controller. This simplifies the system to be a display substrate, which contains electrodes for capacitive touch sensing, a single IC capable of both display and touch, connected through a single FPC to communicate with the host over a single interface.

II. ESD Testing

ESD has been a concern for electronics for a number of years. Although there is some aspects of ESD testing that are still subjective and vary across different industries, some

standards have been developed and widely utilized. Joint Electron Device Engineering Council (JEDEC) has developed ESD testing standards that specifically target electronics component manufactures and their products. Another separate but related body, the International Electrotechnical Commission (IEC) has developed standards that apply to consumer electronic products.

A. *Component Level Testing vs. System Level Testing*

JEDEC specifications are typically applied to electrical components. As such, they are designed to simulate ESD stress a component might see during shipping and manufacturing. Currently, JEDEC has two recommended stimulus models to test an electrical component against, the human body model (HBM) and charged device model (CDM). The HBM model is intended to simulate the handling of a device by an inadequately grounded person, while CDM is simulating a charged device coming into contact with a ground.

IEC specifications are applied to consumer electronics. As they are intended to simulate device handling by a consumer, the amount of ESD stress is usually much greater. There a few primary reasons for this. First, a consumer is assumed to have no ESD control procedures in place while handling the device, allowing them to build up more charge. Second, it is assumed that there is the possibility of ESD discharge through an ungrounded metal object, greatly reducing the resistance seen by the charge as it enters the device. This results in a much higher peak current seen by the device being tested.

B. *Differences between test methods*

The stark difference seen between component level ESD testing and system level ESD testing are primarily due to costs and requirements. The IEC specification is a good metric for consumer electronics, but it would not be cost effective to design individual components to meet such a requirement. Traditionally, a system manufacturer is required to ensure the individual components of the system do not see stresses above what is typically seen by component level testing. However, in the case of TDDI ICs a unique location in the system, the individual component will see higher current and faster rise time than what is covered in JEDEC specifications.

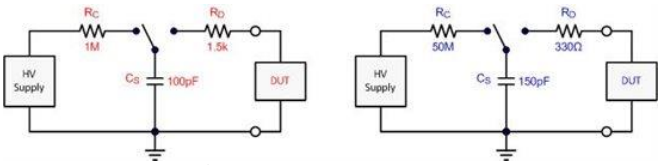

Fig. 2. Comparison of the ESD generator circuits used in JEDEC HBM testing (left) and IEC testing (right). DUT is an abbreviation for Device Under Test. [2]

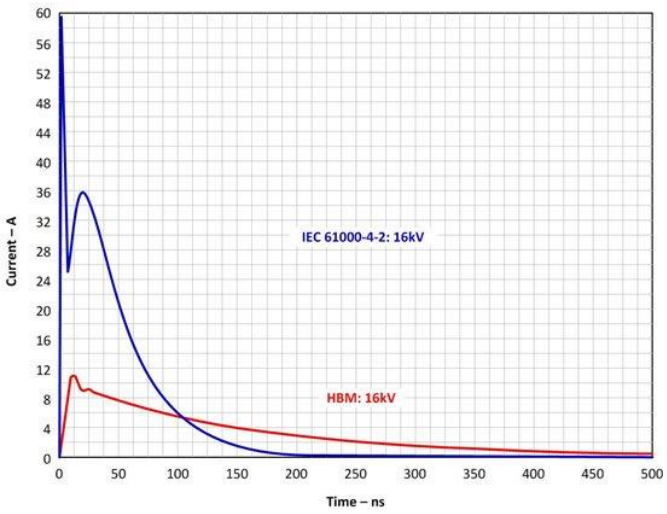

Fig. 3. Comparison of the output current profiles for IEC 61000-4-2:16kv and JEDEC HBM: 16kV through an identical load. [2]

III. ESD FOR TDDI APPLICATIONS

A TDDI IC in a cell phone will typically experience ESD stress beyond what is tested using the JEDEC specification. This is in part due to industrial design concerns that play a major factor in the cell phone market. The drive for larger displays and higher resolutions in a smaller package has led to the display occupying the majority of one face of a cell phone. One condition for IEC testing is particularly difficult for TDDI systems. The device is placed on top of insulating surface with a ground plane underneath. In this configuration, there is no resistive discharge path and the flow of charge through the system is heavily dependent on impedance.

Fig. X shows a schematic representation of IEC testing with the display of the phone facing up and away from the ground plane. In this configuration, the display is not a significant contributor to the discharge path.

Fig. X shows testing done in the alternate orientation with the display facing down, the display capacitance has become the dominate discharge path of ESD.

A. *Transmission Line Pulse Characterization*

In an effort to better model the stress seen by a TDDI IC during an ESD strike, alternative methods have been explored.

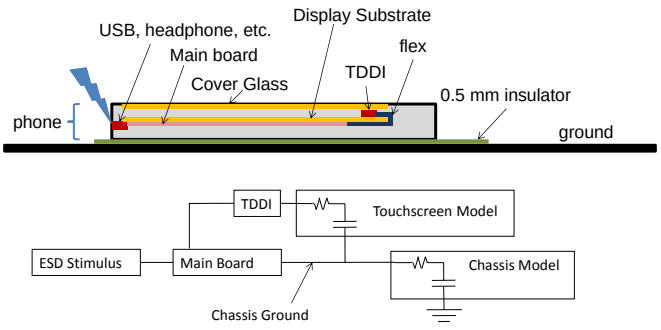

Fig. 4. One example of an IEC 61000-4-2 test. The cell phone is subjected to ESD discharge through an external metal component.

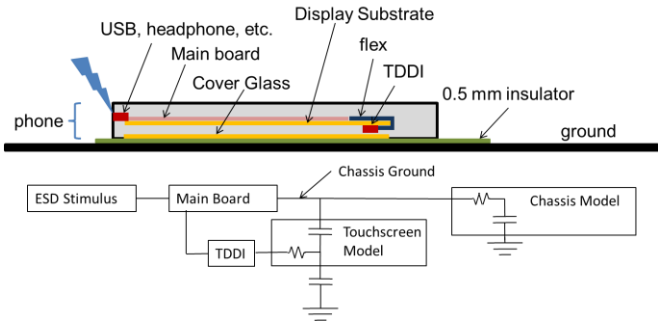

Fig. 5. Similar test to the one described in Fig. 4. In this case the phone touchscreen is face down on the insulator, causing the touchscreen to have a large capacitance to the ground plane.

Transmission Line Pulse (TLP) characterization is a method for characterizing ESD performance as opposed to a pass/fail testing standard like the JEDEC and IEC specifications. TLP characterization uses a long, floating transmission line pre-charged to a voltage and then connected to the device being tested. The initial discharge of the transmission line emulates a typical ESD event, while a method called time-domain reflectometry can be used to measure the impedance of the device as a function of time [3]. TLP characterization will be used primarily for two reasons, it simulates the rise time seen during an IEC event more accurately, and it provides more data on a tested device than a simple pass/fail.

B. *Display Construction*

In theory, the display itself will also play an important role in system level ESD testing. Since the display capacitance is the primary discharge path for the ESD event, its electrical model will determine the charge distribution across the outputs of the IC. The TFTs that make up the display subpixels are highly coupled and resistive, causing the energy of the ESD strike to find many parallel paths through the display. However, since this effect is dependent on the display construction it cannot be relied on and will result in relatively high current sink specification.

In an effort to alleviate system level concerns with respect to TDDI ICs, ESD improvements were made to target a level of performance well beyond the previous performance standard of meeting a 2kV HBM specification. That specification resulted in a peak current of approximately 1.33A. The new designs will target 10A of current handling for all power domains, and 4A for all display side pins due to the charge distribution we expect. In order to realize this, a comprehensive test chip with designed to evaluate individual ESD devices using TLP characterization. The test chip focuses on device sizes, ESD trigger methods, and charge distribution.

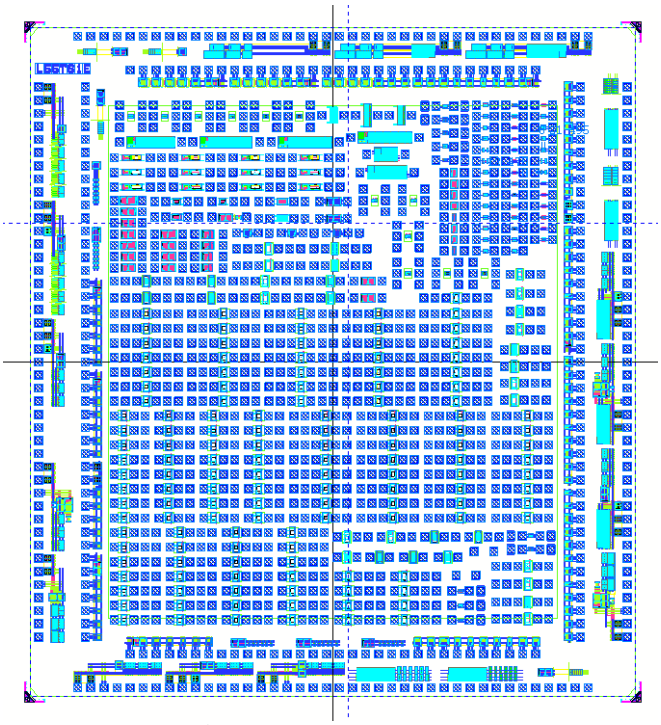

Fig. 6. The entirety of the ESD test chip. Although not all data obtained will be presented, there were over 240 devices on the chip. It also had multi-staged ESD protection schemes and a complete I/O ring to allow it to be packaged and tested.

IV. Device Characterization

Although the full chip ESD scheme consists of a variety of devices due to the specific requirements of each signal, two primary devices were well characterized and used repeatedly, diodes and gate coupled NMOS (GCNMOS). Diodes are placed an I/O pads to prevent the voltage from exceeding the supply voltage for the circuit, while GCNMOS are power supply clamps tasked with preventing the supply voltage from exceeding the maximum operating voltage.

A. *Diode Design*

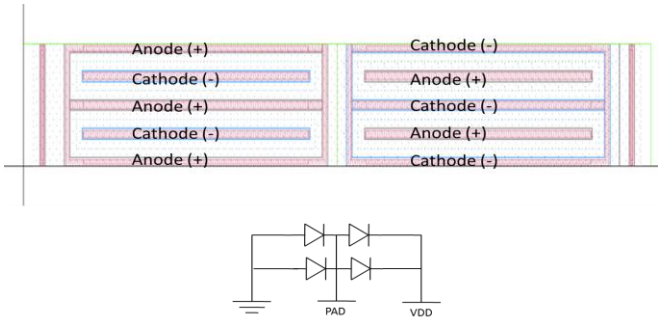

Fig. 7. [Top] Active layers of perimeter diode configuration. Although the 2 parallel diodes drawn could be merged into one larger diode, the lost perimeter of the diode had a negative impact on device performance. [Bottom] Schematic representation of the pictured.

Fig. 7 represents a basic schematic of diode protection for an I/O pad. An ESD diodes performance is not entirely determined by the diode area. Configurations maximizing the perimeter of a diode greatly improve the performance of diode under ESD stress. Also, counter-intuitively, disabling sections of the diode provide better ESD performance. This is due to current density concerns. If a small section of the diode is a preferential path for current, that section will sink more current and have a higher failure rate.

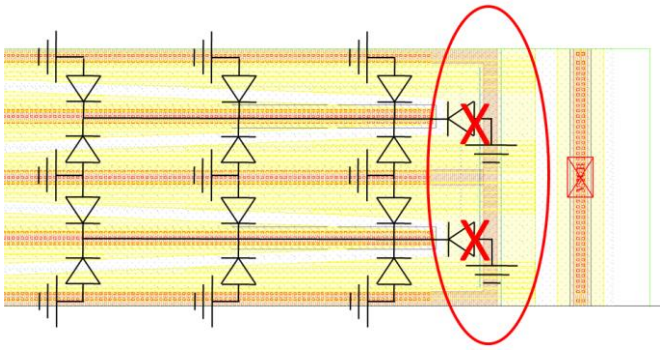

Fig. 8. Removing contacts on the short face of the diode disables the additional diode perimeter seen by the device ends. This is an effort to ensure uniform current distribution throughout the diode.

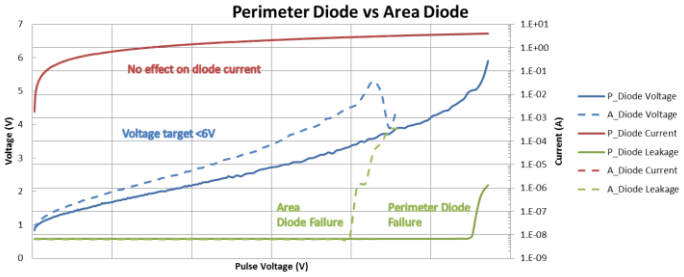

Fig. 9. TLP results comparing diodes drawn to maximize perimeter vs. diodes drawn to a basic area.

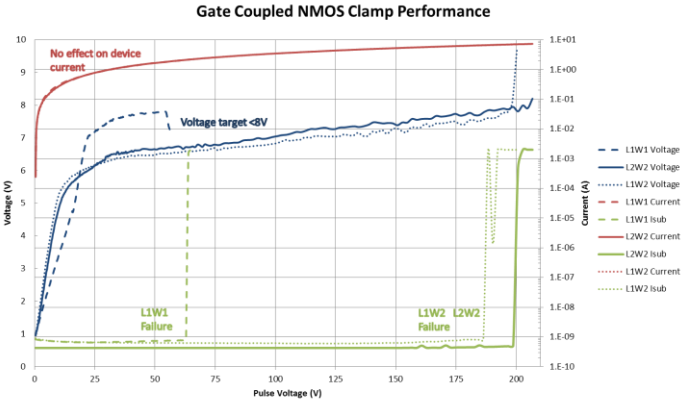

Fig. 10. TLP results for the 3 different configurations of GCNMOS tested. All 3 devices were of equal length and width.

B. Gate Coupled NMOS Design

A GCNMOS device is typically used a power supply clamp. The GCNMOS clamp design was more heavily dependent on traditional device parameters. Although improvements can be made in metallization to target consistent current density, a method called drain ballasting is commonly used to ensure equal current density. By either using a discreet N-well resistance in series with the drain of the NMOS device, or by removing silicide form a portion of the drain, you can create an N-type silicon resistor. This resistor has a positive temperature coefficient of resistance which will effectively balance current throughout the device. If any one portion of the device conducts higher current, it will in turn produce more heat, and increase the resistance of the N-type resistor.

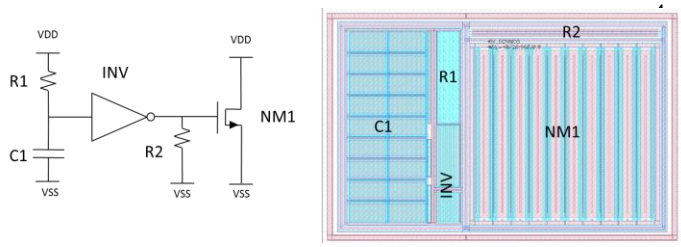

Fig. X. Comparison of the ESD generator circuits used in JEDEC HBM testing (left) and IEC testing (right). DUT is an abbreviation for Device Under Test.

V. Conclusions

Transmission line pulse characterization of ESD devices should improve our ability to predict the outcome of system level ESD testing. It better simulates the conditions seen by a TDDI IC during IEC testing, as well as provides additional data to measure device performance. The total impact of designing ESD with performance beyond typical JEDEC specifications has been extensive engineering effort as well as ~4x increase in die area for the purpose of ESD. In the future, there is hope to reduce the cost impact by developing more advanced ESD schemes utilizing silicon controller rectifiers.

References

Basic format for books:

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