4-1-2011

Scaling the bulk-driven MOSFET into deca-nanometer bulk CMOS technologies

Christopher Urban

SCALING THE BULK-DRIVEN MOSFET INTO DECA-NANOMETER BULK CMOS TECHNOLOGIES

by

Christopher S. Urban

A DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in
Microsystems Engineering
at the
Rochester Institute of Technology

April 2011

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Scaling the Bulk-Driven MOSFET into Deca-Nanometer Bulk CMOS Technologies

By

Christopher S. Urban

Submitted by *Christopher S. Urban* in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microsystems Engineering and accepted on behalf of the Rochester Institute of Technology by the dissertation committee.

We, the undersigned members of the Faculty of the Rochester Institute of Technology, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

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MICROSYSTEMS ENGINEERING PROGRAM
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April 2011

ABSTRACT

Kate Gleason College of Engineering
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Degree: Doctor of Philosophy **Program:** Microsystems Engineering

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Title: Scaling the Bulk-Driven MOSFET into Deca-Nanometer Bulk CMOS Technologies

The International Technology Roadmap for Semiconductors predicts that the nominal power supply voltage, V_{DD}, will fall to 0.7 V by the end of the bulk CMOS era. At that time, it is expected that the long-channel threshold voltage of a MOSFET, V_{T0}, will rise to 35.5% of V_{DD} in order to maintain acceptable off-state leakage characteristics in digital systems. Given the recent push for system-on-a-chip integration, this increasing trend in V_{T0}/V_{DD} poses a serious threat to the future of analog design because it causes traditional analog circuit topologies to experience progressively problematic signal swing limitations in each new process generation.

To combat the process-scaling-induced signal swing limitations of analog circuitry, researchers have proposed the use of bulk-driven MOSFETs. By using the bulk terminal as an input rather than the gate, the bulk-driven MOSFET makes it possible to extend the applicability of any analog cell to extremely low power supply voltages because V_{T0} does not appear in the device's input signal path. Since the viability of the bulk-driven technique was first investigated in a 2 μm *p*-well process, there have been numerous reports of low-voltage analog designs incorporating bulk-driven MOSFETs in the literature – most of which appear in technologies with feature sizes larger than 0.18 μm. However, as of yet, no effort has been undertaken to understand how sub-micron process scaling trends have influenced the performance of a bulk-driven MOSFET, let alone make the device more adaptable to the deca-nanometer technologies widely used in the analog realm today. Thus, to further the field's understanding of the bulk-driven MOSFET, this dissertation aims to examine the implications of scaling the device into a standard 90 nm bulk CMOS process. This dissertation also describes how the major disadvantages of a bulk-driven MOSFET – *i.e.*, its reduced intrinsic gain, its limited frequency response and its large layout area requirement – can be mitigated through modifications to the device's vertical doping profile and well structure. To gauge the potency of the proposed process changes, an optimized *n*-type bulk-driven MOSFET has been designed in a standard 90 nm bulk CMOS process via the 2-D device simulator, ATLAS.

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Dla Mamy, Taty i Dziadka.

Acknowledgements

Over the course of my doctoral studies, I faced a great number of challenges. Fortunately, I was lucky enough to have many caring people in my life who were there to help me overcome every issue that was tossed my way. So, it is only appropriate that I take the time to acknowledge everyone who played a vital role in helping me successfully complete this chapter of my life.

Above all, I would like to express my sincerest gratitude to my parents, Małgorzata and Zygmunt, as well as my grandfather, Florian, for their unwavering support throughout this entire ordeal. Even though I have stumbled many times over the years, you have always been there to prop me back up. I could not have reached this point in my life without you. Dziękuję. Kocham was.

Next, I would like to acknowledge one of the greatest mentors that I have ever had. Dr. Moon – I cannot even begin to express how grateful I am for everything that you have done for me. You spent countless hours with me tackling various technical and personal issues, and you have helped me to grow as an engineer and as an individual by leaps and bounds. You are a wonderful person, and I have truly been blessed to have you to learn from. From the bottom of my heart, thank you so very, very much for your help.

To Eric Bohannon – I don't know if I would have made it through this journey without you. We went into a lot of battles together and we certainly experienced many defeats. However, in the end, we finally found a way to persevere. You have taught me a great deal about how this crazy little world operates, and I am forever thankful for all of your help and for all of the insight that you have bestowed upon me. Even though I've never had a sibling, I can now safely say that I know what it feels like to have a brother.

To Chris Nassar – you are a true friend. You were there to support me through thick and thin during this entire Ph.D. experience and you provided me with many laughs and amusing stories along the way. You played an instrumental role in making the last few years of my life bearable, and for that I thank you.

To Dr. Hirschman and Dr. Rommel – thank you for all of your guidance over the last few years. I am very grateful for the insightful conversations that we had and for the great lengths that you both went to, to ensure that I had continued access to the Silvaco tools that I required.

To Dr. Smith, Dr. Abushagur and Dr. Mukund – thank you for allowing me to participate in the Ph.D. program and for giving me the resources that I needed to complete my doctoral studies.

To Charles Gruener and RIT's Research Computing Group – thank you for fixing the numerous issues that popped up over the years with the Cadence and Silvaco tools and for providing me with the multi-core processing capabilities which enabled me to significantly expand the scope of my simulation investigations.

To Sharon Stevens – thank you for helping me deal with the bureaucratic side of the Ph.D. program. I sincerely appreciate the time you spent making sure that I was *always* on track to obtain my doctoral degree.

And finally, to Dr. Amuso, Dr. Phillips, Ken Snyder, Jim Stefano, Patti Vicari, Florence Layton, Sean Patton, Lance Bradstreet, John McIntyre, Garrett Conte, Mark Pude and Christopher Bailey – thank you for all of the positive energy that you sent my way when I needed it most.

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List of Frequently-Used Variables and Acronyms

1-D	*One-Dimensional*
2-D	*Two-Dimensional*
3-D	*Three-Dimensional*
AC	*Alternating Current*
BD	*Bulk-Driven*
BTBT	*Band-to-Band Tunneling*
C_{bd}	*Bulk-to-Drain Capacitance*
C_{bg}	*Bulk-to-Gate Capacitance*
C_{bs}	*Bulk-to-Source Capacitance*
C_d	*Depletion Capacitance*
C_d'	*Depletion Capacitance per Unit Area*
C_{gd}	*Gate-to-Drain Capacitance*
C_{gs}	*Gate-to-Source Capacitance*
CMOS	*Complementary Metal-Oxide-Semiconductor*
C_{ox}	*Gate Oxide Capacitance*
C_{ox}'	*Gate Oxide Capacitance per Unit Area*
$C_{PW–DNW}$	*p-Well-to-Deep n-Well Capacitance*
DC	*Direct Current*
DD	*Delta-Doped*
DITS	*Drain-Induced Threshold Shift*
DTI	*Deep Trench Isolation*
$\lvert\xi_{x,max}\rvert$	*Magnitude of the Maximum Longitudinal Field*
FinFET	*Fin-Shaped Field Effect Transistor*
f	*Frequency (in Hz)*
$f_{T,BD}$	*Bulk-Driven Cut-Off Frequency*
$f_{T,GD}$	*Gate-Driven Cut-Off Frequency*
GD	*Gate-Driven*
g_m	*Gate Transconductance*
g_{mb}	*Bulk Transconductance*
IBM	*International Business Machines*
ICMR	*Input Common-Mode Range*
I_D	*Drain Current*
k	*Boltzmann Constant (1.38×10^{-23} J/K or 8.62×10^{-5} eV/K)*
L	*Channel Length*
L_g	*Gate Length*
$L_{g,min}$	*Minimum Allowable Gate Length of a Given Process*
MOS	*Metal-Oxide-Semiconductor*
MOSFET	*Metal-Oxide-Semiconductor Field Effect Transistor*
N_a	*Background Doping Concentration of a Uniformly-Doped Substrate (p type)*
$N_{a,eff}$	*Effective (Average) Background Doping Concentration (p type)*
N_{epi}	*Doping Concentration of the Lightly-Doped Channel Region (p type)*
NMOS	*n-Type Metal-Oxide-Semiconductor*
N_δ	*Doping Concentration of the Delta-Doped Region (p type)*
Op-amp	*Operational Amplifier*
PDK	*Process Design Kit*
PMOS	*p-Type Metal-Oxide-Semiconductor*
q	*Electronic Charge (1.602×10^{-19} C)*
QM	*Quantum Mechanical*

RAM	*Random-Access Memory*
RF	*Radio Frequency*
r_o	*Output Resistance*
S	*Sub-Threshold Swing*
SOC	*System-on-a-Chip*
SOI	*Silicon-On-Insulator*
STI	*Shallow Trench Isolation*
T	*Temperature (in Kelvin)*
t_{ox}	*Gate Oxide Thickness*
UD	*Uniformly-Doped*
V_{BS}	*Bulk-to-Source Voltage*
V_{DD}	*Power Supply Voltage*
V_{DS}	*Drain-to-Source Voltage*
V_{DSAT}	*Drain-to-Source Saturation Voltage*
V_{FB}	*Flat-Band Voltage*
V_{GB}	*Gate-to-Bulk Voltage*
V_{GS}	*Gate-to-Source Voltage*
V_T	*Threshold Voltage (for an n-type Device)*
V_{T0}	*Long-Channel Threshold Voltage (for an n-type Device)*
W	*Device Width*
y_d	*Depletion Depth*
y_{epi}	*Epitaxially-Grown Lightly-Doped Channel Layer Thickness*
γ	*Body Effect Coefficient*
ε_0	*Permittivity of Free Space (8.854×10^{-14} F/cm)*
ε_{ox}	*Dielectric Constant of SiO_2 (3.9) Multiplied by the Permittivity of Free Space*
ε_{si}	*Dielectric Constant of Si (11.7) Multiplied by the Permittivity of Free Space*
μ_n	*Low-Field Electron Mobility*
$\mu_{n,eff}$	*Effective (Average) Electron Mobility*
τ_e	*Energy Relaxation Time*
φ_F	*Fermi Potential*
ϕ_t	*Thermal Voltage (26 mV at 300 K)*

1 Introduction

1.1 Recent Trends in the Power Supply and Threshold Voltages

Historically, scaling a MOSFET's gate length, L_g, has greatly enhanced the performance of digital systems in terms of packing density and switching speed. Unfortunately, over time, such scaling has caused the average power, P_{avg}, consumed by these systems to rise considerably since the dynamic component of P_{avg}, denoted $P_{dynamic}$, is directly proportional to the frequency, f, at which a system operates.

To combat the growth in $P_{dynamic}$, the power supply voltage, V_{DD}, has generally been reduced in each new process generation due its quadratic relationship with $P_{dynamic}$ and P_{avg}, as shown below [1] (pp. 257–259):

$$P_{avg} = P_{static} + P_{dynamic} = V_{DD} I_{leakage} + C V_{DD}^2 f \tag{1.1}$$

where C and P_{static} represent the total capacitance of a system and the static power consumed by a system, respectively. To maintain a reasonable level of current drive between processes, the nominal long-channel threshold voltage used in a technology, V_{T0}[†], has typically been lowered along with V_{DD}. However, since a MOSFET's sub-threshold leakage current[‡], $I_{leakage}$, is exponentially dependent upon the threshold voltage, V_T [2]:

$$I_{leakage} = I_s e^{-V_T / \eta \phi_t} \tag{1.2}$$

V_{T0} has not been able to decline as quickly as V_{DD} does in each new process generation because of concerns over increasing P_{avg} through P_{static}.

[†] In this dissertation, V_{T0} is equal to the threshold voltage, V_T, of a MOSFET whose gate length is at least ten times greater than the minimum allowable gate length of a given process, $L_{g,min}$. Therefore, one should expect V_{T0} to be relatively constant for a given device (assuming that V_{BS} is also constant). V_T, on the other hand, may vary as a function of L_g as a result of short-channel effects, halo implantation, *etc.*

[‡] In (1.2), I_s represents the leakage current present in an NMOS device when $V_T = 0$; η is a parameter that depends on the ratio of the bulk-to-gate transconductances (g_{mb}/g_m) and ϕ_t is defined as the thermal voltage (26 mV at 300 K).

To see how disproportionately V_{T0} and V_{DD} have fallen in recent years, the two parameters are plotted in Figure 1.1 for five standard IBM bulk CMOS processes [3]–[7]. From the figure, one can see that unbalanced reductions in V_{T0} and V_{DD} have caused the ratio of V_{T0}/V_{DD} to increase noticeably – from V_{T0}/V_{DD} = 0.50 V/2.50 V = 0.20 to V_{T0}/V_{DD} = 0.29 V/1.00 V = 0.29 – between IBM's 0.25 µm and 65 nm nodes. As one would expect, this trend shall continue on until the end of bulk CMOS scaling, at which point, V_{DD} and V_{T0}/V_{DD} are predicted to reach 0.70 V and 0.355, respectively [8].

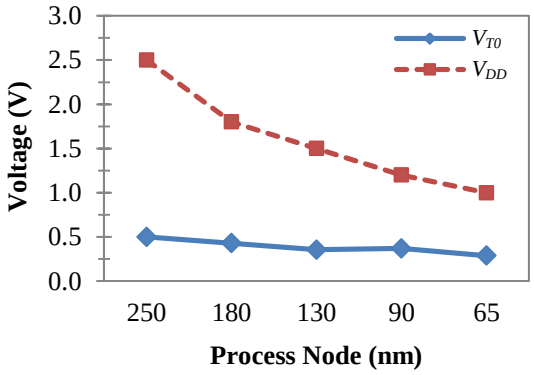


Figure 1.1: A plot of the recent trends seen in V_{T0} and V_{DD} for standard IBM bulk CMOS processes.

In addition to the process-scaling-induced behavior of V_{T0} and V_{DD} described above, there has recently been a growing interest in the wireless communication and biomedical areas to artificially lower the nominal power supply voltages of existing processes to values as low as 0.5 V in order to attain longer battery lives or to permit the use of energy scavenging techniques which harvest power from the environment [9]–[10]. As a consequence of these artificial reductions in V_{DD}, a new-found need has arisen for ultra-low-voltage circuits which can operate with V_{T0}/V_{DD} ratios as high as 0.7.

1.2 The Future of Analog Circuit Design

It is has long been the objective of the silicon industry to create purely digital integrated circuits which are capable of interfacing with the outside world since digital

systems are able to outperform their analog counterparts by a fairly significant margin while utilizing a much smaller amount of layout area. However, given that the outside world is mostly *analog* in nature, this goal has not – and may never – come to fruition. Therefore, for now, it is necessary for the silicon industry to deal with the fact that analog and digital components will have to co-exist on a single chip – this idea is called system-on-a-chip, or SOC – to create a cost-effective design.

In an SOC, analog designs are required to abide by the V_{DD} and V_{T0} targets seen in Figure 1.1[†] since in general, *all* process specifications are geared towards optimizing digital performance metrics. In deca-nanometer technologies, these V_{DD} and V_{T0} targets cause analog circuitry to experience harsh voltage swing limitations because each MOSFET utilized in an analog circuit must be saturated ($V_{GS} \geq V_T$) in order to provide a moderate gain and frequency response.

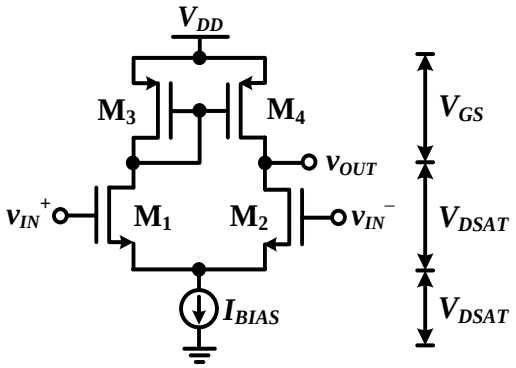


Figure 1.2: The schematic representation of a conventional single-ended differential amplifier.

As an illustration of the voltage swing problem, consider the input common-mode range, ICMR, of a conventional single-ended differential amplifier, such as the one shown in Figure 1.2. By analyzing the input of M_1, one can quickly show that the ICMR of this amplifier is limited to:

$$V_{GS1} + V_{DSAT,IBIAS} \leq \text{ICMR} \leq V_{DD} - |V_{GS3}| - V_{DSAT1} + V_{GS1} \tag{1.3}$$

[†] Low-power technologies will have slightly higher V_{DD} targets than those listed in Figure 1.1 [11]–[12].

Hence, if one were told to use an I_{BIAS} = 20 μA, a $|V_{GS1}| = |V_{GS3}| = V_T$ + 100 mV [13] and an $L_g = 5L_{g,min}$ [8], (1.3) predicts that the amplifier would have an ICMR of 1.65 V (66% of V_{DD}) in a 0.25 μm process if BSIM4 [14] was used to calculate each V_{DSAT}. With identical amplifier specifications, (1.3) predicts that the amplifier would have an ICMR of only 0.43 V (43% of V_{DD}) in a 65 nm process. This represents a 74% decrease in the ICMR over a span of five process generations.

Based on the forecasted projections for V_{DD} and V_{T0} [8] and the growing desire for ultra-low-voltage circuits with large V_{T0}/V_{DD} ratios [9]–[10], it is expected that the ICMR of a conventional single-ended differential amplifier will to fall to a point where it becomes extremely difficult to use the amplifier in the near future [15] (pp. 25–27), [16] (pp. 6–12). This revelation is quite startling because it is not isolated to the case considered above and actually carries over to every other traditional analog circuit topology [15] (pp. 22–37), [16] (pp. 6–12); it also compounds the problems already associated with the scaling of MOSFETs into the deca-nanometer regime – troubles which include: device intrinsic gain limitations brought about by degradation in the output resistance [17], r_o; reduced gate oxide capacitance due to polysilicon gate depletion and quantum mechanical effects [18]; as well as non-negligible gate current due to direct electron (or hole) tunneling through the gate oxide [19].

Naturally, many researchers have investigated the voltage swing issue quite extensively at the device and circuit level. This has led to a wide variety of techniques which can be used to enable analog circuit design at very low power supply voltages. The most notable of these techniques include: floating-gate [20], level-shifted [21], weak inversion [22] (pp. 12–14) and bulk-driven (BD) MOSFETs [23]. The use of thick (gate) oxide devices has also been suggested [24].

Out of all the possibilities mentioned above, the BD MOSFET – first introduced by Guziński, Białko and Matheau in 1987 [23] – has turned out to be one of the most popular low-voltage analog design techniques found in the literature. In a BD MOSFET, the bulk terminal is used as an input rather than the gate. This transforms a MOSFET into a depletion mode-like device because the threshold voltage no longer appears in the device's input signal path.

As one would expect, the BD MOSFET's depletion mode-like behavior does come with a few drawbacks, the most notable of which is a low intrinsic gain due to the device's dependence on g_{mb} rather than g_m [23]. The BD MOSFET is also subject to a small cut-off frequency and a large layout area allotment because it must reside within its own separate well structure in a number of applications. The possibility of inducing latch-up by forward biasing the bulk–source junction has also been a cause for concern [25].

Despite all of the problems listed above, an investigation by Blalock in 1996 [26] revealed that it was possible to design useful bulk-driven differential amplifiers and current mirrors with power supply voltages as low as 1 V in a 2 μm *p*-well process (V_{T0} = 0.7 V); the fear of inducing latch-up was proved to be ill-founded.

Since Blalock's study, numerous reports of bulk-driven differential amplifier and current mirror designs have appeared in the literature[†] (see Section 2.5 of this dissertation for an extensive list of references). Researchers have also published papers extending the BD MOSFET's applicability to other critical analog and RF circuits, such as voltage controlled oscillators (VCOs) [28]–[30], phase-locked loops (PLLs) [9], voltage references [31]–[32], comparators [33]–[34], voltage followers [35]–[37] and mixers [27].

[†] Bulk-driven circuits are rarely implemented in technologies with feature sizes smaller than 0.18 μm. The lone exception to this rule seems to be bulk-driven mixers, which have been fabricated in processes with feature sizes down to 45 nm (for an example, please see [27]).

1.3 The Purpose of this Research

All working knowledge of the BD MOSFET is based on Blalock's work [26] which was performed in a 2 μm *p*-well process in 1996. Since Blalock's thorough investigation of the BD MOSFET, there has been no effort undertaken to understand the short-channel behavior of the device, let alone make the device more adaptable to deca-nanometer processes even though circuits are regularly being published using the BD MOSFET.

As a means of furthering the field's understanding of the BD MOSFET, this dissertation aims to examine the implications of scaling an *n*-type BD MOSFET into a standard 90 nm bulk CMOS technology ($L_{g,min}$ = 80 nm). The ideas contained within this document are intended to make the BD MOSFET more suitable for low-voltage analog applications operating at a V_{DD} = 0.7 V, the minimum power supply voltage predicted for the end of bulk CMOS scaling [8].

Ultimately, this dissertation describes how the major disadvantages of a BD MOSFET – *i.e.*, its reduced intrinsic gain, its limited frequency response and its large layout area allotment – can be mitigated through modifications to the device's vertical doping profile and well structure. To gauge the potency of the proposed process changes, an improved *n*-type BD MOSFET has been designed in the 2-D device simulator, ATLAS [38], and the device's characteristics have been evaluated against a triple-well isolated uniformly-doped BD MOSFET.

A standard 90 nm bulk CMOS process was selected for this work because the march toward non-standard (SOI, FinFET, *etc.*) processes is expected to be gradual for the analog realm [39]. There are two supporting arguments for this line of reasoning. First, it is harder for analog designs to adapt to technologies with smaller feature sizes since

analog circuits are more sensitive to the non-ideal effects present in such technologies as well as the process changes instituted to alleviate these non-ideal effects. Second, it is increasingly cost-prohibitive to move into a newer technology due to the increase in process complexity with each new process generation. This is evidenced by recent market data which shows that the migration to smaller feature sizes is relatively restrained [40]. For these reasons, one can infer that deca-nanometer bulk CMOS processes will be relevant in the silicon marketplace for a long time to come.

1.4 Organization of this Document

The first three sections of this chapter have outlined the path of this research by declaring that the BD MOSFET is one of the most prominent low-voltage analog design techniques found in the literature. To elaborate on this claim, a brief literature review is conducted in Chapter 2 to analyze benefits and limitations of each low-voltage analog design technique introduced in Chapter 1 and to indicate why the BD MOSFET has been chosen as the focal point of this work.

To provide the proper background for this dissertation's study of the BD MOSFET, the long- and short-channel characteristics of the device are examined in Chapter 3 through various mathematical developments and circuit-level simulations[†]. By doing so, it is possible to see how sub-micron process scaling trends have affected the expected advantages of the BD MOSFET.

To mitigate the noted limitations of the BD MOSFET, several process changes are proposed in Chapter 4. With the aid of the 2-D device simulator, ATLAS [38], the effectiveness of the most promising process changes are also evaluated in the chapter.

[†] The rest of this document will focus on *n*-type BD MOSFETs, unless noted otherwise.

Based on the findings of Chapter 4, the design of an improved *n*-type BD MOSFET is presented in Chapter 5 using a standard 90 nm bulk CMOS technology. The benefits of the new design are also examined in the chapter via 2-D device simulations in ATLAS. Following the conclusion of Chapter 5, closing remarks and suggestions for future research are provided in Chapter 6.

2 Low-Voltage Analog Design Techniques

2.1 Floating-Gate MOSFETs

In the literature, one will find many different techniques which have been proposed to enable low-voltage analog design. One notable low-voltage analog design technique involves the use of floating-gate MOSFETs [20]. In a floating-gate MOSFET, there two control gates, G_1 and G_2, which are coupled to a floating gate through two capacitances, C_1 and C_2, as shown in Figure 2.1 for an *n*-type device. When a sufficiently large DC bias voltage is applied to the first control gate, charge flowing from G_1 to the floating gate (via Fowler-Nordheim tunneling) causes the effective threshold voltage of the second control gate to decrease to [20]:

$$V_{T,G2} = V_{T,FG} + \frac{C_2}{C_1}\left(V_{T,FG} - V_{G1}\right) \tag{2.1}$$

where $V_{T,FG}$ is the nominal threshold voltage of the device.

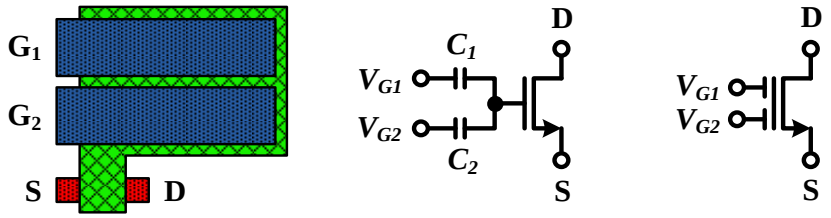
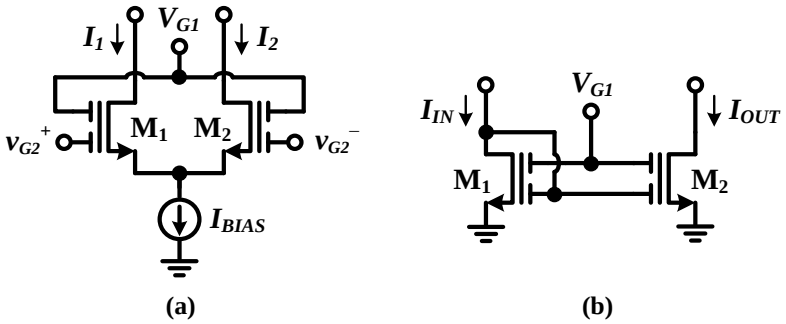


Figure 2.1: An illustration of the (a) layout, (b) device model and (c) symbol of an *n*-type floating-gate MOSFET. S, D, G_1 and G_2 denote the source, drain, first control gate and second control gate terminals, respectively.

Typically, researchers have utilized floating-gate MOSFETs to form many primitive low-voltage analog circuits, such as the differential amplifier and current mirror cells depicted in Figure 2.2(a) and (b), respectively [20]. These circuits turn out to be functionally equivalent to their traditional counterparts since G_2 is generally used as an input terminal while G_1 is used to lower the threshold voltage of G_2, as suggested by (2.1).



(a) (b)

Figure 2.2: The schematic representation of a floating-gate (a) differential amplifier and (b) simple current mirror.

While the floating-gate MOSFET approach is capable of creating differential amplifiers with rail-to-rail ICMRs and current mirrors with small input voltages at V_{DD}s as low as 1 V [41], there are many factors which inhibit the approach from being adopted as a general solution to low-voltage analog design. Of those factors, the most prominent one is that it may become difficult to store charge within the device's floating gate in deca-nanometer technologies due to the presence of direct-tunneling-induced current flowing from the device's floating gate into the channel [42]. The floating-gate MOSFET is also plagued by a low transconductance resulting from the voltage divider formed by C_2 and the floating-gate oxide capacitance[†] at the device's input [43] (pp. 12–14), [44] (pp. 9–10). The amount of layout area consumed by the floating-gate MOSFET is also a concern since C_2 is required to be at least ten times larger than the floating-gate oxide capacitance in order for the device to operate properly [20].

2.2 DC Voltage Level Shifting

2.2.1 Current Mirrors

Figure 2.3(a) shows how DC level shifting can be applied to remove the threshold voltage obstruction from the input of a simple current mirror. In this technique, a bias voltage, V_{BIAS}, is placed between the gate and drain of the current mirror's input device

[†] The capacitance cited here denotes the capacitance seen between the floating gate and the channel – *i.e.*, C_{ox}.

(M_1) such that the mirror's input voltage is lowered to $V_{IN} = V_{GS1} - V_{BIAS}$. The bias voltage can be implemented in many ways, though it is usually realized through the use of a PMOS source follower, as shown in Figure 2.3(b) [44].

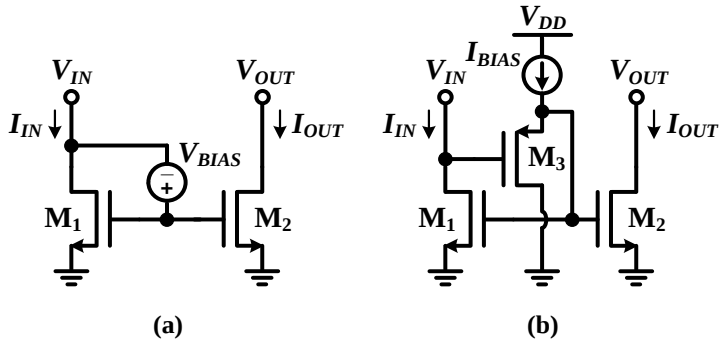


Figure 2.3: The schematic representation of an (a) ideal DC level-shifted simple current mirror (b) and its practical implementation using a PMOS source follower.

While the DC level shifting technique does provide a fairly simple way to reduce the input voltage of a simple current mirror, its simplicity comes at a cost because the approach increases the amount of power consumed by the current mirror (due to the extra bias current, I_{BIAS}). The level shifting technique also sets a lower limit to the permissible current values under which the mirror functions reliably because V_{GS2} is no longer pinned at zero when $V_{IN} = 0$ [21]. Thus, if V_{OUT} is somehow increased while V_{IN} is held at zero, one will see sub-threshold current flowing through M_2 even though no current is flowing through M_1 (ideally) [45]. Furthermore, given that direct-tunneling-induced gate current is no longer negligible in deca-nanometer technologies [42], any gate current generated by M_3 (Figure 2.3(b)) will undoubtedly foster an additional source of inaccuracy between the input and output currents of the mirror [46].

2.2.2 Amplifier Input Stages

Traditionally, the ICMR of an operational amplifier (op-amp) has been expanded through the use of a complementary differential pair input stage [47] (pp. 325–326). In

this configuration, one connects an NMOS and PMOS differential pair in parallel such that when the NMOS pair is conducting, the PMOS pair is not, and vice versa.

Unfortunately, as V_{DD} scales, it becomes extremely difficult to implement the complementary differential pair input stage because of a voltage "dead zone" that forms in the middle of the power supply where neither pair conducts [48]. To eradicate this "dead zone," one can apply the DC level shifting approach from Section 2.2.1 to alter the common-mode level of the stage's input voltages, as seen in Figure 2.4. In this embodiment, a current, I_S, is applied through two equal valued resistors (labeled R_S) in such a way that v_{IN}^+ and v_{IN}^- are shifted upwards (NMOS pair) or downwards (PMOS pair) when they are within the voltage "dead zone" [49]. A level-shifting current generator is then used to dynamically vary I_S in response to v_{IN}^+ and v_{IN}^- to ensure that one of the differential pairs is always conducting.

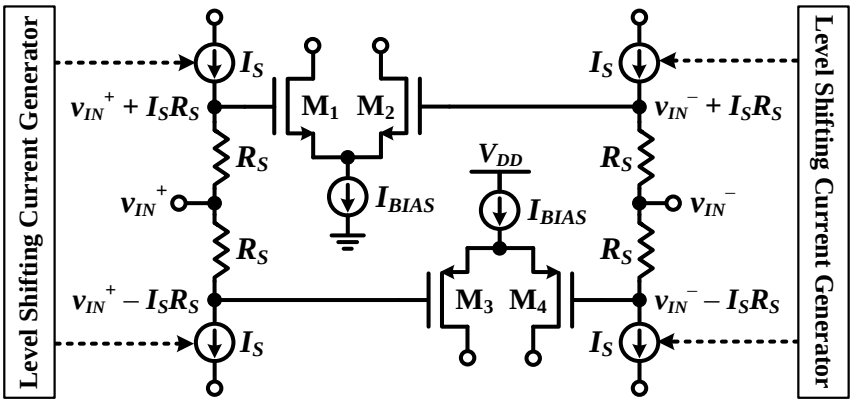


Figure 2.4: An illustration of the dynamic DC level shifting concept applied to a complementary differential pair input stage.

By using the DC level shifting technique on an input stage, it is possible to design op-amps with rail-to-rail ICMRs at power supply voltages as low as 1 V [49]. However, one must again consume more power to achieve this benefit. One will also need to increase the overall complexity of the input stage due to the additional control circuitry that is required to vary I_S.

2.3 Weak Inversion MOSFETs

Weak inversion MOSFETs have always captured the interest of researchers because their transconductance efficiencies, defined as g_m/I_D, are the highest among any region of operation, as shown in Figure 2.5. This behavior is attributed to the fact that the electron flow in weak inversion MOSFETs is dominated by diffusion rather than drift, making the devices' drain currents and transconductances exponentially dependent on V_{GS} [22] (pp. 12–14), [50] (pp. 170–175):

$$I_D = I_s e^{(V_{GS}-V_T)/\eta\phi_t}\left(1-e^{-V_{DS}/\phi_t}\right) \tag{2.2}$$

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{\eta\phi_t} \tag{2.3}$$

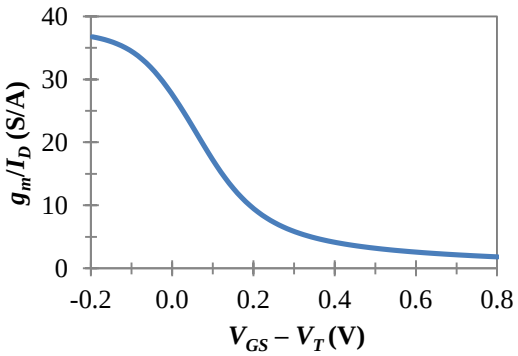


Figure 2.5: A plot of g_m/I_D vs. $V_{GS} - V_T$ for an NMOS device that was simulated using the process design kit for IBM's standard 0.13 µm bulk CMOS technology (W/L_g = 6 µm/0.6 µm, V_{DS} = 1 V and V_{BS} = 0).

As one would expect, weak inversion MOSFETs are naturally attractive for low-voltage analog applications due to their low V_{GS} and V_{DSAT} requirements[†]. This is evidenced by reports of weak inversion op-amps operating with power supply voltages as low as 0.6 V [51]. However, one must remember that the main application of weak inversion MOSFETs has historically been in the biomedical area where operating frequencies range between 1 Hz to 1 kHz [52]. It is not possible to use these devices at much higher frequencies because their drain currents and transconductances are

[†] $V_{DSAT} \approx 4\phi_t$ (104 mV) in the weak inversion region [16] (pp. 6–7).

inherently small in magnitude which limits the charging/discharging rate of capacitances' (*i.e.*, the slew rate) and causes the aspect ratios of the devices to be relatively large.

2.4 Thick Oxide MOSFETs

In recent years, the analog portions of SOCs have been designed with thick (gate) oxide MOSFETs which are normally intended for I/O (input/output) circuits [24]. The motivation for using thick oxide MOSFETs is two-fold: to take advantage of their ability to operate with a higher power supply voltage and to circumvent the direct-tunneling-induced gate leakage problem plaguing thin oxide devices [42].

Unfortunately, when thick oxide devices are used in an SOC, they heighten the risk of an ESD (electrostatic discharge) event occurring within the digital section of the chip since thin oxide devices are still in use there [47] (pp. 659–660). Including a larger and separate power supply voltage also complicates the level shifting interfaces between an SOC's analog and digital components [24].

2.5 Bulk-Driven MOSFETs

Figure 2.6(a) presents the schematic representation of an *n*-type BD MOSFET [23], [26]. In this device, the input voltage is applied to the bulk terminal and a fixed potential[†], V_{BIAS}, is tied to the gate to ensure that an inversion layer is formed within the channel. By reconfiguring a MOSFET in this way[‡], it is possible to obtain a depletion mode-like device – as witnessed in Figure 2.6(b) – because the input voltage ($v_{IN} = v_{BS}$) does not have to overcome a threshold voltage barrier in order for the device to be saturated.

[†] In most cases, V_{BIAS} is set to V_{DD} for an NMOS device and ground (or the negative power supply rail, $-V_{SS}$) for a PMOS device. This eliminates the need for external bias circuitry.

[‡] In the literature, some scholars compare the operation of a BD MOSFET to that of a JFET. This analogy is not quite correct because a BD MOSFET relies upon the transport of minority carriers in the channel, while in a JFET, the current is comprised of *majority* carriers.

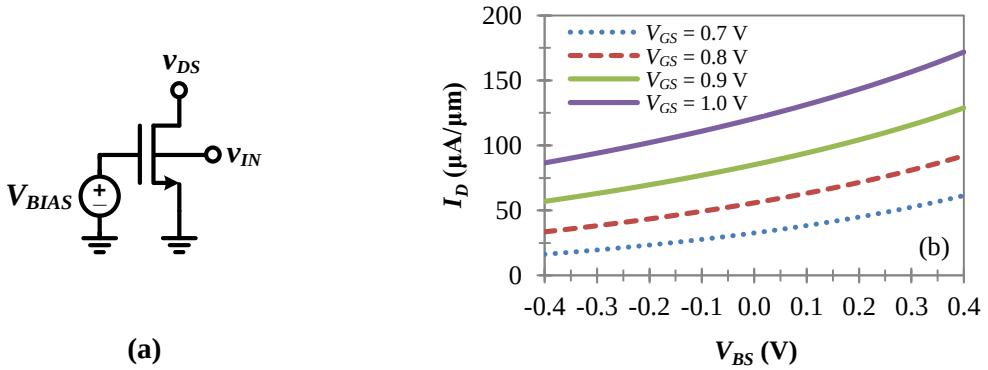


Figure 2.6: (a) The schematic representation of an *n*-type BD MOSFET and (b) a representative plot of an *n*-type BD MOSFET's I_D–V_{BS} characteristics which were generated using an analytical long-channel equation for I_D and the device specifications of a standard 90 nm bulk CMOS technology for four different V_{GS} values (L_g = 400 nm).

In the literature, the BD MOSFET is most commonly found in differential amplifier input stages [10], [15], [23], [26] (pp. 59–68), [44], [53]–[91]. Such amplifiers – referred to as bulk-driven differential amplifiers – function in the same way as their gate-driven (GD) counterparts (due to their structural similarities), except that their voltage gains and frequency responses are now dependent upon g_{mb} and the input capacitance of the bulk terminal.

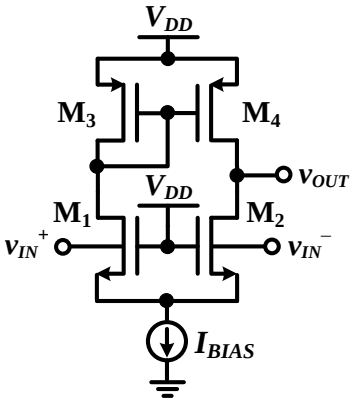


Figure 2.7: The schematic representation of a single-ended bulk-driven differential amplifier.

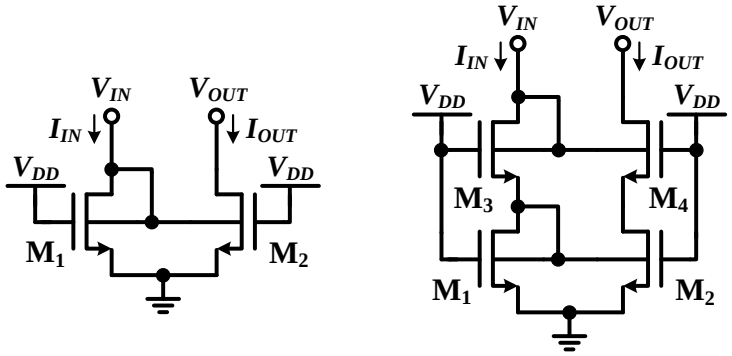
In general, the main advantage of any bulk-driven differential amplifier topology is its ability to provide a rail-to-rail ICMR at power supply voltages where it is difficult for gate-driven differential amplifiers to operate. The rail-to-rail characteristics of a bulk-

driven differential amplifier – like the single-ended example illustrated in Figure 2.7 – can be observed by writing out its ICMR [26][†]:

$$V_{BS1} + V_{DSAT,IBIAS} \leq \mathrm{ICMR_{BD}} \leq V_{DD} - |V_{GS3}| - V_{DSAT1} + V_{BS1} \tag{2.4}$$

and by then noting that V_{BS1} can be positive[‡] or negative.

Another frequently seen application of the BD MOSFET has been in current mirror cells, such as the simple current mirror implementation depicted in Figure 2.8(a) [15] (pp. 88–89), [26] (pp. 36–51), [92]–[102]. As one might expect, a bulk-driven current mirror will also operate in the same way as a gate-driven current mirror (again, due to their structural similarities), except that its input voltage will now depend on V_{BS} rather than V_{GS}.



(a) **(b)**

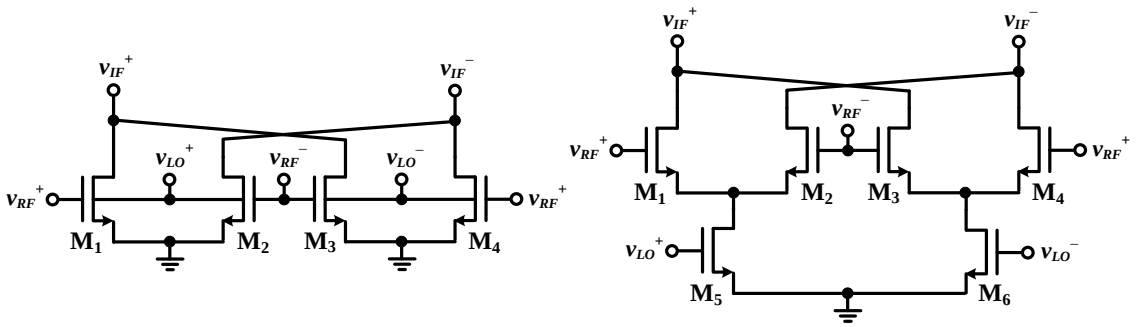
Figure 2.8: The schematic representation of a (a) simple and (b) cascode bulk-driven current mirror.

By choosing to design a simple current mirror with a BD MOSFET instead of a GD MOSFET, one is able to reduce the minimum input voltage of the current mirror topology from $V_T + V_{DSAT}$ to V_{DSAT}. However, it is important to note that in the bulk-driven case, one will generally have to use an advanced current mirror architecture – such as the cascode example shown in Figure 2.8(b) – to accurately mirror and/or scale the

[†] This analysis assumes that $V_{T0}/V_{DD} = 0.7$ and that $V_{DSAT} \approx 0.3$ V.
[‡] To avoid turning on the bulk–source junction diode, V_{BS} must be less than 0.6 V [25].

input current since the simple bulk-driven current mirror suffers from a non-linear input–output current characteristic [26] (pp. 36–51). Therefore, in the instances where a simple gate-driven current mirror is being replaced, one will see a slightly smaller drop in the minimum input voltage when switching to the bulk-driven approach.

An emerging application of the BD MOSFET is in the RF area where it can be employed within a mixer, such as the one illustrated in Figure 2.9(a) [27], [103]–[114]. In a bulk-driven mixer, all four terminals of a MOSFET are utilized simultaneously and each device in the mixer (M_1–M_4) is biased such that its gate-to-source voltage is less than V_T[†]. A local oscillator (LO) signal, v_{LO}, is then sent to each bulk terminal where it modulates V_T and establishes whether the RF input, v_{RF}, will pass through the gate and into the drain. By using both the bulk and gate terminals as AC inputs, the bulk-driven mixer eliminates the need for the differential pair beneath M_1–M_4 in the traditional architecture – see Figure 2.9(b) – [115] (pp. 419–420) which increases the available voltage swing by at least V_{DSAT}.



(a) **(b)**

Figure 2.9: An illustration of exemplary (a) bulk-driven and (b) gate-driven mixer topologies. Note that v_{IF} denotes the intermediate frequency (IF) output.

In addition to the applications discussed so far, the BD MOSFET has also been implemented in many other low-voltage analog and RF circuits, including VCOs

[†] Note that the gate of an *n*-type BD MOSFET is *not* tied to V_{DD} in this configuration.

[28]–[30], PLLs [9], voltage references [31]–[32], comparators [33]–[34] and voltage followers [35]–[37]. Fixed DC potentials have also been applied to the bulk terminals of GD MOSFETs in order to lower their threshold voltages, and thus permit the use of a smaller power supply voltage [116]–[120].

Given the wide assortment of publications on bulk-driven circuitry, it is evident that the BD MOSFET is capable of extending the applicability of many fundamental analog (and RF) building blocks to very low power supply voltages. However, as with all the other low-voltage analog design techniques considered in this chapter, the BD MOSFET is also hindered by a couple of disadvantages. First, the transconductance of the device (g_{mb}) is typically 60–80% less than the transconductance of a GD MOSFET (g_m) based on long-channel theory [26] (pp. 32). This limits both the intrinsic gain as well as the cut-off frequency of the device. Second, since input signal isolation is normally required (except in some instances within bulk-driven current mirrors and mixers), it is necessary for each BD MOSFET to reside within its own separate well. As a result, a BD MOSFET generally consumes more layout area than a GD MOSFET and further suffers from a degraded frequency response due to the added input capacitance from its well structure.

Besides the issues listed above, the BD MOSFET is also plagued by one commonly overlooked aspect – the characteristics of the device were last examined in 2 μm *p*-well process [26]. As a result, it is unknown how sub-micron process scaling trends have influenced the performance of a BD MOSFET and the benefits of its associated circuit topologies. This is a particularly significant concern because only a handful of the publications referenced in this section (predominantly regarding bulk-driven mixers) have been designed in technologies with feature sizes smaller than 0.18 μm.

2.6 Conclusions

This chapter has provided a comprehensive review of the most prominent circuit-level and device-level low-voltage analog design techniques proposed in the literature. Most of these techniques attempt to lower the threshold voltage of a MOSFET to counteract the growth in V_{T0}/V_{DD} that is brought about by sub-micron process scaling trends. For circuit-level approaches, this often leads to added circuit complexity and power consumption, as well as limited applicability. It is for these reasons that circuit-level approaches are not seen as a general solution to low-voltage analog design.

Device-level approaches, on the other hand, tend to suffer from reduced transconductances and substantial increases in layout area due to their inherent device structures and/or operating conditions. Of the device-level approaches reviewed in this chapter, weak inversion, floating-gate and thick oxide MOSFETs are not seen as general solutions to low-voltage analog design. Weak inversion MOSFETs do not qualify because they cannot generate the frequency responses necessary for most analog applications while floating-gate MOSFETs should not be used since they may become unreliable in the presence of significant direct-tunneling-induced gate current. Thick oxide MOSFETs remain undesirable because they complicate the level shifting interfaces between the analog and digital components of an SOC.

Even though the BD MOSFET also suffers from the common problems plaguing device-level approaches, it is the only technique that should not be completely restricted by fundamental material limits or its inherent device structure in a standard deca-nanometer bulk CMOS process. Thus, it will be important to study how the BD MOSFET performs in a deca-nanometer technology since this topic has been virtually ignored in the literature. Once the characteristics of a BD MOSFET are well understood

in the deca-nanometer regime, it will be possible to address the shortcomings of the device – *i.e.*, its low intrinsic gain, its large layout area requirements and its limited frequency response – more appropriately.

3 The Current State of Bulk-Driven MOSFETs

3.1 Device Background

3.1.1 Bulk Transconductance

The operation of a BD MOSFET relies upon the exploitation of the body effect to manifest a change in I_D through V_{BS}, as shown below for an *n*-type long-channel device:

$$I_D = \frac{1}{2}\frac{W}{L}\mu_n C'_{ox}(V_{GS} - V_{T0})^2 = \frac{1}{2}\frac{W}{L}\mu_n C'_{ox}\left[V_{GS} - \left(V_{FB} + 2\varphi_F + \gamma\sqrt{2\varphi_F - V_{BS}}\right)\right]^2 \tag{3.1}$$

where V_{FB} is the flat-band voltage, μ_n is the low-field electron mobility and C'_{ox} is the gate oxide capacitance per unit area; W and L denote the channel width and channel length, respectively. To obtain g_{mb}, the measure of the bulk's control over the channel, one must take the partial derivative of I_D with respect to V_{BS} resulting in:

$$g_{mb} \equiv \frac{\partial I_D}{\partial V_{BS}} = \frac{\gamma g_m}{2\sqrt{2\varphi_F - V_{BS}}} = \frac{g_m}{C'_{ox}}\frac{\varepsilon_{si}}{y_d} = g_m\frac{C'_d}{C'_{ox}} \tag{3.2}$$

where the body effect coefficient, γ, and the Fermi potential, φ_F, are defined as:

$$\gamma \equiv \frac{\sqrt{2q\varepsilon_{si}N_a}}{C'_{ox}} \tag{3.3}$$

$$q\varphi_F \equiv E_i - E_F \tag{3.4}$$

and where q is the electronic charge, N_a is the background doping level of a uniformly-doped *p*-type substrate, E_F is the Fermi level, E_i is the intrinsic Fermi level and ε_{si} is the dielectric constant of Si multiplied by the permittivity of free space, ε_0; C'_d and y_d denote the depletion capacitance per unit area and depletion depth beneath the channel.

3.1.2 Intrinsic Gain

The intrinsic gain of a BD MOSFET can be determined by calculating the voltage gain seen between the bulk and drain terminals of a MOSFET when the source is

grounded – see Figure 3.1. The result of such a calculation – given in (3.5) – indicates that a BD MOSFET's intrinsic gain is similar to that of a GD MOSFET, with the only difference being that its gain is dependent on g_{mb} rather than g_m. Since g_{mb} is 60%–80% less than g_m based on long-channel theory [26] (pp. 32), one can expect a BD MOSFET's intrinsic gain to be lower than that of a GD MOSFET by a comparable margin.

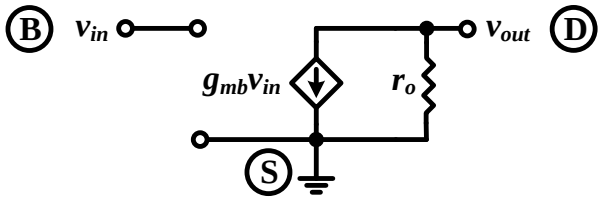


Figure 3.1: The ideal small-signal model of an *n*-type BD MOSFET in the common-source configuration. B, D and S denote the bulk, drain and source terminals, respectively.

$$\frac{v_{out}}{v_{in}} = -g_{mb}r_o \tag{3.5}$$

3.1.3 Layout Area

In deca-nanometer bulk CMOS technologies, GD MOSFETs are isolated from one another via shallow trench isolation (STI). As a result, when utilizing the bulk-driven technique, it is necessary for a BD MOSFET – such as the *n*-type example shown in Figure 3.2 – to reside within a triple-well structure to ensure that its input signal, v_{BS}, is not electrically connected to the input of another BD MOSFET via the common *p*-type substrate (unless this condition is desired).

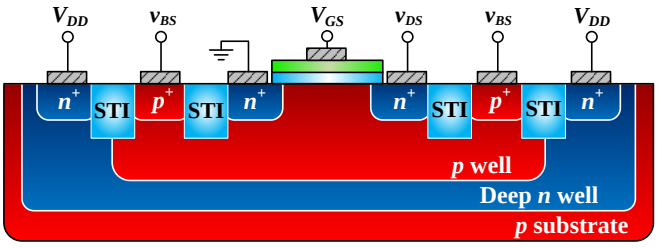


Figure 3.2: The device cross-section of a triple-well-isolated *n*-type BD MOSFET.

Therefore, if one uses the design rules of a 65 nm bulk CMOS process, one will find that an *n*-type BD MOSFET must consume at least $(W + 2.45) \times (L_g + 2.45)$ μm^2 of

layout area if the well-to-well spacing requirements between adjacent BD MOSFETs are included in the calculation[†] [7]. As a comparison, one will find that an *n*-type GD MOSFET must minimally consume just $(W + 0.29) \times (L_g + 0.29)$ μm^2 of layout area.

3.1.4 Cut-Off Frequency

Given that a BD MOSFET's input is at the bulk terminal, it is clear that the device's cut-off frequency, $f_{T,BD}$, will be heavily influenced by the parasitic elements of the device's well structure, bulk–source junction and bulk–drain junction. Thus, to determine $f_{T,BD}$, it is necessary to create an AC model that accounts for these parasitic components. Such an AC model can be found by first considering the NMOS device model presented in Figure 3.3(a) where R_G, R_D, R_S, R_{PW}[‡], R_{DNW} and R_{PSUB} denote the series resistance of gate, drain, source, *p* well, deep *n* well and *p*-type substrate, respectively; D_{bse}, D_{bde}, $D_{PW–DNW}$ and $D_{DNW–PSUB}$ represent the *pn* diodes formed by the bulk–source, bulk–drain, *p*-well–deep *n*-well and deep *n*-well–*p*-substrate junctions, respectively [121].

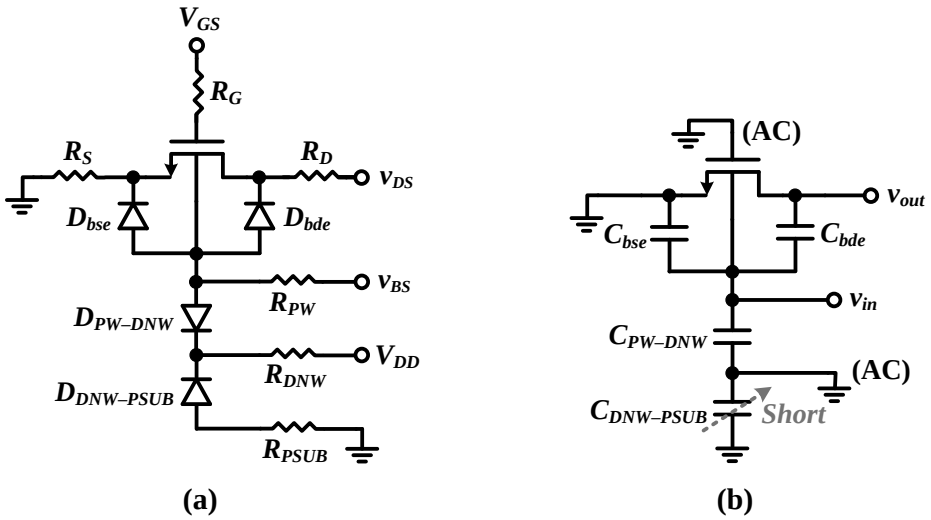


Figure 3.3: (a) The device model and (b) the ideal AC model of a triple-well isolated *n*-type BD MOSFET.

[†] A *p*-type BD MOSFET must consume at least $(W + 1.51) \times (L_g + 1.51)$ μm^2 of layout area in the same process. This is less than an *n*-type device because a *p*-type BD MOSFET does not require a triple-well structure to provide input signal isolation.

[‡] R_{PW} is largely dependent upon the doping level of a *p* well. This resistance can be lowered by surrounding a *p* well with a ring of p^+ contacts to increase the cross-sectional area of the bulk terminal's signal path.

By replacing each *pn* diode in Figure 3.3(a) with its equivalent depletion capacitance and ignoring the series resistance at each terminal for the sake of simplicity, the desired AC model can be constructed for the *n*-type BD MOSFET, as shown in Figure 3.3(b). Interestingly, Figure 3.3(b) indicates that $C_{DNW–PSUB}$ has no effect on an *n*-type BD MOSFET's frequency response since it is effectively shorted out under normal operating conditions[†].

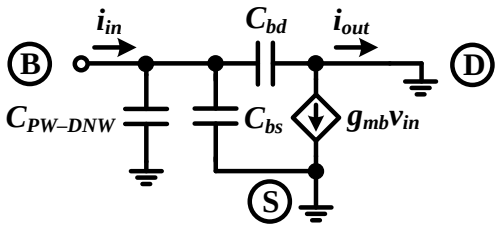


Figure 3.4: The small-signal model of a BD MOSFET (neglecting the bulk-to-gate capacitance, C_{bg}) used to calculate $f_{T,BD}$. B, D and S represent the bulk, drain and source terminals, respectively. i_{in} and i_{out} define the input and output currents of the device.

Since $C_{DNW–PSUB}$ does not alter an *n*-type BD MOSFET's frequency response, one can modify the device's AC model to create the frequency-dependent small-signal model shown in Figure 3.4 for the case when the BD MOSFET's output is short-circuited. From Figure 3.4, it is possible to finally obtain $f_{T,BD}$ by setting the magnitude of i_{out}/i_{in} equal to one and solving for the cut-off frequency, as described in [44] (pp. 37–44) and [122] (pp. 262–263). This approach yields:

$$|i_{out}| \approx g_{mb} v_{in} \tag{3.6}$$

$$|i_{in}| = 2\pi f (C_{PW–DNW} + C_{bs} + C_{bd}) v_{in} \tag{3.7}$$

resulting in a cut-off frequency of:

$$f_{T,BD} = \frac{g_{mb}}{2\pi(C_{PW–DNW} + C_{bs} + C_{bd})} \tag{3.8}$$

[†] In a *p*-type BD MOSFET, the depletion capacitance of the *n*-well–*p*-substrate junction is analogous to $C_{PW–DNW}$ because only one *n* well is required to isolate the device. Hence, there is no $C_{DNW–PSUB}$-like component in the AC model of a *p*-type BD MOSFET.

where C_{bs} and C_{bd} represent the parallel combinations of the intrinsic (C_{bsi} and C_{bdi}) and extrinsic (C_{bse} and C_{bde}) depletion capacitances seen between the body and source and body and drain terminals, respectively. The cut-off frequency of a GD MOSFET, $f_{T,GD}$, can be found in a similar fashion. The result of such an analysis is given below:

$$f_{T,GD} = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{3.9}$$

where C_{gs} and C_{gd} represent the parallel combinations of the intrinsic (C_{gsi} and C_{gdi}) and extrinsic (C_{gse} and C_{gde}) overlap capacitances seen between the gate and source and gate and drain terminals, respectively.

With equations for $f_{T,BD}$ and $f_{T,GD}$ now developed, it is beneficial to calculate $f_{T,BD}/f_{T,GD}$ to see how the cut-off frequency of a BD MOSFET compares to that of a GD MOSFET in a deca-nanometer bulk CMOS process. To provide a basis for this computation, simulation results from a device with W/L_g = 2.5 μm/0.1 μm, I_D = 10 μA, V_{BS} = 0 and $V_{GS} - V_T$ = 70 mV can be used [123] (pp. 297–300). Overall, the simulations show that this device has a C_{gsi} = 4.17 fF and a C_{gdi} = 1.56 fF. Using conservative estimates from [50] (pp. 390–402), one can approximate that $C_{bsi} = 0.425C_{gsi}$ = 1.772 fF and that $C_{bdi} = 0.2C_{gdi}$ = 312 aF. C_{gse} and C_{gde} do not need to be included in the calculation of $f_{T,BD}/f_{T,GD}$ because the largest contribution to C_{gs} and C_{gd} typically comes from C_{gsi} and C_{gdi}, respectively. However, the same cannot be said for C_{bs} and C_{bd} because C_{bse} and C_{bde} are usually on par with or greater than C_{bsi} and C_{bdi} [44] (pp. 42–43). Therefore, using data from a 65 nm process [7] and equations from [50] (pp. 408–409), one can estimate that C_{bse} and C_{bde} are each equal to 2.3 fF. To round out the calculation of $f_{T,BD}/f_{T,GD}$, the value of $C_{PW–DNW}$ can be determined to be 2.62 fF using the formulation

in [26] (pp. 33–34) and the measured data from [121]. Thus, with all the relevant capacitances computed, one can finally express $f_{T,BD}/f_{T,GD}$ as:

$$\frac{f_{T,BD}}{f_{T,GD}} = 0.61\frac{g_{mb}}{g_m} \tag{3.10}$$

Unfortunately, it is likely that (3.10) is an overestimate of $f_{T,BD}/f_{T,GD}$ because the diffusion capacitances of the bulk–source and bulk–drain junctions have been neglected. These diffusion capacitances, denoted C_{bsd} and C_{bdd}, are operative when the bulk–source and bulk–drain junctions become forward-biased since they depend upon the minority carrier current densities flowing through the junctions. With the inclusion of C_{bsd} and C_{bdd}, the total parasitic contribution to the bulk-to-source and bulk-to-drain capacitances becomes $C_{bs} = C_{bsi} + C_{bse} + C_{bsd}$ and $C_{bd} = C_{bdi} + C_{bde} + C_{bdd}$ where[†] [122] (pp. 100–102):

$$C_{bsd} = \frac{q^2 L_n n_{po}}{2kT} e^{qV_{BS}/kT} = \frac{q^2 L_n}{2kTD_n} J_{bs} \tag{3.11}$$

and where k is the Boltzmann constant and T is the temperature (in Kelvin); L_n, D_n and n_{po} represent the electron diffusion length, diffusion constant and equilibrium carrier concentration for a p-type material while J_{bs} corresponds to the minority carrier current density (with units of A/cm^2) flowing through the bulk–source junction.

3.1.5 Input-Referred Noise

To find the minimum input signal level that a BD MOSFET may process with acceptable quality, one must calculate its input-referred noise – *i.e.*, the total equivalent noise seen at the device's input. To do so, it is necessary to consider a MOSFET's dominant sources of noise, which are flicker and thermal noise; the former is attributed to

[†] The equation for C_{bdd} is similar to (3.11) except that the minority carrier current density, now defined J_{bd}, will depend on V_{BD} not V_{BS}.

the trapping and releasing of inversion layer carriers from dangling bonds at the Si–SiO_2 interface [47] (pp. 215–216) while the latter occurs due to the random motion of carriers in the resistive regions of the device's gate, channel and *p* well [47] (pp. 209–215).

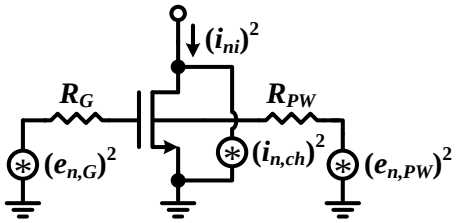


Figure 3.5: An *n*-type MOSFET model including the device's major sources of noise.

The noise contributed by a MOSFET's *p*-well resistance – see Figure 3.5 – is generally represented by a voltage source (with units of V^2) in series with the bulk terminal [26] (pp. 73–78):

$$e_{n,PW}^2 = 4kTR_{PW}\Delta f \tag{3.12}$$

while the noise added by the device's channel resistance is usually modeled by a current source (with units of A^2) in parallel with the channel [26] (pp. 73–78):

$$i_{n,ch}^2 = 4kT\alpha(g_m + g_{mb})\Delta f \tag{3.13}$$

where Δf is the noise bandwidth and α is a fitting parameter which is equal to $^2/_3$ for long-channel devices and $^8/_3$–$^{10}/_3$ for short-channel devices [124]. At the gate terminal, the noise contributed by a MOSFET's series gate resistance [26] (pp. 73–78) can be combined with the device's flicker noise component [47] (pp. 215–216) to form a single voltage source (with units of V^2) in series with the gate:

$$e_{n,G}^2 = \frac{K_F}{C_{ox}'^2 WLf^c}\Delta f + 4kTR_G\Delta f \tag{3.14}$$

where K_F is a process parameter that varies between 5×10^{-31} and 1×10^{-30} C^2/cm^2 and c is a fitting parameter that ranges from 0.7 to 1.2 [50] (pp. 422–424).

Using (3.12)–(3.14), it is possible to group the noise sources from above into a single drain current, i_{ni}^2 (with units of A^2), under the assumption that each noise source is uncorrelated:

$$i_{ni}^2 = i_{ni,ch}^2 + g_m^2 e_{n,G}^2 + g_{mb}^2 e_{n,PW}^2 = \left[\frac{KF}{C_{ox}'^2 WLf^c} g_m^2 + 4kT\left(g_m^2 R_G + g_{mb}^2 R_{PW}\right) + 4kT\alpha(g_m + g_{mb}) \right] \Delta f \quad (3.15)$$

This current can then be transformed into a single voltage source (with units of V^2) in series with the bulk terminal to yield the input-referred noise of a BD MOSFET:

$$e_{ni,BD}^2 = \frac{i_{ni}^2}{g_{mb}^2} = \left\{ \frac{KF}{C_{ox}'^2 WLf^c} \left(\frac{g_m}{g_{mb}} \right)^2 + 4kT \left[R_G \left(\frac{g_m}{g_{mb}} \right)^2 + R_{PW} + \frac{\alpha}{g_{mb}} \left(1 + \frac{g_m}{g_{mb}} \right) \right] \right\} \Delta f \quad (3.16)$$

i_{ni}^2 can also be translated back to the gate terminal to obtain the input-referred noise of a GD MOSFET:

$$e_{ni,GD}^2 = \frac{i_{ni}^2}{g_m^2} = \left\{ \frac{KF}{C_{ox}'^2 WLf^c} + 4kT \left[R_G + R_{PW} \left(\frac{g_{mb}}{g_m} \right)^2 + \frac{\alpha}{g_m} \left(1 + \frac{g_{mb}}{g_m} \right) \right] \right\} \Delta f \quad (3.17)$$

By reviewing (3.16) and (3.17), it is apparent that the input-referred noise of a BD MOSFET is similar in form to that of a GD MOSFET, with the only difference being that the input-referred noise is referenced to g_{mb} in the bulk-driven case rather than g_m. As a result, the input-referred noise of a MOSFET will generally be greater when the bulk is used as an input since g_{mb} is inherently smaller than g_m.

3.1.6 The Well Proximity Effect

During the formation of a triple-well structure, a portion of the incoming *n*-type ions – intended for implantation within a deep *n*-well region – tend to scatter off the edges of protective photoresist (PR) layers and into the exposed *p*-type silicon surface, as illustrated in Figure 3.6. By doing so, these deflected *n*-type ions cause the *effective* surface concentration to continually decrease below the desired doping level as one

approaches the edges of a triple-well structure, giving rise to what is known as the well proximity effect [125]–[126].

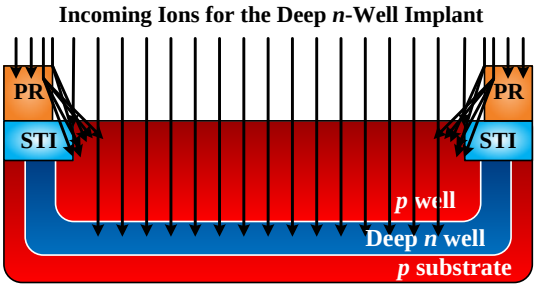


Figure 3.6: The manifestation of the well proximity effect during the formation of a triple well.

As one would expect, the well proximity effect has significant ramifications for triple-well isolated *n*-type BD MOSFETs because it causes V_{T0} to vary as a function of distance over a range of 1 μm near the edges of a triple well. Thus, to maintain acceptable matching properties with neighboring devices, it becomes necessary to increase the layout area of every triple-well isolated *n*-type BD MOSFET by at least 2 μm in each spatial dimension.

3.2 Short-Channel Behavior

In Section 3.1.1, (3.2) was presented to describe the long-channel behavior of g_{mb} in a uniformly-doped device. This equation is commonly cited in publications referencing the bulk-driven technique. Unfortunately, (3.2) fails to account for two crucial phenomena – source/drain charge sharing [127] (pp. 448–450) and the onset of velocity saturation [127] (pp. 455–456) – making it unsuitable for short-channel devices.

To include charge sharing and velocity saturation in a mathematical representation of g_{mb}, it is necessary to begin by re-deriving an equation for the drain current. Thus, using the definitions given in Figure 3.7, one must start with [127] (pp. 431):

$$I_D = W(-Q_I'(x))\upsilon(x) = WC_{ox}'(V_{GS} - V_T - V(x))\upsilon(x) \tag{3.18}$$

where $V(x)$ is the potential, $Q_I'(x)$ is the inversion layer charge density (per unit area) and $\upsilon(x)$ is the carrier velocity along the length of the channel.

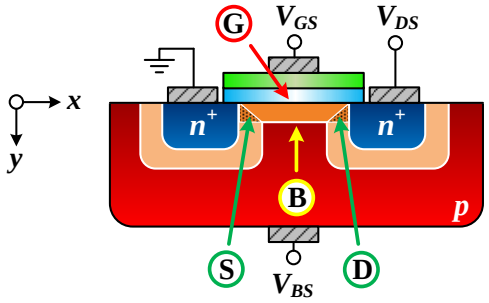


Figure 3.7: The terminal voltage and dimensional definitions used in the short-channel g_{mb} analysis. G, S, D and B denote the depletion charge controlled by the gate, source, drain and bulk, respectively.

Velocity saturation can be incorporated into (3.18) by using the piece-wise carrier velocity model presented in [50] (pp. 280–283). In this model, when the electric field, $\xi(x)$, is less than the critical electric field at which the onset of velocity saturation occurs (ξ_{sat}), one can write the carrier velocity as:

$$\upsilon(x) = \frac{\mu_{n,eff}(-\xi(x))}{\left(1+\frac{-\xi(x)}{\xi_{sat}}\right)} = \frac{\mu_{n,eff}\frac{dV(x)}{dx}}{\left(1+\frac{1}{\xi_{sat}}\frac{dV(x)}{dx}\right)} \tag{3.19}$$

where $\mu_{n,eff}$ denotes the effective electron mobility[†].

Using (3.19), (3.18) can be rearranged to yield:

$$\int_0^L I_D dx = \int_0^{V_{DS}} \left[W\mu_{n,eff} C_{ox}'(V_{GS} - V_T - V(x)) - \frac{I_D}{\xi_{sat}} \right] dV(x) \tag{3.20}$$

By performing the required integration over L and V_{DS}, one can then solve for I_D resulting in (3.21).

[†] There are many scattering mechanisms which contribute to the effective electron mobility. Typically, the mobility resulting from each scattering mechanism is calculated individually and then grouped together with the low-field mobility to form $\mu_{n,eff}$ using the Matthiessen rule. For an example of this process, please see [128].

$$I_D = \frac{\frac{W}{L}\mu_{n,eff}C'_{ox}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}}{\left(1 + \frac{V_{DS}}{\xi_{sat}L}\right)} \tag{3.21}$$

When $\xi(x)$ exceeds ξ_{sat}, the model in [50] (pp. 280–283) predicts that the carrier velocity will saturate at a value of υ_{sat}. As a result, it becomes possible to determine the saturation drain current, I_{DSAT}, by substituting $V(x) = V_{DSAT}$ and $\upsilon(x) = \upsilon_{sat}$ into (3.18):

$$I_{DSAT} = W\upsilon_{sat}C'_{ox}(V_{GS} - V_T - V_{DSAT}) \tag{3.22}$$

By equating (3.21) and (3.22), one gets:

$$V_{DSAT} = \frac{(V_{GS} - V_T)\xi_{sat}L}{(V_{GS} - V_T) + \xi_{sat}L} \tag{3.23}$$

which can then be inserted back into (3.22) to obtain a more useful form of I_{DSAT}:

$$I_{DSAT} = W\upsilon_{sat}C'_{ox}(V_{GS} - V_T)\left[1 - \frac{\xi_{sat}L}{(V_{GS} - V_T) + \xi_{sat}L}\right] \tag{3.24}$$

At this point, it is appropriate to incorporate source/drain charge sharing into the development through the use of a quasi-two-dimensional model for the threshold voltage which captures the roll off observed in V_T as L decreases in a uniformly-doped MOSFET [129]:

$$V_T = V_{T0} - \Delta V_{T0} \tag{3.25}$$

$$\Delta V_{T0} = \frac{2(\phi_c - V_{BS}) + (\phi_c - V_{BS} + V_{DS})\left(1 - e^{-L/l}\right) + 2\sqrt{(\phi_c - V_{BS})^2 + (\phi_c - V_{BS})(\phi_c - V_{BS} + V_{DS})\left(e^{L/l} - 1\right)}}{4\sinh^2\left(\frac{L}{2l}\right)} \tag{3.26}$$

In this model, l is a characteristic length that depends on the depletion depth beneath the channel and ϕ_c is a variable equal to $\varphi_{bi} - 2\varphi_F$ where φ_{bi} is the built-in potential of the bulk–source and bulk–drain junctions; V_{BS} is included in the model by replacing φ_{bi} with $\varphi_{bi} - V_{BS}$.

By using (3.25) and (3.26) in conjunction with (3.24), one can finally find the desired short-channel equation for g_{mb}:

$$g_{mb} = \frac{\partial I_{DSAT}}{\partial V_{BS}} = \frac{\partial I_{DSAT}}{\partial V_T}\frac{\partial V_T}{\partial V_{BS}} = -\frac{\partial I_{DSAT}}{\partial V_{GS}}\frac{\partial V_T}{\partial V_{BS}} = -g_m\frac{\partial V_T}{\partial V_{BS}} = g_m\left(\frac{\gamma}{2\sqrt{2\varphi_F - V_{BS}}} + \frac{\partial \Delta V_{T0}}{\partial V_{BS}}\right) \quad (3.27)$$

where:

$$g_m = W\upsilon_{sat}C'_{ox}\left\{1 - \frac{\xi_{sat}L}{(V_{GS}-V_T)+\xi_{sat}L} + \frac{(V_{GS}-V_T)\xi_{sat}L}{[(V_{GS}-V_T)+\xi_{sat}L]^2}\right\} \quad (3.28)$$

and:

$$\frac{\partial \Delta V_{T0}}{\partial V_{BS}} = \frac{-1}{4\sinh^2\left(\frac{L}{2l}\right)}\left\{\left(3-e^{L/l}\right) + \frac{2\left[(\phi_c - V_{BS}) + \left(e^{L/l}-1\right)(2\phi_c - 2V_{BS} + V_{DS})\right]}{\sqrt{(\phi_c - V_{BS})^2 + (\phi_c - V_{BS})(\phi_c - V_{BS} + V_{DS})\left(e^{L/l}-1\right)}}\right\} \quad (3.29)$$

To confirm the validity of the derived short-channel equation, (3.27) is plotted against L in Figure 3.8(a) along with results from a 2-D ATLAS [38] simulation for an n-type BD MOSFET with a gate oxide thickness, t_{ox} = 1.4 nm, $N_a = 2 \times 10^{18}$ cm^{-3}, $V_{GS} = V_{DS}$ = 1 V and V_{BS} = 0; similar data is displayed in Figure 3.8(b) for a $V_{GS} = V_{DS}$ = 0.5 V. From the figures, it is clear that there is good correlation between (3.27) and ATLAS for L > 200 nm. Below that boundary, (3.27) begins to under-predict the simulated results because (3.25) and (3.26) are only valid for L > 100 nm [129].

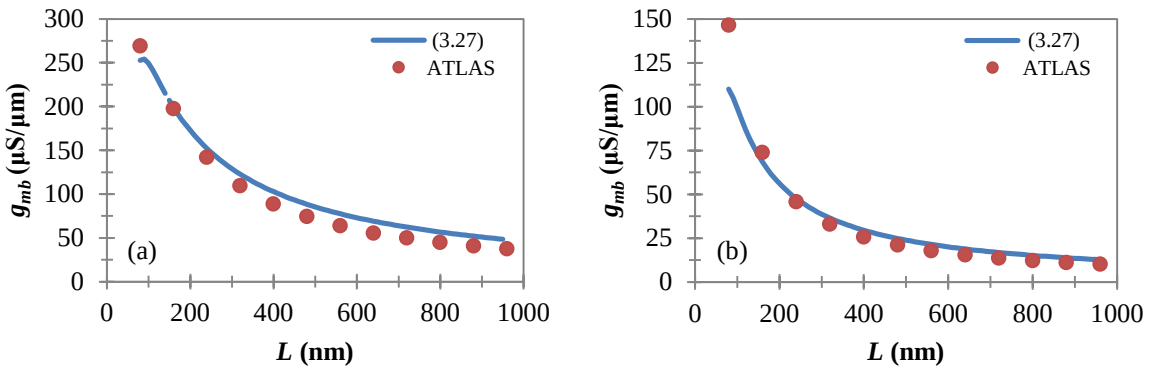


Figure 3.8: A comparison between the derived short-channel equation for g_{mb} and the results of a 2-D ATLAS simulation for a V_{BS} = 0, (a) $V_{GS} = V_{DS}$ = 1 V and (b) $V_{GS} = V_{DS}$ = 0.5 V.

3.3 Process Scaling Trends

As mentioned in Section 2.5, little is known about the BD MOSFET in processes with features sizes smaller than 0.18 μm. Since one of the major goals of this dissertation is to design a BD MOSFET with an improved intrinsic gain and frequency response, one important question to ask would be: what happens to g_{mb} as devices scale into the deca-nanometer regime? While (3.27) adequately describes the short-channel behavior of g_{mb} in a uniformly-doped device, it becomes difficult to derive a tractable equation for g_{mb} in a deca-nanometer process due to the non-ideal mechanisms – *e.g.*, quantum mechanical [130]–[132], [133] (pp. 43–48) and STI stress effects [134]–[137] – and non-uniform doping profiles – resulting from retrograde and halo implant steps [138] (pp. 439–446) – present in the technology.

Therefore, moving forward, it is appropriate to use a circuit simulation tool fitted with experimentally-calibrated process design kits (PDKs) to analyze the behavior of g_{mb} below the 0.18 μm node. By using a circuit simulator that employs such PDKs at this stage of the investigation, one may obtain meaningful results that reflect physical process scaling trends.

3.3.1 Remarks on the Deficiencies of BSIM

In the industry, BSIM [14] is the most commonly used compact model for circuit simulation. While the MOS [139], PSP [140] and EKV [141] Models are becoming more prominent, they are not yet widely used. Therefore, when using a circuit simulator, one should expect to encounter a version of BSIM3 [142] when dealing with a fairly mature process (*e.g.*, a 0.18 μm process) and a version of BSIM4 [14] when working with a more recent technology.

As with any compact model, it is important to investigate any known deficiencies in BSIM to prevent the collection of erroneous data. In the case of a BD MOSFET, there are two key issues which must be considered since the bulk terminal is not normally used as a device input.

To start with, it is well known that g_{mb}/g_m is a monotonically increasing function of V_{BS} up until the point where significant current begins to flow through the bulk–source junction (V_{BS} = 0.6 V [25]). However, as seen in Figure 3.9, this behavior is not always captured by BSIM because of a non-physical discontinuity that exists at V_{BS} = 0 in older versions of the model [15] (pp. 74). Since this issue was eventually corrected in BSIM4.3.0 [143] (Ch. 10, pp. 4), it would be wise to avoid using older versions of BSIM in any bulk-driven circuit simulation where V_{BS} will be greater than zero.

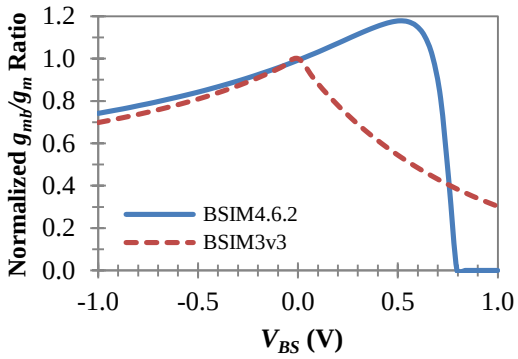


Figure 3.9: A plot of the normalized g_{mb}/g_m ratio (referenced to g_{mb}/g_m at V_{BS} = 0) vs. V_{BS} as predicted by BSIM3v3 and BSIM4.6.2 for an NMOS device.

In addition to the issue mentioned above, it is important to note that as of yet, BSIM does not provide a way to include the depletion capacitance of a BD MOSFET's well structure in a device cell without the use of a model wrapper. As seen in (3.8), this depletion capacitance plays a vital role in determining the frequency response of the device. Hence, to perform an accurate AC simulation on a bulk-driven circuit, one will first need to extract well capacitance data for every BD MOSFET in the circuit from an estimated layout of each device.

3.3.2 Simulation Setup and Results

To see how sub-micron process scaling trends have influenced g_{mb}, and more importantly, g_{mb}/g_m, simulations were performed in the circuit simulator, Cadence Spectre [144], on a *n*-type MOSFET for two different gate lengths, L_g = 300 nm and L_g = 500 nm. The device was simulated using PDKs from IBM's standard 0.25 µm, 0.18 µm, 0.13 µm, 90 nm and 65 nm bulk CMOS technologies [3]–[7] and operated with an I_D = 150 µA, a gate over-drive voltage, $V_{GS} - V_T$ = 300 mV and a V_{BS} = 0 (W was allowed to vary in each process). Two cases were then considered: constant current, where $V_{DS} - V_{DSAT}$ was equal to 200 mV, and constant power ($V_{DS}I_D$), where V_{DS} was set to 1 V. The results for both gate lengths are displayed below in Figure 3.10 and Figure 3.11.

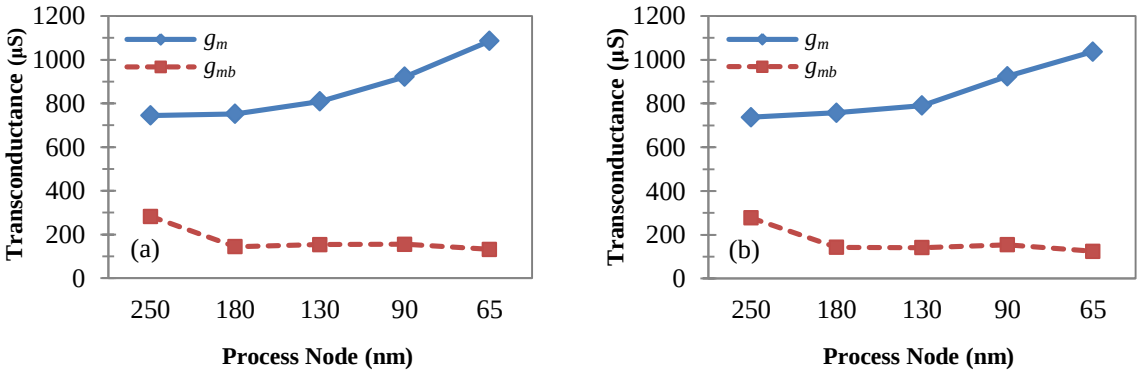


Figure 3.10: A plot of g_{mb} and g_m for an NMOS device (L_g = 300 nm) in various IBM bulk CMOS technologies under (a) constant current and (b) constant power constraints.

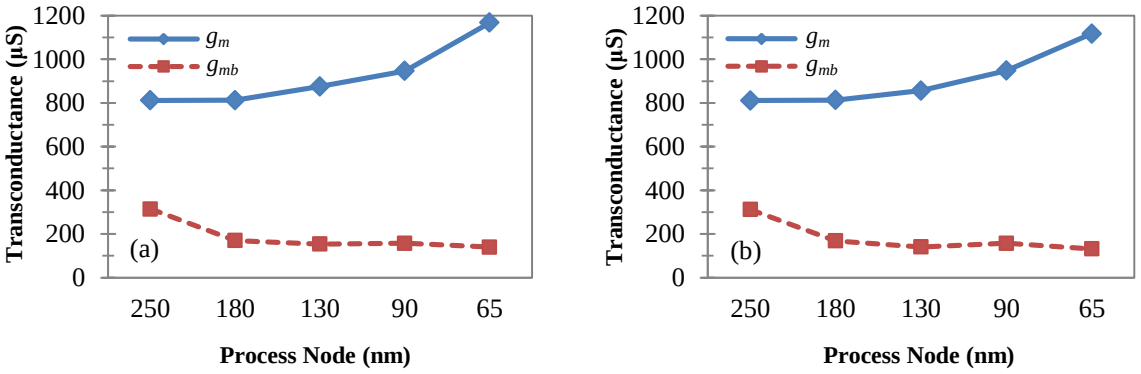


Figure 3.11: A plot of g_{mb} and g_m for an NMOS device (L_g = 500 nm) in various IBM bulk CMOS technologies under (a) constant current and (b) constant power constraints.

Figure 3.10 and Figure 3.11 both indicate that g_{mb}/g_m has decreased by 63% between IBM's 0.25 μm and 65 nm technologies [3]–[7]. This outcome – summarized in Table 3.1 [145] – is mainly brought about due to the fact that g_m has generally grown in each new process generation while g_{mb} has tended to remain constant from the 0.18 μm node onward. The behavior of g_m is easily attributed to the reduction in t_{ox} that occurs from process to process. However, the trend of g_{mb} takes a little more effort to explain.

Table 3.1: The g_{mb}/g_m ratios obtained from the results plotted in Figure 3.10 and Figure 3.11.

Gate Length	Condition	0.25 μm Process	65 nm Process
300 nm	Constant Current	0.380	0.121
	Constant Power	0.377	0.120
500 nm	Constant Current	0.387	0.120
	Constant Power	0.385	0.118

There are two main parameters which control g_{mb} in a process scaling scenario – t_{ox} and V_{T0}. A smaller t_{ox} has a positive influence on g_{mb} because it forces one to increase the *effective* background doping concentration, $N_{a,eff}$[†], to maintain a constant value of V_{T0} (refer to (3.1)–(3.4)) in each new process generation. However, since recent process scaling trends (as described in Section 1.1) dictate that V_{T0} also be reduced from process to process, the required growth in $N_{a,eff}$ is relatively subdued. As a result, y_d, and thus, g_{mb}, remain fairly constant across process technology – due to their square root dependence on the background doping concentration – resulting in the behavior seen between the 0.18 μm and 65 nm nodes in Figure 3.10 and Figure 3.11.

The rather large drop in g_{mb} that occurs between the 0.25 μm and 0.18 μm technologies is thought to be an anomaly because the L_g values considered in this process scaling study are closest to $L_{g,min}$ at the 0.25 μm node. Therefore, since current

[†] In an *n*-type MOSFET, $N_{a,eff}$ is defined as the average *p*-type doping concentration found between the surface of the device and the depletion depth beneath the channel.

technologies utilize halo implantation to improve the performance of digital devices, it is possible that the halo regions are most significantly overlapped in the 0.25 µm case causing $N_{a,eff}$ and thus the observed value of g_{mb} to be noticeably higher in that process[†].

To round out the process scaling study, g_{mb}/g_m was also analyzed against the gate length, as shown in Figure 3.12 for IBM's 0.18 µm and 65 nm technologies. From the figure, one can see that the g_{mb}/g_m ratio tails off as L_g approaches $L_{g,min}$. The roll off in g_{mb}/g_m is credited to source/drain charge sharing since it is likely that the source and drain prefer to steal depletion charge away from the bulk terminal rather than the gate as L_g is reduced because the bulk has weaker control over the channel [145]. Therefore, this finding suggests that bulk-driven circuits should use gate lengths longer than $2L_{g,min}$–$3L_{g,min}$ to maximize the g_{mb}/g_m ratio.

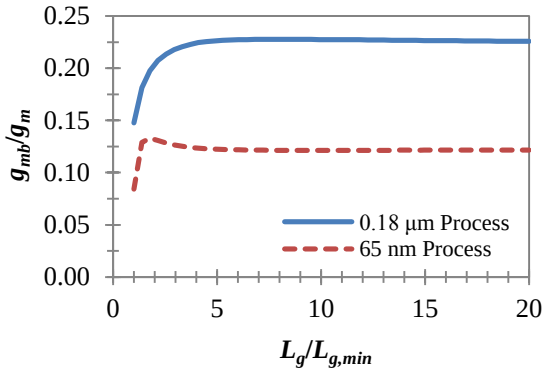


Figure 3.12: A plot of g_{mb}/g_m vs. $L_g/L_{g,min}$ for an NMOS device in IBM's standard 0.18 µm and 65 nm bulk CMOS technologies (V_{GS} = V_{DS} = 1 V, V_{BS} = 0 and W/L_g = 10).

3.4 The Implications of Gate Oxide Scaling on Device Performance

The g_{mb}, g_m and g_{mb}/g_m values of an NMOS device are plotted against t_{ox} in Figure 3.13(a) for a representative 90 nm bulk CMOS technology using the results of a 2-D ATLAS simulation [146]. Ultimately, Figure 3.13(a) suggests that the gate oxide scaling requirements of a BD MOSFET are not as stringent as those of a GD MOSFET

[†] A larger L_g could not be considered in this investigation due to an issue with the 90 nm PDK obtained by the author. The PDK had an artificially low limit on the maximum gate length that could be simulated.

because g_{mb} does not degrade as quickly as g_m does when t_{ox} is increased. These differing trends in g_{mb} and g_m occur because the bulk is able to maintain better control over the channel through its depletion capacitance, C_d, as t_{ox} is made thicker. As a result, if one were to enlarge t_{ox} from 1.4 nm (the typical gate oxide thickness of a standard 90 nm technology [6]) to 1.8 nm, one would see g_{mb} decrease by only 8%. Over that same span, g_m would fall by more than 18%.

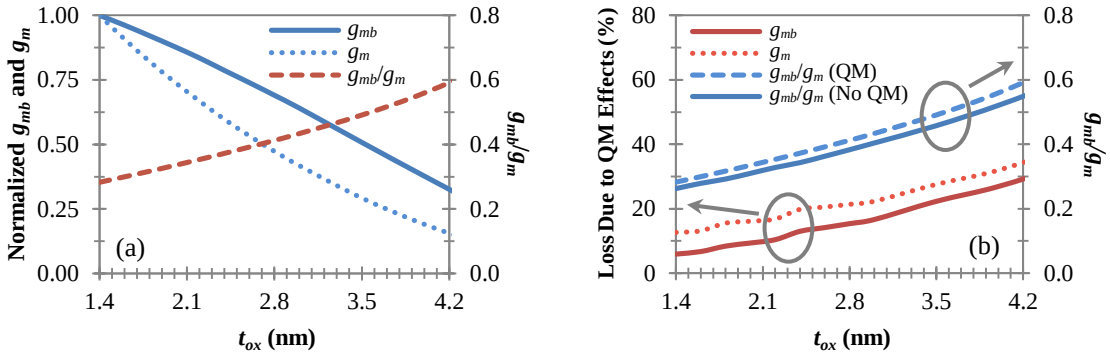


Figure 3.13: (a) A plot of the normalized values of g_{mb} and g_m (referenced to g_{mb} and g_m at t_{ox} = 1.4 nm) as well as g_{mb}/g_m vs. t_{ox} along with (b) a plot of the loss in g_{mb} and g_m caused by quantum mechanical effects vs. t_{ox} (L_g = 400 nm, V_{T0} = 0.3 V at t_{ox} = 1.4 nm, V_{GS} = V_{DS} = 1 V and V_{BS} = 0). The g_{mb}/g_m ratio is also shown in (b) with and without the influence of quantum mechanical effects.

In Figure 3.13(b), the data from Figure 3.13(a) is plotted once more with and without the influence of quantum mechanical (QM) effects[†] [146]. The figure indicates that g_{mb}/g_m is roughly 7% higher when quantum mechanical effects are taken into account. This 7% growth in g_{mb}/g_m signifies that the disparity between the bulk- and gate-driven techniques has decreased, which benefits the bulk-driven approach. The increase in g_{mb}/g_m is attributed to the fact that quantum mechanical confinement in the inversion layer causes C_d to be measured between the depletion depth beneath the channel and the peak of the inversion layer carrier concentration, rather than the Si–SiO_2 interface [147]. Hence, while C_d does degrade as a result of quantum mechanical confinement, its reduction is not as significant as that of C_{ox}.

[†] Polysilicon gate depletion was not accounted for in these simulations.

3.5 The Role of Threshold Voltage in Analog Bulk-Driven Circuitry

When Blalock performed the first-ever in-depth investigation of the BD MOSFET in a 2 μm technology in 1996, he chose to use a V_{DD} = 1 V to demonstrate that it would be feasible to design analog circuits at low power supply voltages if the BD MOSFET was used to augment existing circuit design techniques [26] (pp. 7–9). By lowering the power supply voltage of his 2 μm technology from its nominal value of 5 V to 1 V, Blalock was able to artificially raise the process' V_{T0}/V_{DD} ratio from 0.14 to 0.70 which ensured that each BD MOSFET he used would have a rather small V_{DSAT}.

Since Blalock's study, a 1 V power supply voltage has generally been adopted to verify the low-voltage operation of a bulk-driven circuit in the literature – regardless of what technology was used to implement the circuit. As a result, it turns out that the V_{T0}/V_{DD} ratio is a *decreasing* function of process scaling in the bulk-driven realm. As one would expect, this steady decline in V_{T0}/V_{DD} is *detrimental* to the performance of bulk-driven circuitry[†] because it causes a BD MOSFET's V_{DSAT} to grow in each new process generation.

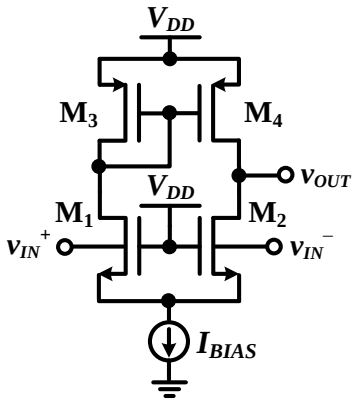


Figure 3.14: The schematic representation of a single-ended bulk-driven differential amplifier.

[†] Recall from Section 1.2 that the opposite is true for the gate-driven realm because a low V_{T0}/V_{DD} ratio *aids* the performance of gate-driven circuitry.

To illustrate the consequences of a *declining* V_{T0}/V_{DD} ratio, consider a bulk-driven differential amplifier – such as the one shown in Figure 3.14 – which has been designed in a 65 nm technology where the nominal V_{DD} and V_{T0} have fallen to 1 V and 0.29 V, respectively [7]. For a $|V_{GS3}| = V_T + 100$ mV [13], $I_{BIAS} = 20$ μA and $L_g = 5L_{g,min}$ [8], one can calculate the ICMR of this amplifier to be:

$$\begin{gathered} V_{BS1} + V_{DSAT,IBIAS} \le \mathrm{ICMR_{BD}} \le V_{DD} - |V_{GS3}| - V_{DSAT1} + V_{BS1} \\ 0 \le \mathrm{ICMR_{BD}} \le 0.78\ \mathrm{V} \end{gathered} \tag{3.30}$$

if BSIM4 [14] is used to determine each V_{DSAT} and if V_{BS1} is kept below its conservative upper limit of 0.6 V [25]. Based on this calculation, one can conclude that the rail-to-rail ICMR expected from the bulk-driven differential amplifier is no longer attainable at such a *low* V_{T0}/V_{DD} ratio because V_{BS1} cannot climb high enough to compensate for the rather large value of V_{DSAT1}.

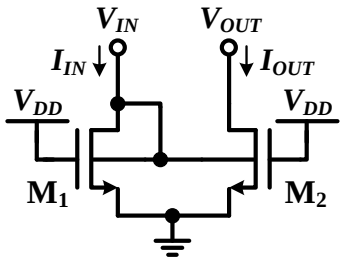


Figure 3.15: The schematic representation of a simple bulk-driven current mirror.

Naturally, a bulk-driven current mirror – such as the one depicted in Figure 3.15 – will also suffer from a *falling* V_{T0}/V_{DD} ratio since its input voltage, $V_{IN} = V_{BS1} = V_{DS1}$, must be greater than V_{DSAT1} in order to provide a reasonably-sized input current. For a $V_{DD} = 1$ V [7], $V_{T0} = 0.29$ V [7], $I_{IN} = 20$ μA and $L_g = 5L_{g,min}$ [8], one can calculate the bulk-driven current mirror's minimum allowable input voltage to be 0.47 V in a 65 nm technology if BSIM4 [14] is used to compute V_{DSAT1}. This input voltage is much higher than that of an equivalent gate-driven current mirror because the gate of the mirroring

device (M_1) is tied to the power supply voltage in the bulk-driven case rather than V_T + 100 mV [13].

Given the above insight, it is likely that the process-scaling-induced growth in V_{DSAT} is responsible for the lack of publications on bulk-driven differential amplifiers and current mirrors below the 0.18 μm node [145]. While the performance of these circuits should improve as V_{DD} scales toward 0.7 V [8], the decrease in V_{DD} may not be enough to alleviate the issues outlined above. Therefore, if one wishes to design bulk-driven circuits in technologies with feature sizes smaller than 0.18 μm, it may be necessary to tie the gate of an *n*-type BD MOSFET to a voltage less than V_{DD} such that the device's V_{DSAT} is lowered adequately. However, doing so would require the generation of an additional bias voltage [85].

3.6 Conclusions

This chapter has provided an extensive review of the long-channel operation of a BD MOSFET and has presented several new contributions to expand the field's understanding of how sub-micron process scaling trends have affected the characteristics of the device, as described below [145]–[146]:

- An equation was developed to model the short-channel behavior of g_{mb} in a uniformly-doped device. This equation had good correlation with 2-D device simulations down to a channel length of 200 nm.
- g_{mb}/g_m was observed to fall from roughly 0.380 to 0.120 between IBM's standard 0.25 μm and 65 nm bulk CMOS technologies. This trend is thought to occur because g_m continually increases in each new process generation due to a reduction in t_{ox} while g_{mb} remains relatively constant since $N_{a,eff}$ and C_d do not rise appreciably if V_{T0} is decreased from process to process along with t_{ox}.
- g_{mb}/g_m was found to roll off for gate lengths close to $L_{g,min}$ as a result of considerable charge sharing between the bulk, source and drain. It was

suggested that bulk-driven circuits use gate lengths longer than $2L_{g,min}$–$3L_{g,min}$ to maximize the g_{mb}/g_m ratio.

- The advantages expected from the bulk-driven differential amplifier and current mirror architectures were shown to disappear if the circuits were used in an environment where V_{T0}/V_{DD} was sufficiently *low*, such as in low-voltage analog applications targeted for technologies with features sizes smaller than 0.18 μm. It was noted that the benefits of these circuits could be regained by tying the gate of an *n*-type BD MOSFET to a bias voltage less than V_{DD}, thereby shrinking V_{DSAT}.
- The gate oxide scaling requirements of a BD MOSFET were found to be less stringent than those of a GD MOSFET because the bulk is able to maintain better control over the channel through its depletion capacitance as t_{ox} is made thicker.
- Quantum mechanical effects were shown to be less detrimental to the performance of a MOSFET when the bulk is used as an input terminal rather than the gate because C_d/C_{ox} grows as the peak of the inversion layer carrier concentration moves away from the Si–SiO_2 interface.

Based on the knowledge gained from this chapter, one can devise a set of three major device design goals to address the deficiencies of a BD MOSFET intended for use within a deca-nanometer bulk CMOS process. Of these guidelines, it will be most important to modify a BD MOSFET's doping profile in such a way that y_d is reduced – *i.e.*, g_{mb} is improved – so that the intrinsic gain, frequency response and input-referred noise limitations of the device can be mitigated as much as possible. Subsequently, it will be necessary to modify a BD MOSFET's well structure in order to reduce the device's layout area requirements and well capacitance (to further improve $f_{T,BD}$), as well as to lessen the consequences of the well proximity effect. Lastly, since bulk-driven circuits require that a process' V_{T0}/V_{DD} ratio be relatively *large*, it would be prudent to investigate whether it is possible to increase a BD MOSFET's long-channel threshold

voltage – *i.e.*, its *effective* background doping concentration – in order to restore the expected advantages of bulk-driven circuitry in deca-nanometer technologies. With these metrics defined, it is now possible to move forward and search for ways to meet the objectives stated above.

4 Improving the Performance of Bulk-Driven MOSFETs

4.1 Methods to Enhance the Bulk Transconductance

4.1.1 Conventional Uniform Doping

Throughout this dissertation, the low transconductance of a BD MOSFET has been identified as a major limitation of the device. Based on (3.2) (from Section 3.1.1), it is apparent that this limitation can be mitigated rather easily by using a uniformly-doped profile in the device and by raising the doping profile's N_a until a sufficient g_{mb} has been achieved. However, since this dissertation will ultimately culminate with the design of a BD MOSFET in a deca-nanometer bulk CMOS process, it is unlikely that such a design approach would be sensible because $N_{a,eff}$ is known to be greater than 1×10^{18} cm^{-3} in the deca-nanometer regime [145]. Thus, if one were to raise a uniformly-doped profile's N_a in an attempt to boost g_{mb} significantly, one would cause an appreciable amount of ionized impurity scattering in the channel, negating any potential enhancement in g_{mb}.

4.1.2 Step, Delta and Counter Doping

While there are currently no known reports of any g_{mb} enhancement techniques in the literature, there has been a fair amount of effort put into modifying the body effect[†] for digital applications, as seen in [148]–[151], [152] (pp. 32–46) and [153] (pp. 49–56). In these publications, three vertical doping profiles have been considered for tailoring the body effect to meet certain specifications – they are called the step-, delta- and counter-doped profiles, and are shown in Figure 4.1.

The fundamental advantage of the step-, delta- and counter-doped profiles is that each profile has the ability to redistribute dopants away from the surface of a MOSFET

[†] The body effect is typically defined as $\Delta V_T = V_T|_{V_{BS}=0} - V_T$ for a particular value of V_{BS}.

and into a region just below the device's channel in such a way that y_d is reduced relative to its nominal depth in a uniformly-doped device for a given value of V_{T0} and $N_{a,eff}$. As a result, these profiles allow y_d and g_{mb} to be controlled through a combination of $N_{a,eff}$ and the thickness of an epitaxially-grown lightly-doped channel region, defined as y_{epi} [151].

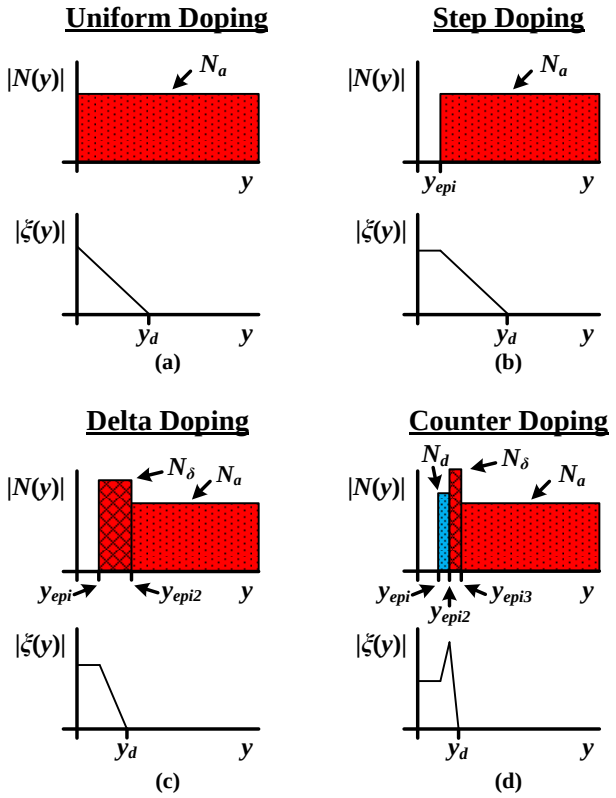


Figure 4.1: A plot of the dopant distribution, $N(y)$, and the electric field, $\xi(y)$, of a (a) uniformly-doped, (b) step-doped, (c) delta-doped and (d) counter-doped profile vs. the vertical depth, y, into the substrate. Note that N_d denotes a region of *n*-type doping while N_a and N_δ correspond to regions of *p*-type doping. The average *p*-type doping concentration for $y < y_{epi}$ is denoted as N_{epi} and is not shown in the figure.

To see how the step-, delta- and counter-doped profiles translate to a BD MOSFET, it is helpful to derive a simple 1-D equation for the long-channel bulk transconductance of each profile and to compare the results to (3.2). To start the analysis, consider the step-doped profile. Using the definitions given in Figure 4.1(b), one can write a piece-wise equation for the profile's charge density as follows:

$$\rho_{SD}(y) = \begin{cases} -qN_{epi} & 0 \le y \le y_{epi} \\ -qN_a & y_{epi} \le y \le y_d \end{cases} \tag{4.1}$$

$\rho_{SD}(y)$ can then be substituted into Poisson's Equation to yield the potential, φ_{SD}. Through a rearrangement of φ_{SD}, the depletion depth can be found to be:

$$y_{d,SD} = \sqrt{\frac{1}{N_a}\left[\frac{2\varepsilon_{si}(2\varphi_F - V_{BS})}{q} + (N_a - N_{epi})y_{epi}^2\right]} \tag{4.2}$$

if φ_{SD} is set to $2\varphi_F - V_{BS}$ at the onset of inversion. With $y_{d,SD}$ obtained, the depletion charge (per unit area) can be written as:

$$Q'_{B,SD} = -qN_{a,eff}y_d = -qN_{epi}y_{epi} - qN_a(y_d - y_{epi}) \tag{4.3}$$

where N_{epi} is defined as the average *p*-type doping concentration for $y < y_{epi}$. The long-channel threshold voltage of the step-doped profile then becomes:

$$V_{T0,SD} \equiv V_{GS}\big|_{\varphi_{SD}=2\varphi_F - V_{BS}} = V_{FB} + 2\varphi_F - \frac{Q'_{B,SD}}{C'_{ox}} = \zeta_{SD} + \gamma\sqrt{(2\varphi_F - V_{BS}) + \frac{q}{2\varepsilon_{si}}(N_a - N_{epi})y_{epi}^2} \tag{4.4}$$

where:

$$\zeta_{SD} = V_{FB} + 2\varphi_F - \frac{q}{C'_{ox}}(N_a - N_{epi})y_{epi} \tag{4.5}$$

Using $V_{T0,SD}$, one can finally express the bulk transconductance of the step-doped profile as:

$$g_{mb,SD} = -g_{m,SD}\frac{\partial V_{T0,SD}}{\partial V_{BS}} = \frac{\gamma g_{m,SD}}{2\sqrt{(2\varphi_F - V_{BS}) + \frac{q}{2\varepsilon_{si}}(N_a - N_{epi})y_{epi}^2}} \tag{4.6}$$

where $g_{m,SD}$ is the gate transconductance of the step-doped profile.

The analysis from above can be repeated for the delta-doped profile (Figure 4.1(c)) by making a slight modification to the charge density equation:

$$\rho_{DD}(y) = \begin{cases} -qN_{epi} & 0 \le y \le y_{epi} \\ -qN_{\delta} & y_{epi} \le y \le y_{epi2} \\ -qN_a & y_{epi2} \le y \le y_d \end{cases} \tag{4.7}$$

In due course, $\rho_{DD}(y)$ results in a depletion depth of:

$$y_{d,DD} = \sqrt{\frac{1}{N_a}\left[\frac{2\varepsilon_{si}(2\varphi_F - V_{BS})}{q} + (N_a - N_{epi})y_{epi}^2 + (N_a - N_\delta)(y_{epi2}^2 - y_{epi}^2)\right]} \tag{4.8}$$

and a long-channel threshold voltage of:

$$V_{T0,DD} = \zeta_{DD} + \gamma\sqrt{(2\varphi_F - V_{BS}) + \frac{q}{2\varepsilon_{si}}\left[(N_a - N_{epi})y_{epi}^2 + (N_a - N_\delta)(y_{epi2}^2 - y_{epi}^2)\right]} \tag{4.9}$$

where:

$$\zeta_{DD} = V_{FB} + 2\varphi_F - \frac{q}{C'_{ox}}\left[(N_a - N_{epi})y_{epi} + (N_a - N_\delta)(y_{epi2} - y_{epi})\right] \tag{4.10}$$

The bulk transconductance of the delta-doped profile then becomes:

$$g_{mb,DD} = \frac{\gamma g_{m,DD}}{2\sqrt{(2\varphi_F - V_{BS}) + \frac{q}{2\varepsilon_{si}}\left[(N_a - N_{epi})y_{epi}^2 + (N_a - N_\delta)(y_{epi2}^2 - y_{epi}^2)\right]}} \tag{4.11}$$

where $g_{m,DD}$ is the gate transconductance of the delta-doped profile.

For the counter-doped profile (Figure 4.1(d)), one can write the charge density equation as follows:

$$\rho_{CD}(y) = \begin{cases} -qN_{epi} & 0 \le y \le y_{epi} \\ q(N_d - N_a) & y_{epi} \le y \le y_{epi2} \\ -qN_\delta & y_{epi2} \le y \le y_{epi3} \\ -qN_a & y_{epi3} \le y \le y_d \end{cases} \tag{4.12}$$

After a few mathematical maneuvers, $\rho_{CD}(y)$ yields a depletion depth of:

$$y_{d,CD} = \sqrt{\frac{1}{N_a}\left[\frac{2\varepsilon_{si}(2\varphi_F - V_{BS})}{q} + (N_a - N_{epi})y_{epi}^2 + N_d(y_{epi2}^2 - y_{epi}^2) + (N_a - N_\delta)(y_{epi3}^2 - y_{epi2}^2)\right]} \tag{4.13}$$

and a long-channel threshold voltage of:

$$V_{T0,CD} = \zeta_{CD} + \gamma\sqrt{(2\varphi_F - V_{BS}) + \frac{q}{2\varepsilon_{si}}\left[(N_a - N_{epi})y_{epi}^2 + N_d(y_{epi2}^2 - y_{epi}^2) + (N_a - N_\delta)(y_{epi3}^2 - y_{epi2}^2)\right]} \tag{4.14}$$

where:

$$\zeta_{CD} = V_{FB} + 2\varphi_F - \frac{q}{C'_{ox}}\left[\left(N_a - N_{epi}\right)y_{epi} + N_d\left(y_{epi2} - y_{epi}\right) + \left(N_a - N_\delta\right)\left(y_{epi3} - y_{epi2}\right)\right] \quad (4.15)$$

As a result, the bulk transconductance of the counter-doped profile then becomes:

$$g_{mb,CD} = \frac{\gamma g_{m,CD}}{2\sqrt{\left(2\varphi_F - V_{BS}\right) + \frac{q}{2\varepsilon_{si}}\left[\left(N_a - N_{epi}\right)y_{epi}^2 + N_d\left(y_{epi2}^2 - y_{epi}^2\right) + \left(N_a - N_\delta\right)\left(y_{epi3}^2 - y_{epi2}^2\right)\right]}} \quad (4.16)$$

where $g_{m,CD}$ is the gate transconductance of the counter-doped profile.

The 1-D analysis performed above for the step-, delta- and counter-doped profiles is summarized in Table 4.1 where the expected behavior of y_d, V_{T0} and g_{mb} is listed for each profile relative to uniform doping under the constraint that N_a is kept constant in each profile. By examining Table 4.1, along with (3.2), (4.6), (4.11) and (4.16), it is apparent that both delta and counter doping have the ability to enhance g_{mb} if N_δ is sufficiently larger than N_d, and if N_d is sufficiently larger than N_a. Step doping, on the other hand, can only improve g_{mb} by raising N_a.

Since N_a corresponds to the doping level of an *n*-type BD MOSFET's *p*-well region, it would not be desirable to increase N_a because doing so would negatively influence C_{PW-DNW}, and thus, $f_{T,BD}$ (refer to Figure 3.2 and (3.8)). It is for this reason that step doping may be discounted as a potential g_{mb} enhancement technique.

Table 4.1: The expected behavior of y_d, V_{T0} and g_{mb} for the step-, delta- and counter-doped profiles relative to uniform doping (N_a is kept constant in each case).

Profile	y_d	V_{T0}	g_{mb}	Notes
Step	↑	↓	↓	$N_{epi} < N_a$
Delta	↓	↑	↑	$N_\delta > N_a$ & $N_{epi} < N_a$
Counter	↓	↑	↑	$N_\delta > N_d > N_a$ & $N_{epi} < N_a$

To gain further insight into the two remaining doping profile candidates, it is necessary to investigate how the bulk transconductances of the delta- and counter-doped

profiles compare to that of a uniformly-doped device at a constant value of V_{T0} since the long-channel threshold voltage is a device specification, not N_a. To complete this task, these doping profiles will be examined more thoroughly in a device simulator in Section 4.4.3.

4.2 Using Deep Trenches to Improve Layout Area Efficiency

The combined area of multiple BD MOSFETs can be reduced considerably by employing a deep trench isolation (DTI) scheme, such as the one illustrated in Figure 4.2 and Figure 4.3 for an *n*-type device. In this configuration, one can place several BD MOSFETs within a single deep *n* well where each device is electrically isolated from one another via deep trenches in the horizontal direction and by a reverse-biased *pn* junction from below. The deep trench depth is chosen such that it extends into a BD MOSFET's deep *n*-well region, but not all the way through to the *p*-type substrate. This allows the deep *n*-well region to be biased through a ring of n^+ contacts along its perimeter [154] and eliminates the well-to-well spacing requirements between adjacent BD MOSFETs.

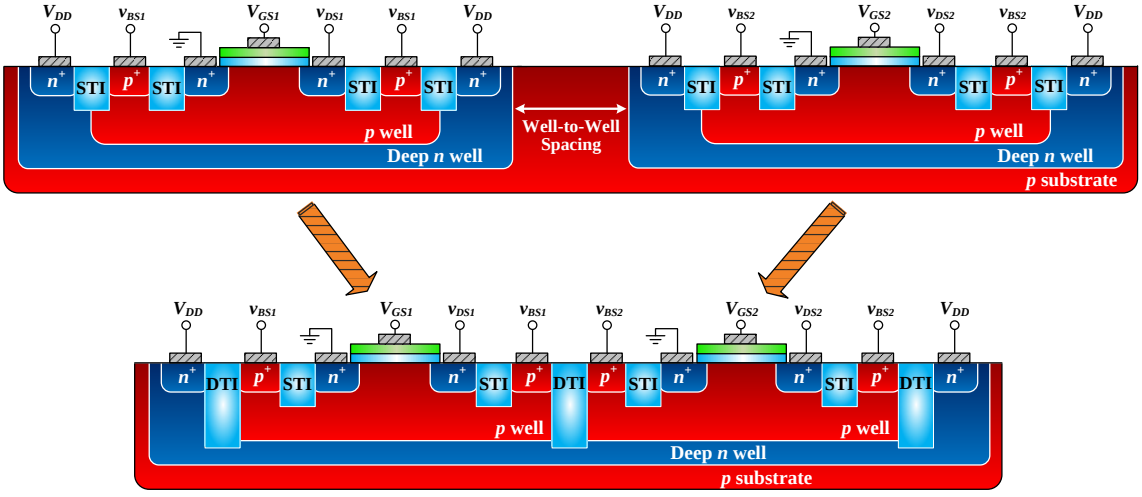


Figure 4.2: An illustration showing how DTI can be used to reduce the layout area requirements of a BD MOSFET – side view.

By choosing a DTI scheme over a triple-well implementation, one can condense the *effective* layout area of an *n*-type BD MOSFET from $(W + 2.45) \times (L_g + 2.45)$ μm^2 [7]

to $(W + 1.56) \times (L_g + 1.56)\ \mu m^2$ in a 65 nm bulk CMOS process. For a device with a $W = 10L_{g,min}$ and an $L_g = 5L_{g,min}$, this brings about an area reduction of 53%.

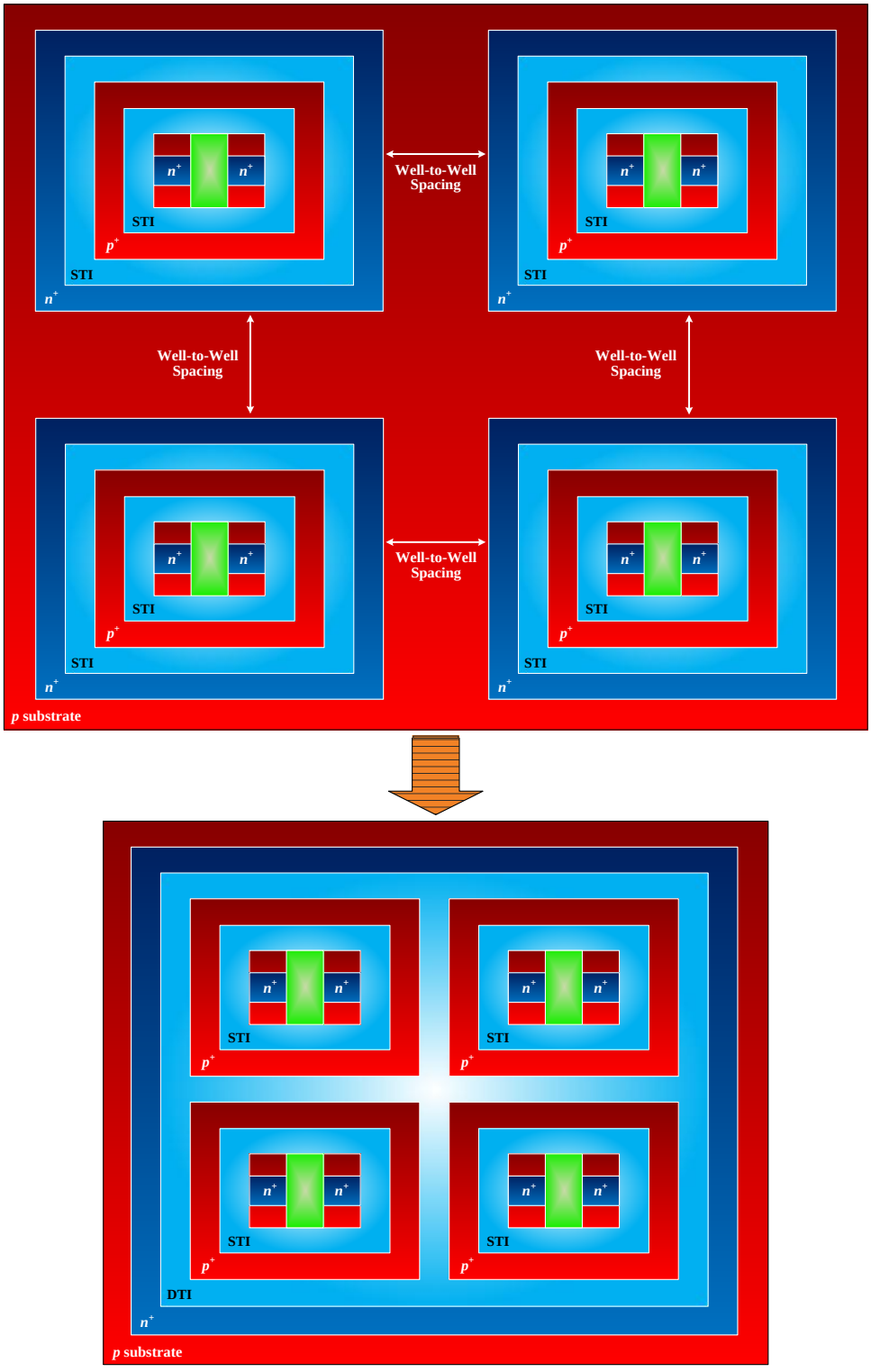


Figure 4.3: An illustration showing how DTI can be used to reduce the layout area requirements of a BD MOSFET – top view.

In addition to eliminating the well-to-well spacing requirements between adjacent BD MOSFETs, a DTI scheme should be able to minimize the well proximity effect's influence on the layout area of an *n*-type BD MOSFET because the device would no longer be surrounded by the edge of a deep *n* well on all sides. DTI should also cause a BD MOSFET's input capacitance to decrease since the isolation scheme removes the sidewall depletion capacitance component from the device's well structure. This could lead to a sizable increase in $f_{T,BD}$, and must be investigated in more detail using a device simulator.

4.3 Deca-Nanometer Technology MOSFET Model Review

To see how delta doping, counter doping and DTI influence the performance of a BD MOSFET, it is beneficial to evaluate the effectiveness of these process changes using ATLAS [38]. But, before any simulation can be executed, one must first ensure that the proper device models have been activated in ATLAS so that the predictions made by the simulator are realistic. Since the ultimate goal of this chapter is to gauge the potency of the aforementioned process changes in a deca-nanometer bulk CMOS process, it is necessary to find device models which can account for the dominant short-channel and quantum mechanical phenomena that are known to exist in the deca-nanometer regime.

4.3.1 The Energy Balance Transport Model

During the course of a typical device simulation, one will step through an iterative process that involves solving a set of carrier transport equations along with Poisson's Equation. The transport equations are used to describe the response of electrons (or holes) to an applied electric field while Poisson's Equation gauges how the movement of these electrons perturbs the electric field within a device.

Usually, electron transport is defined by a set of balance equations that are derived from the Boltzmann Transport Equation since it is computationally taxing to

solve the Boltzmann Transport Equation directly. The simplest and most commonly used approximation of the Boltzmann Transport Equation is known as the Drift–Diffusion Model; it consists of two balance equations representing electron continuity (4.17) and current density (4.18), as shown below [155] (pp. 171–193, 290–291):

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet \mathbf{J_n} + G - R \tag{4.17}$$

$$\mathbf{J_n} = -q\frac{\mathbf{P}}{m_e^*} = -qn\mu_n \nabla V + qD_n \nabla n \tag{4.18}$$

where $G - R$ represents the difference between the generation and recombination rates while $\mathbf{P}$ and m_e^* stand for the momentum and the effective mass of an electron, respectively.

The fundamental limitation of the Drift–Diffusion Model is its assumption that the electron temperature, T_n, is equal to the lattice temperature, T_L. With this constraint, parameters such as the impact ionization rates, the carrier mobility and the drift velocity (υ_d) are linked to a local electric field rather than the spatial variation of T_n. As a result, it is possible to severely underestimate a MOSFET's transconductance and output resistance at deca-nanometer dimensions because one has neglected velocity overshoot [156] and has overestimated the amount of impact ionization [38] (Ch. 3, pp. 24, 105), [157], respectively.

To make the Drift–Diffusion Model more accurate, one must allow T_n to deviate from T_L. This can be accomplished by relating T_n to the average kinetic energy of an electron, which can be written as the sum of an electron's drift and thermal energies [155] (pp. 182–183):

$$W_n = \frac{1}{2}nm_e^*\upsilon_d + \frac{3}{2}nkT_n \tag{4.19}$$

Using (4.19), one can then incorporate electron temperature gradients into the Drift–Diffusion Model by creating an additional balance equation representing the rate of

energy lost by an electron to the lattice [38] (Ch. 3, pp. 24–27), [155] (pp. 181–188). This additional balance equation is shown below:

$$\frac{\partial W_n}{\partial t} = -\nabla \bullet \mathbf{F_n} + \mathbf{J_n} \bullet \nabla V - \frac{3}{2} nk \left(\frac{T_n - T_L}{\tau_e} \right) + G - R \tag{4.20}$$

$$\mathbf{F_n} = W_n \boldsymbol{\upsilon}_\mathbf{d} + nkT_n \boldsymbol{\upsilon}_\mathbf{d} - K_n \nabla T_n \tag{4.21}$$

where K_n stands for the thermal conductivity of an electron and $\mathbf{F_n}$ denotes the flux of energy between an electron and the lattice; τ_e represents the energy relaxation time – *i.e.*, the time needed for the energy (temperature) distribution to reach steady state with the electric field [158].

To complete the modification of the Drift–Diffusion Model, one must alter (4.18) to include a dependence on T_n [155] (pp. 191–193). By including this dependence, one can obtain:

$$\mathbf{J_n} = -qn\mu_n \nabla V + qD_n \nabla n + n\mu_n k \nabla T_n \tag{4.22}$$

The system of equations defined by (4.17) and (4.20)–(4.22) represents what is known as the Energy Balance Transport Model. The model can be activated in ATLAS by selecting **HCTE.EL** in the **MODELS** statement and requires that **BLOCK NEWTON** be chosen in the **METHOD** statement [38] (Ch. 3, pp. 24–27; App. E, pp. 4). To obtain the most accurate results, the I_D–V_{DS} curves predicted by the Energy Balance Transport Model should be calibrated to Monte Carlo simulations using τ_e as a fitting parameter. Commonly cited values of τ_e range between 0.1 ps and 0.2 ps [159]–[162].

4.3.2 Quantum Mechanical Effects

In the channel of a strongly-inverted thin-oxide MOSFET, the peak of the inversion layer carrier concentration, $n(y)$, is found at a distance, y_{inv}, away from the Si surface, as shown in Figure 4.4(a). The movement in $n(y)$ is caused by the formation of a

potential well between the Si–SiO_2 interface and y_{inv}, which forces the conduction band to split near the interface [130]–[132], [133] (pp. 43–48), [147] (pp. 59–105).

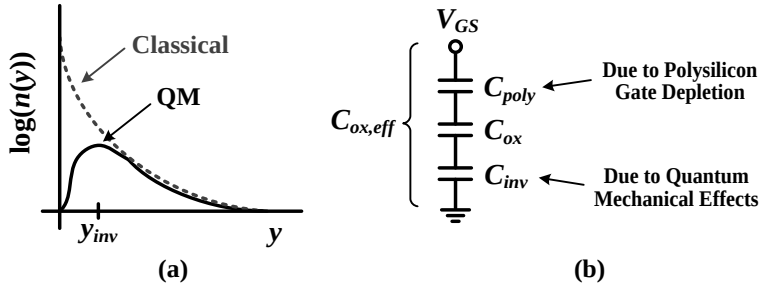


Figure 4.4: (a) A comparison between the classical and quantum mechanical distributions of *n*(*y*) in a MOSFET and (b) an equivalent circuit defining a MOSFET's effective gate oxide capacitance.

The quantum mechanical confinement of $n(y)$ must be considered in thin-oxide MOSFET simulations because it gives rise to a non-negligible inversion layer capacitance (per unit area), C'_{inv}, in series with C'_{ox} and the capacitive term representing polysilicon gate depletion – see Figure 4.4(b). As a consequence of C'_{inv}, the *effective* gate oxide capacitance (per unit area) of a MOSFET becomes [133] (pp. 43–48):

$$C'_{ox,eff} = \left(\frac{1}{C'_{poly}} + \frac{1}{C'_{ox}} + \frac{1}{C'_{inv}} \right)^{-1} = \left(\frac{y_{poly}}{\varepsilon_{si}} + \frac{t_{ox}}{\varepsilon_{ox}} + \frac{y_{inv}}{\varepsilon_{si}} \right)^{-1} \tag{4.23}$$

where ε_{ox} is the dielectric constant of SiO_2 multiplied by ε_0 and y_{poly} is the width of the depletion region in the gate. Quantum mechanical confinement also manifests itself in a MOSFET's *effective* depletion capacitance beneath the channel (per unit area), as seen below [147] (pp. 102–105):

$$C'_{d,eff} = \frac{\varepsilon_{si}}{y_d - y_{inv}} \tag{4.24}$$

The quantum mechanical behavior of $n(y)$ can be predicted in ATLAS by using the Bohm Quantum Potential Model [38] (Ch. 13, pp. 8–12), [163] (**BQP.N** in the **MODELS** statement). The model functions as follows: at a particular bias point, ATLAS solves Poisson's Equation and the corresponding carrier transport equations as it

would classically. ATLAS then proceeds to compute a position-dependent quantum potential, Λ, based on the results of the classical simulation and inserts Λ into (4.22) such that:

$$\mathbf{J_n} = -qn\mu_n \nabla(V - \Lambda) + qD_n \nabla n + n\mu_n k \nabla T_n \tag{4.25}$$

Poisson's Equation is then solved once more along with the modified carrier transport equations, and a new quantum potential is subsequently calculated. This process is repeated until the system converges before moving on to the next bias point. If sufficient accuracy has been achieved after a few iterations, the cycle can be limited through the use of **NBLOCKIT** in the **METHOD** statement.

To obtain the most accurate results, the Bohm Quantum Potential Model should be calibrated to 1-D MOS capacitance–voltage profiles generated by the Schrödinger–Poisson Equation solver in ATLAS. This calibration can be performed by adjusting the fitting parameters, **BQP.NGAMMA** and **BQP.NALPHA**, in the **MATERIAL** statement for the Si region(s) containing the inversion layer of a MOSFET[†] [38] (Ch. 13, pp. 9–11).

4.3.3 Direct-Tunneling-Induced Gate Current

Classically, an electron with energy, E, cannot surmount a barrier, E_B, if $E < E_B$. However, when the barrier is sufficiently thin, it is quantum mechanically possible for tunneling to occur because the wave function, $\Psi(y)$[‡], is non-zero at the transmitted end of the barrier [165] (pp. 143–150). In a MOS system – see Figure 4.5 – the probability of an electron tunneling through a gate oxide barrier has been found to be [147] (pp. 21–23):

$$P_{tunnel}(E) = e^{-2t_{ox}\sqrt{2m_e(E_B - E)}/\hbar} \tag{4.26}$$

[†] Due to an unresolved issue in ATLAS [164], one must set **BQP.NGAMMA = BQP.NALPHA = 0** in the polysilicon gate and gate oxide regions of a MOSFET in order to obtain the expected behavior in $n(y)$. This modification should only have a minor impact on ATLAS' predictions for $C_{ox,eff}$ and $C_{d,eff}$ since quantum mechanical confinement only occurs within the Si region(s) containing the inversion layer of a MOSFET.

[‡] $|\Psi(y)|^2$ denotes the probability of finding an electron at a certain position.

where m_e represents the mass of an electron and $\hbar$ is the reduced Planck's constant.

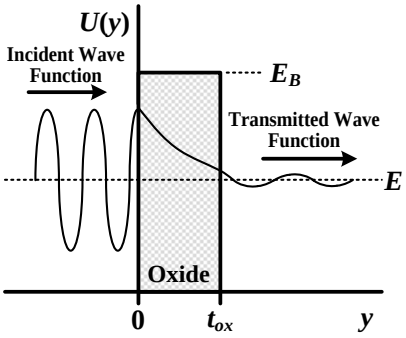


Figure 4.5: An illustration of an electron with energy, E, tunneling through a gate oxide layer with a thickness of t_{ox} for the case when $E < E_B$ ($U(y)$ denotes the potential energy).

Based on (4.26), one can expect an exponential increase in electron tunneling as t_{ox} is reduced. In fact, it turns out that when t_{ox} is on the order of a few nanometers, a non-negligible current will begin to flow through the gate of a MOSFET [42], [46], [166]–[170]. This gate current can be accounted for in ATLAS by selecting **QTUNN.EL**[†‡] in the **MODELS** statement [38] (Ch. 3, pp. 126–131), and the predictions made by the model can be calibrated to experimental data by using the effective mass of an electron in SiO_2 (m_{ox}^*) as a fitting parameter [133] (pp. 49–52), [171]–[172].

4.3.4 Mobility Models

The effective electron (or hole) mobility is characterized by four major mobility degradation mechanisms: ionized impurity scattering, phonon scattering, surface scattering and velocity saturation. Ionized impurity scattering can be included in ATLAS by choosing **CONMOB** in the **MODELS** statement while phonon and surface scattering can be added by activating **CVT** in the **MODELS** statement. Velocity saturation can be enabled by selecting **FLDMOB** in the **MODELS** statement. However, **FLDMOB** must

[†] **QTUNN.EL** will only function if a polysilicon gate region is defined in an ATLAS structure.

[‡] **QTUNN.EL** is a post-processing model that adds a current component to the gate terminal of a MOSFET after ATLAS has converged on a solution for a particular bias point. As a result, **QTUNN.EL** neglects the gate current's contribution to the drain, source and bulk terminal currents.

be augmented with the **EVSATMOD = 0** flag to ensure that the carrier velocity is related to the carrier energy (temperature) rather than the local electric field. For further discussion on the models introduced in this section, please see [38] (Ch. 3, pp. 42–81).

4.3.5 Miscellaneous Model Notes

In any MOSFET device simulation involving analog characterization, one must be sure to incorporate a carrier-energy-dependent impact ionization model (**TOYABE** in the **IMPACT** statement) because of the role that impact ionization plays in determining r_o [38] (Ch. 3, pp. 105–107), [157]. Moreover, when the background doping concentration exceeds 1×10^{18} cm^{-3}, it is also wise to account for band gap narrowing (**BGN** in the **MODELS** statement), Auger recombination (**HNSAUG** in the **MODELS** statement) and band-to-band tunneling (**BBT.KL** in the **MODELS** statement) since these effects become increasingly prominent at such high doping levels [38] (Ch. 3, pp. 9–10, 92–93).

4.3.6 Computational Requirements

By adding the Energy Balance Transport and Bohm Quantum Potential Models to a simulation deck, one will apply extensive computational strain on any computer attempting to run ATLAS. As a result of the models' mathematical complexity, it is not uncommon to see a single ATLAS DC simulation last more than 30 minutes on a 1 GHz, 8 GB RAM workstation for an L_g = 80 nm. To offset some of this computational burden, one can run a single instance of ATLAS on multiple processors by starting a simulation with the following command: **GO ATLAS SIMFLAGS = "–P #"** where # denotes the number of processors to be used in parallel [38] (Ch. 2, pp. 4). The benefit of this command is shown in Figure 4.6 where the normalized run time of a typical ATLAS DC simulation is plotted against the total number of processors utilized to perform the

simulation. From the figure, the significant decrease in simulation time (65%) is evident as the number of processors grows from one to six; the advantage of parallel computing becomes negligible beyond that point.

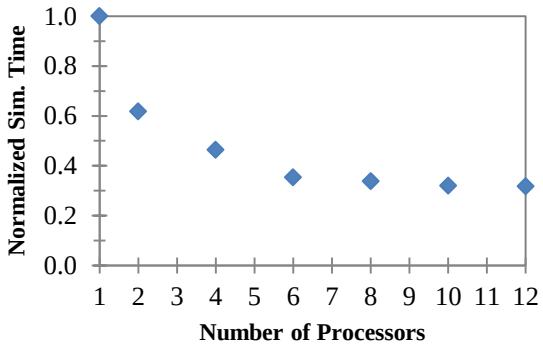


Figure 4.6: A plot of the normalized simulation time vs. the number of processors utilized to run a single ATLAS DC simulation. Note that normalization set the simulation time equal to one when only one processor was being used to perform a simulation.

4.4 The Benefits of Delta Doping, Counter Doping and Deep Trench Isolation

4.4.1 Simulation Setup

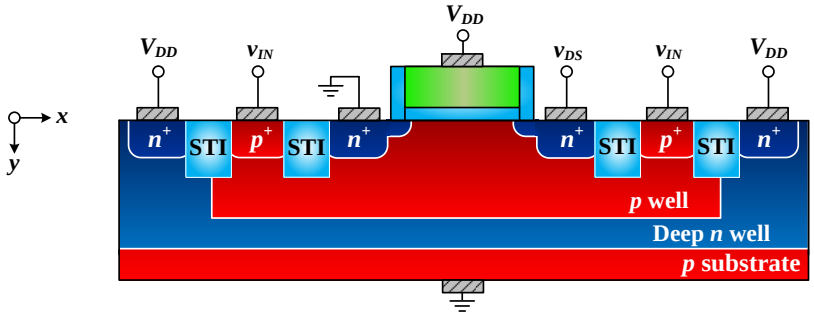


Figure 4.7: An illustration of the *n*-type BD MOSFET device cross-section created in ATLAS to examine the process changes proposed in Section 4.1 and Section 4.2. Note that this illustration does not depict any particular doping profile in the channel region of the device.

Using the electrical device models presented in Section 4.3, it is now possible to execute 2-D device simulations in ATLAS [38] to investigate the degree to which delta doping, counter doping and DTI are capable of improving the performance of a BD MOSFET. In this dissertation, these simulations were performed on an *n*-type BD MOSFET using the device cross-section illustrated in Figure 4.7 and the device mesh

seen in Figure 4.8 and Figure 4.9[†]. The dimensions and specifications of the device were selected to be largely consistent with those of a standard 90 nm bulk CMOS technology [6] and are summarized in Table 4.2.

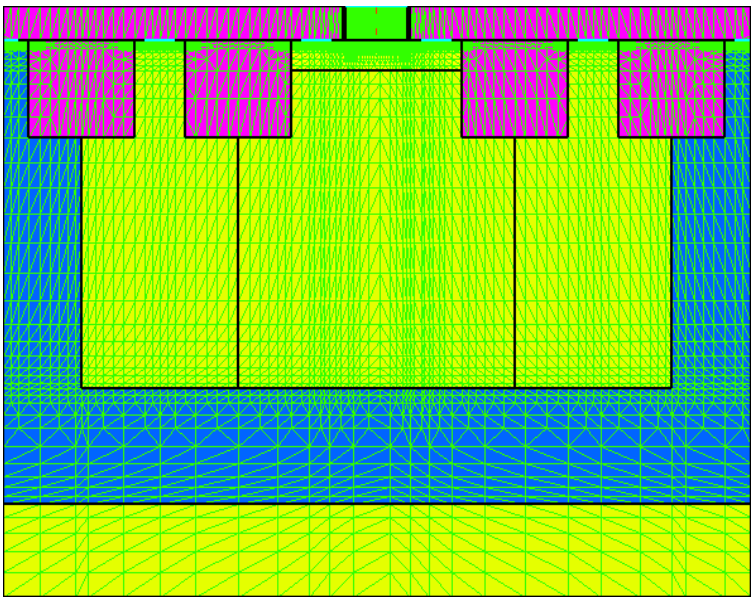


Figure 4.8: A screenshot of the 2-D mesh used to simulate an *n*-type BD MOSFET in ATLAS. Note that this particular image depicts the case in which triple-well isolation was used to isolate the device.

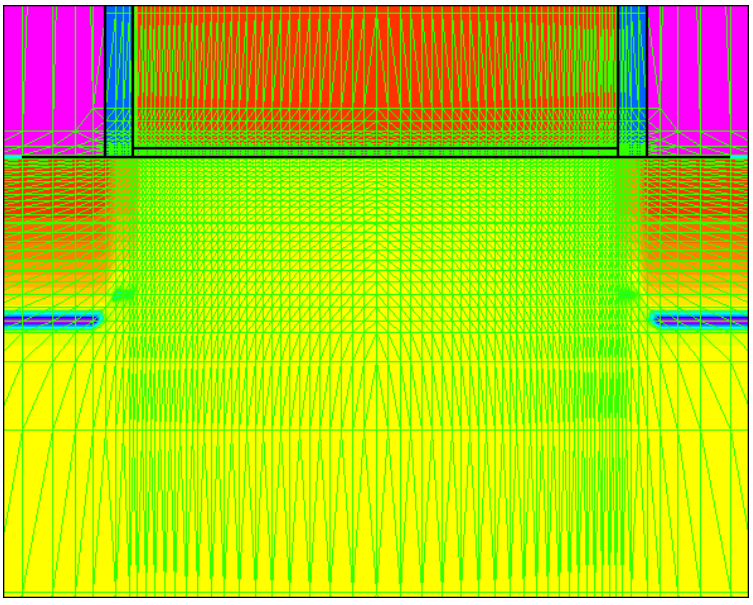


Figure 4.9: A close-up view of the 2-D mesh used to simulate an *n*-type BD MOSFET in ATLAS near the device's source and drain regions.

[†] The ATLAS and DBINTERNAL [173] (App. B, pp. 1–14) codes used to generate the BD MOSFET device cross-section, its mesh and all the subsequent data contained in Chapter 4 can be found in the Appendix starting on page 101 and 109, respectively.

Table 4.2: A list of the device parameters that were used in ATLAS to examine the process changes proposed in Section 4.1 and Section 4.2.

Device Parameter Description	Directionality	Value
Minimum Gate Length	*x*	80 nm
Long-Channel Threshold Voltage[†]	–	0.37 V
SiO_2 Gate Oxide Thickness	*y*	1.8 nm
n^+ Polysilicon Gate Doping Concentration	–	1×10^{20} cm^{-3}
n^+ Polysilicon Gate Height [174]	*y*	150 nm
SiO_2 Spacer Width	*x*	15 nm
p-Well Doping Concentration	–	1×10^{16} cm^{-3}
p-Well Depth	*y*	1.5 μm
Deep *n*-Well Doping Concentration	–	1×10^{17} cm^{-3}
Deep *n*-Well Depth	*y*	2.0 μm
p-Substrate Doping Concentration	–	1×10^{16} cm^{-3}
Source, Drain, *p*-Well and Deep *n*-Well Contact Doping Concentration	–	1×10^{20} cm^{-3}
Source, Drain, *p*-Well and Deep *n*-Well Contact Lateral Abruptness [166]	*x*	4.8 nm/dec
Source, Drain, *p*-Well and Deep *n*-Well Contact Junction Depth	*y*	30 nm
Source, Drain, *p*-Well and Deep *n*-Well Contact Width	*x*	200 nm
Source/Drain Extension Doping Concentration	–	2×10^{19} cm^{-3}
Source/Drain Extension Lateral Abruptness [166]	*x*	4.8 nm/dec
Source/Drain Extension Junction Depth	*y*	25 nm
SiO_2 STI Depth	*y*	0.42 μm
SiO_2 STI Width	*x*	0.42 μm

4.4.2 Model Calibration

To calibrate ATLAS [38] in accordance with the guidelines set forth in Section 4.3, it was necessary to begin by adjusting the Bohm Quantum Potential (BQP) Model to match the capacitance–voltage profile generated by the Schrödinger–Poisson (S–P) Equation for a 1-D uniformly-doped MOS structure with a degenerately-doped n^+ polysilicon gate, $t_{ox} = 1.8$ nm and $N_a = 1.125 \times 10^{18}$ cm^{-3}[‡]. Ultimately, the BQP Model calibration procedure yielded a **BQP.NGAMMA = 1.3** and a **BQP.NALPHA = 1.0** resulting in the curves shown in Figure 4.10.

[†] In Chapter 4–Chapter 6, the threshold voltage (V_T) is defined as the gate-to-source voltage at which $I_D = (2 \times 10^{-7}$ A/μm)/L_g for a $V_{DS} = 50$ mV; V_{T0} is defined as the threshold voltage at $L_g = 10L_{g,min}$.

[‡] The ATLAS code used to perform the calibration of the BQP Model can be found in the Appendix starting on page 110. Note that polysilicon gate depletion was not accounted for in the calibration procedure.

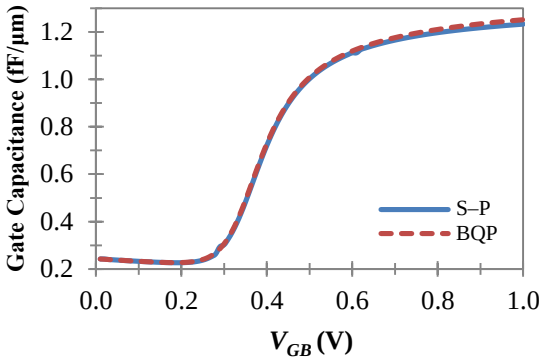


Figure 4.10: A plot of the capacitance–voltage profiles predicted by the Schrödinger–Poisson Equation and the BQP Model (BQP.NGAMMA = 1.3 and BQP.NALPHA = 1.0) for a 1-D MOS structure with a degenerately-doped n^+ polysilicon gate, t_{ox} = 1.8 nm and $N_a = 1.125 \times 10^{18}$ cm^{-3}.

Following the calibration of the BQP Model, the Energy Balance Transport Model was adjusted to replicate the I_D–V_{DS} characteristics predicted by the Monte Carlo device simulator, MCDEVICE [38] (Ch. 19, pp. 1–78), for a uniformly-doped MOSFET with a degenerately-doped n^+ polysilicon gate, t_{ox} = 1.8 nm, L_g = 80 nm and $N_a = 1.125 \times 10^{18}$ cm^{-3} (V_{T0} = 0.37 V)[†]. The outcome of the calibration procedure is depicted in Figure 4.11 for a τ_e = 0.1 ps[‡]. Using the same device, the gate current model, **QTUNN.EL**, was then tuned to reflect experimental data from [133] (pp. 49–52) and [171]–[172], resulting in an $m_{ox}^* = 0.45$.

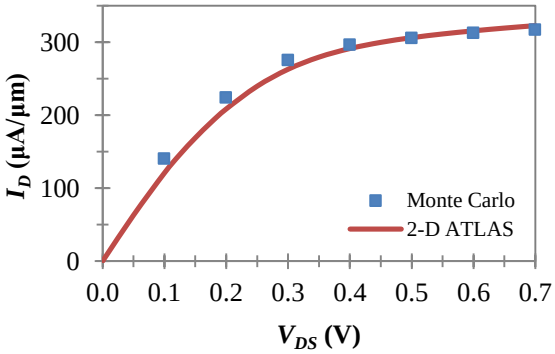


Figure 4.11: A plot of I_D vs. V_{DS} as predicted by Monte Carlo and 2-D ATLAS simulations (τ_e = 0.1 ps) for a uniformly-doped MOSFET with a degenerately-doped n^+ polysilicon gate, t_{ox} = 1.8 nm, $N_a = 1.125 \times 10^{18}$ cm^{-3}, L_g = 80 nm, V_{T0} = 0.37 V, V_{GS} = 0.7 V and V_{BS} = 0.

[†] The MCDEVICE and ATLAS codes used to perform the calibration of the Energy Balance Transport Model can be found in the Appendix starting on page 112 and 115, respectively. Note that quantum mechanical effects and polysilicon gate depletion were not accounted for in the calibration procedure.

[‡] With a τ_e = 0.1 ps and an L_g = 80 nm, ATLAS under-predicts I_D by at least 5% for V_{DS} < 0.4 V. However, this discrepancy in I_D should grow smaller as L_g approaches 250 nm since velocity overshoot does not influence I_D noticeably at such gate lengths [159].

4.4.3 Analysis of the Proposed Doping Profiles

With ATLAS [38] calibrated, delta doping (Figure 4.1(c)) was first examined to gain a greater understanding of how the doping profile influences the characteristics of a BD MOSFET, namely g_{mb}, $g_{mb}r_o$ and $f_{T,BD}$[†]. In the investigation, three lightly-doped channel layer thicknesses (y_{epi}) were considered: 0 nm, 5 nm and 10 nm; in order to maintain a constant V_{T0} = 0.37 V at every y_{epi}, the doping concentration of the delta-doped layer (N_δ) was set to: 1.125×10^{18} cm^{-3}, 1.75×10^{18} cm^{-3} and 3×10^{18} cm^{-3}, respectively. Additionally, the doping level of the lightly-doped channel region (N_{epi}) was held at 1×10^{15} cm^{-3} when y_{epi} was equal to 5 nm and 10 nm to preserve the integrity of the delta-doped profile, while the thickness of the delta-doped layer, $y_{epi2} - y_{epi}$, was kept at 100 nm to ensure that the depletion region beneath the channel terminated within the delta-doped layer for each y_{epi}[‡].

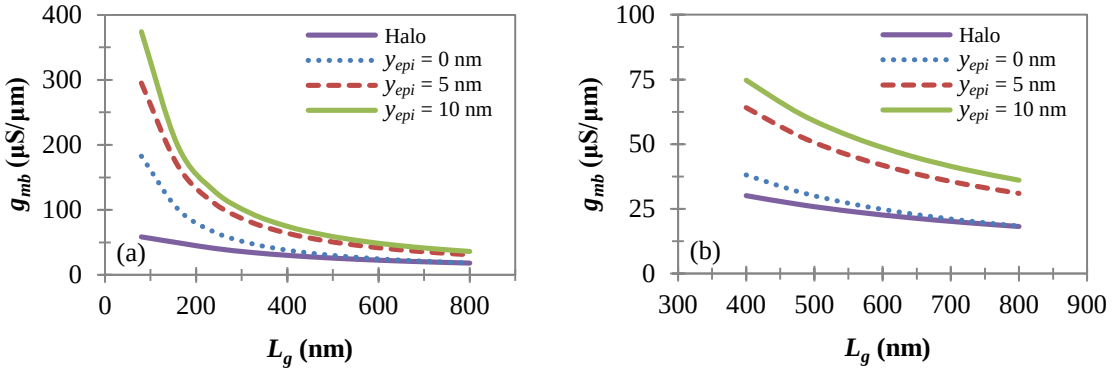


Figure 4.12: A plot of g_{mb} vs. L_g for halo-implanted, uniformly-doped and delta-doped *n*-type BD MOSFETs (V_{T0} = 0.37 V, V_{GS} = V_{DS} = 0.7 V and V_{BS} = 0) at gate lengths ranging from (a) 80 nm to 800 nm and (b) 400 nm to 800 nm. The halo-implanted device had halo lengths and depths equal to 30 nm and 20 nm, respectively; the device's halo regions were doped to 4×10^{18} cm^{-3}.

The bulk transconductances predicted by ATLAS are plotted in Figure 4.12(a) and (b) for the cases when uniform doping (equivalent to y_{epi} = 0 nm since $y_{epi2} > y_d$) and delta

[†] The input-referred noise of a BD MOSFET was not analyzed in this section since ATLAS lacks the ability to predict flicker noise if it does not receive certain process-dependent parameters from measured device data [38] (Ch. 16, pp. 11–12). For similar reasons, mechanical stress was also not accounted for in this section – nor in the investigations carried out in Chapter 5 and Chapter 6 [175] (Ch. 3, pp. 159–161).

[‡] The actual thickness of the delta-doped region is irrelevant as long as $y_{epi2} > y_d$.

doping (y_{epi} = 5 nm and 10 nm) are used in a BD MOSFET [176]. Data from a halo-implanted device are also included in the figures to provide a reference to the doping profile most commonly found in deca-nanometer technologies. From Figure 4.12(a) and (b), one can see that there is a distinct advantage to using delta doping in a BD MOSFET since the doping profile is capable of increasing g_{mb} by 96%–105% relative to a uniformly-doped profile for gate lengths ranging from 80 nm to 800 nm. This growth in g_{mb} is primarily provided by a reduction in y_d, which itself is caused by the redistribution of dopants from $y < y_{epi}$ to $y_{epi} < y < y_d < y_{epi2}$ in such a way that N_δ becomes larger than $N_{a,eff}$ without the subsequent climb in V_{T0}, as illustrated by the diagram in Figure 4.13. However, the growth process is somewhat aided by the decline of ionized impurity scattering in the channel based on the fact that the increase in g_{mb} is larger when y_{epi} is varied from 0 nm to 5 nm, rather than from 5 nm to 10 nm.

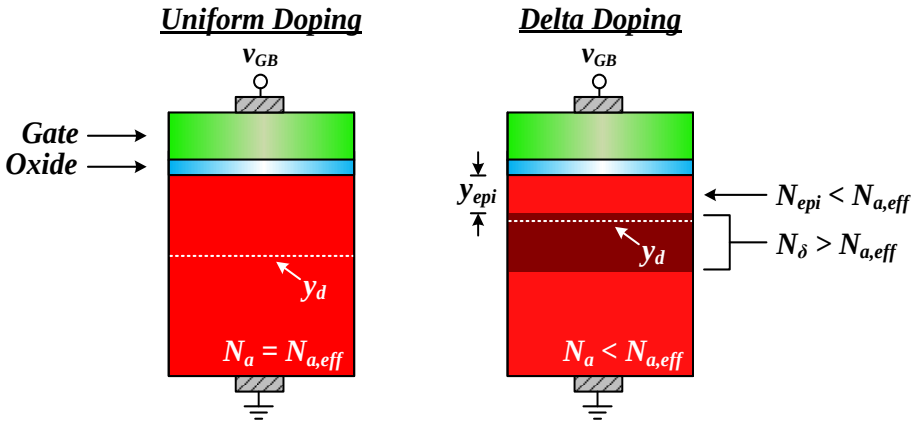


Figure 4.13: A 1-D illustration of how dopants are redistributed between the uniformly-doped and delta-doped profiles in order to obtain a smaller depletion depth at a constant value of $N_{a,eff}$.

Interestingly, Figure 4.12(a) and (b) also show that the bulk transconductances of the halo-implanted and uniformly-doped devices are relatively similar for $L_g \geq 5L_{g,min}$. This most likely occurs because the devices' threshold voltages are approximately equal at those gate lengths. For $L_g < 5L_{g,min}$, the halo-implanted device's heavily-doped halo

regions begin to occupy a larger portion of the channel causing the device's threshold voltage to increase, rather than decrease as in the uniformly-doped case. This causes the growth in the halo-implanted device's bulk transconductance to become suppressed as L_g shrinks since the reduction in its gate over-drive voltage ($V_{GS} - V_T$) negates any benefits brought about by a shorter L_g.

Moving forward, it is important to note that in general, halo-implanted MOSFETs are not desirable for analog applications since they suffer from long-channel DITS (drain-induced threshold shift) [177] (pp. 26–36). This long-channel DITS causes the output resistance of a halo-implanted MOSFET to be an order of magnitude lower than that of a uniformly-doped device for the gate lengths commonly used in analog circuits ($L_g \geq 5L_{g,min}$ [400 nm in a 90 nm process] [8]) [177] (pp. 26–36), which negatively influences the device's intrinsic gain. It is for this reason that halo implantation will no longer be considered throughout the remainder of this dissertation.

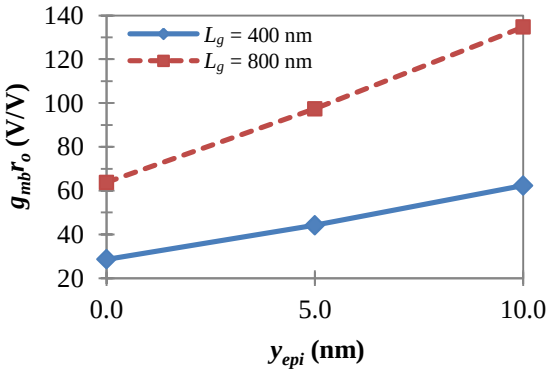


Figure 4.14: A plot of $g_{mb}r_o$ vs. y_{epi} at an L_g of 400 nm and 800 nm (V_{T0} = 0.37 V, V_{GS} = V_{DS} = 0.7 V, V_{BS} = 0 and $r_o \equiv [\partial I_D/\partial V_{DS}]^{-1}$).

The net effect of g_{mb} and r_o is displayed in Figure 4.14 where the intrinsic gain of a BD MOSFET is plotted against y_{epi} for two different gate lengths. Overall, one can see that the intrinsic gain of a BD MOSFET increases by as much as 110% if a delta-doped profile with a y_{epi} = 10 nm is chosen for the device rather than uniform doping.

Intriguingly, the above finding indicates that it is possible for the growth in $g_{mb}r_o$ to exceed that of g_{mb} itself. This additional growth in $g_{mb}r_o$ is attributed to the delta-doped profile's ability to improve a BD MOSFET's long-channel DITS and r_o characteristics [157] as y_{epi} becomes larger.

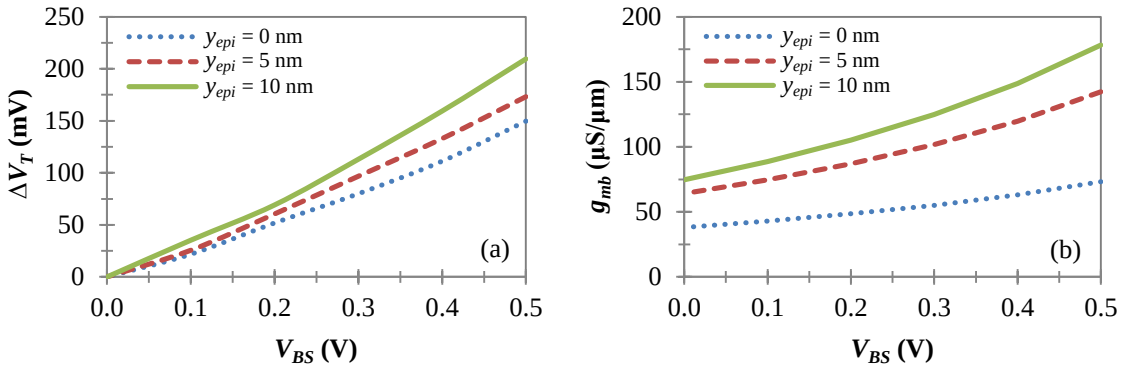


Figure 4.15: A plot of (a) ΔV_T and (b) g_{mb} vs. V_{BS} for three lightly-doped channel layer thicknesses (L_g = 400 nm, V_{GS} = V_{DS} = 0.7 V, V_{T0} = 0.37 V and $\Delta V_T = V_T|_{V_{BS}=0} - V_T$).

When operating a delta-doped BD MOSFET with a $V_{BS} > 0$, one can expect the boost in g_{mb} provided by the delta-doped profile to be larger than that observed in Figure 4.12(a) and (b) as a result of the doping profile's enhanced body effect [149]. This enhanced body effect – witnessed in Figure 4.15(a) – allows a delta-doped BD MOSFET's bulk transconductance to rise by as much as 138% at a y_{epi} = 10 nm if V_{BS} is increased from 0 to 0.5 V – as shown in Figure 4.15(b) – compared to only 92% in a uniformly-doped device.

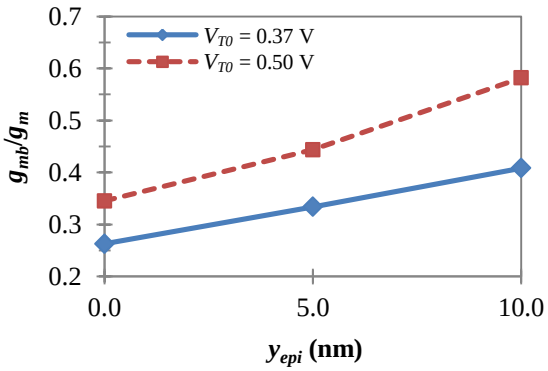


Figure 4.16: A plot of g_{mb}/g_m vs. y_{epi} at a V_{T0} of 0.37 V and 0.50 V (L_g = 400 nm, V_{GS} = V_{DS} = 0.7 V and V_{BS} = 0).

In addition to the benefits described so far, delta doping is also capable of strengthening the bulk terminal with respect to the gate – as seen in Figure 4.16 for a V_{T0} of 0.37 V and 0.50 V – since the doping profile ultimately increases the ratio of t_{ox}/y_d (*i.e.*, C_d/C_{ox}). Given this fact, one may argue that the long-channel threshold voltage – *i.e.*, the *effective* background doping concentration – of a BD MOSFET should be raised as much as possible since doing so would reduce the disparity between the device's bulk and gate transconductances through a supplementary growth in t_{ox}/y_d and would aid in reviving the expected advantages of bulk-driven circuitry in deca-nanometer technologies, as discussed in Section 3.5. Unfortunately, there are a couple of drawbacks to this design approach (besides the well-known consequence of a degraded drive current).

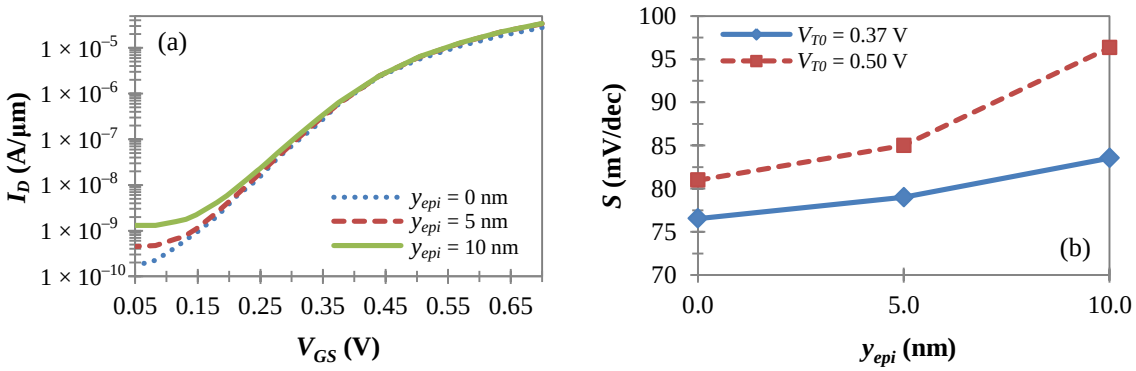


Figure 4.17: (a) A semi-logarithmic plot of I_D vs. V_{GS} for three lightly-doped channel layer thicknesses at a V_{T0} of 0.37 V and (b) a plot of S vs. y_{epi} at a V_{T0} of 0.37 V and 0.50 V (L_g = 400 nm, V_{DS} = 0.7 V and V_{BS} = 0).

In Figure 4.17(a), the sub-threshold behavior of a BD MOSFET is displayed through a semi-logarithmic plot of I_D vs. V_{GS} for three lightly-doped channel layer thicknesses at a V_{T0} of 0.37 V[†]. The extracted values of the device's sub-threshold swing, S, are plotted in Figure 4.17(b) along with similar data from a BD MOSFET with a

[†] The growth in off-state leakage current observed in Figure 4.17(a) occurs due to band-to-band tunneling (BTBT) between the source and drain regions of a BD MOSFET, and is caused by the higher N_δ that accompanies a larger y_{epi}.

V_{T0} = 0.50 V. From these figures, one can see that S rises by 9% between a y_{epi} of 0 nm and 10 nm at a V_{T0} of 0.37 V. The increase in S becomes more dramatic at a V_{T0} = 0.50 V – up to 19% – due to the bulk's growing influence over the channel, as predicted by the ideal definition of the sub-threshold swing [122] (pp. 314–315):

$$S \equiv \left[\frac{\partial \ln(I_D)}{\partial V_{GS}}\right]^{-1} = \frac{kT}{q}\ln(10)\left(1+\frac{C_d}{C_{ox}}\right) \approx (60\text{ mV/dec})\left(1+\frac{g_{mb}}{g_m}\right) \tag{4.27}$$

While a larger S is not overly detrimental to the performance of analog bulk-driven circuitry (since a BD MOSFET's gate is typically tied to a DC bias voltage), it will have negative implications for some RF applications which simultaneously utilize the bulk and gate terminals as device inputs [27], [103]–[114].

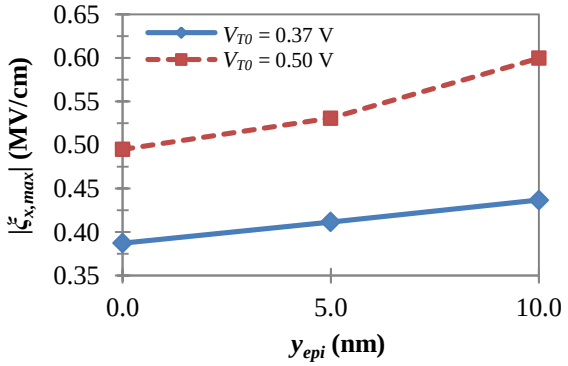


Figure 4.18: A plot of $|\xi_{x,max}|$ vs. y_{epi} at a V_{T0} of 0.37 V and 0.50 V (L_g = 400 nm, V_{GS} = V_{DS} = 0.7 V and V_{BS} = 0).

Along with the climb in S, a larger V_{T0} will also bring about a rapid increase in the magnitude of a BD MOSFET's maximum longitudinal field, $|\xi_{x,max}|$, as shown in Figure 4.18. For a V_{T0} of 0.37 V, $|\xi_{x,max}|$ turns out to be 13% higher if y_{epi} = 10 nm rather than 0 nm. However, when V_{T0} = 0.50 V, the growth in $|\xi_{x,max}|$ becomes 21%. Therefore, it is important to monitor $|\xi_{x,max}|$ if one is designing a high-V_{T0} delta-doped BD MOSFET since the device may experience a noticeable reduction in device lifetime as a result of elevated hot carrier activity near the drain.

As one would expect – based on (3.8) – delta doping's g_{mb}-related benefits do carry over to a BD MOSFET's frequency response, as confirmed by Figure 4.19(a) and (b) where $f_{T,BD}$, determined using Y parameters [178] (Ch. 6, pp. 18–19):

$$f_{T,BD} \equiv f\big|_{|Y_{21}/Y_{11}|=1} \tag{4.28}$$

is plotted against L_g for three lightly-doped channel layer thicknesses[†]. Figure 4.19(a) and (b) both show that a BD MOSFET's $f_{T,BD}$ can be enhanced by 37–50% for gate lengths ranging from 80 nm to 800 nm if one uses a delta-doped profile with a y_{epi} = 10 nm rather than uniform doping. However, the figures also indicate that the increase in $f_{T,BD}$ is less than that observed in Figure 4.12(a) and (b) for g_{mb}. This disparity is attributed to the higher N_δ of the delta-doped profile which negatively influences the extrinsic components of a BD MOSFET's bulk-to-source and bulk-to-drain capacitances, and thus the growth rate of $f_{T,BD}$ with respect to y_{epi}.

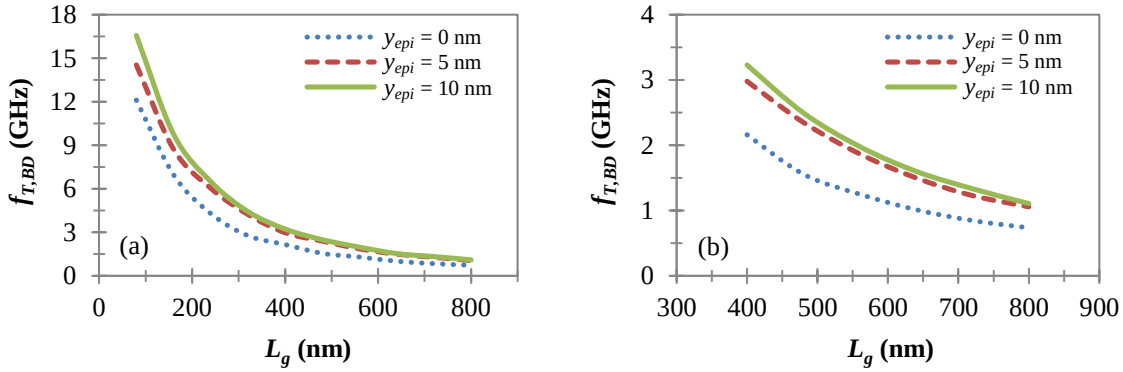


Figure 4.19: A plot of $f_{T,BD}$ vs. L_g for three lightly-doped channel layer thicknesses (V_{T0} = 0.37 V, V_{GS} = V_{DS} = 0.7 V and V_{BS} = 0) at gate lengths ranging from (a) 80 nm to 800 nm and (b) 400 nm to 800 nm.

To ensure that the delta-doped profile is able to maintain the improvements seen in Figure 4.12–Figure 4.19 at any given value of y_{epi}, it is necessary to keep the doping concentration of the profile's lightly-doped channel region sufficiently low to avoid

[†] This definition of $f_{T,BD}$ is equivalent to the one used in Section 3.1.4 since it results in finding the frequency at which the ratio of a BD MOSFET's output-to-input current is equal to one in magnitude under the condition that the device's output terminal is short-circuited.

significant mobility degradation due to ionized impurity scattering. Based on the data plotted in Figure 4.20, it is evident that N_{epi} must remain below 1×10^{17} cm^{-3} to preserve the integrity of the delta-doped profile.

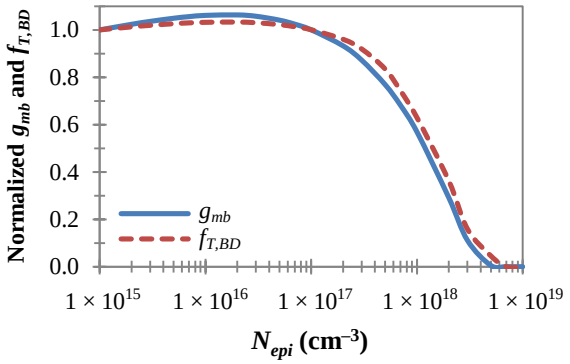


Figure 4.20: A semi-logarithmic plot of the normalized values of g_{mb} and $f_{T,BD}$ (referenced to g_{mb} and $f_{T,BD}$ at $N_{epi} = 1 \times 10^{15}$ cm^{-3}) vs. N_{epi} for a delta-doped *n*-type BD MOSFET with a y_{epi} = 10 nm (L_g = 80 nm, V_{T0} = 0.50 V, $V_{GS} = V_{DS}$ = 0.7 V and V_{BS} = 0).

At this time, it is appropriate to discount counter doping as a potential g_{mb} enhancement technique for deca-nanometer bulk CMOS technologies. The preceding statement is founded on the fact that it is necessary to insert a layer of *n*-type dopants into a delta-doped profile to create a counter-doped profile, as illustrated by Figure 4.1(d). Thus, if one wanted to achieve a V_{T0} equal to that of delta doping, one would have to raise N_{δ} to compensate for the drop in $N_{a,eff}$ caused by the inclusion of a counter-doped layer. Naturally, this increase in N_{δ} would need to be quite large in order to enhance g_{mb} considerably relative to the delta-doped case.

Unfortunately, for the representative technology considered in this section, N_{δ} is already equal to 3×10^{18} cm^{-3} in a delta-doped BD MOSFET with a y_{epi} = 10 nm. So, it is unlikely that a drastic growth in N_{δ} can be tolerated at a y_{epi} of 10 nm since the doping concentration of the delta-doped layer must remain below 1×10^{19} cm^{-3} in order to avoid noticeable BTBT-induced leakage between the device's source and drain regions [179]. As a result, if one were to create a counter-doped BD MOSFET in the same technology,

one would need to use a much smaller value of y_{epi} which would erode any potential improvement in g_{mb} that could be obtained by switching to a counter-doped profile.

4.4.4 Examination of the Deep Trench Isolation Scheme

To determine whether the DTI scheme depicted in Figure 4.3 and Figure 4.4 is capable of enhancing $f_{T,BD}$ to any significant degree, the *n*-type BD MOSFET setup discussed in Section 4.4.1 was modified to accommodate deep trenches between the device's p^+ *p*-well contacts and device's n^+ source and drain contacts [176]. The depths of the deep trenches were chosen to be 1.6 μm so that they would extend into a BD MOSFET's deep *n*-well region, but not all the way through to the *p*-type substrate, as suggested in Section 4.2. The widths of the deep trenches were selected to be the same as the widths of the shallow trenches used in the triple-well isolation scheme (0.42 μm) since the horizontal isolation requirements are the same for both isolation techniques.

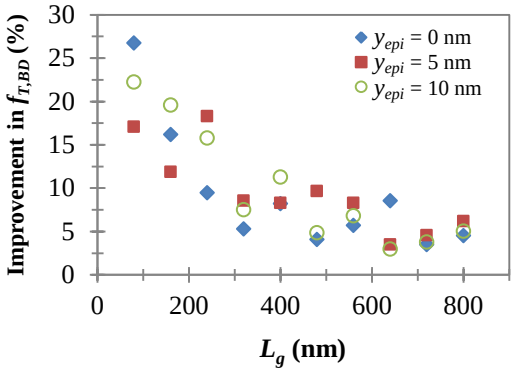


Figure 4.21: A plot of the improvement seen in $f_{T,BD}$ when DTI is used in place of triple-well isolation in uniformly-doped and delta-doped *n*-type BD MOSFETs (V_{T0} = 0.37 V, V_{GS} = V_{DS} = 0.7 V and V_{BS} = 0).

The improvement seen in $f_{T,BD}$ when DTI is used in place of triple-well isolation is plotted in Figure 4.21 for the uniformly-doped and delta-doped BD MOSFETs considered throughout Section 4.4.3. The figure shows that DTI is only capable of moderately increasing $f_{T,BD}$ at gate lengths near $L_{g,min}$. DTI is unable to provide any substantial benefit to $f_{T,BD}$ at longer gate lengths since the sidewall depletion capacitance removed by the DTI

structure becomes much smaller than the depletion capacitance at the bottom of a BD MOSFET's *p* well as L_g is made larger[†].

4.5 Conclusions

This chapter introduced several process changes which had the potential to improve the bulk transconductance and layout area requirements of a BD MOSFET. The potency of the most promising process changes were evaluated in ATLAS [38] using device parameters largely consistent with those found in standard 90 nm bulk CMOS processes and electrical device models which accounted for the dominant short-channel and quantum mechanical phenomena present in the aforementioned technologies. Based on the results obtained in this chapter, the following conclusions can be drawn [176]:

- Delta doping is the best candidate to enhance the bulk transconductance of a BD MOSFET because of its ability to reduce y_d through an increase in y_{epi} at a constant value of $N_{a,eff}$ and V_{T0}. By choosing a delta-doped profile over uniform doping, one can raise g_{mb} by as much as 105% for a y_{epi} = 10 nm and a V_{T0} = 0.37 V. This leads to an improvement in $g_{mb}r_o$ and $f_{T,BD}$ of up to 110% and 50%, respectively.
- The effectiveness of the delta-doped profile is limited by the doping concentration of its lightly-doped channel region. To preserve the integrity of the doping profile at any given value of y_{epi}, one must ensure that N_{epi} remains below 1×10^{17} cm^{-3} in order to avoid an excessive amount of ionized impurity scattering in the channel.
- It is possible to raise a delta-doped BD MOSFET's V_{T0} to acquire a better g_{mb}/g_m ratio. However, it is unlikely that V_{T0} can be raised high enough to restore the expected advantages of bulk-driven circuitry in deca-nanometer technologies since a sizable growth in V_{T0} will be met with noticeable degradation in I_D, S and $|\xi_{x,max}|$ which may not be acceptable for all BD MOSFET applications.

[†] In a physical (*i.e.*, 3-D) implementation of a BD MOSFET, the improvement in $f_{T,BD}$ should be greater than that predicted in Figure 4.21 since a 2-D device simulator cannot account for the triple-well structure's sidewall depletion capacitance present along the length of the device in the *x*–*y* plane.

- By replacing a triple-well isolation scheme with DTI, it is possible to reduce the *effective* layout area of an *n*-type BD MOSFET by approximately 53% in a deca-nanometer bulk CMOS process since DTI is able to eliminate the well-to-well spacing requirements between adjacent BD MOSFETs of the same type.
- The improvement seen in $f_{T,BD}$ when DTI is used in place of triple-well isolation is fairly minor unless a BD MOSFET's gate length is sufficiently close to $L_{g,min}$ because the sidewall depletion capacitance removed by the DTI structure represents only a small portion of the total well capacitance as L_g is made larger.

Using the knowledge acquired in this chapter, it is now possible to move forward and create a BD MOSFET whose performance has been optimized for use within deca-nanometer bulk CMOS technologies. With the aid of 2-D device simulations in ATLAS, the design of such a device will be carried out in Chapter 5 using a standard 90 nm bulk CMOS process.

5 Designing a Superior Bulk-Driven MOSFET

5.1 Device Design Approach

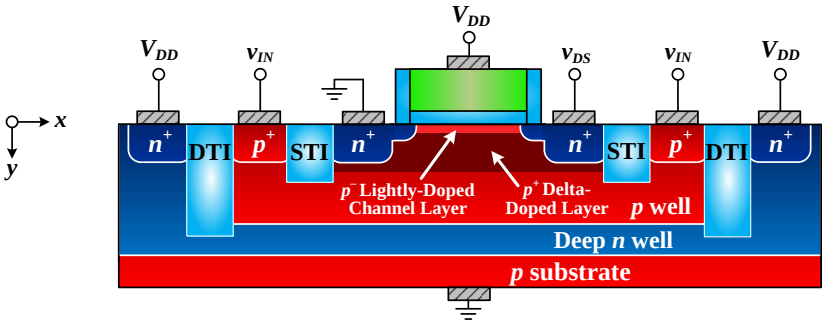


Figure 5.1: An illustration of the deep-trench-isolated delta-doped *n*-type BD MOSFET device cross-section considered throughout Chapter 5.

In Chapter 4, delta doping and DTI were identified as the best candidates to mitigate the major disadvantages of a BD MOSFET. To completely understand the benefits of these process changes, it is necessary to see how they influence the performance of a BD MOSFET in a practical design setting. To accomplish this task, the insight gained from Chapter 4 and the first three chapters of this dissertation were utilized to design a deep-trench-isolated delta-doped (DD) *n*-type BD MOSFET [180] in a standard 90 nm bulk CMOS technology using a $V_{DD} = 0.7$ V [8], ATLAS [38] and the device cross-section illustrated in Figure 5.1[†].

To provide a reference for the delta-doped BD MOSFET design and the results that follow, a triple-well-isolated uniformly-doped (UD) *n*-type BD MOSFET was designated as a control device. The uniformly-doped BD MOSFET's device specifications were selected to be entirely consistent with those of a standard 90 nm bulk CMOS technology [6] such that the device had a $t_{ox} = 1.4$ nm, a $V_{T0} = 0.37$ V, a $y_{epi} = 0$ nm and an $N_\delta = 1.75 \times 10^{18}$ cm^{-3} ($y_{epi2} - y_{epi} = 100$ nm). A full listing of the uniformly-doped BD MOSFET's device parameters can be found in Table 5.1.

[†] The ATLAS code, DBINTERNAL [173] (App. B, pp. 1–14) code and calibration parameters from Section 4.4 were used to generate all the data contained in this chapter.

Table 5.1: A list of the device parameters that were used in the triple-well-isolated uniformly-doped control device for a standard 90 nm bulk CMOS technology.

Device Parameter Description	Directionality	Value
Minimum Gate Length	*x*	80 nm
Long-Channel Threshold Voltage	–	0.37 V
SiO_2 Gate Oxide Thickness	*y*	1.4 nm
p^- Lightly-Doped Channel Layer Doping Concentration	–	1×10^{15} cm^{-3}
p^- Lightly-Doped Channel Layer Thickness	*y*	0 nm
p^+ Delta-Doped Layer Doping Concentration	–	1.75×10^{18} cm^{-3}
p^+ Delta-Doped Layer Thickness	*y*	100 nm
n^+ Polysilicon Gate Doping Concentration	–	1×10^{20} cm^{-3}
n^+ Polysilicon Gate Height	*y*	150 nm
SiO_2 Spacer Width	*x*	15 nm
p-Well Doping Concentration	–	1×10^{16} cm^{-3}
p-Well Depth	*y*	1.5 μm
Deep *n*-Well Doping Concentration	–	1×10^{17} cm^{-3}
Deep *n*-Well Depth	*y*	2.0 μm
p-Substrate Doping Concentration	–	1×10^{16} cm^{-3}
Source, Drain, *p*-Well and Deep *n*-Well Contact Doping Concentration	–	1×10^{20} cm^{-3}
Source, Drain, *p*-Well and Deep *n*-Well Contact Lateral Abruptness	*x*	4.8 nm/dec
Source, Drain, *p*-Well and Deep *n*-Well Contact Junction Depth	*y*	30 nm
Source, Drain, *p*-Well and Deep *n*-Well Contact Width	*x*	200 nm
Source/Drain Extension Doping Concentration	–	2×10^{19} cm^{-3}
Source/Drain Extension Lateral Abruptness	*x*	4.8 nm/dec
Source/Drain Extension Junction Depth	*y*	25 nm
SiO_2 STI Depth	*y*	0.42 μm
SiO_2 STI Width	*x*	0.42 μm

Using the uniformly-doped control device as a starting point, the design of the delta-doped BD MOSFET began by taking advantage of the relaxed gate oxide scaling requirements of the bulk-driven configuration – as discussed in Section 3.4 – to increase t_{ox} from its nominal value of 1.4 nm to 1.8 nm. By making this change in t_{ox}, it was possible to reduce the new design's direct-tunneling-induced gate current density by a factor of 50 while giving up approximately 17% of g_{mb}.

With a gate oxide thickness selected, the design process continued by choosing a y_{epi} and N_δ for the delta-doped BD MOSFET. Based on the data plotted in Figure 4.12

(from Section 4.4.3), it was evident that y_{epi} had to be made as thick as possible to yield the highest g_{mb}. Theoretically, this value of y_{epi} would have been located at a $y_{epi} \approx y_d$ since $N_\delta \rightarrow \infty$ as $(y_d - y_{epi}) \rightarrow 0$. However, due to BTBT concerns [179], y_{epi} was unable to aggressively approach y_d since N_δ was restricted to doping concentrations below 1×10^{19} cm^{-3}. Ultimately, it was determined that at a $V_{T0} = 0.37$ V, y_{epi} could not exceed 12 nm. So, that value of y_{epi} was chosen for the delta-doped BD MOSFET design, resulting in an $N_\delta = 4 \times 10^{18}$ cm^{-3}. But, given that g_{mb} was not at its peak value for an $N_\delta = 4 \times 10^{18}$ cm^{-3} – see Figure 5.2 – it was decided that N_δ should be increased to 6×10^{18} cm^{-3} in order to maximize g_{mb}[†]. As a by-product of this design choice, the delta-doped BD MOSFET's V_{T0} shifted slightly from 0.37 V to 0.41 V.

To complete the design of the delta-doped BD MOSFET, it was necessary to choose a width and depth for the deep trenches used in the device's DTI structure. Given that the design rules and well dimensions utilized in this design process were the same as those considered throughout Section 4.4, the delta-doped design's deep trench widths and depths turned out to be identical to those employed within Section 4.4.4 – *i.e.*, 0.42 μm and 1.6 μm, respectively.

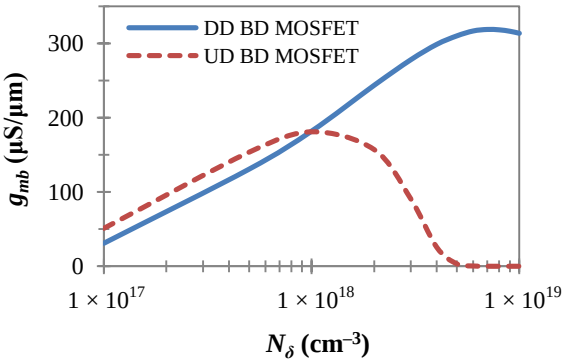


Figure 5.2: A semi-logarithmic plot of g_{mb} vs. N_δ for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (L_g = 80 nm, V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0).

[†] Recall that one of the main conclusions from Chapter 4 was that one is allowed to judiciously raise V_{T0} in order to improve a BD MOSFET's performance as long as the increase in V_{T0} does not significantly degrade parameters such as I_D, S and $|\xi_{x,max}|$.

5.2 Device Design Results

g_{mb} and g_{mb}/g_m are plotted against L_g in Figure 5.3(a) and (b) for the delta-doped and uniformly-doped BD MOSFET designs described in Section 5.1. From the figures, one can see that the new delta-doped design is capable of boosting g_{mb} and g_{mb}/g_m by as much as 113% each[†‡]. Along with these enhancements in g_{mb} and g_{mb}/g_m, Figure 5.4(a) shows that the delta-doped BD MOSFET design is also capable of raising $g_{mb}r_o$ by up to 429%. This growth in $g_{mb}r_o$ is obviously much greater than that of g_{mb}, itself, and is attributed to the new design's delta-doped profile and larger t_{ox} which cause r_o to climb appreciably – see Figure 5.4(b) – in response to the new design's lower long-channel DITS [157] and smaller drain current (recall that $r_o \propto I_D^{-1}$ based on long-channel theory).

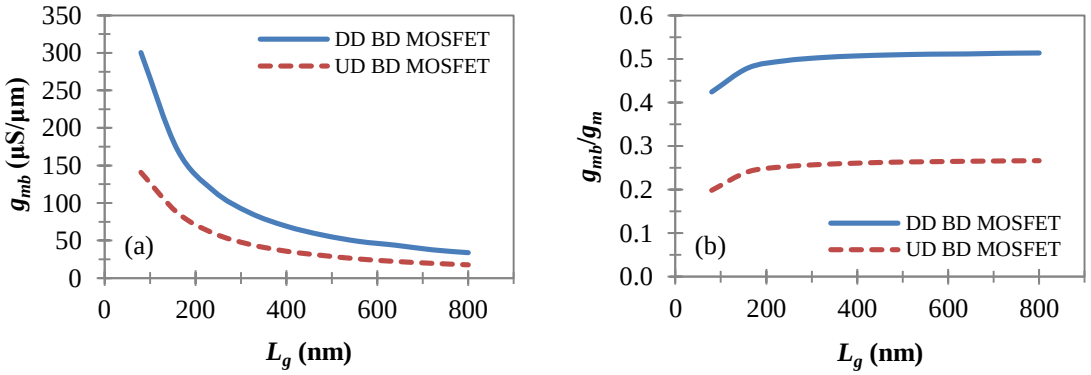


Figure 5.3: A plot of (a) g_{mb} and (b) g_{mb}/g_m vs. L_g for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0).

While the improvements seen in g_{mb}, g_{mb}/g_m and $g_{mb}r_o$ are all quite impressive, the delta-doped BD MOSFET design's smaller drain current – witnessed in Figure 5.5 – can be cited as a reason to reassess the advantage of increasing t_{ox} by 0.4 nm in the proposed design approach since I_D can be as much as 20% lower in the delta-doped case at a

[†] The delta-doped design's gate transconductance turns out to be approximately equal to that of the uniformly-doped control device since the delta-doped design has a higher surface mobility which is able to compensate for the loss in g_m brought about by its thicker t_{ox}.

[‡] As a result of the increase in g_{mb}/g_m, one will see S climb by 16.3 mV/dec to reach 92.8 mV/dec in the delta-doped design when L_g = 400 nm, V_{DS} = 0.7 V and V_{BS} = 0. In addition to this growth in S, one will see $|\xi_{x,max}|$ rise by 0.08 MV/cm to wind up at 0.51 MV/cm in the delta-doped design when L_g = 400 nm, $V_{GS} = V_{DS}$ = 0.7 V and V_{BS} = 0.

V_{BS} = 0. However, given that bulk-driven applications generally require V_{BS} to be greater than zero (for an *n*-type device), the degraded drain current seen at V_{BS} = 0 should not be regarded as a significant concern since the delta-doped design's enhanced body effect allows the design's I_D to become greater than that of its uniformly-doped counterpart when V_{BS} exceeds a certain threshold, as observed in Figure 5.6(a) and (b).

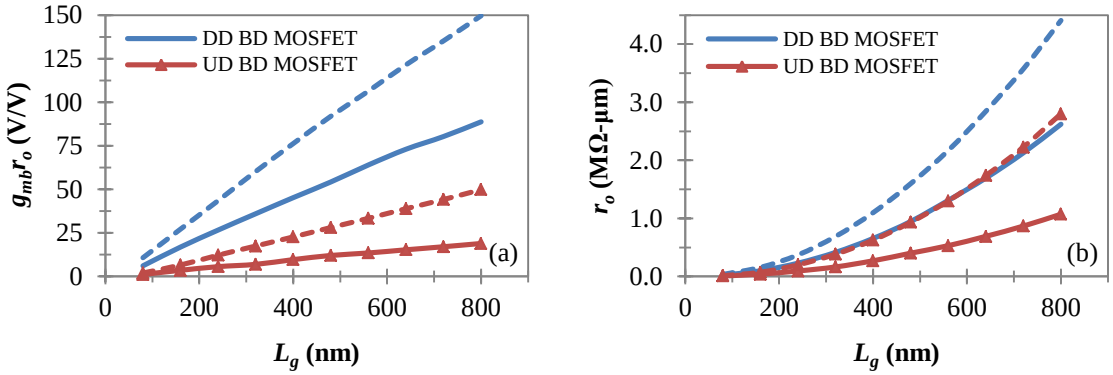


Figure 5.4: A plot of (a) $g_{mb}r_o$ and (b) r_o vs. L_g for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (V_{GS} = 0.7 V and V_{BS} = 0; V_{DS} = 0.4 V [solid lines] and 0.5 V [dashed lines]).

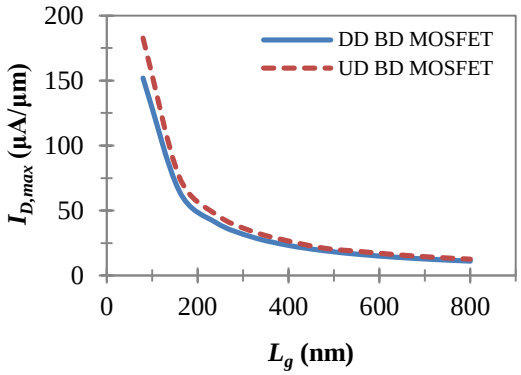


Figure 5.5: A plot of the maximum drain current, $I_{D,max} \equiv I_D$ at V_{GS} = V_{DS} = 0.7 V, vs. L_g for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (V_{BS} = 0).

Another benefit of the delta-doped BD MOSFET design is illustrated in Figure 5.7 where the design's normalized g_{mb}/g_m ratio is plotted against L_g along with similar data from the uniformly-doped control device. Interestingly, Figure 5.7 reveals that the roll-off characteristics of g_{mb}/g_m are superior in the delta-doped case. This behavior is credited to the delta-doped design's stronger bulk terminal which is able to weaken the influence of source/drain charge sharing as L_g shrinks. Naturally, since one

of the main objectives of this dissertation was to mitigate the disparity between g_{mb} and g_m, one would want to avoid using gate lengths within g_{mb}/g_m's roll-off region. Therefore, if one were to (arbitrarily) require the normalized g_{mb}/g_m ratio to remain above 0.95, Figure 5.7 suggests that it would be possible to reduce a BD MOSFET's minimum allowable gate length by about 50 nm by utilizing the delta-doped design[†].

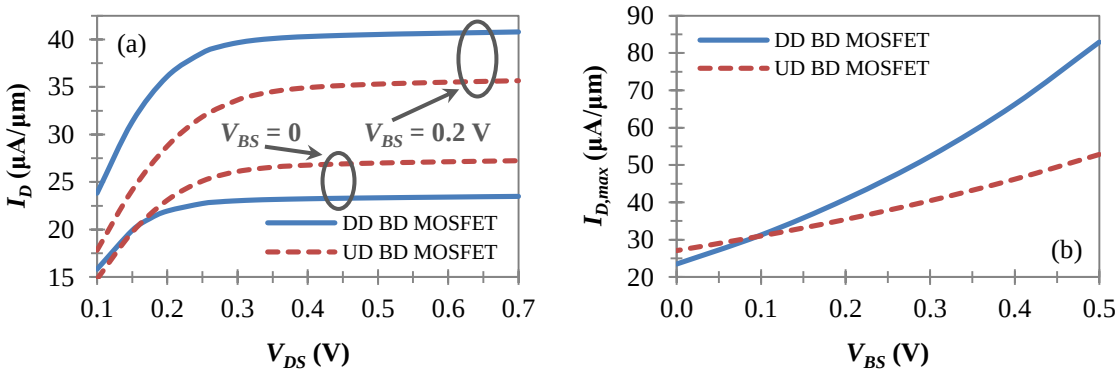


Figure 5.6: (a) A plot of I_D vs. V_{DS} for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (V_{GS} = 0.7 V and L_g = 400 nm) and (b) a plot of $I_{D,max}$ vs. V_{BS} for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (L_g = 400 nm and V_{GS} = V_{DS} = 0.7 V).

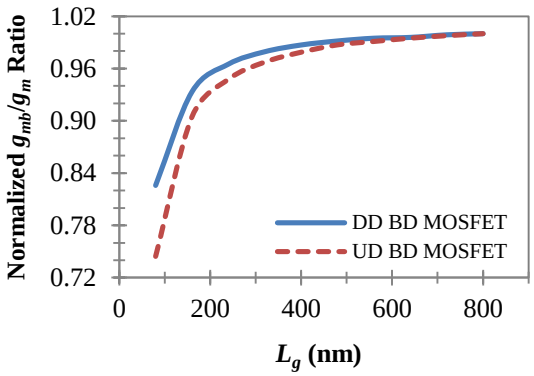


Figure 5.7: A plot of the normalized g_{mb}/g_m ratio (referenced to g_{mb}/g_m at L_g = 800 nm) vs. L_g for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0).

The frequency responses of the delta-doped and uniformly-doped BD MOSFET designs are studied in Figure 5.8(a). The figure shows that the $f_{T,BD}$ of a BD MOSFET can be enhanced by as much as 71% if one follows the design approach outlined in Section 5.1. As one would expect, the bulk of $f_{T,BD}$'s improvement occurs as a result of

[†] Figure 5.7 also suggests that the delta-doped design will be able to reduce a BD MOSFET's minimum allowable gate length by about 50 nm regardless of the threshold that one sets for the normalized g_{mb}/g_m ratio.

the delta-doped design's larger g_{mb}/g_m ratio. This is confirmed by Figure 5.8(b) where $f_{T,BD}/f_{T,GD}$ is observed to rise by as much as 34%. Notably, the growth seen in $f_{T,BD}$ is less than that of g_{mb} (refer to Figure 5.3(a)) because the total input capacitance of the delta-doped design – denoted as $C_{in,bulk}$ in Figure 5.9(a) – turns out to be as much as 40% greater than the total input capacitance of its uniformly-doped counterpart. This increase in $C_{in,bulk}$ is attributed to the new design's higher N_δ which causes the bulk-to-source and bulk-to-drain capacitances of the new design to swell noticeably, as seen in Figure 5.9(b). However, it is important to note that the growth in $C_{in,bulk}$ is slightly dampened by the reduction of C_{PW-DNW} – also witnessed in Figure 5.9(b) – that is brought about by the delta-doped design's DTI structure.

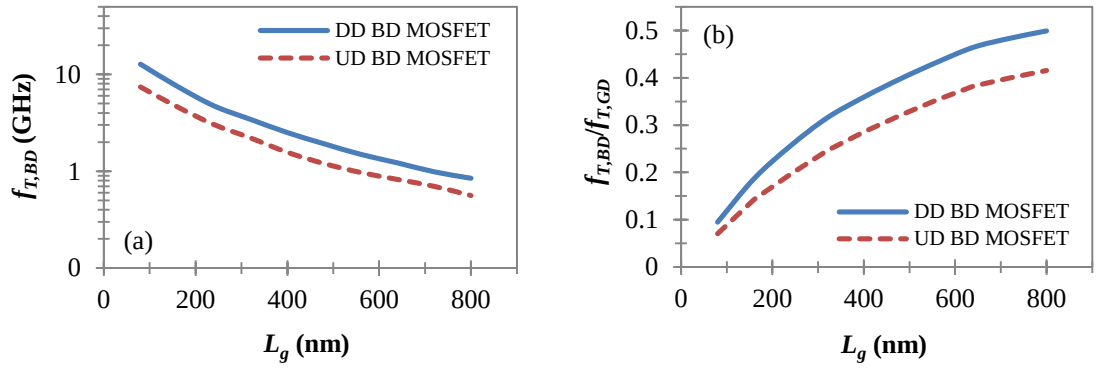


Figure 5.8: (a) A semi-logarithmic plot of $f_{T,BD}$ vs. L_g and (b) a plot of $f_{T,BD}/f_{T,GD}$ vs. L_g for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0).

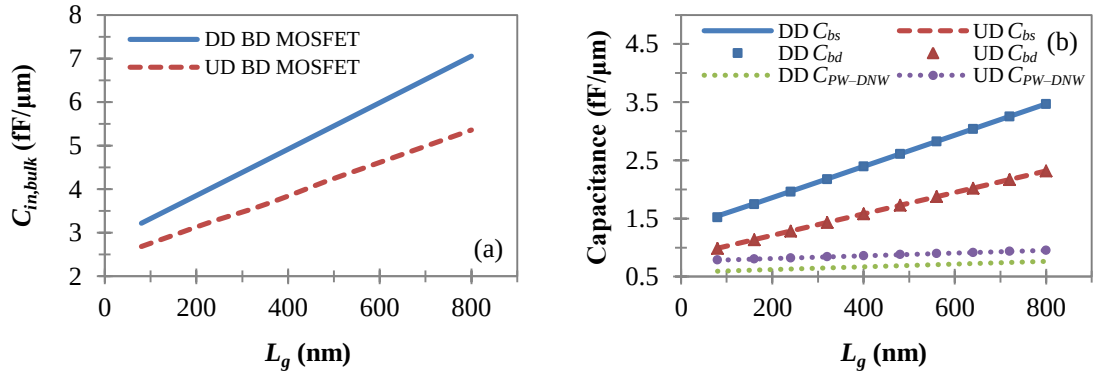


Figure 5.9: (a) A plot of the total input capacitance, $C_{in,bulk} = C_{PW-DNW} + C_{bs} + C_{bd} + C_{bg}$, vs. L_g for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0) and (b) a plot of the uniformly-doped and delta-doped *n*-type BD MOSFETs' dominant capacitive components (C_{PW-DNW}, C_{bs} and C_{bd}) vs. L_g (V_{GS} = 0.7 V, V_{DS} = 0.01 V and V_{BS} = 0).

Figure 5.10(a) and (b) depict the behavior of g_{mb} and g_{mb}/g_m against V_{BS} for the delta-doped and uniformly-doped BD MOSFET designs. Overall, the figures show that g_{mb} and g_{mb}/g_m will be able to grow by 161% and 36%, respectively, in the delta-doped design if V_{BS} is increased from 0 to 0.5 V, compared to 94% and 36%, respectively, in the uniformly-doped case[†].

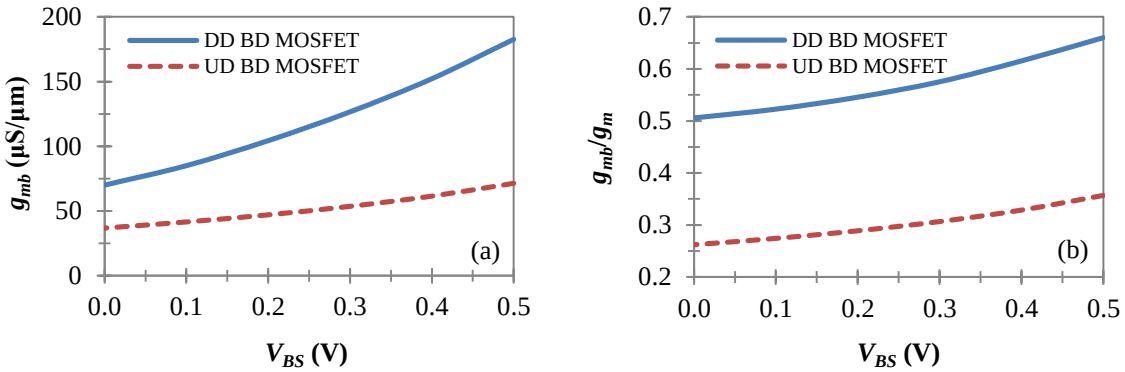


Figure 5.10: A plot of (a) g_{mb} and (b) g_{mb}/g_m vs. V_{BS} for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (L_g = 400 nm and V_{GS} = V_{DS} = 0.7 V).

Figure 5.11 and Figure 5.12 examine the consequences of process variations. In the figures, the deviations in g_{mb} and g_m:

$$\frac{|\Delta g_{mb}|}{g_{mb,nom}} \equiv \frac{|g_{mb} - g_{mb,nom}|}{g_{mb,nom}} \equiv \frac{\left|g_{mb} - \left(g_{mb}\big|_{\Delta N_\delta = 0,\ \Delta y_{epi} = 0}\right)\right|}{g_{mb}\big|_{\Delta N_\delta = 0,\ \Delta y_{epi} = 0}} \tag{5.1}$$

$$\frac{|\Delta g_{m}|}{g_{m,nom}} \equiv \frac{|g_{m} - g_{m,nom}|}{g_{m,nom}} \equiv \frac{\left|g_{m} - \left(g_{m}\big|_{\Delta N_\delta = 0,\ \Delta y_{epi} = 0}\right)\right|}{g_{m}\big|_{\Delta N_\delta = 0,\ \Delta y_{epi} = 0}} \tag{5.2}$$

induced by variations in N_δ and y_{epi} are plotted against:

$$\frac{\Delta N_\delta}{N_{\delta,nom}} \equiv \frac{N_\delta - N_{\delta,nom}}{N_{\delta,nom}} \tag{5.3}$$

and:

$$\Delta y_{epi} \equiv y_{epi} - y_{epi,nom} \tag{5.4}$$

[†] g_{mb}/g_m is enhanced by the same amount in the uniformly-doped and delta-doped designs because the body effect is equally beneficial to both g_{mb} and g_m regardless of how strong the bulk terminal becomes.

where $N_{\delta,nom}$ and $y_{epi,nom}$ are defined as the nominal values of N_δ and y_{epi} used within the uniformly-doped and delta-doped BD MOSFET designs.

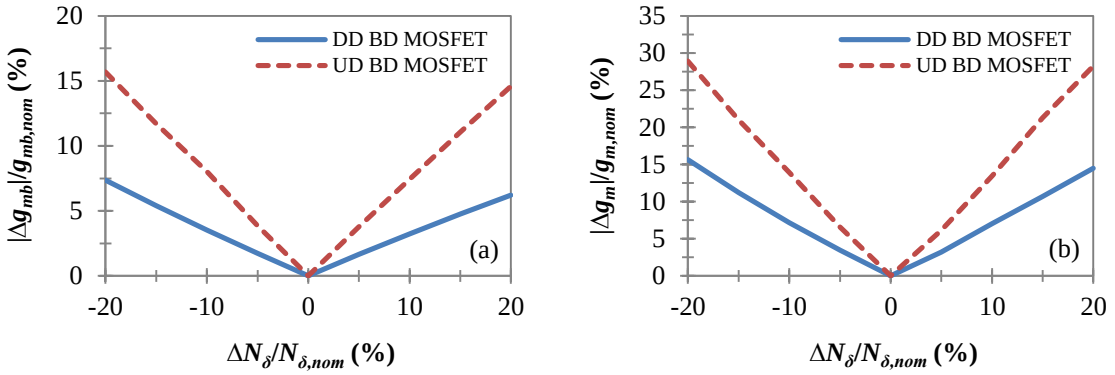


Figure 5.11: A plot of (a) $|\Delta g_{mb}|/g_{mb,nom}$ and (b) $|\Delta g_m|/g_{m,nom}$ vs. $\Delta N_\delta/N_{\delta,nom}$ for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (L_g = 800 nm, V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0).

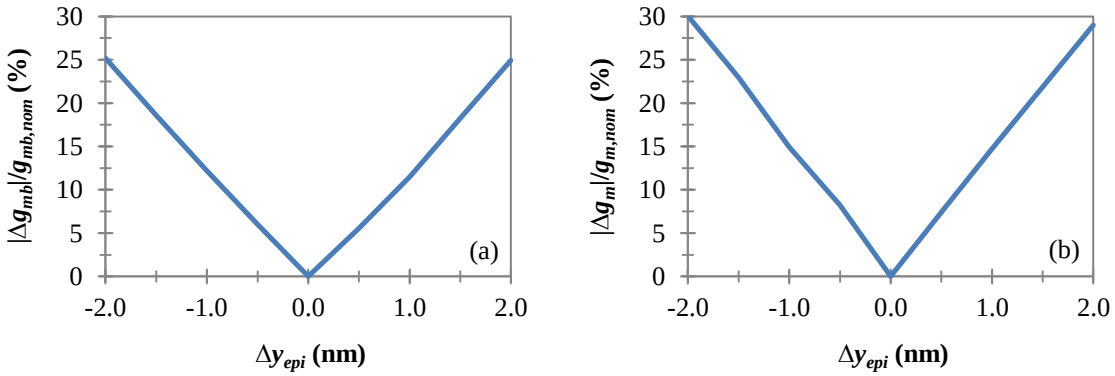


Figure 5.12: A plot of (a) $|\Delta g_{mb}|/g_{mb,nom}$ and (b) $|\Delta g_m|/g_{m,nom}$ vs. Δy_{epi} for the delta-doped *n*-type BD MOSFET design (L_g = 800 nm, V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0).

From Figure 5.11 and Figure 5.12, three intriguing observations can be made. First, g_{mb} and g_m are less susceptible to variations in N_δ in the delta-doped case. This is a direct result of the new design's doping profile which is able to suppress random dopant fluctuation-induced deviations in V_T [181]. Second, compared to g_m, g_{mb} is not as vulnerable to variations in N_δ. This behavior is attributed to the fact that g_{mb} nominally resides near its peak value – refer back to Figure 5.2 – for the designs considered in this chapter while g_m does not, meaning that g_m's rate of change is generally greater than g_{mb}'s with respect to N_δ. Third, while g_{mb} will not fluctuate as much as g_m does when y_{epi} varies, g_{mb}'s immunity to process variations will be severely weakened in such a scenario

since its nominal position near the peak of a g_{mb}–N_δ characteristic is not overly beneficial if $\Delta y_{epi} \neq 0$[†].

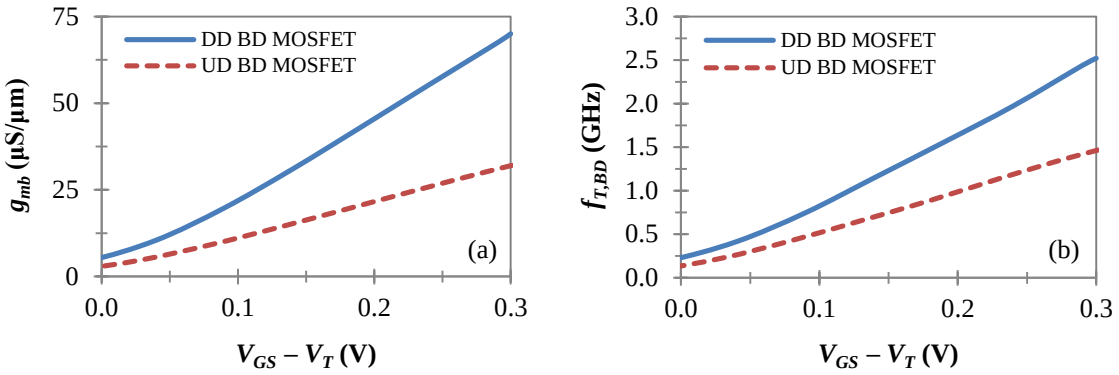


Figure 5.13: A plot of (a) g_{mb} and (b) $f_{T,BD}$ vs. $V_{GS} - V_T$ for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (L_g = 400 nm, V_{DS} = 0.4 V and V_{BS} = 0).

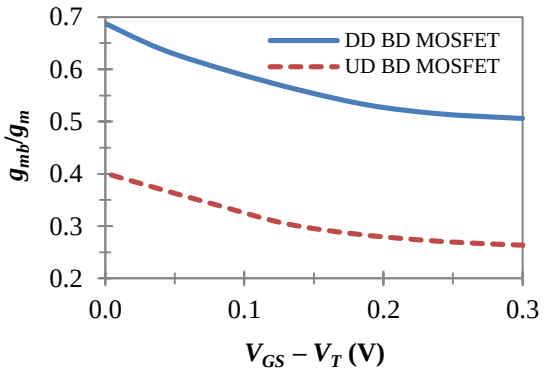


Figure 5.14: A plot of g_{mb}/g_m vs. $V_{GS} - V_T$ for the uniformly-doped and delta-doped *n*-type BD MOSFET designs (L_g = 400 nm, V_{DS} = 0.4 V and V_{BS} = 0).

Up to this point, a majority of the analysis performed on the delta-doped BD MOSFET design has been carried out at a $V_{DD} = 0.7$ V to examine the design's performance at the minimum power supply voltage predicted for the end of bulk CMOS scaling [8]. To provide completeness to this section's investigation, the delta-doped design's key parameters are plotted against the gate over-drive voltage in Figure 5.13 and Figure 5.14 along with similar data from the uniformly-doped control device. Ultimately, the figures show that g_{mb}, g_{mb}/g_m and $f_{T,BD}$ will always be greater in the delta-doped design. In fact, it turns out that the improvement seen in these parameters will be

[†] The same is true for the instances in which L_g and/or t_{ox} vary.

relatively constant with respect to the gate over-drive voltage. Interestingly, Figure 5.14 also reveals that g_{mb}/g_m will increase as the gate over-drive voltage is lowered, reaching a maximum of 0.690 at the edge of moderate inversion in the delta-doped design.

5.3 Differential Amplifier Example

To demonstrate the benefits of the delta-doped BD MOSFET design at the circuit level, the design was placed within a differential amplifier structure – shown in Figure 5.15 [180] – using ATLAS' circuit simulator, MIXEDMODE[†] [38] (Ch. 12, pp. 1–50). The differential amplifier was designed to have an I_{BIAS} = 40 μA at a V_{DD} = 0.7 V and its load devices, M_3 and M_4, were modeled by a current source equal to $I_{BIAS}/2$ in parallel with an output resistance of 250 kΩ to serve as a representative load for the amplifier.

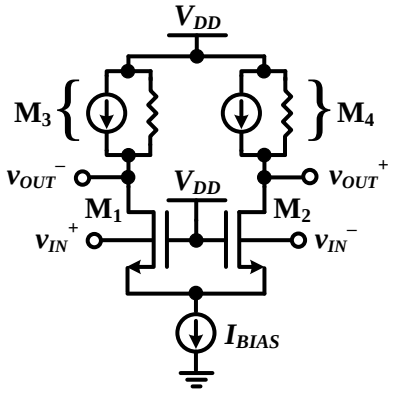


Figure 5.15: A schematic representation of the bulk-driven differential amplifier structure created in MIXEDMODE to demonstrate the benefits of the delta-doped *n*-type BD MOSFET design at the circuit level.

An exemplary plot of the differential amplifier's small-signal voltage gain, A_v, is presented in Figure 5.16. The results show that the delta-doped BD MOSFET design is capable of boosting the differential amplifier's DC gain by over 185% when the amplifier's input voltage is centered around the middle of the power supply [182] (pp. 417, 420–423).

[†] The MIXEDMODE codes used to generate the data contained within Figure 5.16 and Figure 5.17 can be found in the Appendix starting on page 118 and 122, respectively.

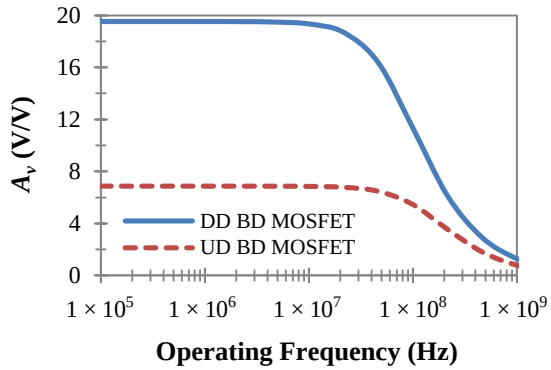


Figure 5.16: A semi-logarithmic plot of A_v vs. operating frequency for the differential amplifier designs utilizing uniformly-doped and delta-doped *n*-type BD MOSFETs (L_g = 400 nm and $v_{IN} = v_{in} + 0.35$ V).

The V_{BS} values of the differential amplifier's input devices are plotted in Figure 5.17 against the amplifier's input common-mode voltage[†]. The figure illustrates that the delta-doped BD MOSFET design is capable of moderately lowering V_{BS1} and V_{BS2} at the positive boundary of the differential amplifier's ICMR. This reduction in V_{BS1} and V_{BS2} is credited to the delta-doped design's enhanced body effect which permits the source voltages of M_1 and M_2 to track V_{IN} more aggressively[‡] and is expected to become increasingly beneficial in applications with smaller nominal V_{T0}/V_{DD} ratios (refer to Section 3.5) since it will aid in keeping V_{BS1} and V_{BS2} away from their conservative upper limit of 0.6 V [25].

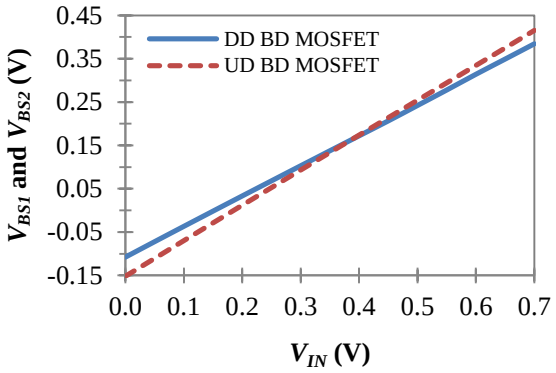


Figure 5.17: A plot of V_{BS1} and V_{BS2} ($V_{BS1} = V_{BS2}$) vs. V_{IN} for the differential amplifier designs utilizing uniformly-doped and delta-doped *n*-type BD MOSFETs (L_g = 400 nm and V_{LOAD} = 0.3 V).

[†] To collect the data for Figure 5.17, M_3 and M_4 were replaced with voltage sources – named V_{LOAD} and equal to 0.3 V – to ensure that an adequate voltage was dropped across the amplifier's load [26] (pp. 59–63).

[‡] Recall that smaller values of V_{GS1} and V_{GS2} are required to maintain a current level of $I_{BIAS}/2$ through M_1 and M_2 when the threshold voltages of M_1 and M_2 decrease.

5.4 Summary of Key Results

This chapter has presented the design of a deep-trench-isolated delta-doped *n*-type BD MOSFET optimized for use within deca-nanometer bulk CMOS technologies[†] and low-voltage analog applications operating at a V_{DD} = 0.7 V, the minimum power supply voltage predicted for the end of bulk CMOS scaling [8]. A summary of the process changes that were implemented to create the delta-doped design are provided below in Table 5.2 for a standard 90 nm bulk CMOS process. A list of the delta-doped design's key results – obtained from ATLAS [38] – are also given in Table 5.3 and Table 5.4 for gate lengths of 400 nm and 800 nm, respectively, along with reference values from the triple-well-isolated uniformly-doped control device described in Section 5.1 [180].

Table 5.2: A summary of the process changes that were implemented to create an optimized *n*-type BD MOSFET in a standard 90 nm bulk CMOS technology.

Parameter	UD BD MOSFET	DD BD MOSFET
t_{ox}	1.4 nm	1.8 nm
N_δ	1.75×10^{18} cm^{-3}	6×10^{18} cm^{-3}
y_{epi}	0 nm	12 nm
V_{T0}	0.37 V	0.41 V
STI/DTI Width	0.42 µm	0.42 µm
STI/DTI Depth	0.42 µm	1.6 µm

Table 5.3: A summary of the key results for the uniformly-doped and delta-doped *n*-type BD MOSFET designs considered in Chapter 5 (L_g = 400 nm, V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0).

Parameter	UD BD MOSFET	DD BD MOSFET	Change
g_{mb}	35.78 µS/µm	69.09 µS/µm	+93.1%
g_{mb}/g_m	0.261	0.507	+94.4%
$g_{mb}r_o$	9.7 V/V	45.3 V/V	+366.8%
I_D	26.60 µA/µm	23.24 µA/µm	–12.7%
$f_{T,BD}$	1.57 GHz	2.51 GHz	+59.9%
$f_{T,BD}/f_{T,GD}$	0.286	0.359	+25.6%
$C_{in,bulk}$[‡]	4.08 fF/µm	5.60 fF/µm	+37.3%

[†] The design approach outlined in Section 5.1 should be equally applicable to a *p*-type BD MOSFET destined for use within a similar technology since a *p*-type device would utilize a degenerately-doped p^+ polysilicon gate [183] which would make the native V_{T0} of the device complementary to that of an *n*-type BD MOSFET.

[‡] The $C_{in,bulk}$ values listed in Table 5.3 and Table 5.4 were obtained at a V_{GS} = 0.7 V, V_{DS} = 0.01 V and V_{BS} = 0.

Table 5.4: A summary of the key results for the uniformly-doped and delta-doped *n*-type BD MOSFET designs considered in Chapter 5 (L_g = 800 nm, V_{GS} = 0.7 V, V_{DS} = 0.4 V and V_{BS} = 0).

Parameter	UD BD MOSFET	DD BD MOSFET	Change
g_{mb}	17.67 μS/μm	33.86 μS/μm	+91.6%
g_{mb}/g_m	0.266	0.513	+92.7%
$g_{mb}r_o$	19.0 V/V	88.8 V/V	+368.4%
I_D	12.65 μA/μm	11.11 μA/μm	–12.2%
$f_{T,BD}$	0.56 GHz	0.86 GHz	+53.8%
$f_{T,BD}/f_{T,GD}$	0.415	0.499	+20.1%
$C_{in,bulk}$	5.73 fF/μm	8.01 fF/μm	+39.9%

6 Conclusions

6.1 Final Remarks on the Bulk-Driven Technique

Based on the results presented in Chapter 4 and Chapter 5, it is clear that the performance of a BD MOSFET can be substantially improved if one incorporates delta doping and DTI into the design of the device. However, since the delta-doped BD MOSFET design proposed in Section 5.1 was unable to make g_{mb} comparable to g_m in a standard 90 nm bulk CMOS process, it is unlikely that the new design approach will permit the bulk-driven technique to become viable as a general solution to low-voltage analog design since g_{mb}/g_m should continually decline as one moves beyond the 90 nm node (based on the findings of Section 3.3). This belief is confirmed by process scaling simulations performed in ATLAS [38] using the new delta-doped design approach[†], the results of which are given in Table 6.1. The table shows that for a $V_{GS} - V_T = 0.3$ V and an $L_g = 400$ nm, g_{mb}/g_m will decrease from 0.450 to 0.370 between representative 90 nm and 45 nm standard bulk CMOS technologies[‡]. The table also shows that g_{mb}/g_m will further degrade in high-κ/metal gate processes, falling due to a supplemental growth in C'_{ox} caused by the elimination of polysilicon gate depletion.

While the BD MOSFET may not be ideal for the deca-nanometer regime, the device and the design approach outlined in this dissertation will still have significant value in low-voltage analog applications targeted for more mature bulk CMOS technologies – *e.g.*, a 0.25 μm or a 0.18 μm process – since those technologies can

[†] In these simulations, t_{ox} and V_{T0} were not allowed to vary from their nominal values in a given process; N_δ was restricted to values below 1×10^{19} cm^{-3}.

[‡] Table 6.1 also indicates that y_{epi} will stay relatively constant from process to process as a result of fairly minor changes in $N_{a,eff}$ (to see why $N_{a,eff}$ does not vary significantly, please see Section 3.3). Given the range of values predicted for y_{epi} between the 90 nm and 45 nm nodes, it will most likely be necessary to use molecular beam epitaxy (MBE) to form the lightly-doped channel layer. However, it may be possible to use ultra-high vacuum chemical vapor deposition (UHV-CVD) in larger technologies where y_{epi} exceeds 20 nm [151].

inherently provide larger g_{mb}/g_m ratios (refer to Section 3.3) and will continue to be in demand for a while to come [39]–[40]. However, if one were to use the BD MOSFET in such applications, it would be wise to operate the device with a reasonable gate over-drive voltage to combat the V_{T0}/V_{DD}-related issues discussed in Section 3.5 and to obtain a larger g_{mb}/g_m ratio, as previously illustrated by Figure 5.14 of Section 5.2.

Table 6.1: A list of the $N_{a,eff}$, y_{epi}, g_{mb} and g_{mb}/g_m values predicted by ATLAS for a standard 90 nm, 65 nm and 45 nm bulk CMOS process, as well as a 45 nm high-κ/metal gate bulk CMOS process (L_g = 400 nm, $V_{GS} - V_T$ = 0.3 V, V_{DS} = 0.4 V and V_{BS} = 0).

Process Type	$N_{a,eff}$	y_{epi}	g_{mb}	g_{mb}/g_m
Standard 90 nm [6]	1.75×10^{18} cm^{-3}	11 nm	74.35 µS/µm	0.450
Standard 65 nm [7]	1.35×10^{18} cm^{-3}	13 nm	75.62 µS/µm	0.402
Standard 45 nm [184]–[185]	1.50×10^{18} cm^{-3}	12 nm	74.74 µS/µm	0.370
High-κ/Metal Gate 45 nm[†] [184]–[185]	1.90×10^{18} cm^{-3}	10 nm	74.54 µS/µm	0.335

6.2 The Findings of this Research

In this dissertation, several key findings were presented to expand the field's understanding of the BD MOSFET. In particular, this dissertation showed that [145]–[146], [176], [180]:

- In the sub-micron regime, g_{mb}/g_m is a monotonically decreasing function of process scaling because g_m continually increases in each new process generation while g_{mb} remains relatively constant due to minor changes in $N_{a,eff}$.
- The gate of an *n*-type BD MOSFET should be tied to a bias voltage less than V_{DD} in environments where V_{T0}/V_{DD} is sufficiently *low* – *e.g.*, in low-voltage analog applications targeted for technologies with feature sizes smaller than 0.18 µm – in order to retain the expected advantages of bulk-driven circuitry.
- The gate oxide scaling requirements of a BD MOSFET are not as stringent as those of a GD MOSFET because the bulk is able to maintain better control over the channel as t_{ox} is made thicker.

[†] An Al–SiO_2 gate stack was utilized in the simulation of the high-κ/metal gate technology; t_{ox} was equal to the equivalent physical gate oxide thickness of the process.

- In deca-nanometer technologies, delta doping is the best candidate to enhance the bulk transconductance of a BD MOSFET because of its ability to efficiently reduce the depletion depth, y_d, without requiring an increase in $N_{a,eff}$ and V_{T0}.

- It is possible to condense the *effective* layout area of a triple-well-isolated *n*-type BD MOSFET considerably by using a DTI structure since DTI is able to eliminate the well-to-well spacing requirements between adjacent BD MOSFETs of the same type.

- While g_{mb} can be noticeably improved via delta doping, it is unlikely that the improvements provided by the doping profile will be enough to make the BD MOSFET viable as a general solution to low-voltage analog design since it is not possible to make g_{mb} comparable to g_m in the deca-nanometer regime. However, a BD MOSFET – coupled with a delta-doped profile and a DTI structure – should still be useful for low-voltage analog applications targeted for mature bulk CMOS technologies – *e.g.*, a 0.25 μm or a 0.18 μm process – since those technologies can inherently provide larger g_{mb}/g_m ratios and will continue to be utilized for the foreseeable future.

6.3 Suggestions for Future Work

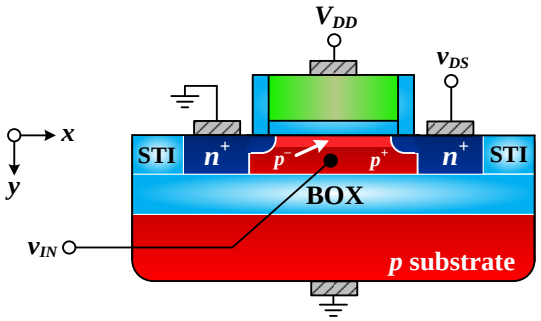


Figure 6.1: The device cross-section of a delta-doped *n*-type BD MOSFET built upon a PD-SOI substrate. Note that the bulk terminal (tied to v_{IN}) is directly connected to the BD MOSFET's active area along the length of the device in the *x* direction.

To extend this dissertation's work on the BD MOSFET, it would be worthwhile to see how a delta-doped BD MOSFET performs on a PD-SOI (partially-depleted SOI) substrate – such as the one shown in Figure 6.1 – as there are low-voltage analog applications where an SOI substrate would be appropriate [186]. Theoretically, $f_{T,BD}$ and

$f_{T,BD}/f_{T,GD}$ should be much greater in a PD-SOI setting because a BD MOSFET would no longer be plagued by a large area-dependent well capacitance and would have smaller bulk-to-source and bulk-to-drain capacitances since its source and drain regions would be abutted to a buried oxide (BOX) layer [15] (pp. 57–61), [138] (pp. 456–460). A PD-SOI substrate should also allow the layout area requirements of an *n*-type BD MOSFET to be similar to the case in which deep trenches are used to isolate the device on a bulk substrate, without requiring any modifications to the device's existing process flow.

References

[1] J.P. Uyemura, *Introduction to VLSI Circuits and Systems*, John Wiley & Sons, 2002.

[2] E. Vittoz and J. Fellrath, "CMOS Analog Integrated Circuits Based on Weak Inversion Operation," *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 224–231, Jun. 1977.

[3] "IBM CMOS6SF Model Reference Guide," Nov. 2006.

[4] "IBM CMOS7SF Model Reference Guide," Oct. 2008.

[5] "IBM CMOS8SF Model Reference Guide," Sep. 2008.

[6] "IBM CMOS9SF Model Reference Guide," Apr. 2006.

[7] "IBM CMOS10SF Model Reference Guide," May 2007.

[8] International Technology Roadmap for Semiconductors, ITRS 2007 Edition. Available Online: http://www.itrs.net/Links/2007ITRS/Home2007.htm.

[9] Y.-L. Lo, W.-B. Yang, T.-S. Chao and K.-H. Cheng, "Designing an Ultralow-Voltage Phase-Locked Loop Using a Bulk-Driven Technique," *IEEE Transactions on Circuits and Systems II*, vol. 56, no. 5, pp. 339–343, May 2009.

[10] M. Trakimas and S. Sonkusale, "A 0.5 V Bulk-Input OTA with Improved Common-Mode Feedback for Low-Frequency Filtering Applications," *Springer Analog Integrated Circuits and Signal Processing*, vol. 59, no. 1, pp. 83–89, Apr. 2009.

[11] "IBM CMS9FLP Model Reference Guide," Jul. 2008.

[12] "IBM CMS10LPe Model Reference Guide," May 2008.

[13] B. Murmann, P. Nikaeen, D.J. Connelly and R.W. Dutton, "Impact of Scaling on Analog Performance and Associated Modeling Needs," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2160–2167, Sep. 2006.

[14] W. Yang, M.V. Dunga, X. Xi, J. He, W. Liu, K.M. Chao, X. Jin, J.J. Ou, M. Chan, A.M. Niknejad and C. Hu, "BSIM4.6.2 MOSFET Model – User's Manual," 2008.

[15] S.C. Terry, "Low-Voltage Analog Circuit Design Using the Adaptively Biased Body-Driven Circuit Technique," Ph.D. Dissertation, The University of Tennessee, Knoxville, Aug. 2005.

[16] S. Chatterjee, "Analog Circuit Design Techniques at 0.5 V," Ph.D. Dissertation, Columbia University, 2006.

[17] M. Pude, C. Macchietto, P. Singh, J. Burleson and P.R. Mukund, "Maximum Intrinsic Gain Degradation in Technology Scaling," *Proceedings of the International Semiconductor Device Research Symposium*, pp. 1–2, Dec. 2007.

[18] S.-H. Lo, D.A. Buchanan and Y. Taur, "Modeling and Characterization of Quantization, Polysilicon Depletion, and Direct Tunneling Effects in MOSFETs with Ultrathin Oxides," *IBM Journal of Research and Development*, vol. 43, no. 3, pp. 327–337, May 1999.

[19] C.-H. Choi, K.-Y. Nam, Z. Yu and R.W. Dutton, "Impact of Gate Direct Tunneling Current on Circuit Performance: A Simulation Study," *IEEE Transactions on Electron Devices*, vol. 48, no. 12, pp. 2823–2829, Dec. 2001.

[20] J. Ramirez-Angulo, S.C. Choi and G. Gonzalez-Altamirano, "Low-Voltage Circuits Building Blocks Using Multiple-Input Floating-Gate Transistors," *IEEE Transactions on Circuits and Systems I*, vol. 42, no. 11, pp. 971–974, Nov. 1995.

[21] S.S Rajput and S.S Jamuar, "Low Voltage Analog Circuit Design Techniques," *IEEE Circuits and Systems Magazine*, vol. 2, no. 1, pp. 24–42, 2002.

[22] D.M. Binkley, *Tradeoffs and Optimization in Analog CMOS Design*, John Wiley & Sons, 2008.

[23] A. Guziński, M. Białko and J. C. Matheau, "Body-Driven Differential Amplifier for Application in Continuous-Time Active-C Filter," *Proceedings of the European Conference on Circuit Theory and Design*, pp. 315–319, Jun. 1987.

[24] M. Pude, P.R. Mukund, P. Singh, K. Paradis and J. Burleson, "Amplifier Gain Enhancement with Positive Feedback," *Proceedings of the International Midwest Symposium on Circuits and Systems*, pp. 981–984, Aug. 2010.

[25] A. Hokazono, S. Balasubramanian, K. Ishimaru, H. Ishiuchi, C. Hu and T.-J.K. Liu, "Forward Body Biasing as a Bulk-Si CMOS Technology Scaling Strategy," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2657–2664, Oct. 2008.

[26] B. Blalock, "A 1-Volt CMOS Wide Dynamic Range Operational Amplifier," Ph.D. Dissertation, Georgia Institute of Technology, Nov. 1996.

[27] O. Schmitz, S.K. Hampel, C. Orlob, M. Tiebout and I. Rolfes, "Low-Voltage Bulk-Driven Mixers in 45nm CMOS for Ultra-Wideband TX and RX," *Proceedings of the NORCHIP Conference*, pp. 119–122, Nov. 2008.

[28] M.J. Deen, R. Murji, N. Jafferali and W. Ngan, "Low-Power CMOS Integrated Circuits for Radio Frequency Applications," *IEE Proceedings – Circuits, Devices and Systems*, vol. 152, no. 5, pp. 509–522, Oct. 2005.

[29] S.-L. Jang, S.-H. Huang, C.-C. Liu and M.-H. Juang, "CMOS Colpitts Quadrature VCO Using the Body Injection-Locked Coupling Technique," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 4, pp. 230–232, Apr. 2009.

[30] S.-L. Jang, C.-Y. Lin and C.-F. Lee, "A Low Voltage 0.35 μm CMOS Frequency Divider With the Body Injection Technique," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 7, pp. 470–472, Jul. 2008.

[31] A. Aldokhaiel, A. Yamazaki and M. Ismail, "A Sub-1 Volt CMOS Bandgap Voltage Reference Based on Body-Driven Technique," *Proceedings of the Northeast Workshop on Circuits and Systems*, pp. 5–8, Jun. 2004.

[32] Z. Zhu and Y. Yang, "A 0.8 V Low-Power CMOS PTAT Voltage Reference," *Proceedings of the International Workshop on VLSI Design and Video Technology*, pp. 1–5, May 2005.

[33] Y.-C. Hung, B.-D. Liu and C.-Y. Tsai, "1-V Bulk-Driven CMOS Analog Programmable Winner-Takes-All Circuit," *Springer Analog Integrated Circuits and Signal Processing*, vol. 49, no. 1, pp. 53–61, Oct. 2006.

[34] Y.-C. Hung and B.-D. Liu, "A Low-Voltage Wide-Input CMOS Comparator for Sensor Application using Back-Gate Technique," *Elsevier Biosensors and Bioelectronics*, vol. 20, no. 1, pp. 53–59, Jul. 2004.

[35] Y. Haga and I. Kale, "CMOS Buffer using Complementary Pair of Bulk-Driven Super Source Followers," *IET Electronics Letters*, vol. 45, no. 18, pp. 917–918, Aug. 2009.

[36] Y. Haga and I. Kale, "Bulk-Driven Flipped Voltage Follower," *Proceedings of the International Symposium on Circuits and Systems*, pp. 2717–2720, 2009.

[37] S. Vlassis and G. Raikos, "Bulk-Driven Differential Voltage Follower," *IET Electronics Letters*, vol. 45, no. 25, pp. 1276–1277, Dec. 2009.

[38] "ATLAS User's Manual," Silvaco Data Systems, Inc., Dec. 4th, 2008.

[39] R. Goering, "InCyte Data Shows Path to Lower Process Nodes," Cadence Design Systems, Apr. 7th, 2009. Available Online: http://www.chipestimate.com/techtalk.php?d=2009-04-07.

[40] TSMC Historical Operation Data (Through the 4th Quarter of 2010). Available Online: http://www.tsmc.com/uploadfile/ir/quarterly/business_info.xls.

[41] P. Hasler and T.S. Lande, "Overview of Floating-Gate Devices, Circuits, and Systems," *IEEE Transactions on Circuits and Systems II*, vol. 48, no. 1, pp. 1–3, Jan. 2001.

[42] A.-J. Annema, B. Nauta, R. van Langevelde and H. Tuinhout, "Analog Circuits in Ultra-Deep-Submicron CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, Jan. 2005.

[43] K.D. Layton, "Low-Voltage Analog CMOS Architectures and Design Methods," Ph.D. Dissertation, Brigham Young University, Dec. 2007.

[44] X. Zhang, "Low Voltage Analog Circuit Design Using Body-Driven Techniques," Ph.D. Dissertation, Dalhousie University, Apr. 2004.

[45] S.S. Rajput and S.S. Jamuar, "Low Voltage, Low Power, High Performance Current Mirror for Portable Analogue and Mixed Mode Applications," *IEE Proceedings – Circuits, Devices and Systems*, vol. 148, no. 5, pp. 273–278, Oct. 2001.

[46] E. Bohannon, C. Washburn and P.R. Mukund, "Investigating the BJT-like Behavior of MOSFETs in Ultra-Deep-Submicron CMOS Technologies with Significant Gate Current," *Proceedings of the International Semiconductor Device Research Symposium*, pp. 1–2, Dec. 2009.

[47] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw Hill, 2001.

[48] S. Mitra and A.N. Chandorkar, "Design of Amplifier with Rail-to-Rail CMR with 1 V Power Supply," *Proceedings of the International Conference on VLSI Design*, pp. 52–56, 2004.

[49] J.F. Duque-Carrillo, J.L. Ausin, G. Torelli, J.M. Valverde and M.A. Deminguez, "1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 1, pp. 33–44, Jan. 2000.

[50] Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd Ed., Oxford University Press, 1999.

[51] L.H.C. Ferreira, T.C. Pimenta and R.L. Moreno, "An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 10, pp. 843–847, Oct. 2007.

[52] L.J. Stotts, "Introduction to Implantable Biomedical IC Design," *IEEE Circuits and Devices Magazine*, vol. 5, no. 1, pp. 12–18, Jan. 1989.

[53] B.J. Blalock, H.W. Li, P.E. Allen and S.A. Jackson, "Body-Driving as a Low-Voltage Analog Design Technique for CMOS Technology," *Proceedings of the Southwest Symposium on Mixed-Signal Design*, pp. 113–118, 2000.

[54] K.D. Layton, D.T. Corner and D.J. Corner, "Bulk-Driven Gain-Enhanced Fully-Differential Amplifier for $V_T + 2V_{dsat}$ operation," *Proceedings of the International Symposium on Circuits and Systems*, pp. 77–80, May 2008.

[55] K.D. Layton, D.T. Comer and D.J. Comer, "Analog Circuit Design at and Below $V_T + 2V_{ds,sat}$," *Proceedings of the Ph.D. Research in Microelectronics and Electronics Conference*, pp. 213–216, Jul. 2007.

[56] J.M. Carrillo, G. Torelli, R. Perez-Aloe and J.F. Duque-Carrillo, "1-V Rail-to-Rail CMOS OpAmp with Improved Bulk-Driven Input Stage," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 508–517, Mar. 2007.

[57] J.M. Carrillo, M.A. Dominguez, J.F. Duque-Carrillo and G Torelli, "Input Common-Mode Voltage Behaviour of CMOS Bulk-Driven Differential Stages," *Proceedings of the European Conference on Circuit Theory and Design*, pp. 267–270, Aug. 2009.

[58] N. Raj, R. Gupta and V. Chopra, "Bulk Driven OTA in 0.18 Micron with High Linearity," *Proceedings of the International Conference on Computer Science and Information Technology*, pp. 478–482, Jul. 2010.

[59] G. Raikos and S. Vlassis, "Low-Voltage Differential Amplifier," *Proceedings of the International Conference on Electronics, Circuits, and Systems*, pp. 136–139, Dec. 2009.

[60] G. Raikos and S. Vlassis, "Low-Voltage CMOS Voltage Squarer," *Proceedings of the International Conference on Electronics, Circuits, and Systems*, pp. 159–162, Dec. 2009.

[61] S. Chatterjee, Y. Tsividis and P. Kinget, "A 0.5-V Bulk-Input Fully Differential Operational Transconductance Amplifier," *Proceedings of the European Solid-State Circuits Conference*, pp. 147–150, Sep. 2004.

[62] X. Zhang and E.I. El-Masry, "A Novel CMOS OTA Based on Body-Driven MOSFETs and its Applications in OTA-C Filters," *IEEE Transactions on Circuits and Systems I*, vol. 54, no. 6, pp. 1204–1212, Jun. 2007.

[63] L.H.C. Ferreira, T.C. Pimenta and R.L. Moreno, "An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing," *IEEE Transactions on Circuits and Systems II*, vol. 54, no. 10, pp. 843–847, Oct. 2007.

[64] T. Stockstad and H. Yoshizawa, "A 0.9-V 0.5-μA Rail-to-Rail CMOS Operational Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 3, pp. 286–292, Mar. 2002.

[65] B.J. Blalock, P.E. Allen and G.A. Rincon-Mora, "Designing 1-V Op Amps Using Standard Digital CMOS Technology," *IEEE Transactions on Circuits and Systems II*, vol. 45, no. 7, pp. 769–780, Jul. 1998.

[66] M. Białko and A. Guziński, "Comments on 'Designing 1-V Op-Amps Using Standard Digital CMOS Technology,'" *IEEE Transactions on Circuits and Systems II*, vol. 46, no. 11, pp. 1448, Nov. 1999.

[67] J. Rosenfeld, M. Kozak and E.G. Friedman, "A Bulk-Driven CMOS OTA with 68 dB DC Gain," *Proceedings of the International Conference on Electronics, Circuits and Systems*, pp. 5–8, Dec. 2004.

[68] Y. Haga, H. Zare-Hoseini, L. Berkovi and I. Kale, "Design of a 0.8 Volt Fully Differential CMOS OTA Using the Bulk-Driven Technique," *Proceedings of the International Symposium on Circuits and Systems*, pp. 220–223, May 2005.

[69] J.M. Carrillo, G. Torelli, R. Perez-Aloe and J.F. Duque-Carrillo, "1-V Rail-to-Rail Bulk-Driven CMOS OTA With Enhanced Gain and Gain-Bandwidth Product," *Proceedings of the European Conference on Circuit Theory and Design*, pp. 261–264, Aug.–Sep. 2005.

[70] J. Rosenfeld, M. Kozak and E.G. Friedman, "A 0.8 Volt High Performance OTA Using Bulk-Driven MOSFETs for Low Power Mixed-Signal SOCs," *Proceedings of the International SOC Conference*, pp. 245–246, Sep. 2003.

[71] B.J. Blalock and P.E. Allen, "A One-Volt, 120-μW, 1-MHz OTA for Standard CMOS Technology," *Proceedings of the International Symposium on Circuits and Systems*, pp. 305–307, May 1996.

[72] F. Bahmani, S.M. Fakhraie and A. Khakifirooz, "A Rail-to-Rail, Constant-G_m, 1-Volt CMOS Opamp," *Proceedings of the International Symposium on Circuits and Systems*, pp. 669–672, May 2000.

[73] F. Bahmani and S.M. Fakhraie, "A Rail-to-Rail 1-Volt CMOS Opamp," *Proceedings of the International Conference on Microelectronics*, pp. 217–219, Nov. 1999.

[74] K. Lasanen, E. Raisanen-Ruotsalainen and J. Kostamovaara, "A 1-V 5 μW CMOS-Opamp with Bulk-Driven Input Transistors," *Proceedings of the International Midwest Symposium on Circuits and Systems*, pp. 1038–1041, 2000.

[75] C. Popa and D. Coada, "A New Linearization Technique for a CMOS Differential Amplifier Using Bulk-Driven Weak Inversion MOS Transistors," *Proceedings of the International Symposium on Signals, Circuits and Systems*, pp. 589–592, Jul. 2003.

[76] I. Grech, J. Micallef, G. Azzopardi and C.J. Debono, "A 0.9 V Wide-Input-Range Bulk-Input CMOS OTA for G_m-C Filters," *Proceedings of the International Conference on Electronics, Circuits and Systems*, pp. 818–821, Dec. 2003.

[77] C.-F. Tai, J.-L. Lai and R.-J. Chen, "Using Bulk-Driven Technology Operate in Subthreshold Region to Design a Low Voltage and Low Current Operational Amplifier," *Proceedings of the International Symposium on Consumer Electronics*, pp. 1–5, 2006.

[78] Y. Haga, R.C.S. Morling and I. Kale, "A New Bulk-Driven Input Stage Design for Sub 1-Volt CMOS Op-Amps," *Proceedings of the International Symposium on Circuits and Systems*, pp. 1547–1550, 2006.

[79] J.M. Carrillo, J.F. Duque-Carrillo and G. Torelli, "Transconductance Enhancement in Bulk-Driven Input Stages," *Proceedings of the International Conference on Electronics, Circuits and Systems*, pp. 13–16, Aug.–Sep. 2008.

[80] J.M. Carrillo, J.F. Duque-Carrillo and G. Torelli, "1-V Continuously Tunable CMOS Bulk-Driven Transconductor for Gm-C Filters," *Proceedings of the International Symposium on Circuits and Systems*, pp. 896–899, May 2008.

[81] X. Zhang and E.I. El-Masry, "A 1.8 V CMOS Linear Transconductor and its Application to Continuous-Time Filters," *Proceedings of the International Symposium on Circuits and Systems*, pp. 1012–1015, May 2004.

[82] X. Zhang and E.I. El-Masry, "A Low-Voltage Body-Driven CMOS Transconductor," *Proceedings of the International Midwest Symposium on Circuits and Systems*, pp. 328–331, Aug. 2002.

[83] R. Fried and C.C. Enz, "Bulk Driven MOST Transconductor with Extended Linear Range," *IEE Electronics Letters*, vol. 32, no. 7, pp. 638–640, Mar. 1996.

[84] L. Zhang, X. Zhang and E. El-Masry, "A Highly Linear Bulk-Driven CMOS OTA for Continuous Time Filters," *Springer Analog Integrated Circuits and Signal Processing*, vol. 54, no. 3, pp. 229–236, Mar. 2008.

[85] M. Trakimas and S. Sonkusale, "A 0.5V Bulk-Input Operational Transconductance Amplifier with Improved Common-Mode Feedback," *Proceedings of the International Symposium on Circuits and Systems*, pp. 2224–2227, May 2007.

[86] K. Lasanen and J. Kostamovaara, "A 1.2-V CMOS *RC* Oscillator for Capacitive and Resistive Sensor Applications," *IEEE Transactions on Instrumentation and Measurement*, vol. 57, no. 12, pp. 2792–2800, Dec. 2008.

[87] S.-W. Pan, C.-C Chuang, C.-H. Yang and Y.-S. Lai, "A Novel OTA with Dual Bulk-Driven Input Stage," *Proceedings of the International Symposium on Circuits and Systems*, pp. 2721–2724, 2009.

[88] G. Raikos and S. Vlassis, "0.8 V Bulk-Driven Operational Amplifier," *Springer Analog Integrated Circuits and Signal Processing*, vol. 63, no. 3, pp. 425–432, Mar. 2010.

[89] J.M. Carrillo, G. Torelli, R. Perez-Aloe, J.M. Valverde and J.F. Duque-Carrillo, "Single-Pair Bulk-Driven CMOS Input Stage: A Compact Low-Voltage Analog Cell for Scaled Technologies," *Elsevier VLSI Integration Journal*, vol. 43, no. 6, pp. 251–257, Jun. 2010.

[90] J.M. Carrillo, G. Torelli, M.A. Dominguez, R. Perez-Aloe, J.M. Valverde and J.F. Duque-Carrillo, "A Family of Low-Voltage Bulk-Driven CMOS Continuous-Time CMFB Circuits," *IEEE Transactions on Circuits and Systems II*, vol. 57, no. 11, pp. 863–867, Nov. 2010.

[91] A. Khateb, D. Biolek and K. Novacek, "On the Design of Low-Voltage Low-Power Bulk-Driven CMOS Current Conveyors," *International Spring Seminar on Electronics Technology*, pp. 318–321, May 2006.

[92] M.W. Murphy, E.I. El-Masry and A.M. Elshurafa, "A High Compliance Input and Output Regulated Body-Driven Current Mirror for Deep-Submicron CMOS," *Proceedings of the International Conference on Microelectronics*, pp. 13–16, Dec. 2006.

[93] S. Terry, B.J. Blalock, L. Yong, B. Dufrene and M. Mojarradi, "Complementary Body Driving – A Low Voltage Analog Circuit Technique for SOI," *Proceedings of the International SOI Conference*, pp. 80–82, Oct. 2002.

[94] X. Zhang and E.I. El-Masry, "A Regulated Body-Driven CMOS Current Mirror for Low-Voltage Applications," *IEEE Transactions on Circuits and Systems II*, vol. 51, no. 10, pp. 571–577, Oct. 2004.

[95] X. Zhang and E.I. El-Masry, "A High-Performance, Low-Voltage, Body-Driven CMOS Current Mirror," *Proceedings of the International Symposium on Circuits and Systems*, pp. 49–52, 2002.

[96] T.-C. Huang, M.-C. Huang and K.-J. Lee, "Built-In Current Sensor Designs Based on the Bulk-Driven Technique," *Proceedings of the Asian Test Symposium*, pp. 384–389, Nov. 1997.

[97] B.J. Blalock and P.E. Allen, "A Low-Voltage, Bulk-Driven MOSFET Current Mirror for CMOS Technology," *Proceedings of the International Symposium on Circuits and Systems*, pp. 1972–1975, Apr.–May 1995.

[98] F. Bautista, S.O. Martınez, G. Dieck and O. Rossetto, "An Ultra-Low Voltage High Gain Operational Transconductance Amplifier for Biomedical Applications," *Proceedings of the Workshop on Design and Architectures for Signal and Image Processing*, 2007.

[99] S.C. Terry, M.M. Mojarradi, B.J. Blalock and J.A. Richmond, "Adaptive Gate Biasing – A New Solution for Body-Driven Current Mirrors," *Proceedings of the ACM Great Lakes Symposium on VLSI*, pp. 472–477, 2005.

[100] J. Mulder, A.C. van der Woerd, W.A. Serdijn and A.H.M. van Roermund, "Application of the Back Gate in MOS Weak Inversion Translinear Circuits," *IEEE Transactions on Circuits and Systems I*, vol. 42, no. 11, pp. 958–962, Nov. 1995.

[101] B. Aggarwal and M. Gupta, "Low-Voltage Bulk-Driven Class AB Four Quadrant CMOS Current Multiplier," *Springer Analog Integrated Circuits and Signal Processing*, vol. 65, no. 1, pp. 163–169, Oct. 2010.

[102] A. Kumar and G.K. Sharma, "Bulk Driven Circuits for Low Voltage Applications," *Old City Publishing Journal of Active and Passive Electronic Devices*, vol. 8, pp. 237–245, 2009.

[103] N. Jafferali and M.J. Deen, "Low-Voltage and Low-Power 1.9 GHz Body-Input Downconversion Mixer," *Proceedings of the Canadian Conference on Electrical and Computer Engineering*, pp. 1413–1416, May 2004.

[104] K. Schweiger and H. Zimmermann, "Low-Voltage Low-Power Highly Linear Down-Sampling Mixer in 65 nm Digital CMOS Technology," *Proceedings of the Workshop on Design and Diagnostics of Electronic Circuits and Systems*, pp. 1–4, Apr. 2008.

[105] K. Schweiger and H. Zimmermann, "High-Gain Double-Bulk Mixer in 65 nm CMOS with 830 μW Power Consumption," *ETRI Journal*, vol. 32, no. 3, pp. 457–459, Jun. 2010.

[106] G. Kathiresan and C. Toumazou, "A Low Voltage Bulk Driven Downconversion Mixer Core," *Proceedings of the International Symposium on Circuits and Systems*, pp. 598–601, Jul. 1999.

[107] O. Schmitz, S.K. Hampel, C. Orlob, M. Tiebout and I. Rolfes, "Body Effect Up- and Down-Conversion Mixer Circuits for Low-Voltage Ultra-Wideband Operation," *Springer Analog Integrated Circuits and Signal Processing*, vol. 64, no. 3, pp. 233–240, Sep. 2010.

[108] C. Kienmayer, M. Tiebout, W. Simburger and A.L. Scholtz, "A Low-Power Low-Voltage NMOS Bulk-Mixer with 20 GHz Bandwidth in 90 nm CMOS," *Proceedings of the International Symposium on Circuits and Systems*, pp. 385–388, May 2004.

[109] C.-L. Kuo, B.-J. Huang, C.-C. Kuo, K.-Y. Lin and H. Wang, "A 10–35 GHz Low Power Bulk-Driven Mixer Using 0.13 μm CMOS Process," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 7, pp. 455–457, Jul. 2008.

[110] D. Van Vorst and S. Mirabbasi, "Low-Voltage Bulk-Driven Mixer with On-Chip Balun," *Proceedings of the International Symposium on Circuits and Systems*, pp. 456–459, May 2008.

[111] D. Van Vorst and S. Mirabbasi, "Low-Power 1V 5.8 GHz Bulk-Driven Mixer with On-Chip Balun in 0.18μm CMOS," *Proceedings of the Radio Frequency Integrated Circuits Symposium*, pp. 197–200, Apr. 2008.

[112] K.-H. Liang, H.-Y. Chang and Y.-J. Chan, "A 0.5–7.5 GHz Ultra Low-Voltage Low-Power Mixer Using Bulk-Injection Method by 0.18-μm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 7, pp. 531–533, Jul. 2007.

[113] R. Salmeh, "An Ultra Low Power ESD Protected Mixer in 90nm RF CMOS," *Proceedings of the International Midwest Symposium on Circuits and Systems*, pp. 47–50, Aug. 2006.

[114] C.-Y. Wang and J.-H. Tsai, "A 51 to 65 GHz Low-Power Bulk-Driven Mixer Using 0.13 μm CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 8, Aug. 2009.

[115] T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd Ed., Cambridge University Press, 2004.

[116] S. Chatterjee, Y. Tsividis and P. Kinget, "0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, Dec. 2005.

[117] D. Wu, R. Huang, W. Wong and Y. Wang, "A 0.4 V Low Noise Amplifier Using Forward Body Bias Technology for 5 GHz Application," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 7, pp. 543–545, Jul. 2007.

[118] A.L. Coban, P.E. Allen and X. Shi, "Low-Voltage Analog IC Design in CMOS Technology," *IEEE Transactions on Circuits and Systems I*, vol. 42, no. 11, pp. 955–958, Nov. 1995.

[119] P. Monsurro, S. Pennisi, G. Scotti and A. Trifiletti, "Switched-Capacitor Body-Biasing Technique for Very Low Voltage CMOS Amplifiers," *Proceedings of the European Conference on Circuit Theory and Design*, pp. 257–260, Aug.–Sep. 2005.

[120] P.E. Allen, B.J. Blalock and G.A. Rincon, "Low Voltage Analog Circuits Using Standard CMOS Technology," *Proceedings of the International Symposium on Low Power Design*, pp. 209–214, 1995.

[121] P. Park and C.P. Yue, "Modeling of Triple-Well Isolation and the Loading Effects on Circuits up to 50 GHz," *Proceedings of the Custom Integrated Circuits Conference*, pp. 217–220, Sep. 2008.

[122] S.M. Sze and K.K. Ng, *Physics of Semiconductor Devices*, 3rd Ed., John Wiley & Sons, 2007.

[123] R.J. Baker, *CMOS Circuit Design, Layout and Simulation*, 2nd Ed., John Wiley & Sons, 2005.

[124] A.A. Abidi, "High-Frequency Noise Measurements on FET's with Small Dimensions," *IEEE Transactions on Electron Devices*, vol. 33, no. 11, pp. 1801–1805, Nov. 1986.

[125] P.G. Drennan, M.L. Kniffin and D.R. Locascia, "Implications of Proximity Effects for Analog Design," *Proceedings of the Custom Integrated Circuits Conference*, pp. 169–176, 2006.

[126] "Minimization of Well-Proximity Effect by Means of 2D and 3D Monte Carlo Simulation of Retrograde Well Implantation," *Silvaco Simulation Standard*, vol. 19, no. 1, pp. 13–16, Jan.–Mar. 2009.

[127] R.S. Muller, T.I. Kamins and M. Chan, *Device Electronics for Integrated Circuits*, 3rd Ed., John Wiley & Sons, 2003.

[128] M.-S. Liang, J.Y. Choi, P.K. Ko and C. Hu, "Inversion-Layer Capacitance and Mobility of Very Thin Gate-Oxide MOSFET's," *IEEE Transactions on Electron Devices*, vol. 33, no. 3, pp. 409–413, Mar. 1986.

[129] Z.-H. Liu, C. Hu, J.-H. Huang, T.-Y. Chan, M.-C. Jeng, P.K. Ko and Y.C. Cheng, "Threshold Voltage Model for Deep-Submicrometer MOSFETs," *IEEE Transactions on Electron Devices*, vol. 40, no. 1, pp. 86–95, Jan. 1993.

[130] S. Takagi and A. Toriumi, "Quantitative Understanding of Inversion-Layer Capacitance in Si MOSFET's," *IEEE Transactions on Electron Devices*, vol. 42, no. 12, pp. 2125–2130, Dec. 1995.

[131] Y. Zhiping, R.W. Dutton and R.A. Kiehl, "Circuit/Device Modeling at the Quantum Level," *IEEE Transactions on Electron Devices*, vol. 47, no. 10, pp. 1819–1825, Oct. 2000.

[132] J.A. Lopez-Villanueva, P. Cartujo-Casinello, J. Banqueri, F. Gamiz and S. Rodriguez, "Effects of the Inversion Layer Centroid on MOSFET Behavior," *IEEE Transactions on Electron Devices*, vol. 44, no. 11, pp. 1915–1922, Nov. 1997.

[133] B.P. Wong, A. Mittal, Y. Cao and G. Starr, *Nano-CMOS Circuit and Physical Design*, John Wiley & Sons, 2005.

[134] M. Miyamoto, H. Ohta, Y. Kumagai, Y. Sonobe, K. Ishibashi and Y. Tainaka, "Impact of Reducing STI-Induced Stress on Layout Dependence of MOSFET Characteristics," *IEEE Transactions on Electron Devices*, vol. 51, no. 3, pp. 440–443, Mar. 2004.

[135] Y.M. Sheu, C.S. Chang, H.C. Lin, S.S Lin, C.H. Lee, C.C. Wu, M.J. Chen and C.H. Diaz, "Impact of STI Mechanical Stress in Highly Scaled MOSFETs," *Proceedings of the International Symposium on VLSI Technology, Systems, and Applications*, pp. 76–79, Oct. 2003.

[136] Y.M. Sheu, K.Y.Y. Doong, C.H. Lee, M.J. Chen and C.H. Diaz, "Study on STI Mechanical Stress Induced Variations on Advanced CMOSFETs," *Proceedings of the International Conference on Microelectronic Test Structures*, pp. 205–208, Mar. 2003.

[137] L. Yuhao and D.K. Nayak, "Enhancement of CMOS Performance by Process-Induced Stress," *IEEE Transactions on Semiconductor Manufacturing*, vol. 18, no. 1, pp. 63–68, Feb. 2005.

[138] B. El-Kareh, *Silicon Devices and Process Integration: Deep Submicron and Nano-Scale Technologies*, Springer Science+Business Media, Inc., 2009.

[139] R. van Langevelde, A.J. Scholten and D.B.M. Klaassen, "Physical Background of MOS Model 11," Apr. 2003.

[140] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, G.D.J. Smit, A.J. Scholten and D.B.M. Klaassen, "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 1979–1993, Sep. 2006.

[141] M. Bucher, C. Lallement, C. Enz and F. Krummenacher, "Accurate MOS Modelling for Analog Circuit Simulation Using the EKV Model," *Proceedings of the International Symposium on Circuits and Systems*, pp. 703–706, May 1996.

[142] Y. Cheng, M. Chan, K. Hui, M.-C. Jeng, Z. Liu, J. Huang, K. Chen, J. Chen, R. Tu, P.K. Ko and C. Hu, "BSIM3v3 Manual," 1996.

[143] "ModelLib User's Manual," Simucad, Jan. 14th, 2009.

[144] "Virtuoso Spectre Circuit Simulator Reference," Cadence Design Systems, Inc., Jun. 2008.

[145] C. Urban, J.E. Moon and P.R. Mukund, "Scaling the Bulk-Driven MOSFET," *Proceedings of the International Conference on Microelectronics*, pp. 42–45, Dec. 2009.

[146] C. Urban, J.E. Moon and P.R. Mukund, "Designing Bulk-Driven MOSFETs in Scaled Technologies," *Proceedings of the International Semiconductor Device Research Symposium*, pp. 1–2, Dec. 2009.

[147] L. Wang, "Quantum Mechanical Effects on MOSFET Scaling Limit," Ph.D. Dissertation, Georgia Institute of Technology, Aug. 2006.

[148] C. Wann, F. Assaderaghi, R. Dennard, C. Hu, G. Shahidi and Y. Taur, "Channel Profile Optimization and Device Design for Low-Power High-Performance Dynamic-Threshold MOSFET," *Proceedings of the International Electron Devices Meeting*, pp. 113–116, Dec. 1996.

[149] H.C. Wann, C. Hu, K. Noda, D. Sinitsky, F. Assaderaghi and J. Bokor, "Channel Doping Engineering of MOSFET with Adaptable Threshold Voltage Using Body Effect for Low Voltage and Low Power Applications," *Proceedings of the International Symposium on VLSI Technology, Systems, and Applications*, pp. 159–163, May–Jun. 1995.

[150] H. Koura, M. Takamiya and T. Hiramoto, "Optimum Conditions of Body Effect Factor and Substrate Bias in Variable Threshold Voltage MOSFETs," *Japanese Journal of Applied Physics*, vol. 39, no. 4B, pp. 2312–2317, Apr. 2000.

[151] K. Noda, T. Tatsumi, T. Uchida, K. Nakajima, H. Miyamoto and C. Hu, "A 0.1-μm Delta-Doped MOSFET Fabricated with Post-Low-Energy Implanting Selective Epitaxy," *IEEE Transactions on Electron Devices*, vol. 45, no. 4, pp. 809–814, Apr. 1998.

[152] S.H.S. Tang, "Dynamic Threshold MOSFETs for Future Integrated Circuits," Ph.D. Dissertation, University of California at Berkeley, 2001.

[153] H.-J. Wann, "Advanced MOSFET Devices for VLSI Memory and Logic," Ph.D. Dissertation, University of California at Berkeley, 1996.

[154] C. Wann, J. Harrington, R. Mih, S. Biesemans, K. Han, R. Dennard, O. Prigge, C. Lin, R. Mahnkopf and B. Chen, "CMOS with Active Well Bias for Low-Power and RF/Analog Applications," *Proceedings of the Symposium on VLSI Technology*, pp. 158–159, 2000.

[155] M. Lundstrom, *Fundamentals of Carrier Transport*, Addison–Wesley, 1990.

[156] D. Sinitsky, F. Assaderaghi, M. Orshansky, J. Bokor and C. Hu, "Velocity Overshoot of Electrons and Holes in Si Inversion Layers," *Elsevier Solid-State Electronics*, vol. 41, no. 8, pp. 1119–1125, 1997.

[157] J.H. Huang, Z.H. Liu, M.C. Jeng, P.K. Ko and C. Hu, "A Physical Model for MOSFET Output Resistance," *Proceedings of the International Electron Devices Meeting*, pp. 569–572, Dec. 1992.

[158] P. Walker and H. Mizuta, "Energy-Balance Modeling of Short Channel Single-GB Thin Film Transistors," *Proceedings of the Workshop on Modeling and Simulation of Electron Devices*, pp. 19–20, Aug. 2005.

[159] D. Munteanu, G. Le Carval and G. Guegan, "Impact of Technological Parameters on Non-Stationary Transport in Realistic 50 nm MOSFET Technology," *Elsevier Solid-State Electronics*, vol. 46, no. 7, pp. 1045–1050, Jul. 2002.

[160] A. Mannargudi and D. Vasileska, "Quantum Confinements in Highly Asymmetric Sub-Micrometer Device Structures," *Elsevier Superlattices and Microstructures*, vol. 34, no. 3–6, pp. 347–354, Sep.–Dec. 2003.

[161] R. Granzner, V.M. Polyakov, F. Schwierz, M. Kittler, R.J. Luyken, W. Rösner and M. Städele, "Simulation of Nanoscale MOSFETs using Modified Drift-Diffusion and Hydrodynamic Models and Comparison with Monte Carlo Results," *Elsevier Microelectronic Engineering*, vol. 83, no. 2, pp. 241–246, Feb. 2006.

[162] O.M. Nayfeh and D.A. Antoniadis, "Calibrated Hydrodynamic Simulation of Deeply-Scaled Well-Tempered Nanowire Field Effect Transistors," *Proceedings of the International Conference on Simulation of Semiconductor Processes and Devices*, pp. 305–308, Sep. 2007.

[163] G. Iannaccone, G. Curatola and G. Fiori, "Effective Bohm Quantum Potential for Device Simulators based on Drift Diffusion and Energy Transport," *Proceedings of the International Conference on Simulation of Semiconductor Processes and Devices*, pp. 275–278, Sep. 2004.

[164] Private Communication with Steve Broadbent, Silvaco Data Systems, Inc., Oct.–Nov. 2009.

[165] J.P. McKelvey, *Solid State Physics for Engineering and Material Science*, Krieger Publishing, 1993.

[166] J.D. Plummer and P.B. Griffin, "Material and Process Limits in Silicon VLSI Technology," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 240–248, Mar. 2001.

[167] Y. Taur, D.A. Buchanan, W. Chen, D.J. Frank, K.E. Ismail, S.-H. Lo, G.A. Sai-Halasz, R.G. Viswanathan, H.-J.C. Wann, S.J. Wind and H.-S. Wong, "CMOS Scaling into the Nanometer Regime," *Proceedings of the IEEE*, vol. 85, no. 4, pp. 486–504, Apr. 1997.

[168] H.-S.P. Wong, D.J. Frank, P.M. Solomon, C.H.J. Wann and J.J. Welser, "Nanoscale CMOS," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 537–570, Apr. 1999.

[169] A.F. Tasch, "The Challenges in Achieving Sub-100 nm MOSFETs," *Proceedings of the International Conference on Innovative Systems in Silicon*, pp. 52–60, Oct. 1997.

[170] J.W. McPherson, "Reliability Challenges for 45nm and Beyond," *Proceedings of the Design Automation Conference*, pp. 176–181, 2006.

[171] S.-H. Lo, D.A. Buchanan, Y. Taur and W. Wang, "Quantum-Mechanical Modeling of Electron Tunneling Current from the Inversion Layer of Ultra-Thin-Oxide nMOSFET's," *IEEE Electron Device Letters*, vol. 18, no. 5, pp. 209–211, May 1997.

[172] W.-C. Lee and C. Hu, "Modeling Gate and Substrate Currents due to Conduction- and Valence-Band Electron and Hole Tunneling," *Proceedings of the Symposium on VLSI Technology*, pp. 198–199, 2000.

[173] "VWF Interactive Tools," Silvaco Data Systems, Inc., Jul. 18th, 2005.

[174] S.-.H. Lo, D.A. Buchanan and Y. Taur, "Modeling and Characterization of Quantization, Polysilicon Depletion, and Direct Tunneling Effects in MOSFETs with Ultrathin Oxides," *IBM Journal of Research and Development*, vol. 43, no. 3, pp. 327–337, May 1999.

[175] "ATLAS User's Manual," Silvaco Data Systems, Inc., Jul. 6th, 2010.

[176] C. Urban, J.E. Moon and P.R. Mukund, "Scaling the Bulk-Driven MOSFET into Deca-Nanometer Bulk CMOS Processes," *Elsevier Microelectronics Reliability*, vol. 51, no. 4, pp. 727–732, Apr. 2011.

[177] K. Cao, "Advanced Compact Modeling of MOSFETs," Ph.D. Dissertation, University of California at Berkeley, 2002.

[178] M. Golio (Editor) *et al.*, *RF and Microwave Semiconductor Device Handbook*, CRC Press, 2003.

[179] C.-H. Shih, Y.-M. Chen and C. Lien, "Design Strategy of Localized Halo Profile for Achieving Sub-50 nm Bulk MOSFET," *Elsevier Microelectronics Reliability*, vol. 44, no. 7, pp. 1069–1075, Jul. 2004.

[180] C. Urban, J.E. Moon and P.R. Mukund, "Designing Bulk-Driven MOSFETs for Ultra-Low-Voltage Analogue Applications," *IOP Semiconductor Science and Technology*, vol. 25, no. 11, pp. 1–8, Nov. 2010.

[181] A. Asenov and S. Saini, "Suppression of Random Dopant-Induced Threshold Voltage Fluctuations in Sub-0.1-μm MOSFET's with Epitaxial and δ-doped Channels," *IEEE Transactions on Electron Devices*, vol. 46, no. 8, pp. 1718–1724, Aug. 1999.

[182] P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, 2nd Ed., Oxford University Press, 2002.

[183] M.T. Bohr, R.S. Chau, T. Ghani and K. Mistry, "The High-k Solution," *IEEE Spectrum*, vol. 44, no. 10, pp. 29–35, Oct. 2007.

[184] J. Hicks, D. Bergstrom, M. Hattendorf, J. Jopling, J. Maiz, S. Pae, C. Prasad and J. Wiedemer, "45nm Transistor Reliability," *Intel Technology Journal*, vol. 12, no. 2, pp. 131–144, Jun. 2008.

[185] D. Scansen, "Under the Hood: 45 nm: What Intel Didn't Tell You," Semiconductor Insights, Jan. 21st, 2008. Available Online: http://www.eetimes.com/design/signal-processing-dsp/4005680/Under-the-Hood-45-nm-What-Intel-didn-t-tell-you.

[186] G.K. Celler and S. Cristovoleanu, "Frontiers of Silicon-on-Insulator," *Journal of Applied Physics*, vol. 93, no. 9, pp. 4955–4978, May 2003.

Appendix

Bulk-Driven MOSFET Device Structure

ATLAS Code

```
go atlas simflags="-P 8"

################################
# Global Variable Definitions #
################################

# Gate Oxide Thickness
set tox=0.0018
set toxmesh=$tox*(-1)
# p-well Doping Level
set Na=1e16
# Deep n-well Doping Level
set Ndnw=1e17
# Substrate Doping Level
set Nsub=1e16
# Delta Doping Level (When Enabled)
set Nd=6e18
# Halo Doping Level (When Enabled)
set Nhalo=4e18
# Lightly-Doped Channel Doping Level (When Enabled)
set Nepi=1e15
# Gate Length
set Length=0.08
# S/D Contact Size
set xcont=0.2
# STI Width
set xsti=0.42
# STI Depth
set ysti=0.42
# DTI Width
set xdt=$xsti
# Deep n-well Contact Size
set xdnw=$xcont/2
# Leftmost Bulk Contact Definition- Right Side
set xb=($xdt+$xdnw)
# Source Contact Definition- Left Side
set xs=$xb+$xcont+$xsti
# S/D Junction Depth
set yj=0.03
# LDD Junction Depth (When Enabled)
set yjLDD=0.025
# LDD Length (When Enabled- Otherwise Ln=0)
set Ln=0.015
# S/D and Bulk Contact Doping
set Nsd=1e20
# LDD Doping (When Enabled)
set NLDD=2e19
# Drain Contact Definition- Left Side
set xd=$xs+$xcont+$Length+2*$Ln
# Rightmost Bulk Contact Definition- Left Side
set xb2=$xd+$xcont+$xsti
# Rightmost Bulk Contact Definition- Right Side
set xb3=$xb2+$xcont
# End of Device Definition in the x Direction
set xl=$xb3+$xdt+$xdnw
# Depth of Lightly-Doped Channel (When Enabled)
set tepi=0.012
# Depth of Delta-Doped Region (When Enabled)
set tepi2=$tepi+0.1
# Depth of p well
set ypw=1.5
```

```
# Depth of Deep n well
set ydnw=$ypw+0.50
# Depth of Substrate
set ysub=$ydnw+0.4
# DTI Depth
#set ydt=$ysti
set ydt=$ypw+0.065
# Halo Width (When Enabled)
set xh=0.03
# Halo Depth (When Enabled)
set yh=0.02
# Electrode Spacing from Contact Edge
set co=0.04
# Lateral Characteristics of S/D and Bulk Contacts
set lat=0.003
# Gate Height
set tpoly=$toxmesh-0.15
# Terminal Voltages
set Vdd=0.7
set Vgs=0.7
set Vds=0.7
set Vbs=0
# Energy Relaxation Time
set tau_e=0.1e-12

####################
# Mesh Definition #
####################

mesh space.mult=1.0

x.mesh loc=0.00                       spac=0.0300
x.mesh loc=($xdnw-$co)                spac=0.0300
x.mesh loc=$xdnw                      spac=0.0450
x.mesh loc=($xb-$xdt/2-0.0001)        spac=0.0250
x.mesh loc=($xb-$xdt/2)               spac=0.0001
x.mesh loc=($xb-$xdt/2+0.0001)        spac=0.0250
x.mesh loc=$xb                        spac=0.0450
x.mesh loc=($xb+$co)                  spac=0.0300
x.mesh loc=($xb+$xcont-$co)           spac=0.0300
x.mesh loc=($xb+$xcont)               spac=0.0450
x.mesh loc=($xb+$xcont+$xsti/2)       spac=0.0450
x.mesh loc=$xs                        spac=0.0275
x.mesh loc=($xs+$co)                  spac=0.0275
x.mesh loc=($xs+$xcont-$co)           spac=0.0150
x.mesh loc=($xs+$xcont+$Ln)           spac=0.0020
x.mesh loc=$xl/2                      spac=0.0250*($Length)
x.mesh loc=($xd-$Ln)                  spac=0.0015
x.mesh loc=($xd+$co)                  spac=0.0150
x.mesh loc=($xd+$xcont-$co)           spac=0.0275
x.mesh loc=($xd+$xcont)               spac=0.0275
x.mesh loc=($xb2-$xsti/2)             spac=0.0450
x.mesh loc=$xb2                       spac=0.0450
x.mesh loc=($xb2+$co)                 spac=0.0300
x.mesh loc=($xb3-$co)                 spac=0.0300
x.mesh loc=$xb3                       spac=0.0450
x.mesh loc=($xb3+$xdt/2-0.0001)       spac=0.0250
x.mesh loc=($xb3+$xdt/2)              spac=0.0001
x.mesh loc=($xb3+$xdt/2+0.0001)       spac=0.0250
x.mesh loc=($xl-$xdnw)                spac=0.0450
x.mesh loc=($xl-$xdnw+$co)            spac=0.0300
x.mesh loc=$xl                        spac=0.0300

y.mesh loc=$tpoly                     spac=0.1250
y.mesh loc=($toxmesh-0.005)           spac=0.0020
y.mesh loc=($toxmesh-0.0025)          spac=0.0010
y.mesh loc=$toxmesh                   spac=$tox/4
y.mesh loc=0.00                       spac=$tox/4
y.mesh loc=0.0001                     spac=0.00075
y.mesh loc=0.0025                     spac=0.0010
y.mesh loc=($tepi-0.0001)             spac=0.0015
```

```
y.mesh loc=$tepi                        spac=0.0001
y.mesh loc=($tepi+0.0001)               spac=0.0015
y.mesh loc=$yj                          spac=0.0025
y.mesh loc=($yj+0.05)                   spac=0.0300
y.mesh loc=($yj+0.10)                   spac=0.0600
y.mesh loc=$ysti                        spac=0.1000
y.mesh loc=($ypw-0.5)                   spac=0.1250
y.mesh loc=($ypw-0.0001)                spac=0.0250
y.mesh loc=$ypw                         spac=0.0001
y.mesh loc=($ypw+0.0001)                spac=0.0250
y.mesh loc=($ypw+$ydnw)/2               spac=0.0750
y.mesh loc=($ydnw-0.0001)               spac=0.0350
y.mesh loc=$ydnw                        spac=0.0001
y.mesh loc=($ydnw+0.0001)               spac=0.0500
y.mesh loc=$ysub                        spac=0.1000

# Remove Un-Needed Node Points to The Left and Right of the Gate Contact
eliminate rows x.min=0 x.max=($xs+$xcont-0.001) \
       y.min=$tpoly y.max=-0.0001
eliminate rows x.min=($xd+0.001) x.max=$xl y.min=$tpoly y.max=-0.0001
eliminate rows x.min=0 x.max=($xs+$xcont-0.001) \
       y.min=$tpoly y.max=-0.0001
eliminate rows x.min=($xd+0.001) x.max=$xl y.min=$tpoly y.max=-0.0001

# Bulk Contact & STI Node Reduction
eliminate rows x.min=0 x.max=$xs y.min=0.0005 y.max=$tepi
eliminate rows x.min=($xd+$xcont) x.max=$xl y.min=0.0005 y.max=$tepi
eliminate rows x.min=0 x.max=$xdnw y.min=0.0005 y.max=($yj+0.05)
eliminate rows x.min=($xl-$xdnw) x.max=$xl y.min=0.0005 y.max=$yj
eliminate rows x.min=($xb+$xcont+0.0025) x.max=($xs-0.005) \
       y.min=0.0005 y.max=($ysti-0.01)
eliminate rows x.min=($xd+$xcont+0.0025) x.max=($xb2-0.005) \
       y.min=0.0005 y.max=($ysti-0.01)
eliminate rows x.min=($xb+$xcont+0.05) x.max=($xs-0.05) \
       y.min=0.0005 y.max=($yj+0.1)
eliminate rows x.min=($xb+$xcont+0.05) x.max=($xs-0.05) \
       y.min=0.0005 y.max=($yj+0.1)
eliminate rows x.min=($xd+$xcont+0.05) x.max=($xb2-0.05) \
       y.min=0.0005 y.max=($yj+0.1)
eliminate rows x.min=($xd+$xcont+0.05) x.max=($xb2-0.05) \
       y.min=0.0005 y.max=($yj+0.1)

# Substrate Node Reduction (Below Channel Region)
eliminate columns x.min=($xs+$xcont) x.max=$xd y.min=($yj+0.05) y.max=$ysub
eliminate columns x.min=($xs+$xcont) x.max=$xd y.min=($yj+0.05) y.max=$ysub
eliminate columns x.min=($xs+$xcont-$co) x.max=($xd+$co) \
       y.min=($yj+0.1) y.max=$ysub
eliminate columns x.min=0 x.max=$xl y.min=($ypw+0.1) y.max=$ysub
eliminate columns x.min=0 x.max=$xl y.min=($ypw+$ydnw)/2 y.max=$ysub

# Deep Trench Node Reduction
eliminate rows x.min=($xdnw+0.0025) x.max=($xb-0.005) y.min=0.0005 \
       y.max=($yj+0.1)
eliminate rows x.min=($xb3+0.0025) x.max=($xl-$xdnw-0.005) y.min=0.0005 \
       y.max=($yj+0.1)
eliminate rows x.min=($xdnw+0.05) x.max=($xb-0.05) y.min=0.0005 \
       y.max=($yj+0.1)
eliminate rows x.min=($xb3+0.05) x.max=($xl-$xdnw-0.05) y.min=0.0005 \
       y.max=($yj+0.1)
eliminate rows x.min=($xdnw+0.05) x.max=($xb-0.05) y.min=0.0005 \
       y.max=($ydt-0.01)
eliminate rows x.min=($xb3+0.05) x.max=($xl-$xdnw-0.05) y.min=0.0005 \
       y.max=($ydt-0.01)

############################
# Device Region Definitions #
############################

# Deep n well
region number=1 x.min=0 x.max=$xl y.min=0 y.max=$ydnw material=Silicon
```

```
# Central p well
region number=2 x.min=($xs-$xsti/2) \
        x.max=($xd+$xcont+$xsti/2) y.min=0 y.max=($yj+0.1) material=Silicon
region number=3 x.min=($xs-$xsti/2) \
        x.max=($xd+$xcont+$xsti/2) y.min=($yj+0.1) y.max=$ypw material=Silicon

# Gate Oxide
region number=4 x.min=($xs+$xcont+$Ln) x.max=($xd-$Ln) y.min=$toxmesh \
        y.max=0 material=SiO2

# Rest of p well
region number=5 x.min=($xdnw+$xdt/2) x.max=($xs-$xsti/2) y.min=0 y.max=$ypw \
        material=Silicon
region number=6 x.min=($xd+$xcont+$xsti/2) x.max=($xl-$xdnw-$xdt/2) y.min=0 \
        y.max=$ypw material=Silicon

# STI
region number=7 x.min=($xb+$xcont) x.max=$xs y.min=0 y.max=$ysti material=SiO2
region number=8 x.min=($xd+$xcont) x.max=$xb2 y.min=0 y.max=$ysti material=SiO2

# Gate Poly
region number=9 x.min=($xs+$xcont+$Ln) x.max=($xd-$Ln) \
        y.min=$tpoly y.max=$toxmesh material=Poly

# Air/Vacuum
region number=10 x.min=0 x.max=($xs+$xcont+$Ln) y.min=$tpoly y.max=0 material=Air
region number=11 x.min=($xd-$Ln) x.max=$xl y.min=$tpoly y.max=0 material=Air

# Substrate
region number=12 x.min=0 x.max=$xl y.min=$ydnw y.max=$ysub material=Silicon

# DTI
region number=13 x.min=$xdnw x.max=$xb y.min=0 y.max=$ydt material=SiO2
region number=14 x.min=$xb3 x.max=($xl-$xdnw) y.min=0 y.max=$ydt material=SiO2

# Oxide Spacers
region number=15 x.min=($xs+$xcont) x.max=($xs+$xcont+$Ln) y.min=$tpoly y.max=0 \
        material=SiO2
region number=16 x.min=($xd-$Ln) x.max=$xd y.min=$tpoly y.max=0 material=SiO2

####################################
# Electrode and Contact Definitions #
####################################

electrode name=gate number=1 x.min=($xs+$xcont+$Ln) x.max=($xd-$Ln) \
        y.min=$tpoly y.max=$tpoly
electrode name=source number=2 x.min=($xs+$co) x.max=($xs+$xcont-$co) \
        y.min=0 y.max=0
electrode name=drain number=3 x.min=($xd+$co) x.max=($xd+$xcont-$co) \
        y.min=0 y.max=0
electrode name=pwell number=4 x.min=($xb+$co) x.max=($xb+$xcont-$co) y.min=0 \
        y.max=0
electrode name=pwell number=5 x.min=($xb2+$co) x.max=($xb3-$co) y.min=0 y.max=0
electrode name=nwell number=6 x.min=0 x.max=($xdnw-$co) y.min=0 y.max=0
electrode name=nwell number=7 x.min=($xl-$xdnw+$co) x.max=$xl y.min=0 y.max=0
electrode name=substrate number=8 x.min=0 x.max=$xl y.min=$ysub y.max=$ysub

contact name=gate neutral
contact name=source neutral exclude_near
contact name=drain neutral exclude_near
contact name=pwell neutral exclude_near
contact name=nwell neutral exclude_near
contact name=substrate neutral exclude_near

#############################
# Device Doping Definitions #
#############################

# Delta Doping (When Enabled)
doping uniform conc=$Na p.type noyrolloff y.top=$tepi y.bottom=($yj+0.1) \
        regions=2
```

```
doping uniform conc=$Nd p.type noyrolloff y.top=$tepi y.bottom=$tepi2 \
       regions=2
doping uniform conc=$Nepi p.type noyrolloff y.top=0 y.bottom=$tepi regions=2

# Uniform Doping (When Enabled)
#doping uniform conc=$Nd p.type regions=2

# Substrate Doping
doping uniform conc=$Ndnw n.type regions=1
doping uniform conc=$Na p.type regions=3
doping uniform conc=$Na p.type regions=5
doping uniform conc=$Na p.type regions=6
doping uniform conc=$Nsub p.type regions=12

# Bulk Contact Definition
doping gaussian junction=$yj conc=$Nsd p.type x.left=$xb x.right=($xb+$xcont) \
       lat.char=$lat regions=5
doping gaussian junction=$yj conc=$Nsd p.type x.left=$xb2 x.right=$xb3 \
       lat.char=$lat regions=6

# Deep n-well Contact Definition
doping gaussian junction=$yj conc=$Nsd n.type x.left=0 x.right=$xdnw \
       lat.char=$lat regions=1
doping gaussian junction=$yj conc=$Nsd n.type x.left=($xl-$xdnw) x.right=$xl \
       lat.char=$lat regions=1

# Drain-Side Halo Definition
#doping gaussian junction=$yh conc=$Nhalo  p.type x.left=($xd-$Ln-$xh) \
#      x.right=($xd-$Ln+$xh) lat.char=0.005 regions=2

# Source-Side Halo Definition
#doping gaussian junction=$yh conc=$Nhalo  p.type \
#      x.left=($xs+$xcont+$Ln-$xh) x.right=($xs+$xcont+$Ln+$xh) \
#      lat.char=0.005 regions=2

# Gate Doping
doping uniform conc=1e20 n.type regions=9

# Drain LDD Definition
doping gaussian junction=$yjLDD conc=$NLDD n.type x.left=($xd-$Ln) \
       x.right=($xd+$xcont) lat.char=$lat regions=2

# Source LDD Definition
doping gaussian junction=$yjLDD conc=$NLDD n.type x.left=$xs \
       x.right=($xs+$xcont+$Ln) lat.char=$lat regions=2

# Drain Contact Definition
doping gaussian junction=$yj conc=$Nsd  n.type x.left=$xd \
       x.right=($xd+$xcont) lat.char=$lat regions=2

# Source Contact Definition
doping gaussian junction=$yj conc=$Nsd n.type x.left=$xs \
       x.right=($xs+$xcont) lat.char=$lat regions=2

# Structure Output File for MIXEDMODE Simulations
struct outfile=MIXEDMODE.str

material region=1 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e taumob.el=$tau_e
material region=2 bqp.ngamma=1.3 bqp.nalpha=1 taurel.el=$tau_e taumob.el=$tau_e
material region=3 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e taumob.el=$tau_e
material region=4 bqp.ngamma=0 bqp.nalpha=0 mc=0.45
material region=5 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e taumob.el=$tau_e
material region=6 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e taumob.el=$tau_e
material region=7 bqp.ngamma=0 bqp.nalpha=0
material region=8 bqp.ngamma=0 bqp.nalpha=0
material region=9 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e taumob.el=$tau_e
material region=10 bqp.ngamma=0 bqp.nalpha=0
material region=11 bqp.ngamma=0 bqp.nalpha=0
material region=12 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e taumob.el=$tau_e
material region=13 bqp.ngamma=0 bqp.nalpha=0
material region=14 bqp.ngamma=0 bqp.nalpha=0
```

```
material region=15 bqp.ngamma=0 bqp.nalpha=0
material region=16 bqp.ngamma=0 bqp.nalpha=0

# Plot of Device Structure
tonyplot -set contours2.set

################################
# Electrical Simulation Setup #
################################

# Model Summary
# hnsaug = Auger Recomb.; fldmob = Velocity Sat.; cvt & conmob = Mobility Degradation
# consrh = SRH Recomb.; bqp.n = Quantum Potential Correction
# fermidirac = Fermi-Dirac Stat's; hcte.el = Energy Balance Transport Model
# toyabe = Impact Ionization; qtunn.el = Quantum/Direct Oxide Tunneling
# bbt.kl = Band-to-Band Tunneling

method block newton nblockit=2 maxtrap=6 itlimit=50

models conmob consrh bgn cvt fldmob evsatmod=0 hnsaug ni.fermi fermidirac \
       hcte.el qtunn.el bqp.n bbt.kl print temperature=300
impact toyabe tausn=$tau_e tausp=$tau_e

extract name="Reset Clk" clock.time start.time=0

###################
# Linear VT Sweep #
###################

solve init
solve vdrain=0.05 vgate=-0.05 vnwell=0.05
solve name=nwell vnwell=0.10 vfinal=0.35 vstep=0.05
solve name=nwell vnwell=0.40 vfinal=$"Vdd" vstep=0.10

# Enable When Vbs > 0
#solve name=pwell vpwell=0.00625 vfinal=0.0125 vstep=0.00625
#solve name=pwell vpwell=0.05 vfinal=($"Vbs"-0.05) vstep=0.05
#solve vpwell=$"Vbs"

log outf=vt_lin.log
solve name=gate vgate=0 vfinal=$"Vgs" vstep=0.05

extract name="vt" \
(x.val from curve(abs(v."gate"),abs(i."drain")) where y.val=(2e-7/$"Length"))

# MOS Cap. Calibration for Gate Current Model
#extract name="Ig_lin" \
#(y.val from curve(abs(v."gate"),abs(i."gate")) where x.val=$"Vgs")

# ID/VGS plot for Linear VT Extraction
tonyplot vt_lin.log
tonyplot -set contours-V.set

log off

###################
# ro Calculation #
###################

log outf=ro_sweep.log
solve name=drain vdrain=0.10 vfinal=0.175 vstep=0.025
solve name=drain vdrain=0.20 vfinal=$"Vds" vstep=0.05

extract name="ro" \
1/(y.val from curve(abs(v."drain"),abs(dydx(v."drain",i."drain"))) \
       where x.val=$"Vds")

extract name="Idsmax" \
(y.val from curve(abs(v."drain"),abs(i."drain")) where x.val=$"Vds")
```

```
extract name="Ig_sat" \
(y.val from curve(abs(v."drain"),abs(i."gate")) where x.val=$"Vds")

extract name="Id/Ig" ($"Idsmax"/$"Ig_sat")

# ro/VDS plot
tonyplot ro_sweep.log -set ro.set

# Maximum E-field Calculation
struct outfile=test.str
extract init infile="test.str"
extract name="Exmax" min.conc impurity="E Field X" material="Silicon" mat.occno=3 \
        y.val=0.005
extract name="Eymax" max.conc impurity="E Field Y" material="Silicon" mat.occno=1 \
        x.val=$"xl"/2

log off

####################
# gmb Calculation #
####################

solve name=pwell vpwell=($"Vbs"-0.00625) vfinal=($"Vbs"-0.0125) vstep=-0.00625

log outf=gmb_sweep.log
solve vpwell=($"Vbs"-0.03)
solve name=pwell vpwell=($"Vbs"-0.0275) vfinal=($"Vbs"-0.0175) vstep=0.0025
solve name=pwell vpwell=($"Vbs"-0.015) vfinal=($"Vbs"-0.005) vstep=0.005
solve name=pwell vpwell=$"Vbs" vfinal=($"Vbs"+0.03) vstep=0.005

# gmb/VBS plot
tonyplot gmb_sweep.log -set gmb_pwell.set

extract name="gmb" \
(y.val from curve(abs(v."pwell"),abs(dydx(v."pwell",i."drain"))) \
        where x.val=$"Vbs")

log off

solve name=pwell vpwell=($"Vbs"+0.025) vfinal=$"Vbs" vstep=-0.025

##################
# fT Calculation #
##################

log outf=FreqGD.log y.param inport=gate outport=drain \
        in2port=source out2port=source
solve prev terminal=1 ac freq=7e8 fstep=1.75 mult.f nfsteps=10 vss=0.001
tonyplot FreqGD.log -set yparam.set

extract name="fTGD" (x.val from \
curve(elect."freq", \
((((y.real."21")^2+(y.imag."21")^2)/((y.real."11")^2+(y.imag."11")^2))^(1/2))) \
where y.val=1)
log off

log outf=FreqBD.log y.param inport=pwell outport=drain \
        in2port=source out2port=source
solve prev terminal=4 ac freq=3e8 fstep=1.75 mult.f nfsteps=7 vss=0.001
tonyplot FreqBD.log -set yparam.set

extract name="fTBD" (x.val from \
curve(elect."freq", \
((((y.real."21")^2+(y.imag."21")^2)/((y.real."11")^2+(y.imag."11")^2))^(1/2))) \
where y.val=1)

extract name="fTBD_fTGD" ($"fTBD"/$"fTGD")

log off
```

```
########################################
# Capacitance Calculation (When Enabled) #
########################################

#log outf=cap.log
#solve terminal=4 ac freq=1 fstep=1e6 mult.f nfsteps=1 vss=0.001
#tonyplot cap.log -set cap.set

#extract name="Cbd" abs(y.val from \
#curve(elect."freq",c."pwell""drain") where x.val=1e6)
#extract name="Cbs" abs(y.val from \
#curve(elect."freq",c."source""pwell") where x.val=1e6)
#extract name="Cbg" abs(y.val from \
#curve(elect."freq",c."gate""pwell") where x.val=1e6)
#extract name="Cpw/dnw" abs(y.val from \
#curve(elect."freq",c."nwell""pwell") where x.val=1e6)
#extract name="Cbb" abs(y.val from \
#curve(elect."freq",c."pwell""pwell") where x.val=1e6)

#log off

##################
# gm Calculation #
##################

log outf=gm_sweep.log
#tonyplot -set contours-V.set
solve name=gate vgate=$"Vgs" vfinal=($"vt"-0.10) vstep=-0.065

extract name="gm" \
(y.val from curve(abs(v."gate"),abs(dydx(v."gate",i."drain"))) where x.val=$"Vgs")

# Sub-Threshold Swing Calculation
extract name="S" \
        1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))*1000

# Saturation VT Calculation
extract name="Sat_vt" \
(x.val from curve(abs(v."gate"),abs(i."drain")) where y.val=(2e-7/$"Length"))

extract name="DITS" (($"vt"-$"Sat_vt")*1000)/($"Vds"-0.05)
extract name="gmb_gm" abs($"gmb"/$"gm")
extract name="gm_ro" ($"gm"*$"ro")
extract name="gmb_ro" ($"gmb"*$"ro")

# Substrate Current Calculation
extract name="Ipwell_max" \
(y.val from curve(abs(v."gate"),abs(i."pwell")) where x.val=$"Vgs")

# gm/VGS plot
#tonyplot gm_sweep.log -set S.set
#tonyplot gm_sweep.log -set gm.set

log off

# End of Simulation Time Calculation
extract name="Time" clock.time

quit
```

```
go internal

# Load BD MOSFET ATLAS File from Page 101
load infile=gmb_test_doping_finalwell.in

#########################################################
# Parametric Sweep of the Delta Doping Concentration #
#########################################################

#save type=sdb outfile=Nd.dat
#sweep parameter=Nd type=list range="5e17, 1e18, 2e18, 3e18, 4e18, 5e18, \
#       6e18, 7e18, 8e18, 9e18, 1e19"
#endsave

#######################################
# Parametric Sweep of the Gate Length #
#######################################

save type=sdb outfile=L.dat
sweep parameter=Length type=list range="0.08, 0.16, 0.24, 0.32, 0.4, 0.48, \
        0.56, 0.64, 0.72, 0.8"
endsave

############################
# Parametric Sweep of VBS #
############################

#save type=sdb outfile=Vbs.dat
#sweep parameter=Vbs type=list range="0.5, 0.4, 0.3, 0.2, 0.1, 0"
#endsave

############################
# Parametric Sweep of VDS #
############################

#save type=sdb outfile=Vds.dat
#sweep parameter=Vds type=list range="0.7, 0.6, 0.5, 0.4, 0.3, 0.2"
#endsave

quit
```

Bohm Quantum Potential Model Calibration

ATLAS Code

```
go atlas simflags="-P 8"

################################
# Global Variable Definitions #
################################

# Gate Oxide Thickness
set gate_ox=0.0018
set Xoxmesh=$gate_ox*(-1)
# Background Doping Level
set Na=1.125e18
# Gate Length
set Length=0.08
# Depth of Substrate
set ysub=0.08
# End of Device in the x Direction
set xl=$Length

###################
# Mesh Definition #
###################

mesh space.mult=1.0

x.mesh loc=0.00          spac=0.0
x.mesh loc=$Length       spac=$Length

y.mesh loc=$Xoxmesh      spac=$gate_ox/20
y.mesh loc=0.0000        spac=$gate_ox/20
y.mesh loc=0.0001        spac=0.00075
y.mesh loc=0.0025        spac=0.0010
y.mesh loc=0.0100        spac=0.0010
y.mesh loc=0.0250        spac=0.0025
y.mesh loc=$ysub         spac=0.0050

#############################
# Device Region Definitions #
#############################

# Substrate
region number=1 x.min=0 x.max=$xl y.min=0 material=Silicon

# Gate Oxide
region number=2 x.min=0 x.max=$xl y.min=$Xoxmesh \
         y.max=0 material=SiO2

#####################################
# Electrode and Contact Definitions #
#####################################

electrode name=gate number=1 x.min=0 x.max=$xl \
         y.min=$Xoxmesh y.max=$Xoxmesh
electrode name=substrate number=2 x.min=0 x.max=$xl y.min=$ysub y.max=$ysub

contact name=gate n.poly
contact name=substrate neutral

#############################
# Device Doping Definitions #
#############################

doping uniform conc=$Na p.type regions=1
```

```
# Plot of Device Structure
tonyplot -set contours2.set

###################
# S-P Simulation #
###################

model schrodinger eigens=10 qminconc=1.0e5 ox.schro fermi \
          qy.min=$Xoxmesh qy.max=0.05 num.direct=3 new.eig
method climit=1.0e-2 carriers=0

solve init

log outf=SP.log
solve name=gate vgate=0.0 vstep=0.01 vfinal=1.0 qscv
log off

###################
# BQP Simulation #
###################

model fermi bqp.n bqp.ngamma=1.3 bqp.nalpha=1.0
method climit=1.0e-2 carriers=0

solve init

log outf=BQP.log
solve name=gate vgate=0.0 vstep=0.01 vfinal=1.0 qscv
log off

tonyplot -overlay SP.log BQP.log -set qscv.set

quit
```

Energy Balance Transport Model Calibration

MCDEVICE Code

```
go atlas

################################
# Global Variable Definitions #
################################

# Gate Length
set Length=0.08
# S/D Contact Definitions
set xcont=0.05
set co=0.02
# LDD Length
set Ln=0.015
# Gate Oxide Thickness
set tox=-0.0018
# Gate Height
set tpoly=(-0.005+$tox)
# Depth of Substrate
set ysub=0.08
# Location of Drain Contact in the x Direction
set xd=($xcont+$Length+2*$Ln)
# End of Device in the x Direction
set xl=($xd+$xcont)

# Device Contact Mesh Parameters
set Scon=($xcont-$co)
set Dcon=($xd+$co)
set Bcon=($ysub-0.0001)
set Gcon1=($xcont+$Ln)
set Gcon2=($xd-$Ln)
set Gcony=($tpoly+0.0001)
set SS1=($xcont-0.0075)
set SS2=($xd+0.0075)

# x and y Node Definitions
# @xcont-co
set pos2=(($xcont-$co)/0.001+1)
# @xcont
set pos3=($co/0.00075+$pos2)
# @xcont+Ln
set pos4=($Ln/0.00035+$pos3)
# @xd-Ln
set pos5=($Length/0.00035+$pos4)
# @xd
set pos6=($Ln/0.00035+$pos5)
# @xd+co
set pos7=($co/0.00075+$pos6)
# @xl
set pos8=(($xcont-$co)/0.001+$pos7)
# @ysub
set posy=(($ysub-0.08)/0.01+87)

# Current Estimation Mesh Parameters
set pt1=($xcont-0.002)
set pt2=($xcont+$Ln-0.002)
set pt3=$xl/2
set pt4=($xd-$Ln+0.002)
set pt5=($xd+0.002)

#############################
# MCDEVICE Simulation Setup #
#############################

mcdevice
```

```
algo mode=2 carrier=e iter=2000 dt=0.1e-15 restart=no
poisson tstep=2
output restart=-1 outfiles=yes init=1 \
  currentlogfile="BD_current.log" \
  currentramplogfile="BD_current_ramp.log" \
  solstrfile="BD_sol.str" \
  summaryoutfile="BD_summary.out" \
  tstep=1000
particle n=60000

####################
# Mesh Definition #
####################

xmesh node=1      loc=0.0000
xmesh node=$pos2  loc=($xcont-$co) ratio=1.00
xmesh node=$pos3  loc=$xcont       ratio=1.00
xmesh node=$pos4  loc=($xcont+$Ln) ratio=1.00
xmesh node=$pos5  loc=($xd-$Ln)    ratio=1.00
xmesh node=$pos6  loc=$xd          ratio=1.00
xmesh node=$pos7  loc=($xd+$co)    ratio=1.00
xmesh node=$pos8  loc=$xl          ratio=1.00

ymesh node=1      loc=$tpoly
ymesh node=3      loc=$tox         ratio=1.0000
ymesh node=8      loc=0.0000       ratio=1.0000
ymesh node=13     loc=0.0005       ratio=1.0000
ymesh node=87     loc=0.0800       ratio=1.0508
ymesh node=$posy  loc=$ysub        ratio=1.0508

#############################
# Device Region Definitions #
#############################

# Entire Device Boundaries
region n=1 mat=Air type=out boundp=(0.0,$xl,$tpoly,$ysub)

# Substrate
region n=2 mat=Si type=mc boundp=(0.0,$xl,0.0,$ysub)

# Gate Oxide
region n=3 mat=SiO2 type=block boundp=($Gcon1,$Gcon2,$tox,0.0)

# Source Contact
region n=4 mat=Si type=contact boundp=(0.0,$Scon,0.0000,0.0001) \
       name="source"

# Drain Contact
region n=5 mat=Si type=contact boundp=($Dcon,$xl,0.0000,0.0001) \
       name="drain" usefermi=1

# Gate Contact
region n=6 mat=Poly type=contact boundp=($Gcon1,$Gcon2,$tpoly,$tox) \
       name="gate"

# Substrate contact
region n=7 mat=Si type=contact boundp=(0.0,$xl,$Bcon,$ysub) \
       name="substrate"

###################################
# Drain Current Estimation Regions #
###################################

# Near the Source Terminal
cregion boundp=($pt1,$pt3,0.0,0.08)
cregion boundp=($pt2,$pt3,0.0,0.08)

# Near the Drain Terminal
cregion boundp=($pt3,$pt4,0.0,0.08)
cregion boundp=($pt3,$pt5,0.0,0.08)
```

```
# Across the Entire Channel
cregion boundp=($pt1,$pt5,0.0,0.08)
cregion boundp=($pt2,$pt4,0.0,0.08)

############################
# Carrier Scattering Models #
############################

ssregion boundp=($SS1,$SS2,$tox,$ysub)
seregion boundp=($SS1,$SS2,$tox,$ysub)
matdef N=4 name="SiO2" eps=3.9 barrier=3.15 rough=0.0

############################
# Device Doping Definitions #
############################

# Substrate Definition
doping dopant=B conc=1.125e18 \
  boundp=(0.000,$xl,0.0,$ysub)

# Source Contact Definition
doping dopant=As conc=1e20 \
  boundp=(0.0000,$xcont,0.0,0.0001) \
  char =(0.0001,0.003,0.0001,0.014)

# Source LDD Definition
doping dopant=P conc=2e19 \
  boundp=(0.0000,$Gcon1,0.0,0.0001) \
  char =(0.0001,0.003,0.0001,0.015)

# Drain Contact Definition
doping dopant=As conc=1e20 \
  boundp=($xd,$xl,0.0,0.0001) \
  char =(0.003,0.0001,0.0001,0.014)

# Drain LDD Definition
doping dopant=P conc=2e19 \
  boundp=($Gcon2,$xl,0.0,0.0001) \
  char =(0.003,0.0001,0.0001,0.015)

# Gate Contact Definition
doping dopant=As conc=1e20 \
  boundp=($Gcon1,$Gcon2,$tpoly,$tox)

############################
# Drain Current Calculations #
############################

solve vgate=0.7 vdrain=0.7
tonyplot BD_current.log -set MC.set
tonyplot BD_sol.str -set mcdeviceex03_sol_str.set

quit
```

```
go atlas simflags="-P 8"

################################
# Global Variable Definitions #
################################

# Gate Oxide Thickness
set tox=0.0018
set toxmesh=$tox*(-1)
# Substrate Doping Level
set Na=1.125e18
# Gate Length
set Length=0.08
# S/D Contact Size
set xcont=0.05
# Source Contact Definition- Left Side
set xs=0
# S/D Junction Depth
set yj=0.03
# LDD Junction Depth (When Enabled)
set yjLDD=0.025
# LDD Length (When Enabled- Otherwise Ln=0)
set Ln=0.015
# S/D Contact Doping
set Nsd=1e20
# LDD Doping (When Enabled)
set NLDD=2e19
# Drain Contact Definition- Left Side
set xd=$xs+$xcont+$Length+2*$Ln
# End of Device Definition in the x Direction
set xl=$xd+$xcont
# Depth of Substrate
set ysub=0.08
# Electrode Spacing from Contact Edge
set co=0.02
# Lateral Characteristics of S/D Contacts
set lat=0.003
# Gate Height
set tpoly=$toxmesh-0.005
# Terminal Voltages
set Vdd=0.7
set Vgs=0.7
set Vds=0.7
set Vbs=0
# Energy Relaxation Time
set tau_e=0.1e-12

###################
# Mesh Definition #
###################

mesh space.mult=1.0

x.mesh loc=$xs                          spac=0.0275
x.mesh loc=($xs+$co)                    spac=0.0275
x.mesh loc=($xs+$xcont-$co)             spac=0.0150
x.mesh loc=($xs+$xcont+$Ln)             spac=0.0020
x.mesh loc=$xl/2                        spac=0.0020
x.mesh loc=($xd-$Ln)                    spac=0.0015
x.mesh loc=($xd+$co)                    spac=0.0150
x.mesh loc=($xd+$xcont-$co)             spac=0.0275
x.mesh loc=$xl                          spac=0.0275

y.mesh loc=$tpoly                       spac=0.1250
y.mesh loc=($toxmesh-0.005)             spac=0.0020
y.mesh loc=($toxmesh-0.0025)            spac=0.0010
y.mesh loc=$toxmesh                     spac=$tox/4
```

```
y.mesh loc=0.00                         spac=0.00005
y.mesh loc=0.0001                       spac=0.00005
y.mesh loc=0.0015                       spac=0.00005
y.mesh loc=0.0125                       spac=0.0015
y.mesh loc=$yj                          spac=0.0025
y.mesh loc=$ysub                        spac=0.0100

# Remove Un-Needed Node Points To The Left and Right of the Gate Contact
eliminate rows x.min=0 x.max=($xs+$xcont-0.001) \
          y.min=$tpoly y.max=-0.0001
eliminate rows x.min=($xd+0.001) x.max=$xl y.min=$tpoly y.max=-0.0001
eliminate rows x.min=0 x.max=($xs+$xcont-0.001) \
          y.min=$tpoly y.max=-0.0001
eliminate rows x.min=($xd+0.001) x.max=$xl y.min=$tpoly y.max=-0.0001

############################
# Device Region Definitions #
############################

# Substrate
region number=1 x.min=0 x.max=$xl y.min=0 y.max=$ysub material=Silicon

# Gate Oxide
region number=2 x.min=$xs x.max=$xl y.min=$toxmesh \
          y.max=0 material=SiO2

# Gate Poly
region number=3 x.min=($xs+$xcont+$Ln) x.max=($xd-$Ln) \
          y.min=$tpoly y.max=$toxmesh material=Poly

# Air/Vacuum
region number=4 x.min=0 x.max=($xs+$xcont+$Ln) y.min=$tpoly y.max=0 material=SiO2
region number=5 x.min=($xd-$Ln) x.max=$xl y.min=$tpoly y.max=0 material=SiO2

###################################
# Electrode and Contact Definitions #
###################################

electrode name=gate number=1 x.min=($xs+$xcont+$Ln) x.max=($xd-$Ln) \
          y.min=$tpoly y.max=$toxmesh
electrode name=source number=2 x.min=$xs x.max=($xs+$xcont-$co) \
          y.min=0 y.max=0
electrode name=drain number=3 x.min=($xd+$co) x.max=($xd+$xcont) \
          y.min=0 y.max=0
electrode name=substrate number=4 x.min=0 x.max=$xl y.min=$ysub y.max=$ysub

contact name=gate n.poly
contact name=source neutral exclude_near
contact name=drain neutral exclude_near
contact name=substrate neutral exclude_near

############################
# Device Doping Definitions #
############################

# Uniform Doping
doping uniform conc=$Na p.type regions=1

# Gate Doping
doping uniform conc=1e20 n.type regions=3

# Drain LDD Definition
doping gaussian junction=$yjLDD conc=$NLDD phosphorus x.left=($xd-$Ln) \
          x.right=($xd+$xcont) lat.char=$lat regions=1

# Source LDD Definition
doping gaussian junction=$yjLDD conc=$NLDD phosphorus x.left=$xs \
          x.right=($xs+$xcont+$Ln) lat.char=$lat regions=1
```

```
# Drain Contact Definition
doping gaussian junction=$yj conc=$Nsd arsenic x.left=$xd \
          x.right=($xd+$xcont) lat.char=$lat regions=1

# Source Contact Definition
doping gaussian junction=$yj conc=$Nsd arsenic x.left=$xs \
          x.right=($xs+$xcont) lat.char=$lat regions=1

material region=1 taurel.el=$tau_e taumob.el=$tau_e

# Plot of Device Structure
tonyplot -set contours2.set

##############################
# Electrical Simulation Setup #
##############################

# Model Summary
# hnsaug = Auger Recomb.; fldmob = Velocity Sat.; cvt & conmob = Mobility Degradation
# consrh = SRH Recomb.; fermidirac = Fermi-Dirac Stat's
# hcte.el = Energy Balance Transport Model

method block newton maxtrap=6
models conmob consrh cvt fldmob evsatmod=0 hnsaug ni.fermi fermidirac \
          hcte.el print temperature=300

###################
# Linear Vt Sweep #
###################

solve init
solve vdrain=0.05 vgate=-0.05

# Enable When Vbs > 0
#solve name=substrate vsubstrate=0.00625 vfinal=0.0125 vstep=0.00625
#solve name=substrate vsubstrate=0.05 vfinal=($"Vbs"-0.05) vstep=0.05
#solve vsubstrate=$"Vbs"

log outf=vt_lin.log
solve name=gate vgate=0 vfinal=$"Vgs" vstep=0.05

extract name="vt" \
(x.val from curve(abs(v."gate"),abs(i."drain")) where y.val=(2e-7/$"Length"))

# ID/VGS plot for Linear VT Extraction
tonyplot vt_lin.log

log off

############################
# Drain Current Calculation #
############################

log outf=ro_sweep.log
solve name=drain vdrain=0.10 vfinal=0.175 vstep=0.025
solve name=drain vdrain=0.20 vfinal=$"Vds" vstep=0.05

extract name="Idsmax" max(abs(i."drain"))

# ID/VDS plot
tonyplot ro_sweep.log -set idvd.set
tonyplot -set contours-V.set

log off

quit
```

Bulk-Driven MOSFET Differential Amplifier Example

MIXEDMODE Frequency Response Code

```
go atlas simflags="-P 8"

################################
# Global Variable Definitions #
################################

# Terminal Voltages
set Vdrain=0.7
set Vgate=0.7
set Vpwell=0.35
# Desired Drain Current
set Id=2e-5
set gdrain=$Id/($Vdrain-0.05)
set Ist=$gdrain*0.05-1e-9
# Energy Relaxation Time
set tau_e=0.1e-12
# Output Resistance of the Load Devices
set RL=250e3

################################
# MIXEDMODE Simulation Setup #
################################

.BEGIN

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$ MIXEDMODE Circuit Element Definitions                                    $
$ Element Node1 Node2 (Ref_Node1 Ref_Node2) DC_Value (AC_Value)           $
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

VG       1   0   0.05
VD       3   0   0.05
VINAC1   6   2   0.00   AC   0.5
VINAC2   2   7   0.00   AC   0.5
VINDC    2   0   0.05

GD1      3   4   3      0    $gdrain
Istart1  4   3   $Ist
RD1      4   3   $RL
GD2      3   8   3      0    $gdrain
Istart2  8   3   $Ist
RD2      8   3   $RL
ES       5   0   3      0    (0.1/0.7)

$ Import the BD MOSFET Structures from the ATLAS File on Page 101 (Width is in Microns)
AM1    6=pwell 4=drain 5=source 1=gate 1=nwell 0=substrate width=0.8
+      infile=MIXEDMODE.str
AM2    7=pwell 8=drain 5=source 1=gate 1=nwell 0=substrate width=0.8
+      infile=MIXEDMODE.str

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$ MIXEDMODE Circuit Analysis Definitions $
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

.LOG outfile=differential_amplifier
.NODESET V(1)=0.05 V(2)=0.05 V(3)=0.05 V(4)=0.05 V(6)=0.05 V(7)=0.05 V(8)=0.05
.OPTIONS M2LN RELPOT TEMP=300 TNOM=300

$ Relax the DC Tolerance & Increase the Number of Circuit/Device Iterations
$ Limit the Max. Allowable Change in a Node Voltage between Circuit/Device Iterations
.NUMERIC TOLDC=50e-3 IMAXDC=100 VCHANGE=0.7

$ Ramp Up the DC Terminal Voltages to Their Final Values
.DC VG      0.10   $Vgate    0.05
```

```
.DC VINDC   0.10   $Vpwell   0.05
.DC VD      0.10   $Vdrain   0.05

$ Sweep the Input Voltage vs. Frequency
.AC DEC 3 1e5 1e10

.END

########################################
# ATLAS Model Statements for AM1 and AM2 #
########################################

models device=AM1 region=1 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=2 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=3 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=4 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=5 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=6 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=7 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=8 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=9 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=10 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=11 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=12 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=13 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=14 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=15 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=16 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print

models device=AM2 region=1 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=2 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=3 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=4 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=5 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=6 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=7 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=8 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=9 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=10 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=11 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=12 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=13 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
```

```
models device=AM2 region=14 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=15 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM2 region=16 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print

##########################################
# ATLAS Material Statements for AM1 and AM2 #
##########################################

material device=AM1 region=1 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=2 bqp.ngamma=1.3 bqp.nalpha=1 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=3 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=4 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=5 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=6 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=7 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=8 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=9 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=10 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=11 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=12 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=13 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=14 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=15 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=16 bqp.ngamma=0 bqp.nalpha=0

material device=AM2 region=1 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM2 region=2 bqp.ngamma=1.3 bqp.nalpha=1 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM2 region=3 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM2 region=4 bqp.ngamma=0 bqp.nalpha=0
material device=AM2 region=5 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM2 region=6 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM2 region=7 bqp.ngamma=0 bqp.nalpha=0
material device=AM2 region=8 bqp.ngamma=0 bqp.nalpha=0
material device=AM2 region=9 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM2 region=10 bqp.ngamma=0 bqp.nalpha=0
material device=AM2 region=11 bqp.ngamma=0 bqp.nalpha=0
material device=AM2 region=12 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM2 region=13 bqp.ngamma=0 bqp.nalpha=0
material device=AM2 region=14 bqp.ngamma=0 bqp.nalpha=0
material device=AM2 region=15 bqp.ngamma=0 bqp.nalpha=0
material device=AM2 region=16 bqp.ngamma=0 bqp.nalpha=0

########################################
# ATLAS Impact Statements for AM1 and AM2 #
########################################

impact device=AM1 region=1 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=2 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=3 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=5 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=6 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=9 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=12 toyabe tausn=$tau_e tausp=$tau_e
```

```
impact device=AM2 region=1 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM2 region=2 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM2 region=3 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM2 region=5 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM2 region=6 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM2 region=9 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM2 region=12 toyabe tausn=$tau_e tausp=$tau_e

############################
# ATLAS Method Statements #
############################

# Relax the Carrier Concentration and Carrier Temperature Tolerances
# Reduce the BQP Model Iterations

method block newton nblockit=1 clim.eb=1e15 tmin.fact=0.2 bqpr.tol=1e-20 \
       itlimit=50

################################################
# Restart ATLAS to Plot the MIXEDMODE AC Results #
################################################

go atlas
tonyplot differential_amplifier_ac_1.log -set AC.set

quit
```

MIXEDMODE Input Common-Mode Range Code

```
go atlas simflags="-P 8"

################################
# Global Variable Definitions #
################################

# Terminal Voltages
set Vdrain=0.7
set Vgate=0.7
set Vpwell=0.7
# Desired Drain Current
set Id=2e-5
# Energy Relaxation Time
set tau_e=0.1e-12

################################
# MIXEDMODE Simulation Setup #
################################

.BEGIN

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$ MIXEDMODE Circuit Element Definitions                                    $
$ Element Node1 Node2 (Ref_Node1 Ref_Node2) DC_Value (AC_Value)            $
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

VG     1    0    0.05
VD     3    0    0.05
VIN    2    0    0.05    AC    1

RD     3    4    15000
RS     5    0    1e6
IS     5    0    2e-8

$ Import the BD MOSFET Structure from the ATLAS File on Page 101 (Width is in Microns)
$ Half-Circuit Analysis Only
AM1       2=pwell 4=drain 5=source 1=gate 1=nwell 0=substrate width=3.4
+         infile=MIXEDMODE.str

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$ MIXEDMODE Circuit Analysis Definitions $
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

.LOG outfile=single_device
.NODESET V(1)=0.05 V(2)=0.05 V(3)=0.05 V(4)=0.05 V(5)=0.00
.OPTIONS M2LN RELPOT TEMP=300 TNOM=300

$ Relax the DC Tolerance & Increase the Number of Circuit/Device Iterations
$ Limit the Max. Allowable Change in a Node Voltage between Circuit/Device Iterations
.NUMERIC TOLDC=35e-3 IMAXDC=100 VCHANGE=0.7

$ Ramp Up the DC Terminal Voltages to Their Final Values
.DC VG         0.10    $Vgate     0.05
.DC VD         0.10    $Vdrain    0.05
.DC IS    DEC  1e-6    $Id        10
.DC VIN        0.00    $Vpwell    0.05

.END

#################################
# ATLAS Model Statements for AM1 #
#################################

models device=AM1 region=1 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
        ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=2 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
        ni.fermi fermidirac hcte.el bqp.n bbt.kl print
```

```
models device=AM1 region=3 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=4 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=5 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=6 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=7 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=8 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=9 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=10 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=11 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=12 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=13 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=14 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=15 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print
models device=AM1 region=16 conmob consrh bgn cvt fldmob evsatmod=0 hnsaug \
       ni.fermi fermidirac hcte.el bqp.n bbt.kl print

####################################
# ATLAS Material Statements for AM1 #
####################################

material device=AM1 region=1 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=2 bqp.ngamma=1.3 bqp.nalpha=1 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=3 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=4 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=5 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=6 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=7 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=8 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=9 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=10 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=11 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=12 bqp.ngamma=0 bqp.nalpha=0 taurel.el=$tau_e \
       taumob.el=$tau_e
material device=AM1 region=13 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=14 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=15 bqp.ngamma=0 bqp.nalpha=0
material device=AM1 region=16 bqp.ngamma=0 bqp.nalpha=0

###################################
# ATLAS Impact Statements for AM1 #
###################################

impact device=AM1 region=1 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=2 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=3 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=5 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=6 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=9 toyabe tausn=$tau_e tausp=$tau_e
impact device=AM1 region=12 toyabe tausn=$tau_e tausp=$tau_e
```

```
############################
# ATLAS Method Statements #
############################

# Relax the Carrier Concentration and Carrier Temperature Tolerances
# Reduce the BQP Model Iterations

method block newton nblockit=1 clim.eb=2e15 tmin.fact=0.2 bqpr.tol=1e-20 \
       itlimit=50

################################################
# Restart ATLAS to Plot the MIXEDMODE DC Results #
################################################

go atlas
tonyplot single_device_dc_4.log -set DC-SD.set

quit
```