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Effects of Solder Paste Volume on PCBA Assembly Yield and Reliability

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EFFECTS OF SOLDER PASTE VOLUME ON PCBA ASSEMBLY
YIELD AND RELIABILITY

By

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Abstract

Solder paste printing is the most common method for attaching surface mount devices to printed circuit boards and it has been reported that a majority of all assembly defects occur during the stencil printing process. It is also recognized that the solder paste printing process is wholly responsible for the solder joint formation of leadless package technologies such as Land Grid Array (LGA) and Quad-Flat No-Lead (QFN) components and therefore is a determining factor in the long-term reliability of said devices. The goal of this experiment is to determine the acceptable lower limit for solder paste volume deposit tolerances during stencil printing process to ensure both good assembly yield and reliability expectations. Stencils with modified aperture dimensions at particular locations for LGA and QFN package footprints were designed in order to vary the solder paste volume deposited during the stencil printing process. Solder paste volumes were measured using Solder Paste Inspection (SPI) system. Low volume solder paste deposits were generated using the modified stencil designs to evaluate assemble yield. Accelerated Thermal Cycling (ATC) was used to determine the reliability of the solder joints. For the LGAs, solder joints formed with higher paste volume survived longer in ATC compared to lower volume joints. Low solder paste volume deposits did not affect BGA devices in ATC. Transfer efficiency numbers for both good assembly yield and good reliability are reported for LGA, QFN and BGA devices. This research provides valuable data because, very little data is available on solder paste volume tolerance limits in terms of assembly yield and reliability. Manufacturers often use ±50% of stencil aperture volume with no evidence of its effectiveness in determining yield and reliability of the solder joints.

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List of Abbreviations

SMT   Surface Mount Technology

SMD   Surface Mount Device

THT   Through Hole Technology

SPI   Solder Paste Inspection

PCB   Printed Circuit Board

ATC   Accelerated Thermal Cycling

LGA   Land Grid Array

BGA   Ball Grid Array

QFN   Quad-Flat-No-Leads

TAL   Time Above Liquidus

TE   Transfer Efficiency

BTC   Bottom Terminated Components

CTE   Coefficient of Thermal Expansion

SA   Standard Aperture

UA   Undersized Aperture

Chapter 1: Introduction to Research

1.1 Introduction

Integrated circuits are packed in different kinds of packages to protect them from heat, humidity, electrical discharges and other environmental factors which may affects the functionally of the integrated circuit. These packages provide electrical connections between various components and the PCB and help to make the assembly of the integrated circuit on to the printed circuit boards (PCB's) an easy process. There are two major assembly techniques used to assemble these packages on to the PCB, Through-Hole Technology (THT) and Surface Mount Technology (SMT). Through-hole technology refers to the mounting scheme used for electronic components that involves the use of leads on the components that are inserted into holes drilled in the PCB and soldered to pads on the opposite side either by manual assembly (hand placement) or by the use of automated insertion mount machines. Figure 1 shows a graphic of a PCB assembled with THT.
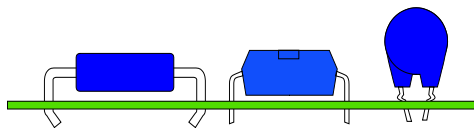
Figure 1 Through Hole Technology

SMT is a method of attaching components on to the PCB surface directly with solder paste. A fully automated SMT assembly line requires a stencil printer, component

placement machine and a reflow oven. Electronic devices designed for this technology are called Surface-Mount Devices (SMD). SMT has almost replaced the traditional through-hole technology (THT) in the current industry. Both technologies can be used on the same boards according to the product requirement. Figure 2 represents a graphic of a PCB assembled using SMT.
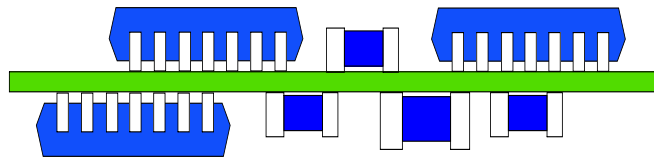
Figure 2 Surface Mount Technology

Some of the package types used for SMT either have solder balls attached to the bottom of the package like Ball Grid Arrays (BGA's) or have flat surface without any leads like Land Grid Arrays (LGA's) and Quad Flat No Leads (QFN's) also known as Bottom Terminated Devices (BTCs).

Majority of defects in SMT process can be related to stencil printing process (Biemans 2011).
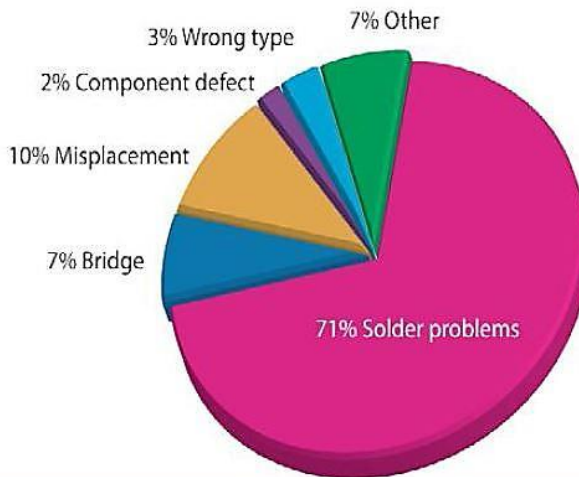
Figure 3 Break down of SMT defect (Biemans,2011)

A reliable solder joint is dependent on the solder paste volume deposition on the PCB during stencil printing process. Different package types have different solder paste volume requirements. To eliminate the defects during stencil printing process solder paste inspection machines (SPI) are being used to screen the PCB's after stencil printing process. The SPI machine scans the PCB's with a shadow moiré technique and high resolution cameras to calculate the solder paste deposit volume. This can then be used to determine if the deposit is acceptable based on the tolerances set by the operator.

1.2 Problem Statement

The SPI tolerance limits are determined subjectively. Review of literature also indicates that there is little research done on the determination of SPI tolerance limits. Many manufacturers set the allowable paste volume tolerance to +/-50% of the stencil aperture volume with little or no evidence of its effectiveness in determining yield and reliability of the solder joints. As defects occur only after the reflow process, effective

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determination of SPI tolerance limits should be based on feedback from post-reflow inspection (Huang C 2011) and reliability testing. SPI machine set up with incorrect tolerance limits would become ineffective in catching print related defects. So the problem of subjective SPI tolerance limits is addressed in this report, by determining SPI tolerance limits based on assembly yield results and reliability results.

1.3 Research Objective

The goal of this research is to determine the SPI tolerances limits for different package types to achieve good yield and reliability. Different stencil designs with different aperture sizes configurations are used to vary the solder paste volume. The SPI tolerance limits are determined from assembly yield data and reliability data generated from this experiment.

1.4 Research Methodology

This thesis work is performed in two stages. In stage one, several boards were printed and paste volume data was collected and analyzed. Based on the print volume data several stencil designs were designed. All the stencils used were stainless steel laser cut stencils from DEK. At the end of stage one SPI tolerance limits for good assembly yield were determined. In stage two all the boards assembled with SPI tolerance limits from stage one were subjected to Accelerated Thermal Cycling (ATC) and reliability of those packages were determined in terms of paste volume. Suggestions for SPI tolerance limits were made to achieve high assembly yield and good reliably. A detailed explanation of the experiment procedure is given in chapter 3.

Chapter 2: Literature Review

2.1 Introduction

SMT is the process of soldering electronic components onto the conductive pads of PCB. The SMT process consists of three sub-processes: printing solder paste onto the substrate, automatic placement of components onto their designated locations and reflow of the substrate along with components to form a solder joint. The Literature Review shows that 52-71% of SMT defects can be attributed to the solder paste printing process (Jianbiao Pan 1999). As the trend of product miniaturization continues to happen, the need for assembling area array type packages with high I/O increases. The assembly of these area array packages involves depositing very small solder paste deposits, wherein the surface tension effects are dominant over the viscous flow of the solder paste. For this reason, printing of solder paste through small apertures usually results in stencil clogging and incomplete paste transfer. An in-depth understanding of how to screen the defects is needed to achieving acceptable print yields.

2.2 Solder Paste Printing

In the solder paste printing process, solder paste is deposited onto the PCBs before placing the components with the help of a stencil printer. The advantage of doing it is to achieve high production speed and cost reduction, stencil printing is widely adopted in the industry for solder paste printing.

According to (Amalu 2011), controlling the exact amount of solder paste deposited on the PCB is one of the main challenges at second level packaging. The solder paste deposited on the solder pads varies from pad to pad within a PCB, and it also varies from one PCB to another. This inconsistency is because of many variables involved in the stencil printing, and the problem of not achieving consistent printing becomes worse with fine pitch apertures. Hence, there is a need for a better understanding of solder paste printing process (Amalu 2011). According to (Nguty 1999) the quality of solder paste printing process is dominated by the flow of solder paste into the stencil aperture and the aperture emptying process. The Solder paste must have the ability to deform easily into the stencil aperture when sheared and flow out of the stencil aperture during paste release (Durairaj 2001). According to (Yang 2005) three sequential stages in stencil printing proces are illustrated in Figure 4. In the first stage, a squeegee forces the solder paste to roll in front of its blade for some distance before shearing off the paste in stencil apertures as the squeegee moves over the stencil. In the second stage, the hydrodynamic pressure that is generated during the paste roll injects the solder paste into the stencil apertures. Finally,

in the third stage, solder paste is left on the pad of the substrate after the PCB is mechanically separated from the stencil. As the board moves away from the stencil, the solder paste experiences forces at the pad surface and aperture walls. As shown in Figure 5, the adhesive frictional force operating between the stencil walls and the solder paste competes directly with the adhesive pull force between the solder paste and the PCB bond pad. The net force determines the final release of paste from the stencil aperture (Durairaj 2001).
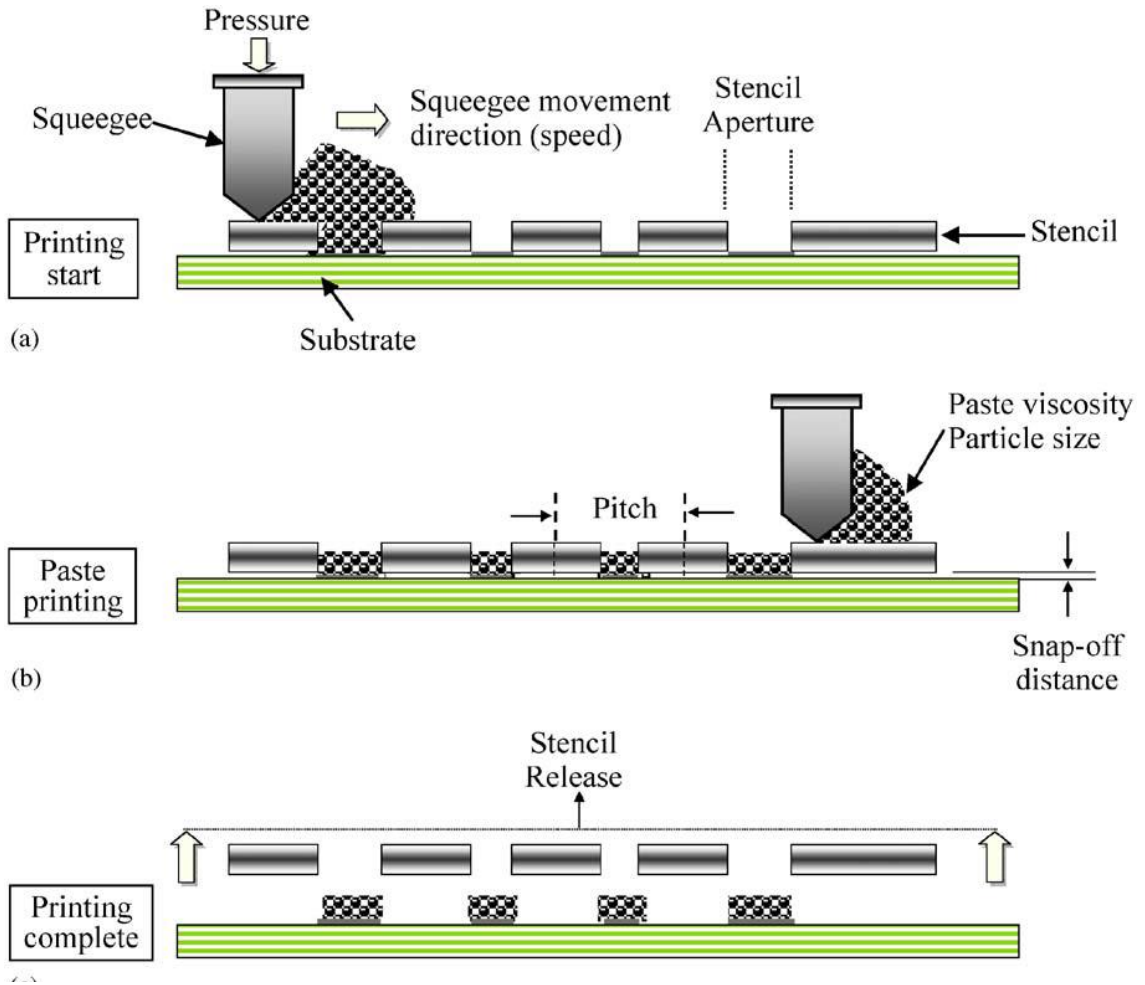
Figure 4 Stencil Printing Process (Pan,1999)
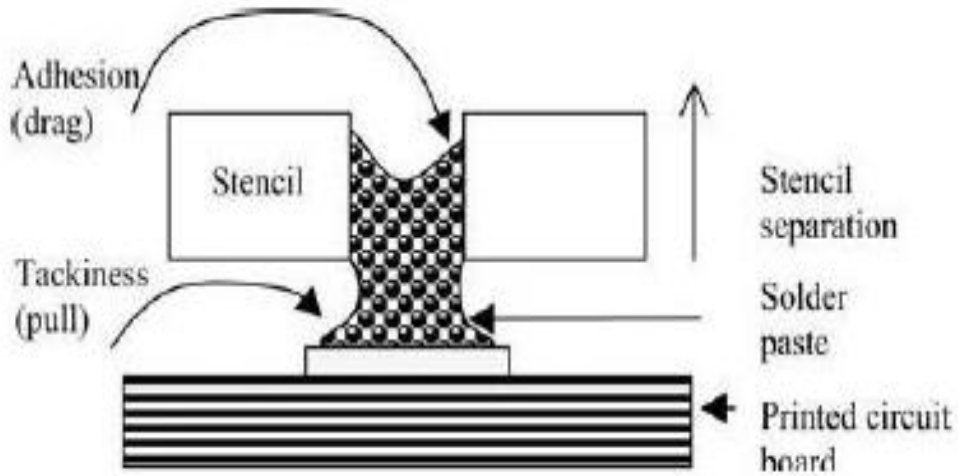
Figure 5 Aperture Emptying Process (Durairaj, 2001)

2.2.1 Factors affecting solder paste printing

A number of process parameters influence the solder paste printing process. According to (Haslehurst.L. 1996), the process parameters can be categorized into four groups: printer, paste, environmental and stencil. Squeegee pressure, squeegee speed, stencil separation speed and print direction are the key processes in stencil printing. Literature Review indicates that area ratio and aspect ratio are important factors in addressing the challenges of solder paste printing (Durairaj 2001), showed experimentally that aspect ratio should be higher than 1.25 and area ratio should be greater than 0.6. Paste transfer is also directly impacted by particle size and other paste related properties.

2.2.1.1 Aspect ratio and Area ratio

Aspect ratio is defined as the ratio of aperture width (W) to the stencil thickness (T).

$$\text{Aspect Ratio} = \frac{Aperture\ Width}{Stencil\ Thickness} = \frac{W}{T} \quad \text{(Durairaj 2001)}$$

Area ratio is defined as the ratio of the area of the aperture opening (L*W) to the area of the aperture wall (2T * (L+W))

$$\text{Area Ratio} = \frac{Area\ of\ aperture\ opening}{Area\ of\ aperture\ wall} = \frac{L*W}{2*T*(L+W)} \quad \text{(Durairaj 2001)}$$

The dimensions of stencil aperture used in the calculation of Aspect ratio and Area ratio are illustrated in Figure 6.
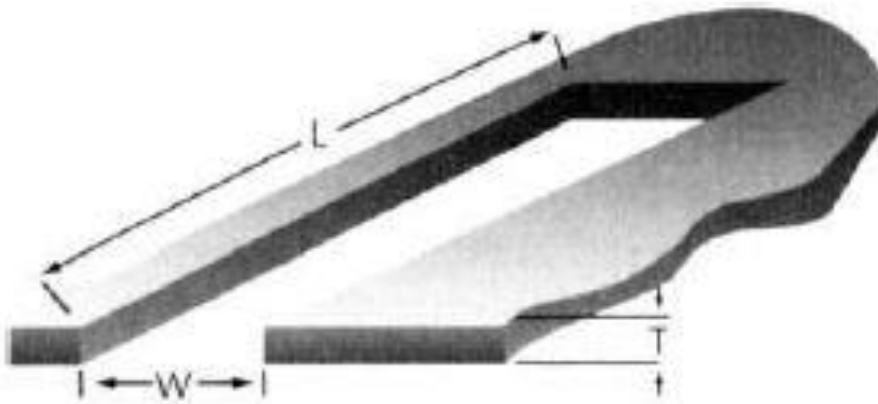
Figure 6 Dimensions of stencil aperture (Burr, 1998)

(Amalu 2011), grouped the critical variables, that influence the solder paste deposition, into five categories: Solder Paste, Stencil, Substrate, Printer and Environmental parameters that are shown in Figure 7. The stencil and substrate parameters do not change during the manufacturing process, but the remaining three of the five parameters stated above, vary either automatically or on their own. A change in properties of the solder paste during printing process significantly impacts the paste transfer efficiency.
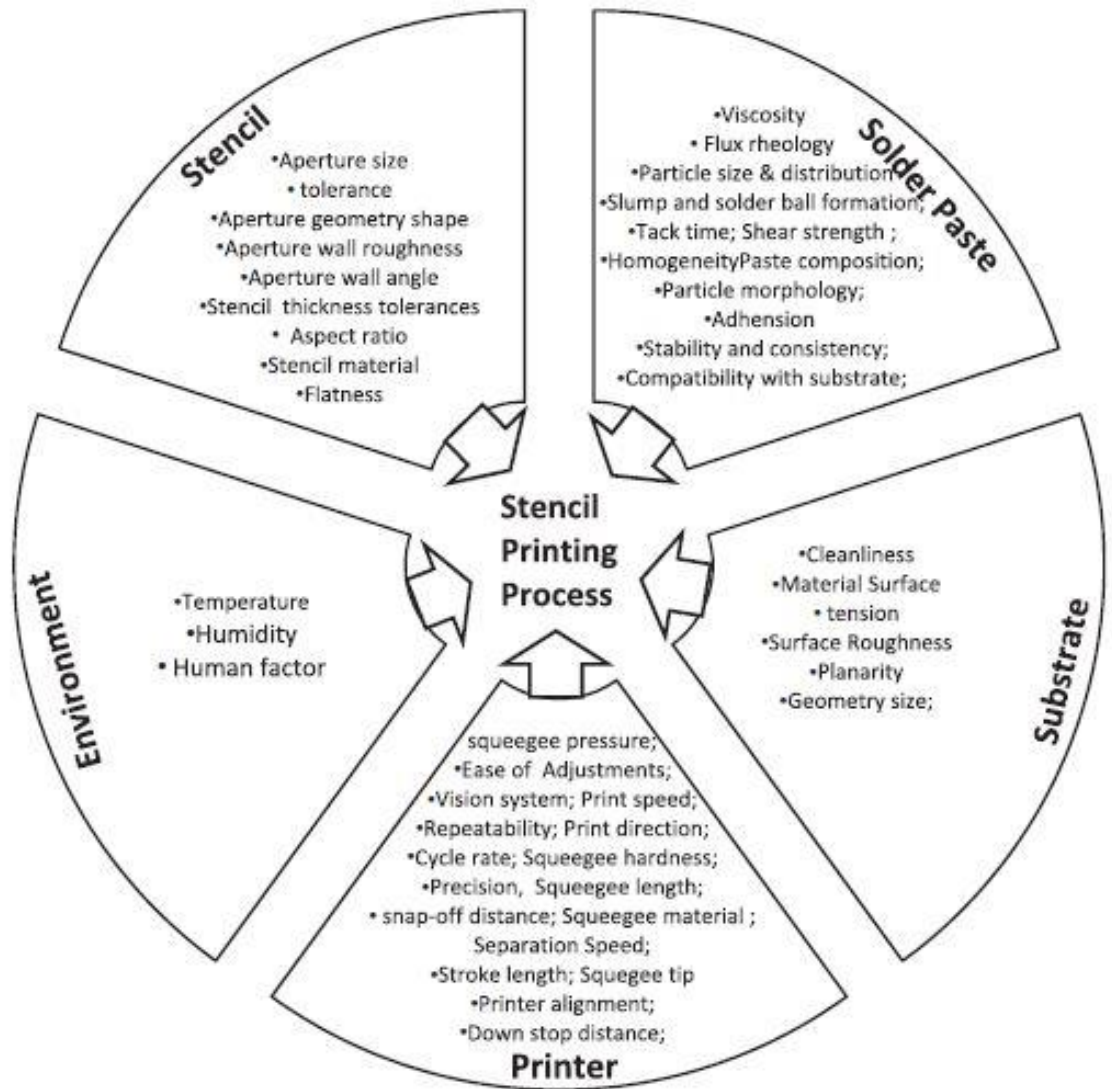
Figure 7 Solder paste printing variables (Amalu, 2011)

(Yang 2005), proposed "a hierarchical view of influence variables of the stencil printing" that is shown in Figure 8.
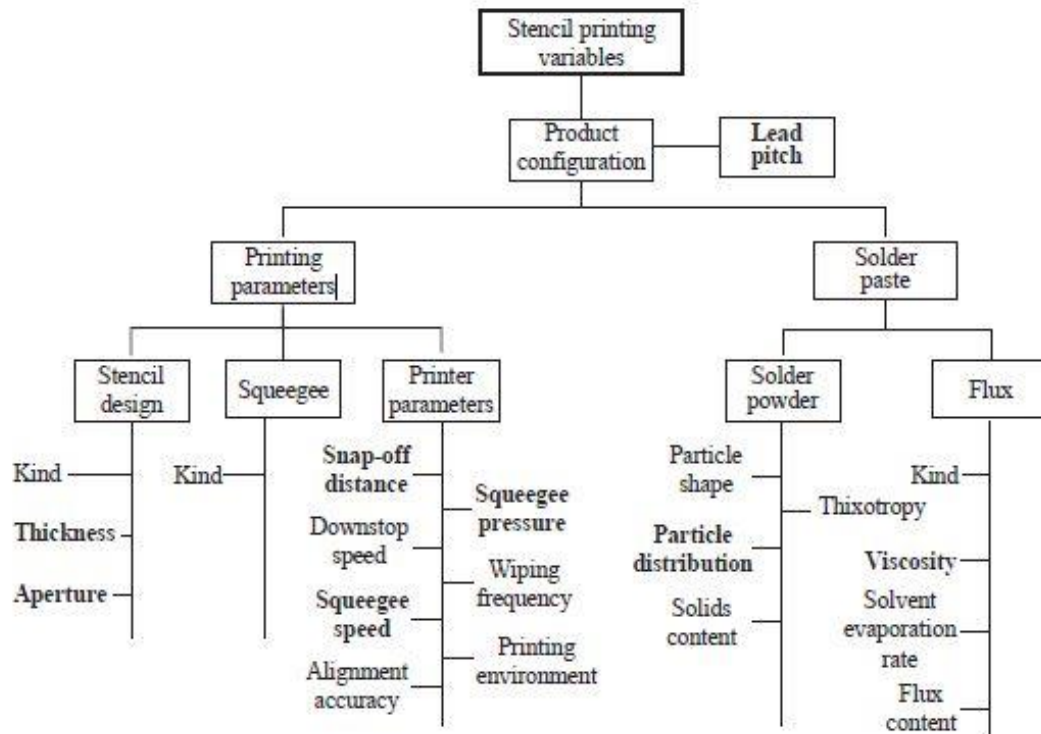
Figure 8 A hierarchical view of influence variables of stencil printing (Yang, 2005)

2.2.2 Evaluation of the solder paste printing process

(Lau 1997), evaluated the solder paste printing process and developed the five level hierarchies for the solder paste printing process and states that such hierarchical evaluation of the solder paste printing process is essential for improving the concerned process. According to (Lau 1997), following are the five major factors that determine the quality of solder joint: (i) The choice of stencil opening geometry; (ii) The matching of the solder paste; (iii) The control of the waiting time (iv) The selection of the squeegee material; and (v) The parameter setting of printing machine. Descriptions of the five factors mentioned are as follows:

2.2.2.1 Choice of stencil opening geometry

Chemical etching, laser cutting, and electroforming are the three different stencil fabrication processes that are used in the stencil manufacturing industry. The Chemical etching process usually produces a knife edge shaped aperture opening, which affects the release of solder paste especially when the aperture opening is less than 25µm. Therefore, an additional process called electropolishing is employed after chemical etching, to smoothen the knife edge shaped aperture openings. The laser cutting process yields a stencil opening such that the bottom is slightly larger than the top, and such internal taper on aperture walls favors the better release of solder paste from the stencil. The electroforming process can produce a stencil with very fine and smooth aperture with vertically tapered walls. The stencils fabricated through the electroforming process favors a smooth release of solder paste even at fine pitch aperture openings (Lau, 1997).

2.2.2.2 Matching of solder paste

The quality of the solder paste printing process is greatly influenced by the composition of solder paste and its corresponding properties. Few characteristics of the solder paste, such as viscosity, wetting, metal composition, particle shape and size, and also the flux activity play a significant role in the solder paste printing process (Lau, 1997).

2.2.2.3 Control of waiting time

The wait time of the solder paste after being deposited onto their designated solder pads affects the solder joint quality. This is because after solder paste printing, the paste slumps, spreads and absorbs moisture from the environment. The slumping effect gets more significant for fine pitch components than when compared with normal components. Excessive wait time can also lead to other defects such as solder balls. Therefore, the wait time before reflow should be controlled (Lau, 1997).

2.2.2.4 Selection of squeegee material

A squeegee is used to spread the solder paste across the stencil and allow the transfer of solder paste through the stencil onto the PCB. A harder squeegee favors better paste transfer when compared to a softer squeegee. A soft squeegee is preferred while using a stepped stencil. However, using a soft squeegee may cause scooped printing, due to the spring back property of the soft squeegee. A metal squeegee, usually made from stainless steel, is used as a hard squeegee, and it does not create scooping problem (Lau, 1997).

2.2.2.5 Settings of solder printing process

The solder paste printing process is highly affected by five print machine parameters. Those are printing pressure, printing speed, snap off, parallelism of the squeegee, and the squeegee angle. "Environmental conditions such as humidity and temperature also impact the solder printing process" (Lau, 1997). The effects of the parameters mentioned above are explained below

Low print speed may lead to inconsistent fill in of stencil apertures because the low squeegee speed may not favor the roll of solder paste in front of the squeegee. High print speed will cause loss of viscosity in the solder paste that may lead to slumping and misprint. High pressure may push down the squeegee into stencil apertures and scoop out some of the solder paste. On the other hand, if the squeegee pressure is too light, the solder paste may not adhere to the solder pads. The distance to which the PCB is mechanically separated at a controlled speed is known as the snap-off distance. The squeegee angle is the angle at which the squeegee gets in contact with the stencil. The squeegee angle affects the forces that are required to roll the solder paste in front of the squeegee and push the solder paste into the stencil apertures. When the squeegee travel direction is perpendicular to the longer side of the stencil aperture, then the aperture is called a perpendicular aperture. When the squeegee travel direction is parallel to the longer side of the stencil aperture, then the aperture is called parallel aperture. Both perpendicular and parallel apertures are shown in Figure 9. (Jianbiao Pan 1999), showed experimentally that a stencil with perpendicular apertures can deposit 5-6% more volume than a stencil with parallel apertures.
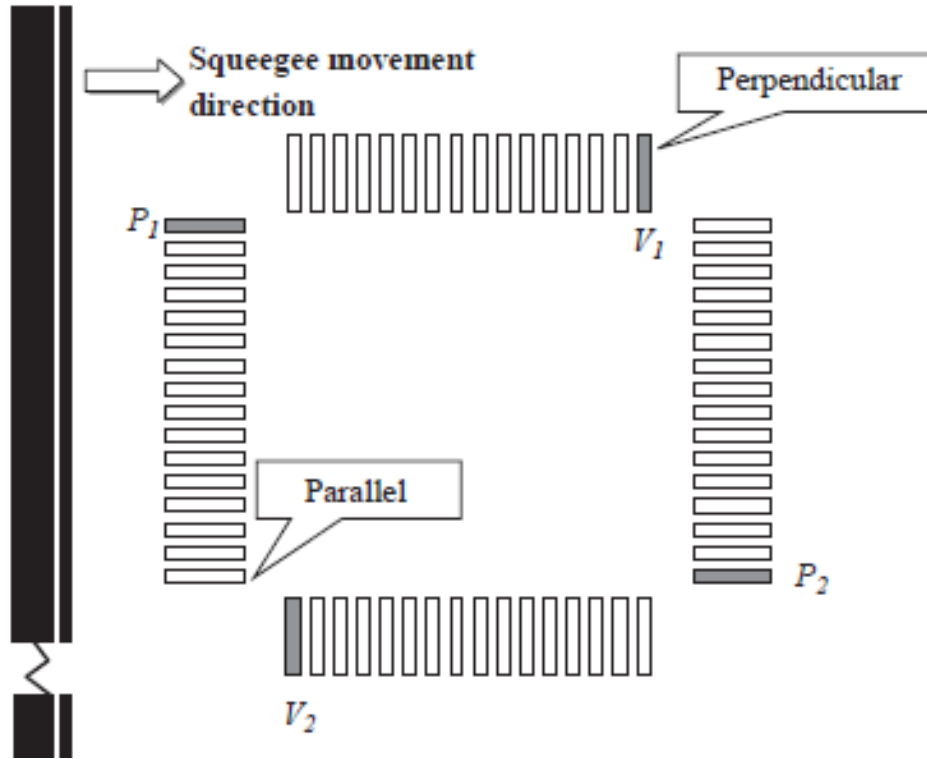
Figure 9 Perpendicular and Parallel Apertures (Pan, 1999)

2.2.3 Solder paste rheology

For several reasons such as low cost, a low melting point when compared to its alternatives, good mechanical strength and comparatively good solderability, Sn-Ag-Cu(SAC) solder alloy is considered as the most promising lead-free solder alloy (Kim 2003). As the print quality of the solder paste is directly impacted by its rheological properties such as flow, slump resistance, and tack value, rheology of solder paste is gaining significance (Mallik 2008), proposed that microscopic distributions of solder powders strongly affect the rheological behavior of the solder paste. The solder paste is considered as a non-Newtonian fluid that exhibits thixotropic behavior. Amalu, et al. (2011), established the way the transfer efficiency of lead-free solder is affected by "solder paste rheology and stencil aperture cavity size" (Amalu 2011). According to (Durairaj 2001), consistent withdrawal of the solder paste is highly dependent on the paste rheology at minuscule aperture sizes. This is because the surface tension dominates viscous flow at smaller aperture sizes and, therefore, impacts the paste transfer efficiency. The constituents of the solder flux are shown below, in Figure 10.
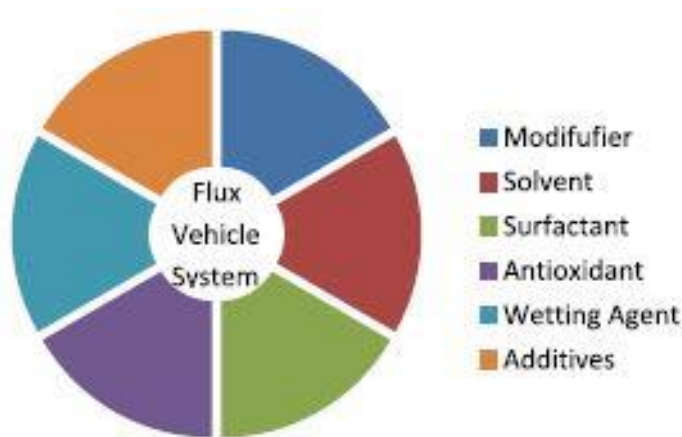
Figure 10 Constituents of solder flux (Amalu, 2011)

2.2.4 Optimization of stencil printing parameters

Stencil print parameters play a key role in improving the SMT yield. This section lists the important print parameters and the research that have been done in the optimization of those key print parameters.

(Sekharan 2006), conducted a half factorial DOE by considering five factors at two levels and obtained optimal settings for a solder paste printing process. squeegee pressure, squeegee speed, snap off, separation speed and stencil wipe frequency were the five different factors that were considered for performing the DOE. The height of the solder paste deposition was considered as a response variable. The interactions of the snap off and the separation speed, the print speed and the squeegee pressure, and the separation speed and the stencil wipe frequency were identified as significant interactions that influenced the solder paste height deposition. The results of the DOE indicated that among the two levels chosen for each factor, a high squeegee pressure, high printing speed, low snapoff , low separation speed were part of optimal print parameters. The authors have also shown a 20% percent improvement in response variable by performing a validation run with the optimal print parameters.

Pan, et al. (2004), identified the critical variables that influence the height, area, and volume of the solder paste deposition. The authors used ANOVA to examine the influence of aperture size and shape, thickness of the stencil, surface finish of the board, solder paste type and print speed on the solder paste deposition. Their analysis has shown that thickness of the stencil and size of the aperture are the two most critical variables that influence the solder paste deposited.

(Liu 2006), employed a Taguchi DOE approach to investigate the effect of the stencil thickness, the squeegee pressure, the PCB separation speed, and the squeegee speed on the stencil printing process. The transfer efficiency of solder paste volume was considered as a response variable in the experiment. Out of the four factors studied, stencil thickness had an obvious effect on the volume transfer efficiency. The PCB separation speed and the squeegee printing speed had a minor effect, and squeegee pressure had no significant effect on the response variable. Quicker separation of the PCB contributed towards a higher transfer efficiency.

2.3 SMT defects due to poor solder paste printing

The usage of miniature components continues to increase as the demand for small handheld devices is increasing day-by-day. The manufacturing defects that occur during the assembly of the components can affect the service life of the small handheld devices. Hence, there is a requirement to understand these defects and stop/control these defects at the assembly level. According to (Ladani 2008) the most frequent defects such as smear, insufficient solder, component shift, tombstoning, and solder bridging, are directly related to solder paste printing and solder reflow process. The following section of this report includes a brief description of several defects that are related to poor solder paste printing.

2.3.1 Insufficient solder

Insufficient solder is a common problem at the stencil printing stage. Here the aperture clogging does not allow complete transfer of solder paste and, as a result, the deposited solder volume is less than target solder volume. Insufficiency is caused by a few factors such as (1) Inadequate paste rheology (2) stencil thickness (3) aperture orientation (4) pitch dimension (5) improper aperture design (6) insufficient squeegee pressure (7) powder size (8) poor aperture quality. According to (Lee 2001), as the pitch decreases below 30mils, the print defect rate increases very rapidly. At a pitch below 30 mils, insufficiency becomes a dominant defect because clogging of the stencil aperture increases with decreasing aperture size (Lee 2001) as shown in Figure 11.
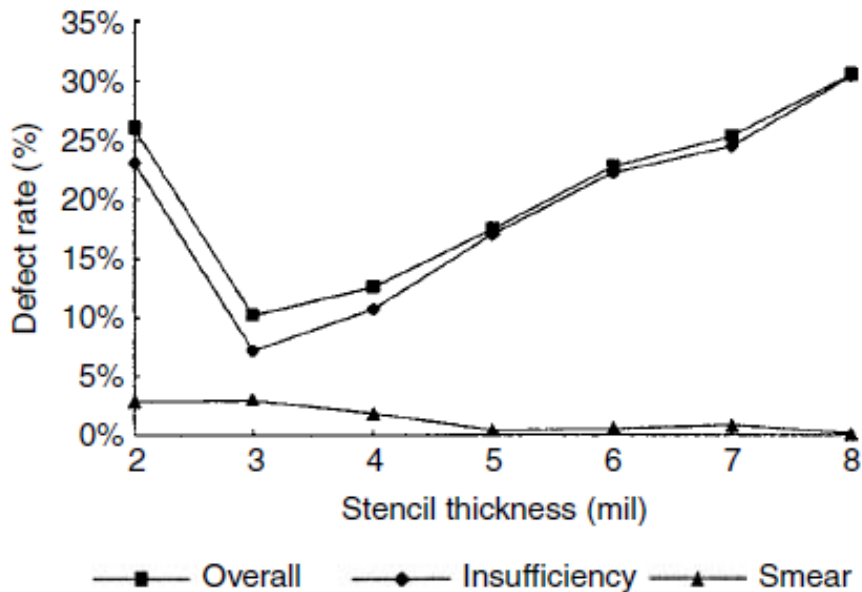
Figure 11 Effect of stencil thickness on print defects (Lee, 2001)

2.4 Solder Paste Inspection

2.4.1 Need for Solder Paste Inspection

The solder paste printing process is a crucial assembly process in SMT that determines the quality of the solder joints. According to (Burr, 1997) the solder paste printing process is considered a "black art" because there are 39 variables involved in the solder paste printing process and the relationship between those 39 variables is not completely understood. The volume of the solder paste deposited onto the PCB is considered to be a good predictor of solder joint reliability and for this reason; an ideal printing process is aimed at achieving consistent volume on a repeatable basis (Biemans 2011).

The boards rejected due to defects would either be reworked or scrapped. Rework is a non-value adding process, and it requires excessive cost and resources. If not properly controlled, reworked solder joints can be less reliable and susceptible to fail. Reworked solder joints are less reliable and are vulnerable to fail at customer site which can lead to expensive warranty repairs. Scrapping a board incurs additional cost to the manufacturer and also affects their product delivery timelines. The excess cost of rework and constant market pressure to reduce cycle time has driven the manufacturer to look for ways to reduce or eliminate defects upstream in the process (Burr, 1997).

Value added to the board increases as the board moves from one stage to another. Because of this reason, it is desirable to catch and prevent defects at an early stage. Washing a misprinted board consumes much less cost and resources than the resources consumed in reworking a fully processed board. Rework cost can be estimated by using

the 10X rule, which states that the rework cost at each stage will be ten times greater than that in the previous stage. For instance if correcting a misprint of solder paste is calculated to be $0.50, correcting the failure after reflow would cost $5.00 and correcting the same failure after the board is integrated into the system would cost $50.00. If somehow the defect escapes from all the inspection stages and the board fails at the customer site, the cost to recall the product and correct it could be as high as $500.00 or even more (Riddle 2007). The 10X rule could easily justify the cost and resources invested in setting up a SPI machine and implementing an in-line solder paste inspection. The 10X rule explained in *Figure 12*. Many electronics manufacturing services providers have a market requirement to perform 100% solder paste inspection. "These factors combined with the ongoing need for continuous process improvement drives the need for solder paste inspection" (Gunn 2001).
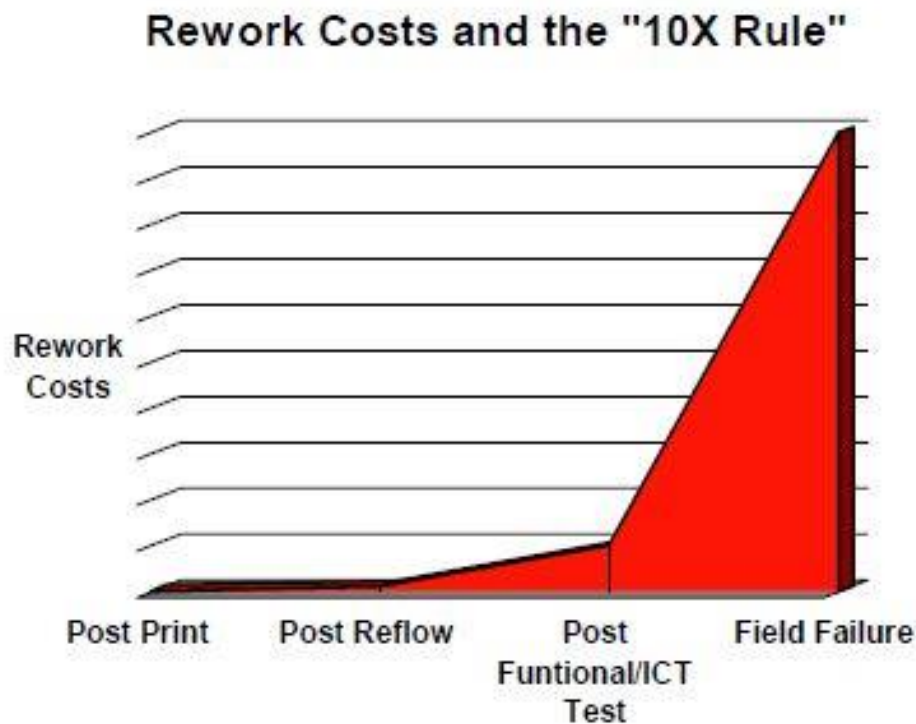
Figure 12 Rework cost and 10X rule (Riddle, 2007)

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Inspection of the solder paste after printing is a potential way to eliminate or reduce most of the defects. Numerous publications are available online which reiterate the importance of an in-line SPI machine. According to (Johnson 2003), if a SPI machine is useful for stopping at least a few customer site board failures, the investment made on the SPI machine would be recovered within a short period. According to Daniels (1996), EMS providers believe that their profit margins can be increased by increasing the process quality but not by quoting higher prices or by lowering quality standards. The profit that manufacturers gain by supplying products with long term reliability is immeasurable. For these reasons, many manufacturers are starting to give importance to inspecting boards immediately after solder paste printing by deploying in-line SPI machines. However, SPI does not eliminate the need for post-reflow inspection stages such as visual inspection, AOI, Automatic X-ray Inspection (AXI), and In-Circuit Test (ICT) (Burr, 1997).

2.4.2 Determining Solder Paste Inspection (SPI) variance

(Chen 2011), worked on determining reasonable SPI tolerance limits based on solder paste volume distribution obtained from mass production data collection. The SPI tolerance limits were determined for certain packages on three different production boards. To determine SPI tolerance limits, the authors collected SPI data of certain packages on three production boards and related the data to inspection feedback from Automatic X-ray Inspection (AXI). The SPI tolerance limits for different packages are summarized in Table 1,Table 2 and Table 3.

Package	Average	Minimum	Maximum	StDev	SPI tolerance limits
BGA	137.0%	102.0%	191.0%	11.00%	105% - 180%
QFP	124.0%	84.3%	171.0%	13.90%	85% - 165%
0402	85.8%	63.7%	137.0%	9.56%	65% - 130%
0603	115.0%	85.0%	150.0%	8.87%	85% - 145%
0805	109.0%	89.8%	163.0%	6.93%	90% - 140%
1206	108.0%	90.6%	167.0%	7.47%	95% - 140%
2512	94.2%	81.0%	133.0%	6.05%	80% - 125%
SO8	115.0%	85.7%	154.0%	7.94%	90% - 145%
SOP8	115.0%	93.9%	139.0%	5.64%	95% - 135%

Table 1 SPI solder volume% information for X board (chen, 2011)

Package	Average	Minimum	Maximum	StDev	SPI tolerance limits
0402 & 0603	116.0%	78.9%	191.0%	10.2%	85% - 146%
0805 & Above	114.1%	83.9%	156.8%	10.7%	82% - 146%
SOP <=20 mils pitch	102.3%	76.7%	131.0%	7.9%	78% - 126%
SOP >20 mils pitch	103.5%	79.5%	138.1%	9.6%	75% - 130%
BGA <=20 mils pitch	108.1%	59.4%	131.9%	5.4%	92% - 124%
BGA >20 mils pitch	102.4%	94.5%	111.7%	2.6%	95% - 110%
QFN < = 12 mils	98.2%	75.7%	125.4%	8.6%	73% - 124.1%
QFP < = 20 mils	112.3%	32.8%	152.7%	13.6%	72% - 153%

Table 2 SPI solder volume% information for Y board (Chen, 2011)

Package	Average	Minimum	Maximum	StDev	SPI tolerance limits
BGA 0.4 mm pitch	87.7%	52.3%	115.8%	9.9%	57% - 110%
BGA 0.5 mm pitch	73.1%	46.4%	109.6%	9.2%	50% - 100%
0201	71.2%	43.3%	113.9%	10.7%	50% - 120%
0402	92.1%	70.4%	137.7%	11.1%	65% - 135%
Shield Frame	85.7%	63.1%	135.7%	9.9%	60% - 135%

Table 3 SPI solder volume % information for Z board (Chen, 2011)

It can be noticed from Table 1, Table 2 and Table 3 that the SPI tolerances vary not just from package to package but also from one board to another.

2.4.3 Functioning of Solder Paste Inspection machine

2.4.3.1 2D Area Measurement Techniques

Initially, conventional Automated Optical Inspection (AOI) machines were used for verifying the correctness of solder paste deposit after the solder paste printing. Later special inspection algorithms were developed to measure important parameters such as shape, smearing, offset, coverage, slumping and bridging by using stencil Gerber data as the input file for inspection programming. Later, better algorithms were developed for 2D SPI inspection that dramatically increased the inspection capabilities of 2D SPI. However, the disadvantage of 2D technology is that it cannot be used to obtain height and volume of the solder paste deposit (Biemans 2011).

In 2D area measurement technique, the method used to collect an image of the solder paste deposit highly influences the solder paste area measurement. Usually, an image is acquired through two schemes: contrast based and texture based inspection. After the image is acquired, image processing algorithms are applied to the image to separate the image of solder paste from its background images such as solder mask, silk screen, copper traces and bare FR4. A gray scale comparison technique, shown in Figure 13, is employed in the contrast base image processing analysis. In the texture base analysis, shown in   Figure *14*, the solder paste is discriminated from its surroundings by using a special image texture of the solder paste (Electronics 2012).
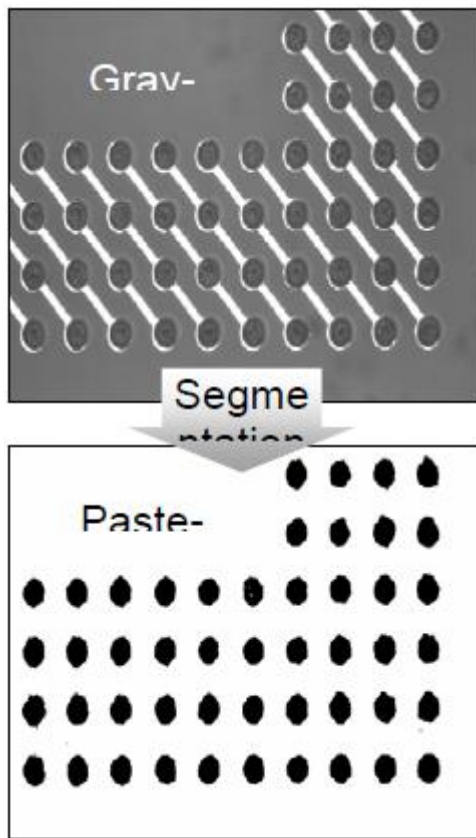
Figure 13 Contrast base, gray scale image
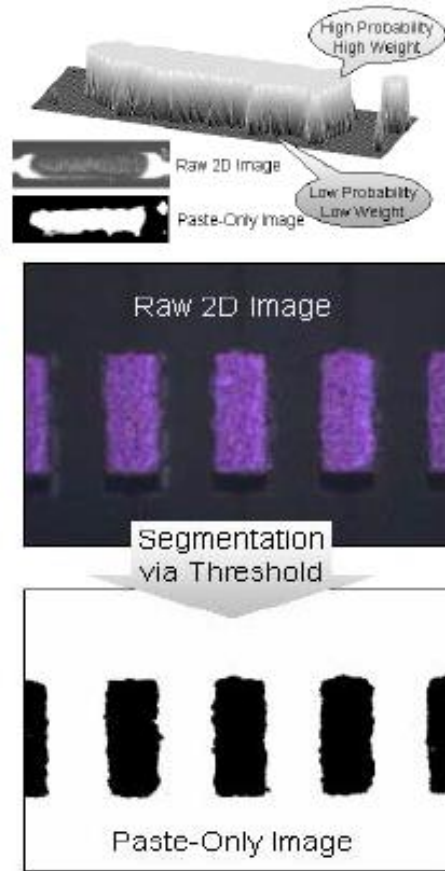
Figure 14 Textured base image (Mohanty, 2008)
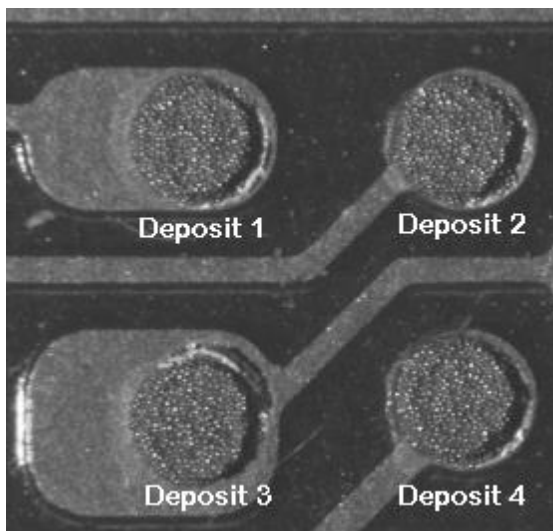
Figure 15 2D image of solder deposits (Mohanty, 2008)
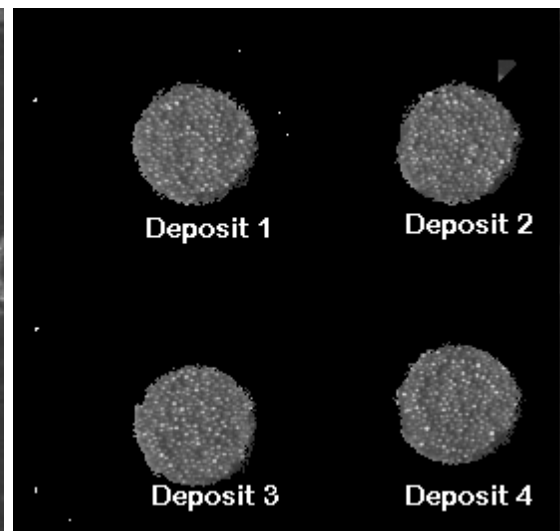
Figure 16 Segmented 2D image of solder deposits

2.4.3.2 3D area measurement technique

In this technique, the image representing the height of the solder deposit at each pixel is the basis for 3D area measurements. The most common methods used to measure the solder paste height in 3D SPI are Phase shift moiré and Laser triangulation methods. In both the techniques, only the height of the solder paste deposit is measured. Area and volume of each deposit are obtained by integrating the height data of each XY pixel. The accuracy of the height of the deposit depends on choosing a correct reference, which is called a 'zero reference.' Ideally the solderable pad of the PCB is used as a zero reference. But as solder paste covers the pad after printing, the pad surface cannot be used as a zero reference. For this reason, the area surrounding the circumference of the pad is taken as a zero reference. As the area surrounding the circumference of the pad is slightly higher than the pad surface, the height offset is applied to the measured value. The height offset is calculated using a golden board (Biemans 2011).

2.4.3.3 Laser triangulation method

Laser triangulation method is one of the oldest technologies used to measure the height of the solder paste deposit. In this method, "a laser slit beam is projected by a laser head, and a camera is used to capture the reflected laser lines. The laser head is moved in defined pitches to cover the target area" (Electronics 2012).

2.4.3.4 Moiré topography

This is a method used for solder height measurement. This method uses tridimensional measurement by phase modulation. In this method, "lines are projected on an object as of modulated inference fringes" (Biemans 2011). The height of the object is calculated "by moving the observation grating that creates the lines" (Biemans 2011). The height calculation using Moiré topography is shown in Figure 17.
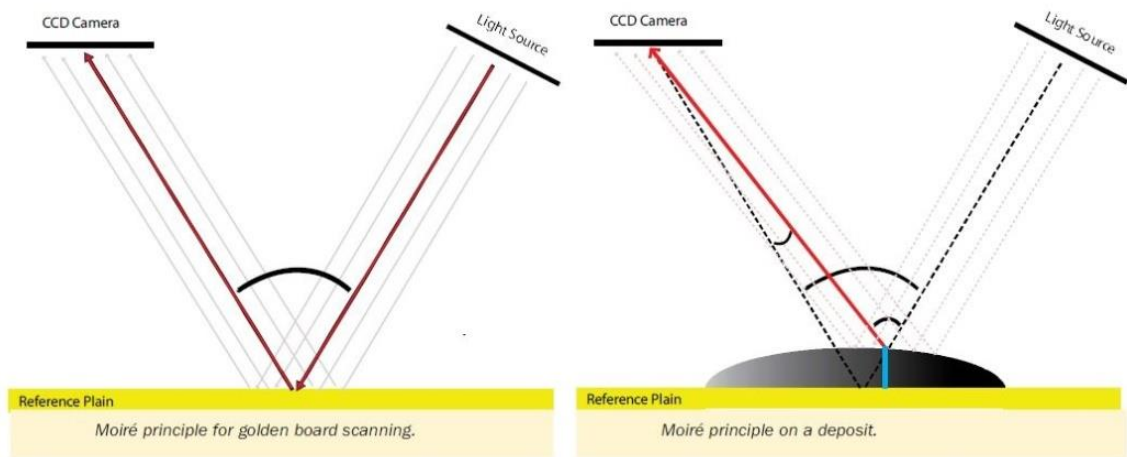
Figure 17 Height calculation using Moiré topography (Biemans, 2011)

2.4.3.5 Dual multisampling laser systems

Dual multisampling laser system combines the advantages of both the Laser triangulation method and the Moiré topography. The lasers used in this method can inspect the PCBs with different colors and can also eliminate shadow effects. This method of inspection is much faster and accurate than either of the methods explained above (Biemans 2011).

2.4.4 Importance of true height measurement

The accurate measurement of height is critical to SPI measurement because it has a direct correlation with solder volume and defects, it was reported that the accurate inspection of solder volume aids in improving the final quality of the product (Kulkarni 2014).

2.4.4.1 Possible causes of Incorrect Volume

Usually, the actual volume of the solder paste deposited is different from the target volume because "solder paste printing is a complicated process and many factors can contribute to variation in solder paste deposition" (CyberOptics 2013). Rheology and composition of solder paste, stencil and squeegee used and process parameters are the primary factors that affect the solder paste deposition. Detailed descriptions of all factors that affect the solder printing process have been mentioned in Sections 2.2.1 and 2.2.2. The solder paste deposits do not have perfect square edges, especially in the case of fine pitch packages. Precise volume measurement becomes difficult when the solder deposits do not have perfect square edges, and if the SPI image acquisition system adopts the image filtering

technique, the calculated volume would not be an accurate representation of actual volume (Kulkarni 2014). The effect of image filtering is shown in Figure 18.
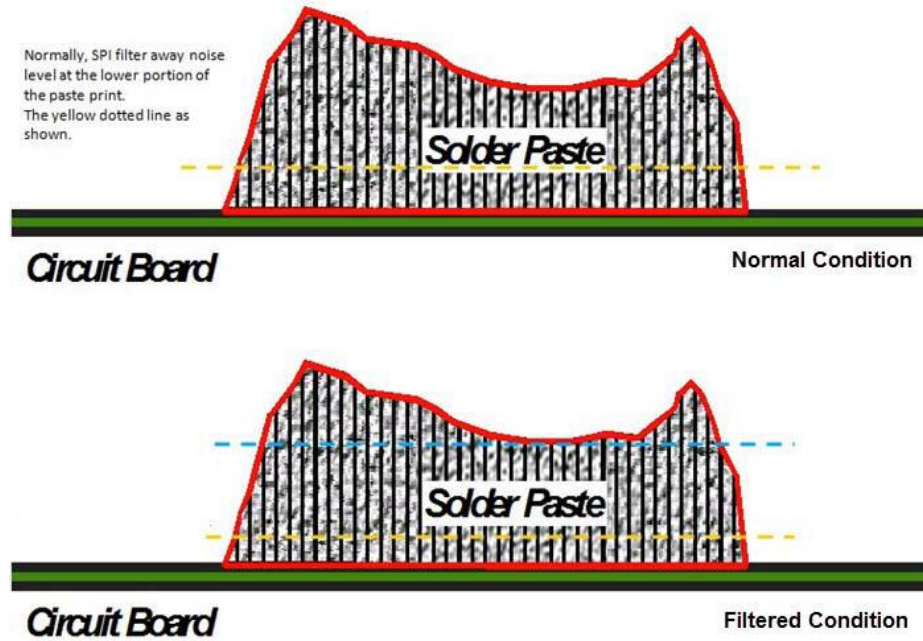
Figure 18 Solder Paste Height Value under normal condition and after filtering Source (Kulkarni, 2014)

Chapter 3: Research Methodology

3.1 Introduction

To address the issue of solder deposit variability and to ensure a good assembly process (i.e. high yield), manufacturers may require that a paste deposit meet a specific criterion. Often this criterion is in the form of an allowable volume tolerance. Ideally, this tolerance has been established through research and experience, but the research was unable to find any published paste deposit volume tolerances for a high yield assembly process. Instead, there appears to be a consensus that up to +/-50% of the stencil aperture volume is an acceptable deposit size for most packaging technologies.

By establishing the normal variations in typical solder paste printing processes for selected package assemblies, it was identified and then intentionally produced solder paste deposit volumes representing relatively low transfer efficiencies were induced. These deposits were strategically incorporated into an otherwise normal assembly process in order to evaluate their effect on the assembly yield and reliability of the devices under test.

3.2 Research Overview

In order to study the effect of paste volume variability on yield and reliability it was first necessary to determine the typical variability of a standard assembly process. This was accomplished by screening solder paste over 30 test boards using a previously established

process which produced known good results (i.e. defect free, electrically functional assemblies).

The process was begun by stencil printing Indium 8.9 type 4.5 solder paste over the motherboards using a DEK Infinity printer equipped with 60 degree stainless steel squeegees. The paste contained SAC305 solder particles and was a no-clean formulation.

The print deposits were then measured using a Koh-Young ASPIRE 2 Solder Paste Inspection (SPI) system. Data collected included paste deposit height, area and volume. Post processing of the collected data was performed to determine the minimum, maximum and average deposit volume of the 'good' process for each component type and histograms of the collected volume data were produced for each motherboard footprint location.

Because the measured volumes from the 'good' process were known to yield functional assemblies 100% of the time, artificially induced low-volume deposit outliers were required for this experiment to ensure that the lower acceptability limit could be determined. These outliers were generated by reducing the stencil aperture dimensions at four to sixteen solder joint positions for each component type while the remaining solder joint positions maintained the previously used aperture sizes.

With the modified stencils in hand, solder paste was once again printed over the test boards and the deposit characteristics were measured with the ASPIRE SPI. Due to natural print variability, some of the deposits generated with the reduced aperture sizes were significantly smaller than the targeted volumes. These prints were excluded from the assembly analysis as they were deemed too small for practical purposes.

However, prints that were found to be within the desired test range were utilized in a small-scale assembly build. In these instances, components were placed on the test boards using Universal Instruments GSM pick and place machine and subsequently reflow soldered in a Vitronics-Soltec XPM 1030N forced convection oven using a nitrogen atmosphere with an oxygen level of less than 50ppm.

The reflow process was designed to heat the specimens at a rate of 48^0C per minute from room temperature to a peak temperature of 240^0C to 244^0C before cooling at a rate of 57^0C per minute. Total time above liquidus (TAL, 217^0C) was approximately 45 seconds, shown in Figure 19.
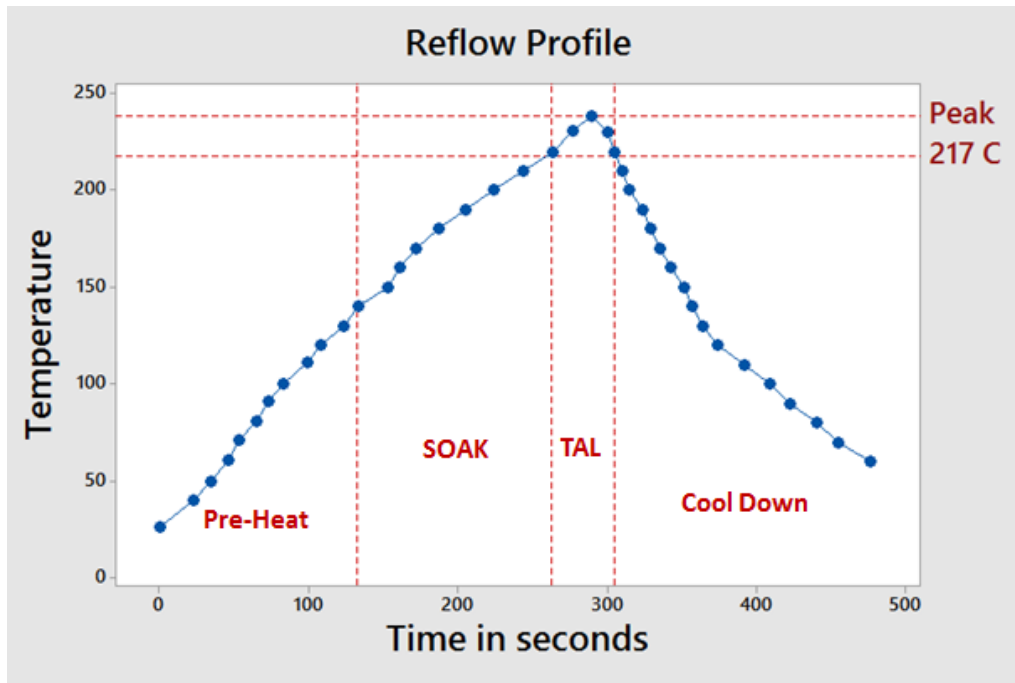
Figure 19 Reflow Profile

The samples were then inspected using electrical resistance readings and x-ray imaging to determine if the assembly was successful.

When a solder joint location was identified as electrically open after reflow processing, the corresponding paste volume was determined from the SPI data and classified as 'insufficient'. Ultimately, the largest paste deposit resulting in a non-functional solder joint was then used to define the minimum acceptable deposit volume for each component type.

After the minimum acceptable deposit volume has been determined, Successful (i.e. electrically good) component to motherboard assemblies were subjected to an accelerated thermal cycle environment using a Thermotron F-110 chamber. The thermal profile developed for this experiment systematically cycled between -40^0C and 125^0C with 15 minute dwell times maintained at the temperature extremes. Temperature transition rates were between 6^0C and 7^0C per minute resulting in a total cycle time of 80 minutes, see Figure 20.
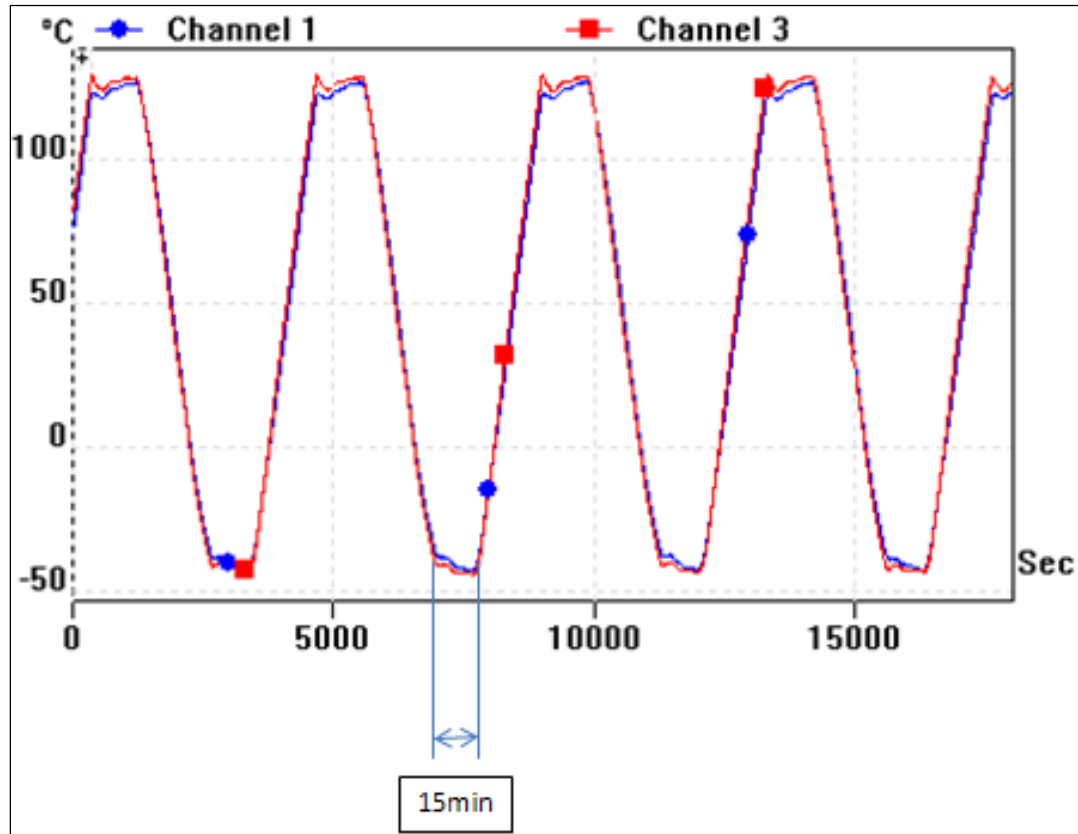
Figure 20 Thermal Cycling profile -40^{0}C to 125^{0}C

3.3 Test Vehicle

The test vehicles utilized in this experiment were constructed using stitch patterned motherboard footprints and mating dummy surface mount devices. When successfully reflow soldered, these vehicles produced continuous daisy-chains that allowed for simple electrical testing of the newly created first level solder joint interconnections.

The boards were constructed using 370HR laminate. Each board contained eight copper layers and had a total mask to mask thickness of 2.5mm. Each copper layer was formed from ½oz foil with the outer layers plated to approximately 1oz total copper thickness.

Layers 1 and 8 were used for signal transmission while inner layers 2 through 7 were non-functional dummy planes.

The boards were acquired with immersion gold over electroless nickel (ENIG) or copper OSP surface finishes. Each board was mechanically routed to include multiple coupons each containing one or more footprints for surface mount device attachment. In addition to input and output traces, each footprint also contained probe points to facilitate failure location isolation with an ohm-meter. For this experiment, two LGA, two QFN and two BGA designs were evaluated.
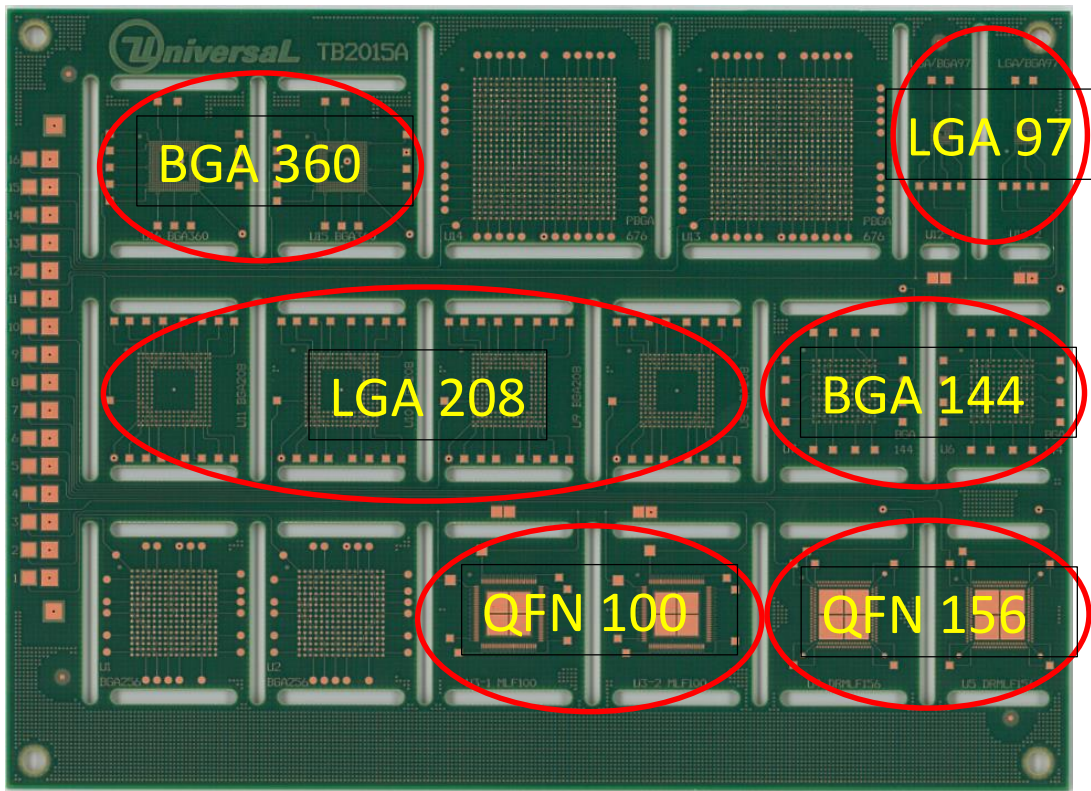
Figure 21 Test Vehicle bare board Cu-OSP surface finish

Figure 22 Test Vehicle Assembled

3.4 Package Types

For this experiment LGA 208, LGA 97, QFN 100, QFN 156, BGA 144 and BGA 360 were evaluated. All components were dummy components and acquired from practical components.

3.4.1 Land Grid Array (LGA) 208

ENIG Surface Finish   Cu-OSP Surface Finish   Bottom Side of the component
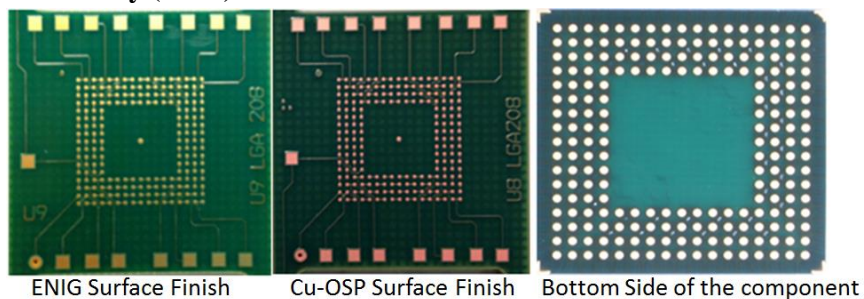
Figure 23.LGA 208 ENIG, Cu-OSP surface finish coupons and component bottom side

The LGA208 device was a 15x15mm component consisting of 208 I/O arranged at 0.8mm pitch using a 17x17 depopulated array pattern. The component attachment pads were defined by mask openings of 0.4mm in diameter and were finished with gold over nickel (Ni/Au) plating.

The LGA208 motherboard footprint pads measured 0.376mm in diameter and were defined by mask openings of 0.5mm (i.e. solder mask defined geometry).

Due to limited sample size only LGA 208 was evaluated on both ENIG and Cu-OSP surface finishes.

3.4.2 Land Grid Array (LGA) 97
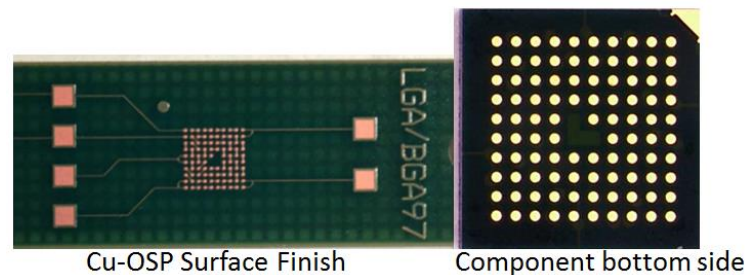
Figure 24 Cu-OSP surface finish coupons and component bottom side

The LGA97 component is a 5x5mm package containing 97 attachment pads arranged at 0.4mm pitch using a 10x10 depopulated array pattern. The component pads are Ni/Au finished and solder mask defined with exposed diameters of approximately 0.2mm.

The matching LGA97 motherboard land pattern contains attachment pads that measure 0.25mm in diameter surrounded 0.337mm mask openings (i.e. non-solder mask defined).

3.4.3 Quad Flat No Lead (QFN) 100

Cu-OSP Surface Finish   Component bottom side
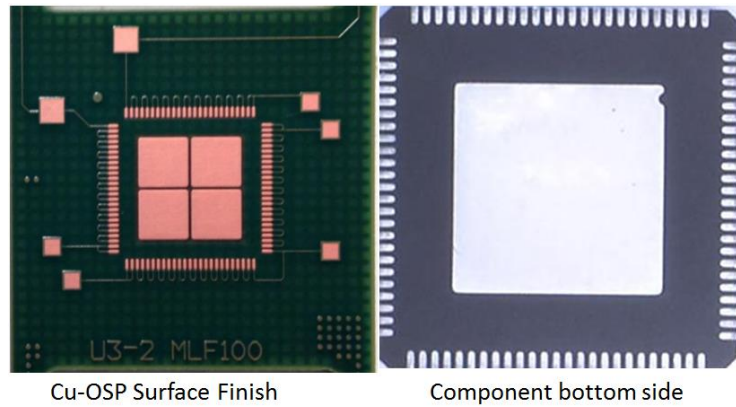
Figure 25 Cu-OSP surface finish coupons and component bottom side

The QFN100 component was a 12x12mm package containing a perimeter array of 100 attachment pads spaced at 0.4mm pitch and an exposed thermal die paddle. The attachment pads were bullet shaped and measured approximately 0.6x0.2mm while the thermal die paddle measured 6.9x6.9mm. The device was acquired with a matte Sn surface finish.

Due to the fine pitch of the device, the QFN100 motherboard pads were non-solder mask defined by using a mask trench design (i.e. no mask between pads). Nominal pad size was 0.25x0.78 mm. Four large pads, each measuring 3.8x3.8mm were included on the motherboard for thermal die paddle soldering.

3.4.4 Quad Flat No Lead (QFN) 156

Cu-OSP Surface Finish   Component bottom side
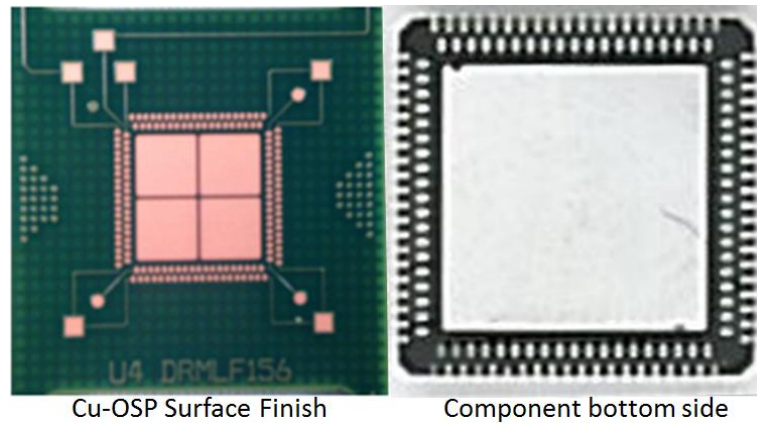
Figure 26.QFN156 Cu-OSP surface finish coupon and component bottom side

The QFN156 is a dual row device consisting of 156 I/O arranged at 0.5mm pitch. The component measures 12x12mm and contains a large thermal die paddle. The attachment lands measure approximately 0.2x0.4mm with the inner row pads being oval in shape and the outer row pads being bullet shaped. The exposed die paddle measures 8.9x8.9mm. The device was procured with a matte Sn finish.

All QFN156 motherboard attachment pads were bullet shaped, measuring 0.27x0.44mm. The pads were non-solder mask defined using 0.05mm mask clearance per side. The center of the footprint contains four large pads for die paddle soldering, each measuring 4.8mm per side.

3.4.5 BGA 144

Cu-OSP Surface finish   Bottom Side of Component
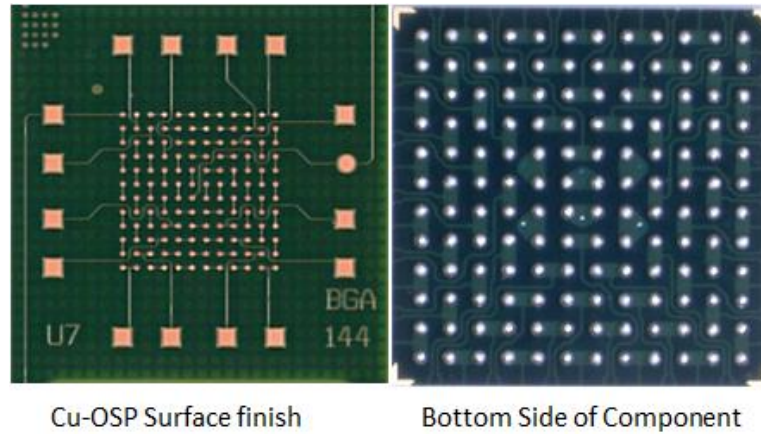
Figure 27 BGA 144 Cu-OSP surface finish coupon and component bottom side

BGA 144 footprint for a 144 I/O BGA. The attachment pads measure 0.38mm in diameter and are non-solder mask defined. Mask openings are 0.6mm diameter.

The BGA 144 component was a 13x13mm package containing a grid array of 144 ball attachment with a pitch of 1mm. It had a silicon die measuring approximately 10x10mm and 0.3mm thick.

3.4.6 BGA 360

Cu-OSP Surface Finish   Component bottom side
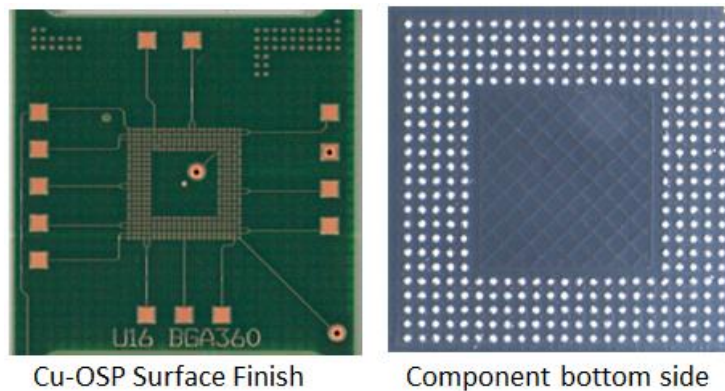
Figure 28 BGA 360 Cu-OSP surface finish coupon and component bottom side

BGA 360 footprint for a 360 I/O BGA. The attachment pads measure 0.3mm in diameter and are non-solder mask defined. Mask openings are 0.6mm diameter.

The BGA 360 component was a 10x10mm package containing a grid array of 360 ball attachment with a pitch of 0.4mm. It had a silicon die measuring approximately 5x5mm and 0.3mm thick.

3.5 Stencil Designs

All stencils used for this study were fabricated using 4mil thick stainless steel foil and cut using laser technology.

In order to evaluate the minimum solder paste deposit volume required to both form a good electrical connection and a reliable solder joint, two or three undersized aperture sizes were designed into the stencil foils for each device type. These undersized apertures targeted transfer efficiencies of 30, 40 and 50% for BGA and QFN components and TE of 60, 75 and 80% for the LGA devices. Additionally, an oversized aperture targeting 120% TE was included for the LGA208 component. A summary of the standard and modified stencil aperture designs may be found in Table 4.

Device	Standard Aperture Size (mil)	TE Range	Standard Aperture Shape	Modified Aperture Size (mil)	TE Range
LGA 97	10.2x10.2	71%-108%	Rounded Square	9.6x9.6	60%-82%
				9.0x9.0	45%-66%
				8.1x8.1	9%-51%
LGA 208	15	81%-125%	Circle	18	130%-160%
				12.8x12.8	77%-99%
				11.9x11.9	61%-80%
				9.4x9.4	43%-58%
QFN 100	27.8x7.8	73%-131%	Bullet	17.8x7.8	49%-74%
				13x7.8	35%-50%
				8.9x7.8	6%-34%
QFN 156	15.7x7.8	53%-116%	Bullet	10.7x7.8	41%-81%
				7.1x7.8	17%-40%
				5.3x7.8	Not Assembled
BGA 144	15	81%-120%	Circle	10.6	50%
				9.48	40%
				8.2	30%
BGA 360	10.2x10.2	67%-111%	Rounded Square	7.24	50%
				6.48	40%
				5.6	30%
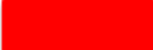
= Not Tested in ATC

Table 4 Summary of stencil designs

The position of each undersized or oversized aperture was chosen based on package construction and/or existing failure analysis information acquired from an earlier assembly and a -40^0C to 125^0C accelerated thermal cycling (ATC) experiment using similar components and test board footprints.

For the LGA devices, four undersized aperture positions were included in each stencil design. These apertures were placed below the footprint diagonals and included one

outermost solder joint position and three solder joint positions arranged beneath the package die shadow region (Figure 29 and Figure 30). The outermost positions were chosen because both devices historically showed a tendency to fail due to corner joint solder fatigue during thermal cycling. The die shadow positions were chosen because solder joint failure in the die shadow region may occur under certain conditions, such as the formation of an undersized solder joint. For LGA 208, an additional design with oversized joints was included to test the effect of oversize solder deposits in ATC (Figure 31). In this instance, the oversized solder deposits were placed at the corner most joint positions.

Figure 29 LGA 208 stencil aperture layout. Green indicates standard stencil aperture positions, red indicates undersized aperture positions.

Figure 30 LGA 97 stencil aperture layout. Green indicates standard stencil aperture positions, red indicates undersized aperture positions.
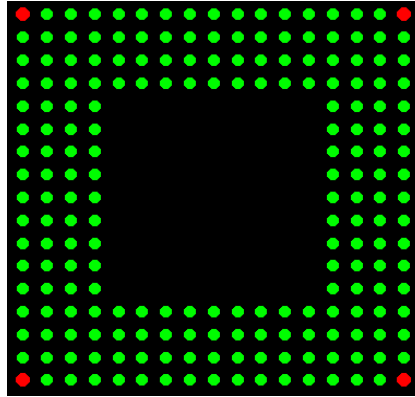
Figure 31 LGA 208 stencil aperture layout. Green indicates standard stencil aperture positions, red indicates oversized aperture positions.

For the QFN components, the undersized apertures were placed at the corner most solder joint positions, which had been found to fail earliest in thermal cycle testing. In the case of the QFN100, this design amounted to eight undersized apertures whose positions are shown in Figure 32.
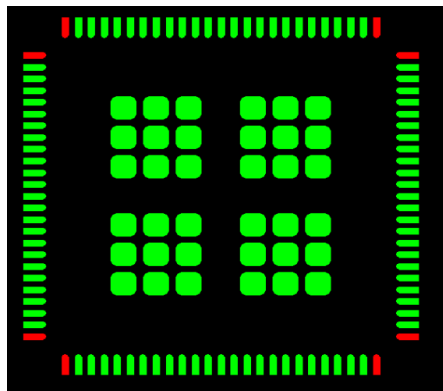
Figure 32 QFN 100 stencil aperture layout. Green indicates standard stencil aperture positions, red indicates undersized aperture positions.

With the dual-row QFN156 the undersized apertures were included at the 16 corner most solder joint positions shown in Figure 33, which were believed to be the most susceptible to fatigue failure when subjected to thermal cycle testing.
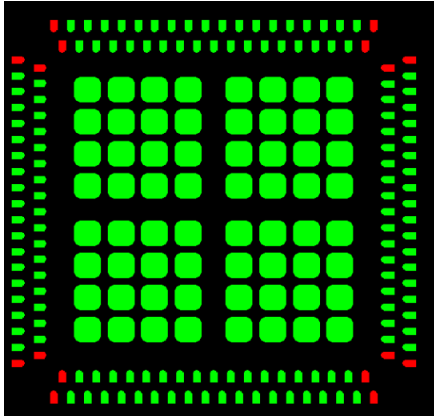
Figure 33 QFN 156 stencil aperture layout. Green indicates standard stencil aperture positions, red indicates undersized aperture positions.

For the BGA 144 component, four undersized apertures were placed alone the diagonal with one undersized aperture at the North-West corner solder joint position and the other three undersized apertures in the inner rows as shown in Figure 34 .
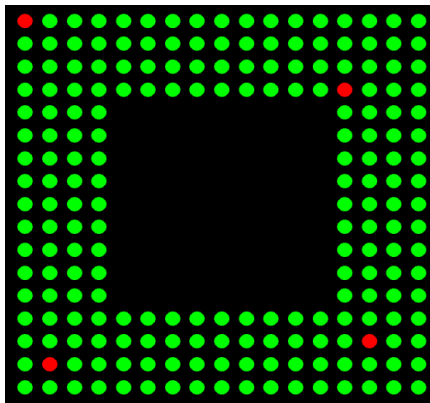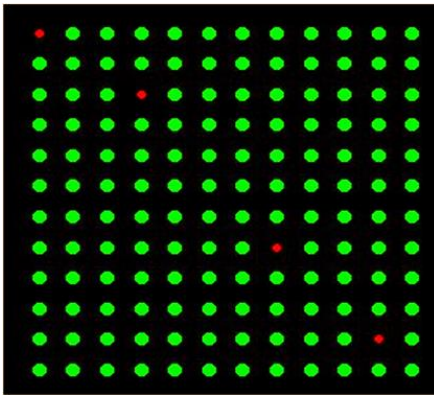

Figure 34 BGA 144 stencil aperture layout. Green indicates standard stencil aperture positions, red indicates undersized aperture positions.

For the BGA 360 component, four undersized apertures were placed alone the diagonals with two undersized apertures one at the North-West corner solder joint position and one at South- East corner joint position and the other two undersized apertures were in the inner rows near the die edge as shown in Figure 35.
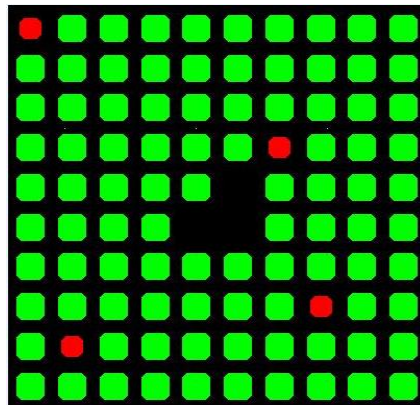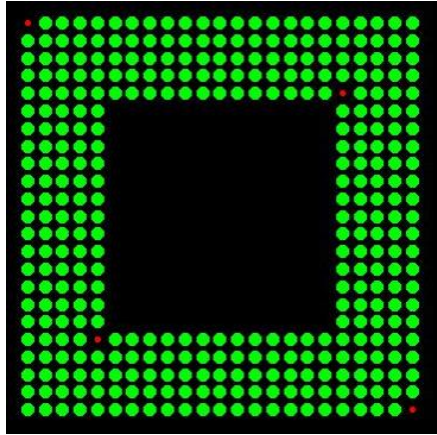
Figure 35 BGA 360 stencil aperture layout. Green indicates standard stencil aperture positions, red indicates undersized aperture positions.

3.6 Equipment and process setting

All the assembly build and experimental testing was done at Universal Instruments Advanced Processing Lab (APL).

3.6.1 Stencil Printer

A DEK stencil printer was used. With the following printing parameters:
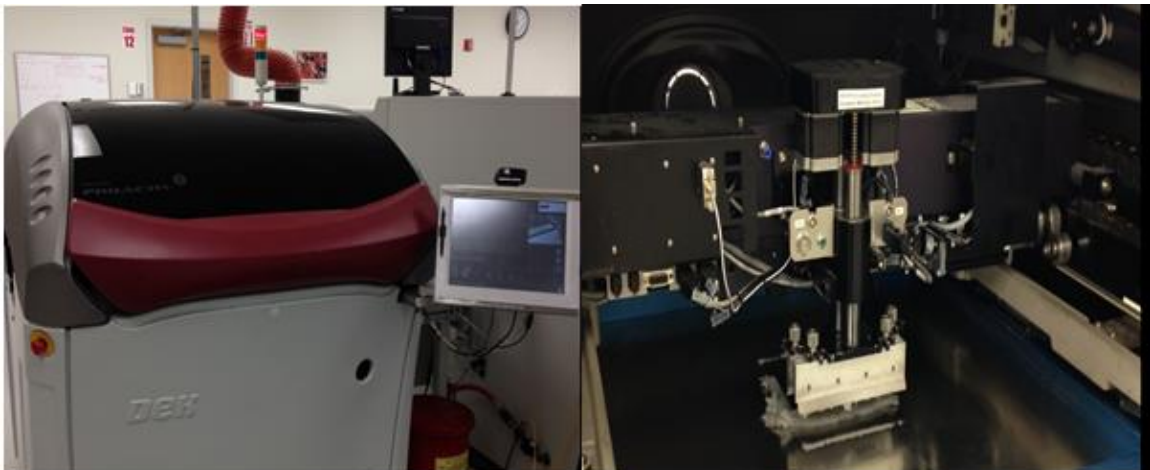
Figure 36 Stencil Printer

- Printing Pressure = 12 kg

- Printing Speed = 10mm/sec

- Separation Speed = 2.0mm/sec

- 60^0 angle squeeze

All boards were fully supported and contact printed (i.e., zero standoff) No standoff is used it was a contact printing process. Same settings were used to maintain steady process.

3.6.2 Solder Paste Inspection System

SPI is an automated visual inspection of printed circuit board (PCB), where cameras at different angles autonomously scans the PCB under test for solder paste printing defects. A Koh Young KY8030-3 SIP system was used to screen the solder paste deposits. The system was programed to measures the height, area and volume of the solder paste deposit printed during the stencil printing process. For initial assemble yield test all the boards which had very low solder paste deposits were also passed.
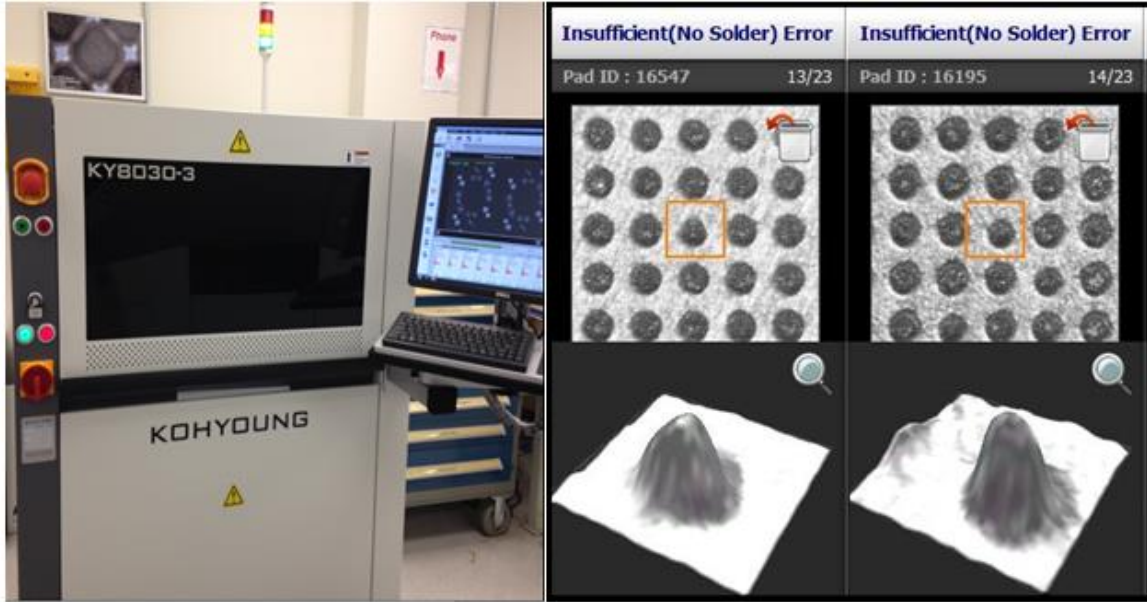
Figure 37 Solder Inspection System

3.6.3 Component Placement Machine

Figure 38 Component Placement Machine

Component placement machine also known as pick and place machine are used for high speed and accurate assemblies. A FUZION component placement machine was used to populate the PCB board. Components were fed to the machine using matrix trays. The machine had an In-line 7 head, a program for the test board was created using the PCB design dimensions. The machine picks the components using vacuum nozzles and places it exact on its foot print on the board using alignment and vision systems. It uses high resolution cameras to identify the components and inspect them to find any damage or missing features.

3.6.4 Reflow Oven

Figure 39 Reflow Oven

The reflow oven used contains 10 heating zones and 3 cooling zones, which can be individually controlled for temperature. The PCB moves through the oven on a conveyor belt, and is therefore subjected to a controlled time-temperature profile. The heat source is from ceramic infrared heaters, which transfers the heat to the assemblies by means of radiation. The Oven also uses fans to force heated air towards the assemblies. PCBs were assembled in an oxygen-free atmosphere using Nitrogen (N2). This minimizes oxidation of the surfaces to be soldered.

Figure 40 shows the user interface of the reflow oven, we can see all the heating and cooling zones and the temperatures which they are set to.
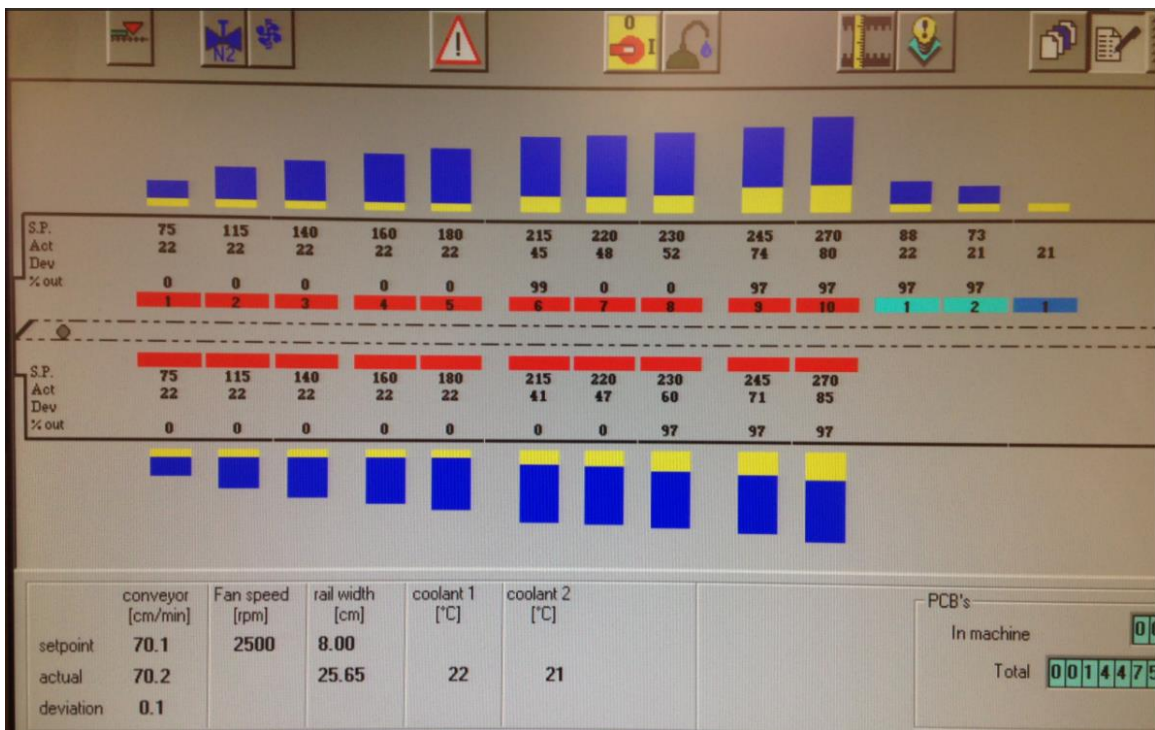
Figure 40 Reflow Oven User Interface

3.6.5 X-Ray Inspection

An x-ray inspection produces images of the object similar to optical inspection. Instead of visible light it uses x-rays that are generated by an x-ray tube, that pass through the object. Opposite the x-ray emitter is a detector that converts x-ray into visible light creating an optical image which is then picked up by a camera. The image is produced due to the different absorption of x-rays when passing through the object and can therefore reveal structures inside the object that are hidden from outside view.

Figure 41 X-Ray Inspection System

3.6.6 Thermal Chamber

Figure 42 Thermal Chamber

The concept of accelerated testing is to compress time and accelerate the failure mechanisms in a reasonable test period so that product reliability can be assessed. Accelerated thermal cycling is an accelerated test where the product is subjected to thermal stress and strain due to Coefficient of thermal expansion (CTE) mismatch. For this test a thermal chamber is used which has rapid heating and cooling rates in this case - 40^0C to 125^0C in 15 min (i.e.11^0C per min).

3.6.7 Event Detector

Event Detectors are used for reliability testing of solder joints based on continuous, electrical resistance monitoring during accelerated cycling testing. Event Detectors perform continuous electrical monitoring for short-duration resistance variations on large numbers of channels. A threshold resistance can be adjusted according to the experiment and failures with resistance above the threshold are detected by the monitoring system. A 400 ohm threshold resistance was used for this experiment. The event detector used had 256 channels, multiple event detectors can be connect together to increase the number of channels. Wires are plugged into the event detector using a 32 port female connector as shown in Figure 43.

Figure 43 Event Detector

Chapter 4: Results and Discussions

4.1 Assembly Results

A standard SMT process was used to assemble all the components. The results discussed will give a detailed understanding of the paste volume effects on assembly yield.

4.1.1 LGA 208

The standard aperture used to assemble the LGA 208 on Cu-OSP motherboards was a 15mil circle which produced deposit sizes ranging from 578 mil^3 to 885 mil^3 and an average TE of 98% as shown in Figure 44.
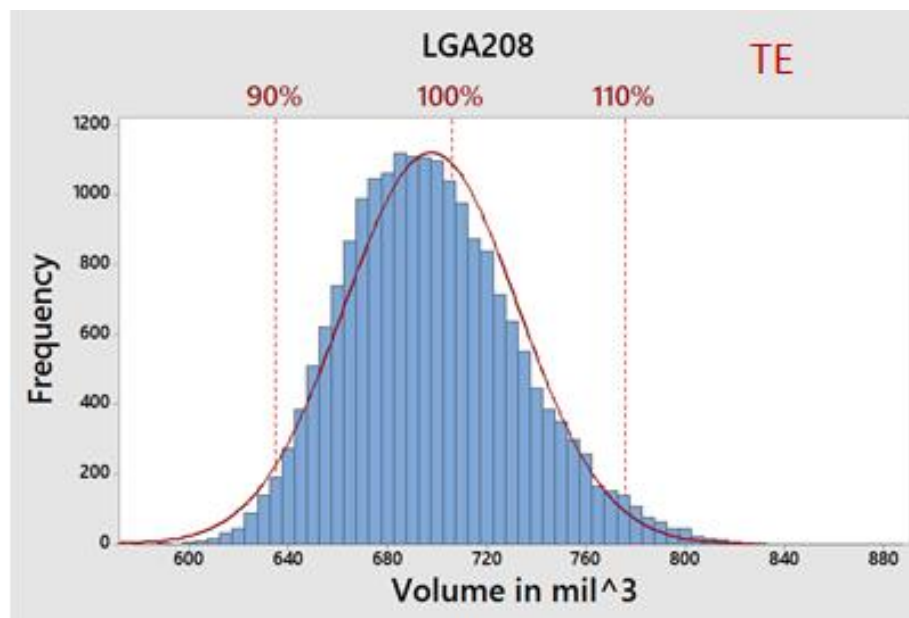
Figure 44 LGA 208 paste volume distribution for standard aperture

The undersized stencil apertures evaluated measured 12.8x12.8mil (UA1), 11.9x11.9mil (UA2), and 9.4x9.4mil (UA3) and were designed to target 60% to 85% TE relative to the standard aperture volume. The designs were evaluated for both ENIG and Cu-OSP motherboard surface finishes.

For the samples assembled to Cu-OSP motherboards, the TE of the intentionally undersized deposits varied from 43% to 99% (308 to 698 mil^3). Electrical testing would find that paste deposits measuring less than 45% TE (319 mil^3) failed to form working solder joints while deposits measuring above 319 mil^3 always formed a soldered joint refer to Figure 45.

Figure 45 Comparison of Standard Aperture (SA) paste deposit volumes and Undersized Apertures (UA1, UA2, UA3) paste deposit volumes used to assemble LGA 208 on Cu-OSP motherboards.

The x-ray image found in Figure 46 contains an LGA 208 non-functional solder joint formed by a 45% TE (317 mil^3) paste deposit. In this instance the joint is clearly smaller than its neighbors and was easily detected using x-ray inspection and electrical testing.
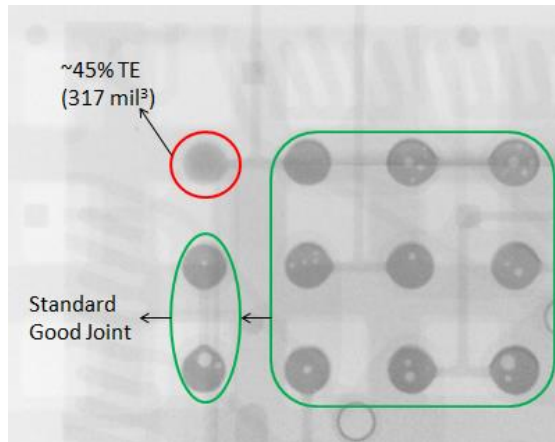
Figure 46 X-ray image of LGA 208 on Cu-OSP with a non-functional solder joint with 45% TE (317 mil3).

For the samples assembled to ENIG motherboards, the TE of the intentionally undersized LGA 208 deposits varied from 40% to 90% (308 to 635 mil^3). In this instance, no electrical opens were detected after reflow soldering.
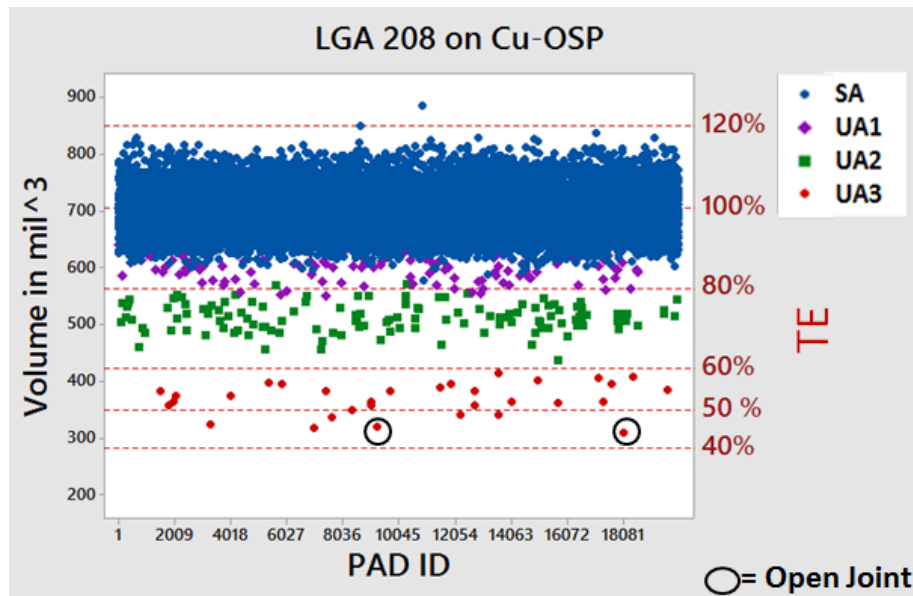

Figure 47 Comparison of Standard Aperture (SA) paste deposit volumes and Undersized Apertures (UA1, UA2, UA3) paste deposit volumes used to assemble LGA 208 on ENIG motherboards.

However, x-ray imaging would reveal that some of the solder joints were not visually appealing. As shown in Figure 48, a joint formed with as little as 40% TE (309 mil^3) appears to be significantly undersized relative to its average sized neighbors. Given that the motherboard finish was ENIG, the lack of wet out at the noted joint position is surprising.
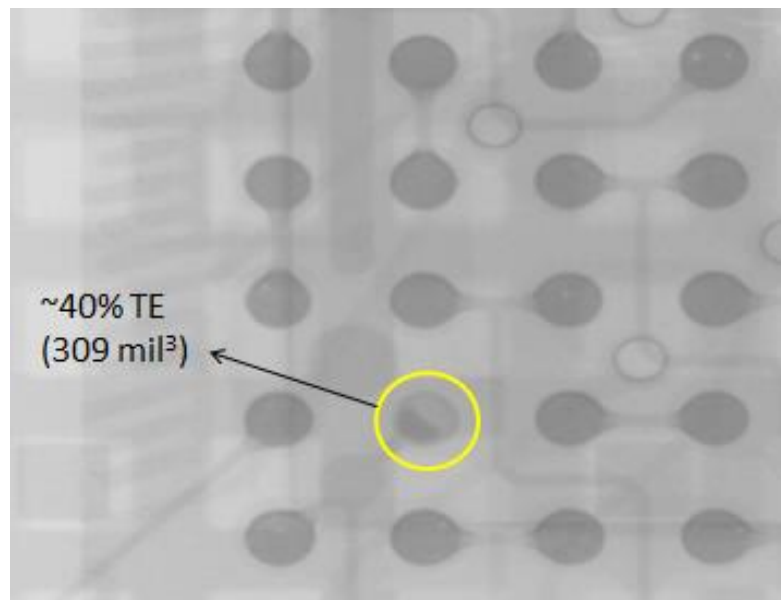
Figure 48 X-ray image of LGA 208 on ENIG with a functional solder joint with 40% TE (309 mil^3).

4.1.2 LGA 97

A standard stencil aperture size of 10.2x10.2mil was evaluated for the LGA 97 device. This aperture was found to produce an average TE of approximately 86% (360mil^3). The smallest deposit created with the standard design was 60% TE (249mil^3) while the largest deposit measured was 112% TE (464mil^3). A histogram of the standard aperture deposit volume data may be found in Figure 49.
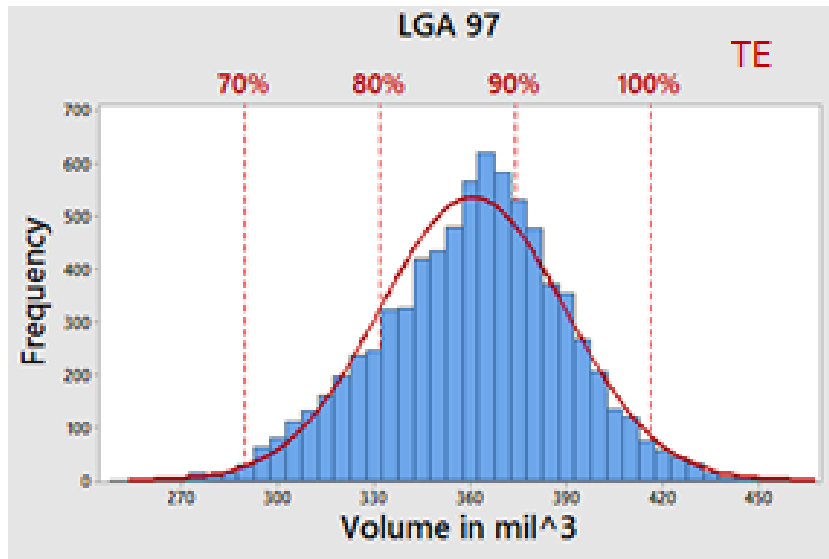
Figure 49 LGA 97 paste volume distribution for standard aperture.

The undersized stencil apertures utilized for LGA 97 assembly measured 9.6x9.6mil (UA1), 9.0x9.0mil (UA2), 8.1x8.1mil (UA3) and were designed to target a TE range of 50 to 85% relative to the standard aperture volume.

For the samples assembled to Cu-OSP motherboards, the TE of the intentionally undersized deposits varied from a low of 9% to a high of 82% (38 to 339mil^3) relative to the standard aperture volume. Electrical testing would find that paste deposits measuring less than 37% TE (156mil^3) typically failed to form a functional solder joint while paste deposits measuring above 37% TE appeared to work. The results of the LGA 97 assembly on Cu-OSP motherboards are summarized in Figure 50.
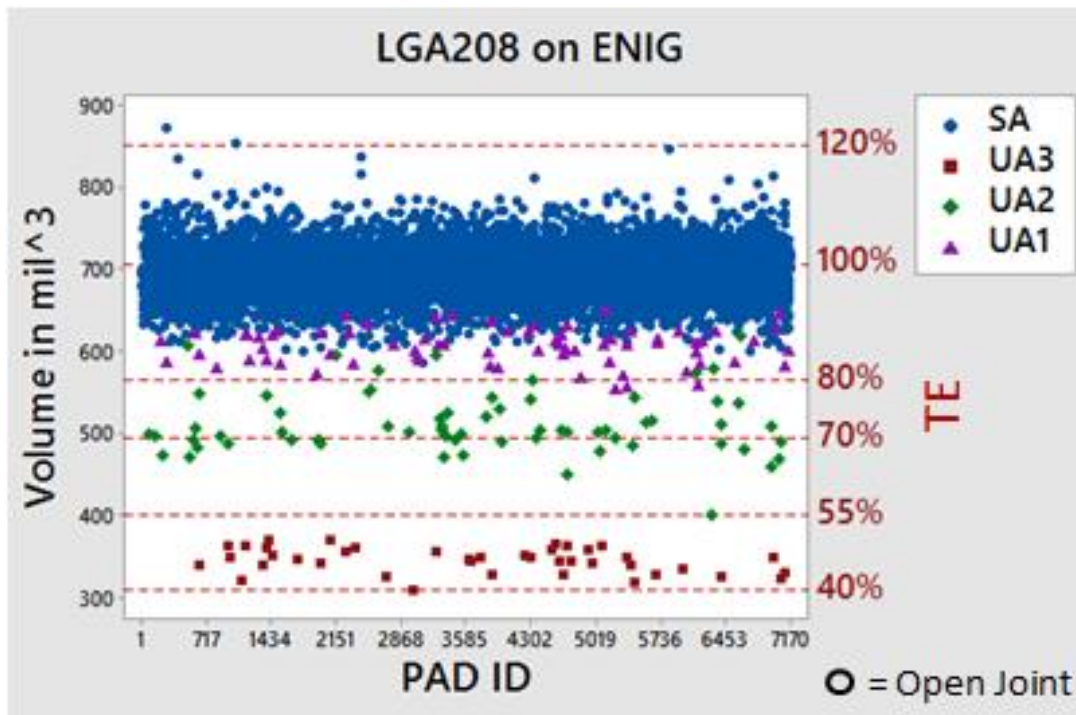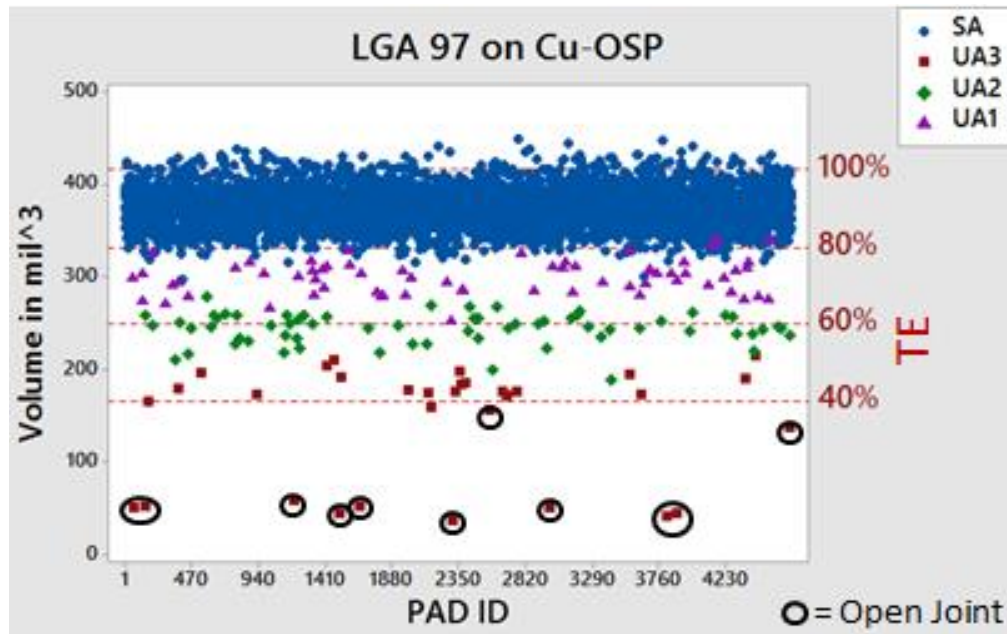
Figure 50 Comparison of Standard Aperture (SA) paste deposit volumes and Undersized Apertures (UA1, UA2, UA3) paste deposit volumes used to assemble LGA 97 on Cu-OSP motherboards. Joints formed with the equivalent of 37% TE or less was electrically unacceptable.

The x-ray image found in Figure 51 shows a non-functional LGA 97 solder joint formed by a 37% TE (156 mil^3). In this image, the joint appears to be slightly smaller than its neighbors, but not so small as to be rejected by x-ray examination. Instead, electrical testing was necessary to verify that this joint position was responsible for the assembly defect.
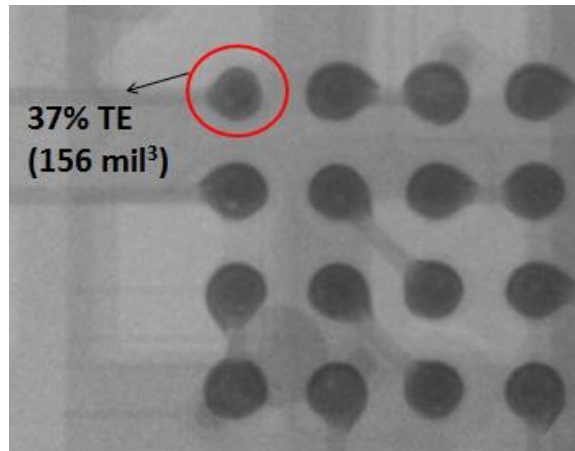
Figure 51 X-ray image of LGA 97 on Cu-OSP with a non-functional solder joint with ~37% TE (156 mil3).

4.1.3 QFN 100

A standard stencil aperture size of 27.5x7.8mil was evaluated for the QFN 100 device and was found to yield an average TE of approximately 104%. The smallest deposit created with the standard design was 78% TE (678mil^3) while the largest measured 130% TE (1125mil^3). A histogram of the standard deposit volume data may be found in Figure 52.
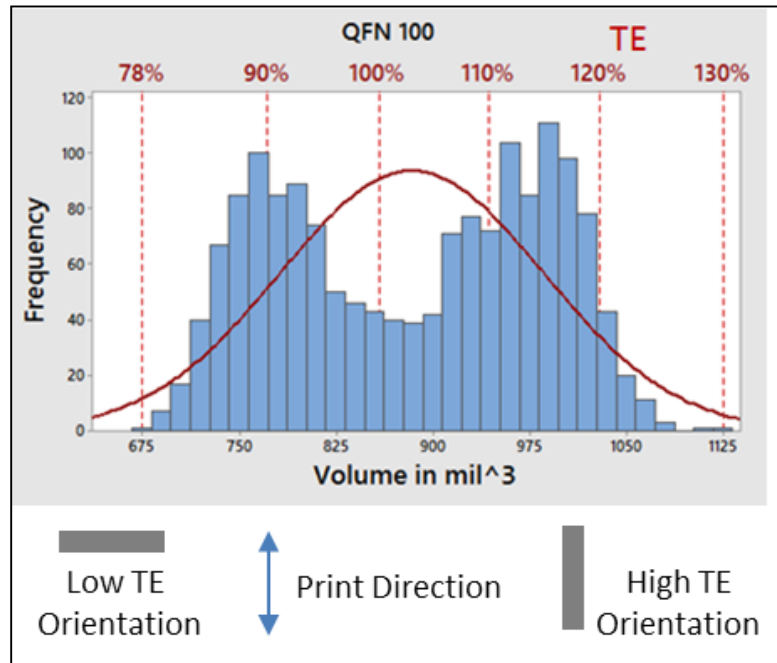
***Figure 52 QFN 100 paste volume distribution for standard aperture design. Bimodal
distribution is apparent.***

As shown in Figure 52, there is a bimodal distribution of the solder paste deposit volumes
for the QFN 100 assembly. This is due to the orientation of the rectangular stencil
aperture relative to the print direction. When the length of the aperture is oriented
perpendicular to the print direction, the TE is higher than the TE when the aperture is
oriented with the length parallel to the print direction. This effect is commonly observed
during the printing process and is highly influenced by the aperture dimensions, paste
type, and other factors.

The undersized stencil apertures used for QFN 100 analysis measured 17.8x7.8mil
(UA1), 13x7.8mil (UA2), and 8.9x7.8mil (UA3) and were designed to target 30 to 50%
TE relative to the standard aperture volume.

For the QFN 100 samples assembled to Cu-OSP motherboards, the TE of the intentionally undersized deposits varied from a low of just 5% to a high of 74% (57 to 635mil^3).

Electrical testing would find that two paste deposits measuring less than 15% TE (135mil^3) failed to form a functional solder joint while deposits greater than 15% TE were likely to function. These results can be seen by examining in Figure 53. In Figure 53 the two deposit sizes that resulted in non-functional solder joints have been circled. These deposits, which are colored red, were created using the Undersized Aperture 3 (UA3) design, which was the smallest aperture evaluated. Deposits created with apertures UA2 (green), UA1 (purple) and the standard aperture (SA; blue) always produced a functional solder joint.
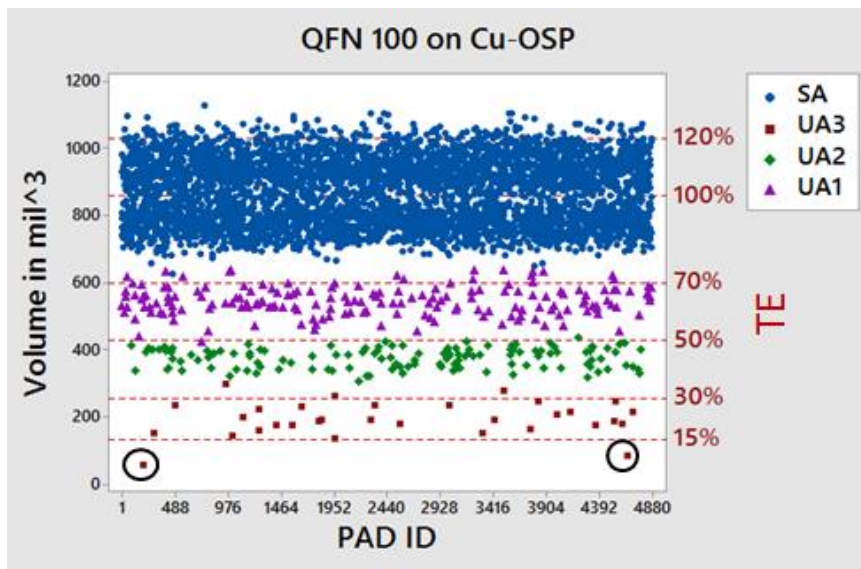
Figure 53 Comparison of Standard Aperture (SA) and Undersized Aperture (UA1,UA2,UA3) paste deposit volumes used to assemble QFN 100 to Cu-OSP motherboards. Deposit sizes greater than 135mil³ formed functional solder joints.

Based on electrical test data, it is clear that outlier deposits with very low TE can produce a functional solder joint for the QFN 100 device on Cu-OSP motherboards. However, this does not mean that such low transfer efficiencies are acceptable in practice. Take for example, the x-ray image found in Figure 54 which contains a functional solder joint formed with 15% TE. The solder joint is quite small relative to its average sized neighbors and is neither visually appealing, or presumably, mechanically robust.

Figure 54 X-ray image of QNF 100 on Cu-OSP with a functional solder joint with 15% TE (135 mil^3).

In this instance, and like many other engineering challenges, it is best to include a safety factor to ensure that a good practice is established. Therefore, going forward, it was decided that a TE of at least 30% was required for the QFN 100 to ensure a good assembly yield with a visually acceptable solder joint on Cu-OSP.

4.1.4 QFN 156

A standard aperture size of 15.7x7.8mil was used for the QFN 156 assembly. This aperture design resulted in paste deposit volumes ranging from 53% to 113% TE (246 to 539 mil^3) with an average volume of 402 mil3, or an average TE of 86% as shown in Figure 55.

Figure 55 QFN 156 paste volume distribution for standard aperture.

Undersized apertures measured 10.7x7.8mil (UA1), 7.1x7.8mil (UA2) and were designed to target a 40% to 50% TE relative to the standard aperture volume. During the assembly process the actual transfer efficiency ranged from a low of 17% to a high of 73% (81 to 338 mil^3). In this instance the two deposits formed with 28% TE or less failed to produce an electrically good solder joint as indicated in Figure 56.

Figure 56 Comparison of Standard Aperture (SA) paste deposit volumes and Undersized Apertures (UA1,UA2) paste deposit volumes used to assemble QFN 156 to Cu-OSP motherboards.

4.1.5 BGA 144

A standard stencil aperture size of 15 mil circle was evaluated for the BGA 144 device and was found to yield an average TE of approximately 98%. The smallest deposit created with the standard design was 81% TE (575 mil^3) while the largest measured 120% TE (849 mil^3). A histogram of the standard deposit volume data may be found in Figure 57.
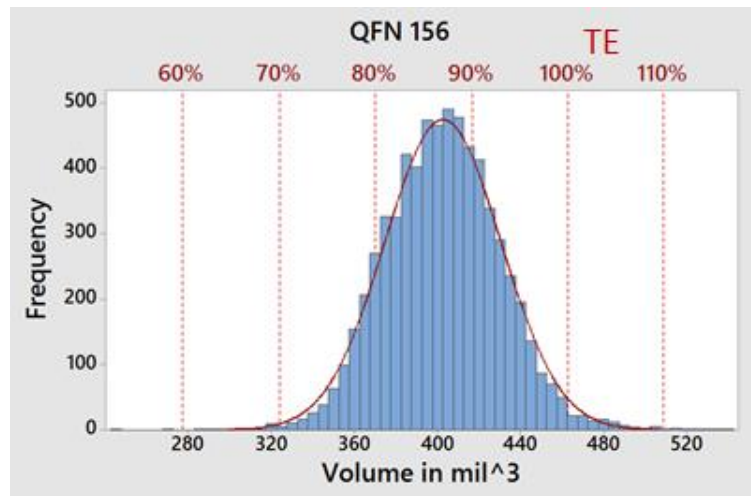
Figure 57 BGA 144 paste volume distribution for standard aperture.

Undersized apertures measured 10.6mil (UA1), 9.4mil (UA2) and were designed to target a 40% to 50% TE relative to the standard aperture volume. During the assembly process the actual transfer efficiency ranged from a low of 30% to a high of 53% (215 to 362 mil^3). In this instance no assembly defects were observed. Solder paste volume data for BGA 144 is displayed in Figure 58.
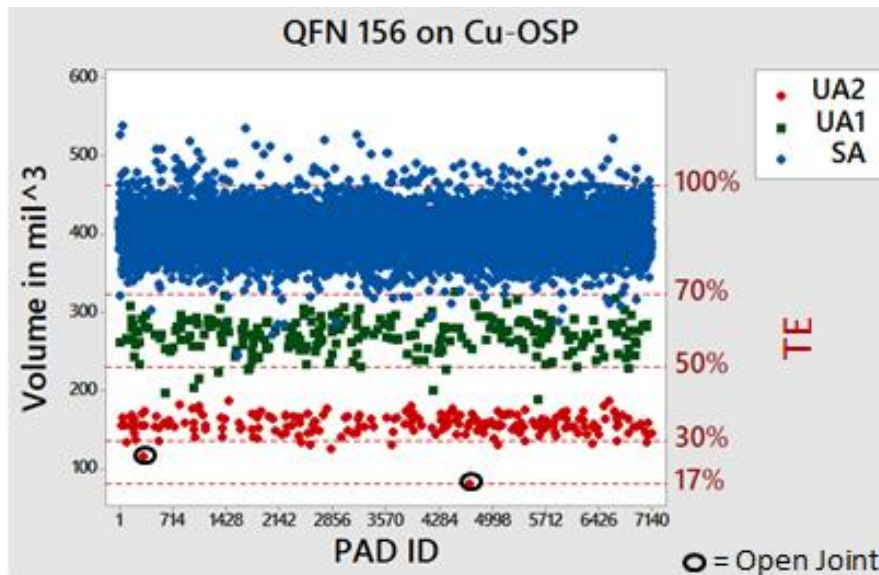
Figure 58 Comparison of Standard Aperture (SA) paste deposit volumes and Undersized Apertures (UA1,UA2) paste deposit volumes used to assemble BGA 144 to Cu-OSP motherboards.

The X-ray image found in Figure 59 shows that the undersized paste deposit generated during stencil printing process had a very little effect on the volume of the solder joint formed after reflow. This is because BGA's already solder balls attached to them; in this case the BGA 144 had a 20mil solder ball which is relatively large when compared to the amount of solder paste printed.
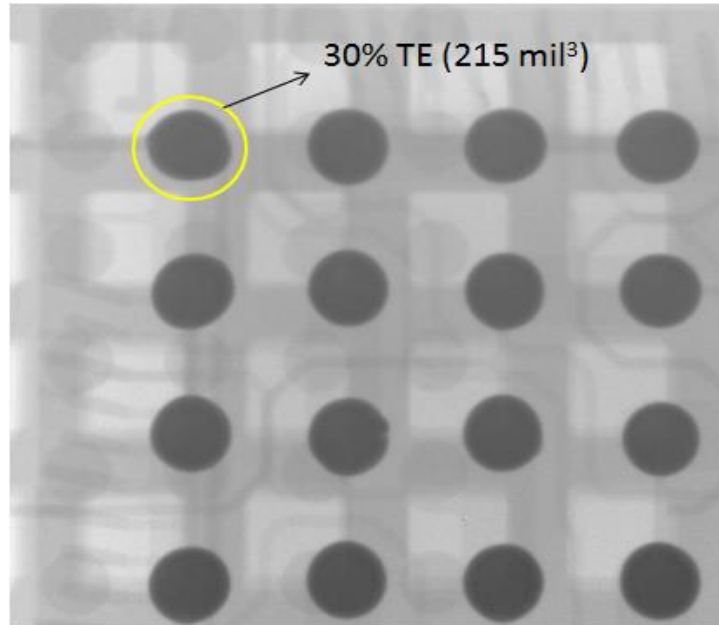
Figure 59 X-ray image of BGA 144 on Cu-OSP with a functional solder joint with ~30% TE (215 mil³).

4.1.6 BGA 360

A standard stencil aperture size of 10.7x10.7 was evaluated for the BGA 360 device and was found to yield an average TE of approximately 84%. The smallest deposit created with the standard design was 66% TE ($281mil^3$) while the largest measured 110% TE ($463mil^3$). A histogram of the standard deposit volume data may be found in Figure 60.
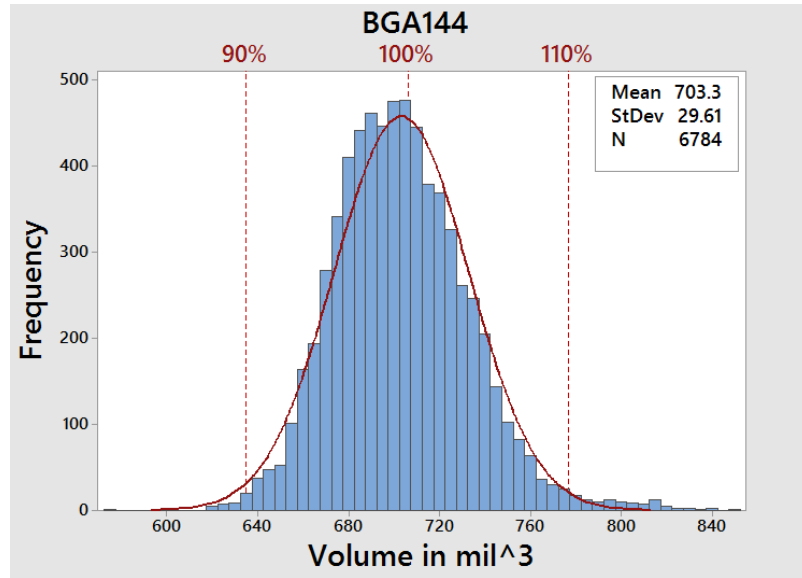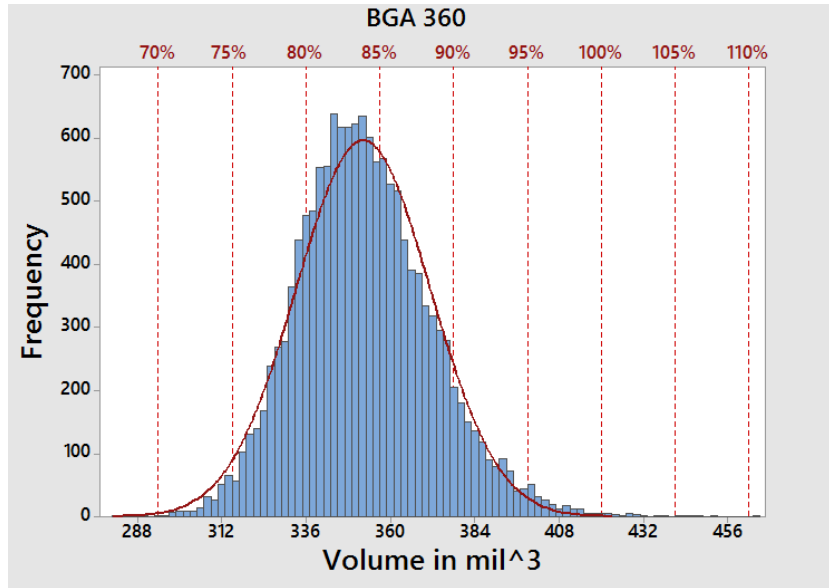
Figure 60 BGA 360 paste volume distribution for standard aperture.

Undersized apertures measured 7.2mil (UA1), 6.4mil (UA2) and were designed to target a 40% to 50% TE relative to the standard aperture volume. During the assembly process the actual transfer efficiency ranged from a low of 0% to a high of 34% (0 to 145 mil^3). Because it is a BGA it managed to form an electrically functional joint even though the PCB pad had no paste printed on it. The solder paste volume data for BGA 360 can be found in Figure 61.
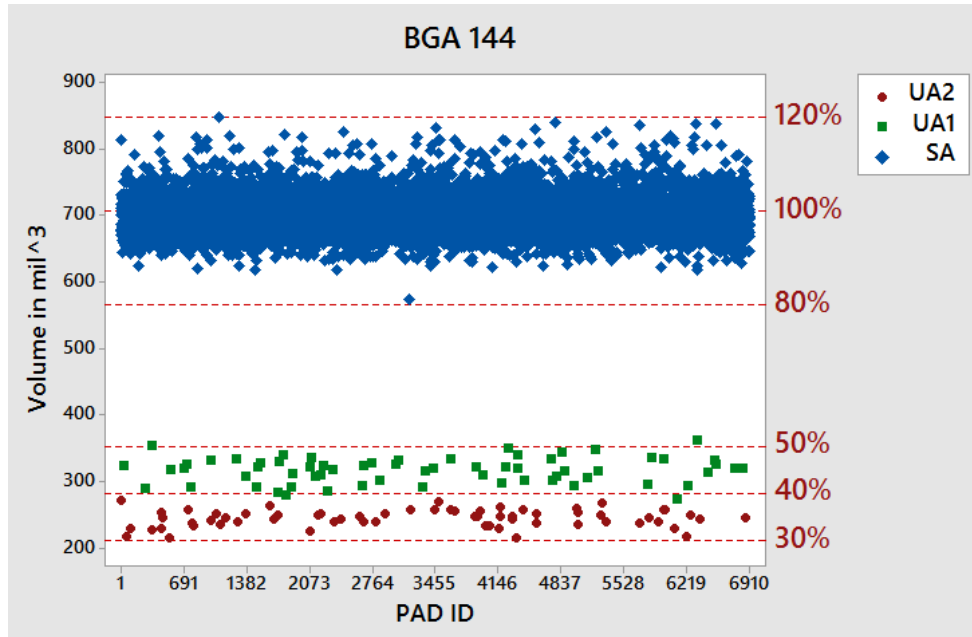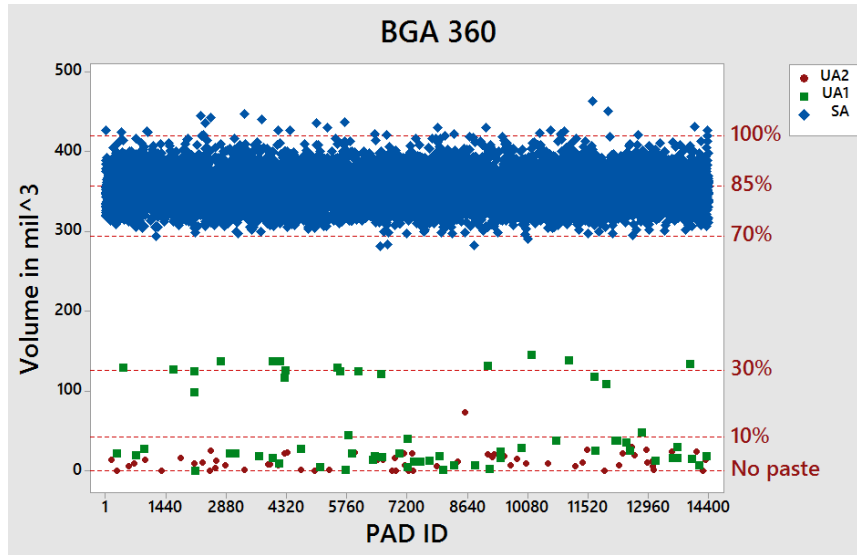
Figure 61 Comparison of Standard Aperture (SA) paste deposit volumes and Undersized Apertures (UA1, UA2) paste deposit volumes used to assemble BGA 360 to Cu-OSP motherboards.

The X-ray image found in Figure 62 shows that the PCB pad which had no paste deposited during stencil printing process has formed an electrically functional solder joint after reflow. This is because BGA's already solder balls attached to them; in this case the BGA 360 had a ~10mil solder ball attached to it.
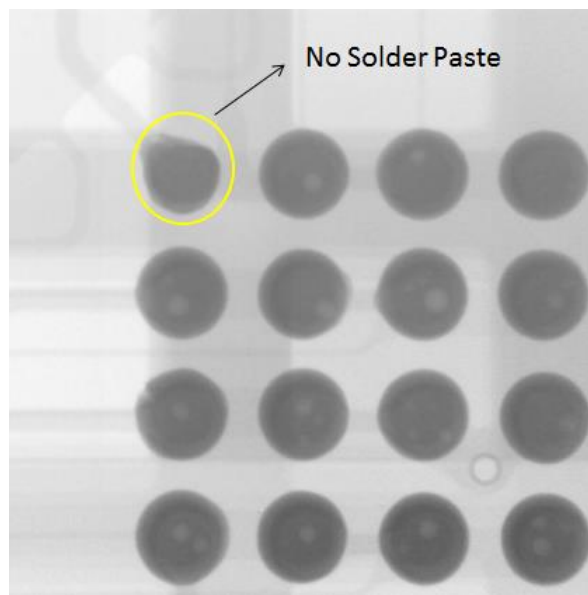
Figure 62 X-ray image of BGA 360 on Cu-OSP with a functional solder joint when no paste was printed on the pad.

4.2 Reliability Results

All the samples which passed assembly yield tolerance determined from the assembly results were subjected to accelerated thermal cycling using a -40^{0}C to 125^{0}C thermal profile. Table 5 shows the TE ranges for each component tested in ATC.

Component	Surface Finish	Min TE	Max TE
LGA 208	Cu-OSP/ENIG	61%	160%
LGA 97	Cu-OSP	45%	112%
QFN 100	Cu-OSP	35%	130%
QFN 156	Cu-OSP	41%	116%
BGA 144	Cu-OSP	30%	120%
BGA 360	Cu-OSP	0%	115%

Table 5 Transfer efficiencies ranges tested in ATC.

4.2.1 LGA 208 on Cu-OSP

Thermal cycling results for the entire LGA 208 population on Cu-OSP motherboards is contained in Figure 63. The data has been separated by stencil (control, Target 85% TE, Target 70% TE) and plotted using Weibull distributions.

The control samples (Blue) had a TE ranging from 81% to 125%, the target 85% TE samples (Red) had a TE ranging from 77%-99% and the target 70% TE samples (Green) had a TE ranging from 61%-81%.
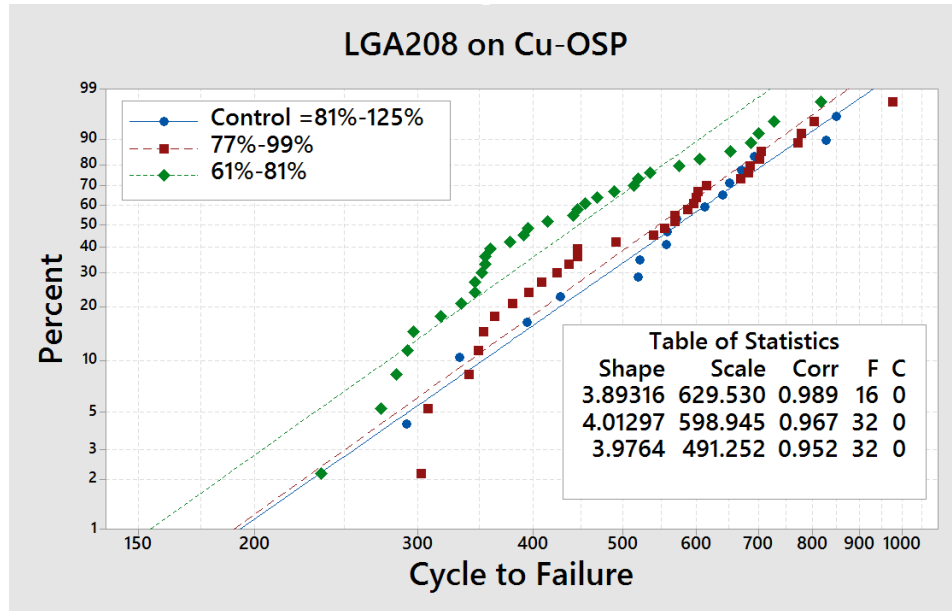
Figure 63 Weibull plot comparing solder joint reliability of control LGA 208 samples with Target T.E 85% and Target T.E 70% LGA 208 samples on Cu-OSP surface finish.

From Figure 63 there is a significant 22% reduction in characteristic lifetime for the samples created with a target TE of 70% at the outlier solder joint positions, but just a 4% reduction in characteristic lifetime of the samples created with a target value of 85% TE at the outlier positions.

Failure analysis would reveal that the LGA 208 device fails due to corner joint solder fatigue, and images of typical fatigue cracks may be found in Figure 64. Furthermore, the devices with intentional low-volume outliers almost always failed at the outlier solder joint, partly due to the fact that only one corner position contained an intentional outlier.

Figure 64 a. LGA 208 control sample corner joint failure @ 428 cycles, b. LGA 208 85% sample corner joint failure @ 341 cycles, c. LGA 208 75% sample corner joint failure @ 335 cycles.

Because the outliers were by far the most likely positions to fail, and because the deposits sizes varied significantly, the lifetime results were also examined as a scatter plot of deposit volume versus component lifetime (Figure 65). This analysis considers the measured paste deposit volume of the identified failure location and its effect on component life.
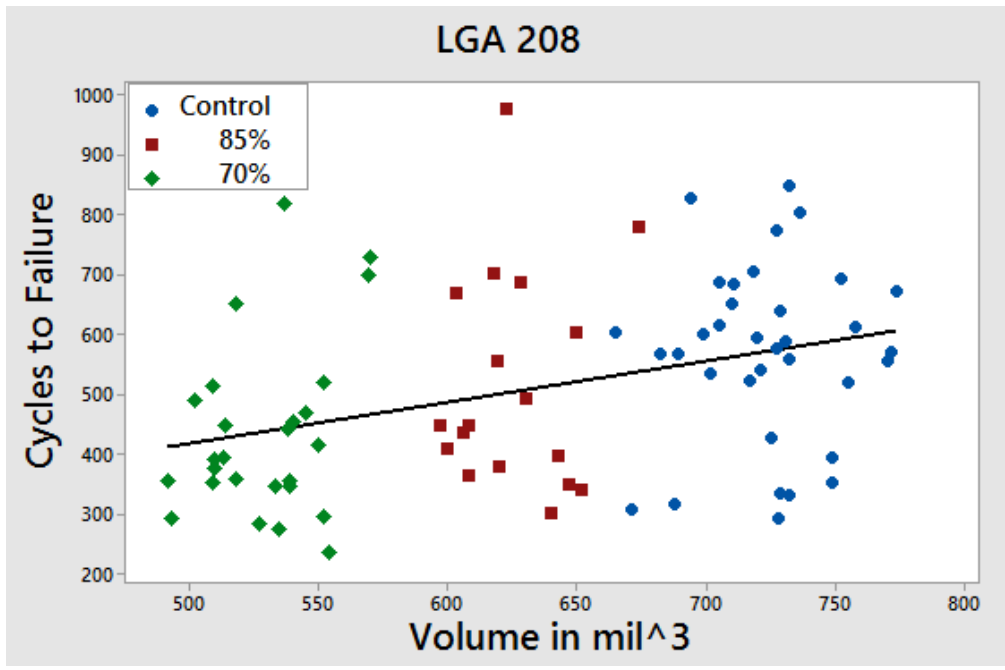
Figure 65 Cycles to Failure Vs. Volume for LGA 208 on Cu-OSP PCB.

Using this technique, a trend is clearly established showing a nearly 50% increase in lifetime when increasing the solder deposit size from 500 to 775mil3 although there is considerable scatter in the data. This analysis shows that the effect of outlier size is far greater than the initial Weibull plots indicated.

Because the LGA 208 sample sizes were reasonably large, another Weibull analysis was performed by grouping the failures into sets based on the Transfer efficiency of the failed joint.
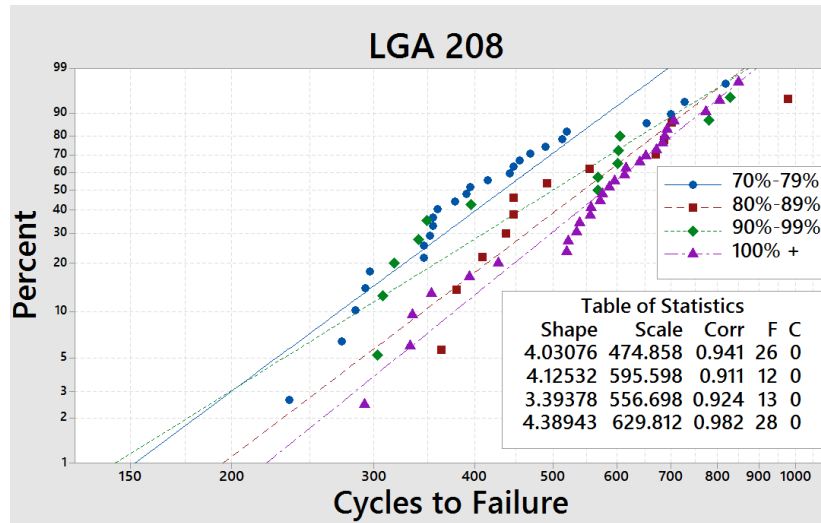
Figure 66 Weibull plot based on Transfer Efficiency of the failed joint of LGA 208 on Cu-OSP motherboards.

From Figure 66 it is clear that increase in TE improved the life time of LGA 208 components. There in a drop in reliability between the 80%-89% TE samples and 90%-99% TE samples but the difference is life time is only 6%. Therefore anything above 80% TE for LGA 208 would give similar reliability results as control samples.

4.2.2 LGA 208 on ENIG

Figure 67 shows the failure of LGA 208 on ENIG surface finish. The failure occurred in the bulk solder during thermal cycling due to fatigue.
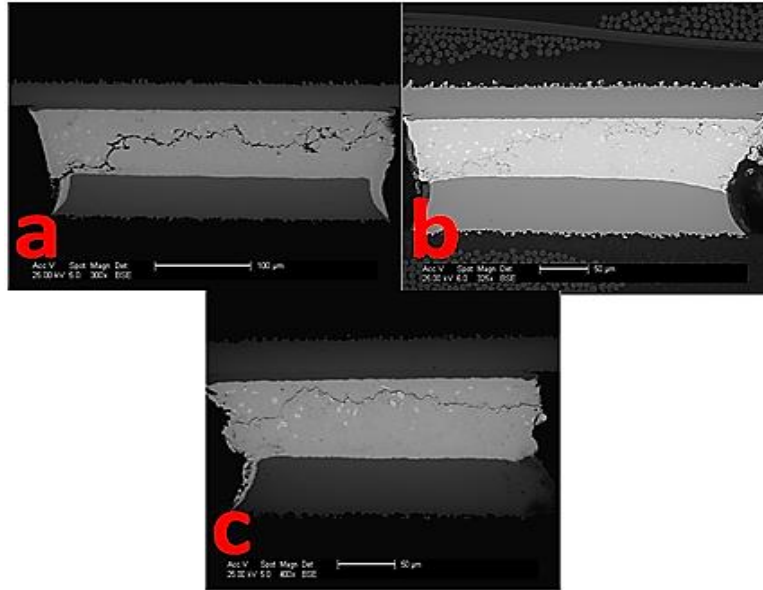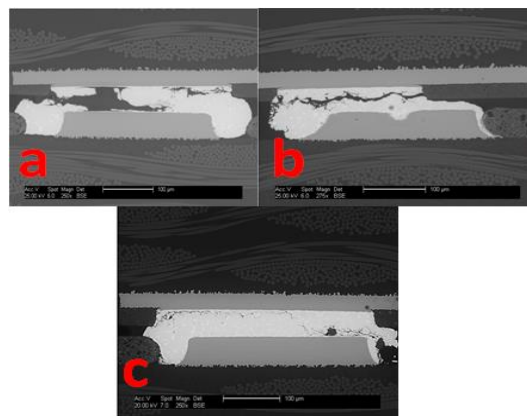

Figure 67 a. LGA 208 120% sample corner joint failure @578 Cycles, b. LGA 208 Control sample corner joint failure @387 Cycles, c. LGA 208 85% sample corner joint failure @353 Cycles.

From Figure 68 it is evident that T.E 120% LGA 208 samples have performed better than control samples and target T.E 85% samples. There is 35% increase in failure life time from control samples to T.E 120% samples and 25% reduction in failure life time from control samples to T.E 85% samples. Suggesting higher paste volume deposits has better reliability for LGA 208.
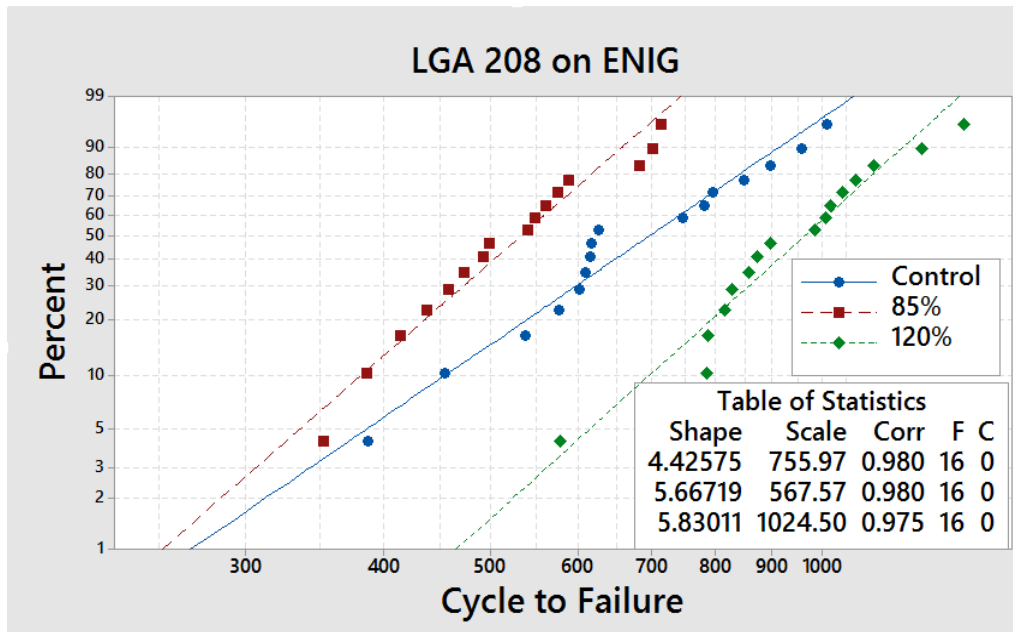
Figure 68 Weibull plot comparing solder joint reliability of control LGA 208 samples with Target T.E 120% and Target T.E 85% LGA 208 samples on ENIG surface finish.

4.2.3 LGA 97 on Cu-OSP

The data has been separated by stencil (control, Target 85% TE, Target 70% TE) and plotted using Weibull distributions.
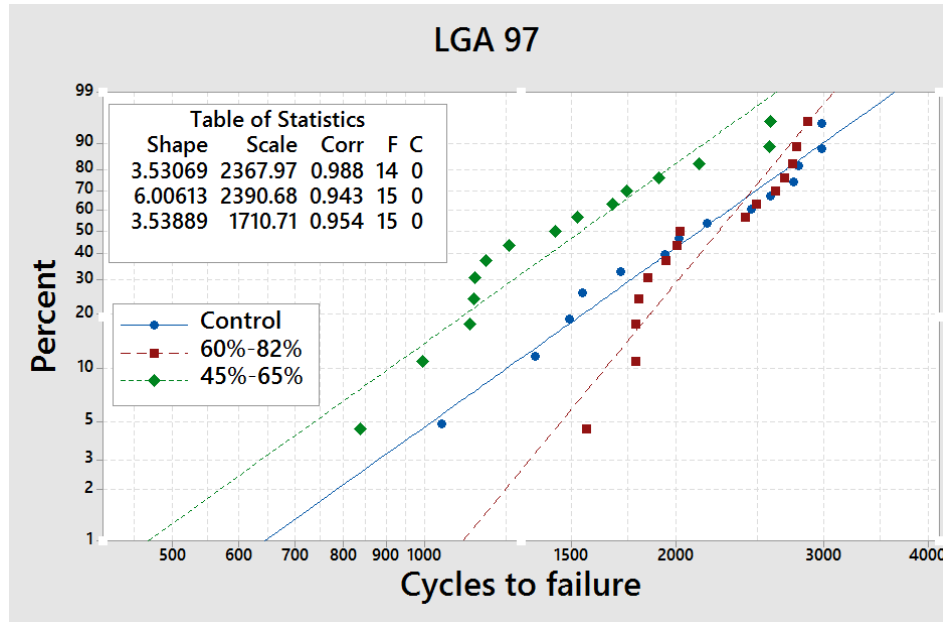
Figure 69 Weibull plot comparing solder joint reliability of control LGA 97 samples with Target T.E 85% and Target T.E 70% LGA 97 samples on Cu-OSP surface finish.

The control samples (Blue) had a TE ranging from 71% to 112%, the target 85% TE samples (Red) had a TE ranging from 60%-82% and the target 70% TE samples (Green) had a TE ranging from 45%-65%.

From Figure 69 there is no significant difference in characteristic lifetime for the samples created with a target TE of 85% at the outlier solders joint positions and control samples, but there is 27% reduction in characteristic lifetime of the samples created with a target value of 70% TE at the outlier positions. Showing a same trend as LGA 208, indicating increasing the TE increases lifetime. So for LGA 97 TE above 70% would give comparable reliability results as control samples.

4.2.4 QFN 100 on Cu-OSP

The QFN 100 was evaluated using a standard assembly process which produced an average TE of 104% (i.e. Control samples) and with outlier apertures targeting a minimum 40% and 50% TE on Cu-OSP motherboards.

Due to print variability the standard process actually resulted in TE of 74 to 144% while the 40% target volume design resulted in TE of 35 to 50% and the 50% target volume design resulted in TE of 46 to 74%. Because there was little to no overlap in the TE ranges, the three stencil designs were evaluated independently and three Weibull plots were produced to compare the lifetime results. These Weibull plots, as contained in Figure 70, indicate that the standard design (Control) resulted in a QFN 100 assembly with a characteristic lifetime (N63.2) of 2112 cycles with first failure being detected at cycle 976.
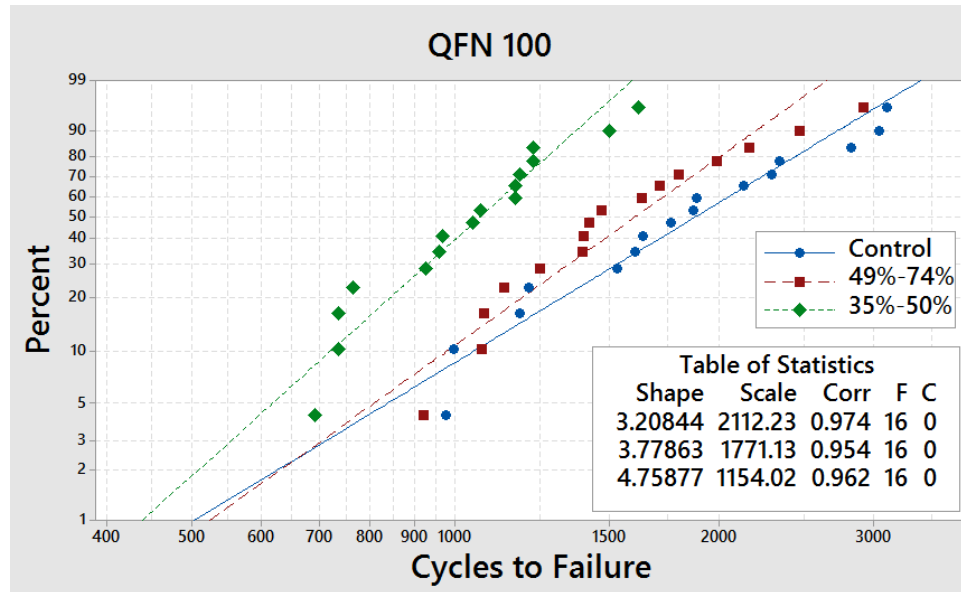
Figure 70 Weibull plot comparing solder joint reliability of control QFN100 samples to Target TE 50% and Target TE 40% QFN100 samples.

The Weibull also show that the 50% target TE samples did not perform as well as the control. In this case the first failure was detected around cycle 919 and characteristic lifetime of the sample set was 1771 cycles, or a 16% reduction from the control.

Continuing on, the lifetime analysis of the 40% TE samples shows that these devices performed significantly worse than either the control or 50% TE specimens. In this instance the target value of 40% TE resulted in first failure at cycle 700 and a characteristic lifetime of just 1154 cycles, which is a reduction of 43% versus the control.

Electrical test of QFN 100 was able to isolate the daisy-chain failure locations to specific rows of solder joints and failure analysis by cross-sectioning was used to determine which solder joint was responsible for electrical failure. The analysis reveals that the QFN 100 component fails during thermal cycling due to a solder joint fatigue mechanism. As shown in Figure 71, the joints tend to fail due to fracture near the component attachment pad. In all samples evaluated, the crack path appears to have

propagated through the bulk solder just below the CuSn intermetallic that forms at component pad surface.

Figure 71 a. QFN 100 control sample corner joint failure @976 Cycles, b. QFN 100 target TE 50% sample corner joint failure @919 Cycles, c. QFN 100 target TE 40% sample corner joint failure @691 Cycles.

In most instances, the failed solder joint position for each QFN 100 device was at the corner of the device. Because the outlier deposits were placed at the corners of the packages, the failure analysis results confirm that the presence of the reduced TE deposits is responsible for the reduction of the measured lifetime of the packages.

4.2.5 QFN 156 on Cu-OSP

The data has been separated by stencil (control, Target 50% TE, Target 40% TE) and plotted using Weibull distributions.

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The control samples had a TE ranging from 53%-116%, the target 50% TE samples had a TE ranging from 41%-81% and the target 40% TE samples had a TE ranging from 17%-40%.

From Figure 72 it is evident that control QNF 156 samples have performed better than target TE 50% and target TE 40% samples. There is 17% and 23% reduction in failure life time for target TE 50% samples and target TE 40% samples respectively when compared to control samples. Suggesting higher paste volume deposits at corner pads has improved the reliability for QFN 156 samples.

Figure 72 Weibull plot comparing solder joint reliability of control QFN 156 samples with Target T.E 50% and Target T.E 40% QNF 156 samples.
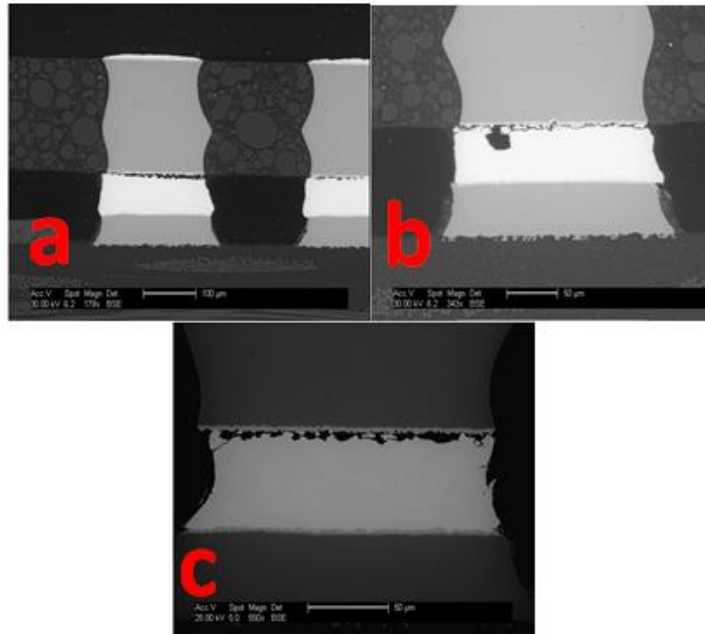
Figure 73 a. QFN 156 control sample corner joint failure @362 Cycles, b. QFN 156 target T.E 50% sample corner joint failure @393 Cycles, c. QFN 156 target T.E 40% sample corner joint failure @386 Cycles.

Figure 73 shows the failure of QFN 156 samples. These failures also take place at the component side as shown in the figure. All components have failed near the IMC interface. The failure mode is similar to QFN 156.

4.2.6 BGA 144 on Cu-OSP:

Figure 74 Weibull plot comparing solder joint reliability of control BGA144 samples with Target T.E 50% and Target T.E 40% BGA 144 samples.

From Figure 74 it is evident that target TE 40% samples performed better than target TE 50% and Control samples. Target TE 40% samples shows 38% and target T.E 50% samples show 11% improvement in failure life time than control samples. Suggesting lower paste volume at a corner joint has improved the reliability of BGA 144 samples.
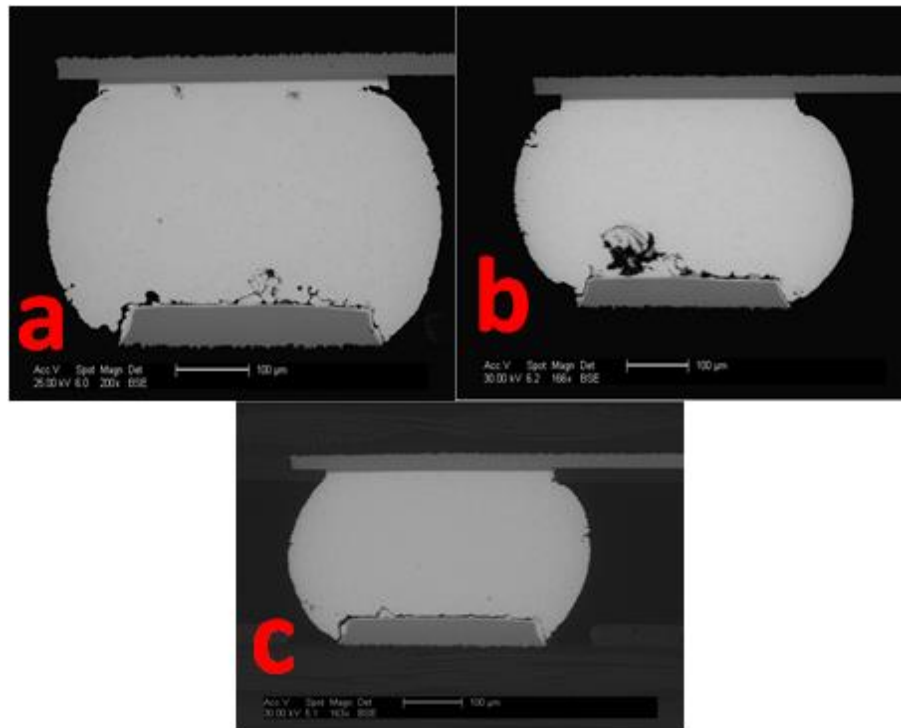
Figure 75 . a) BGA 144 control sample corner joint failure @972 cycles, b) BGA 144 target T.E 50% sample corner joint failure @783 Cycles , c) BGA 144 target T.E 40% sample corner joint failure @915 Cycles.

Figure 75 shows the failed joints of BGA 144. The failure of the joint was on the board side, a thin crack is initiated at the high stress region of the solder joint and propagates all the way till it causes a complete electrical contact failure in thermal cycling.
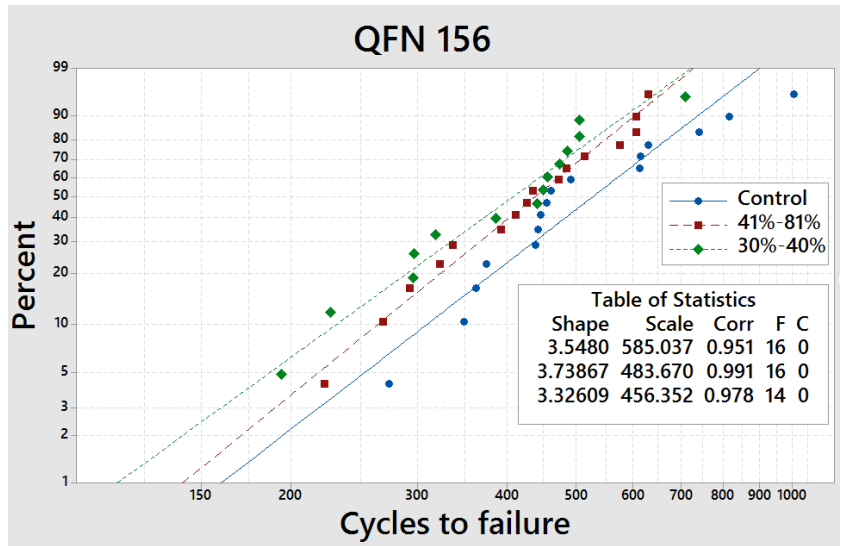
4.2.7 BGA 360 on Cu-OSP
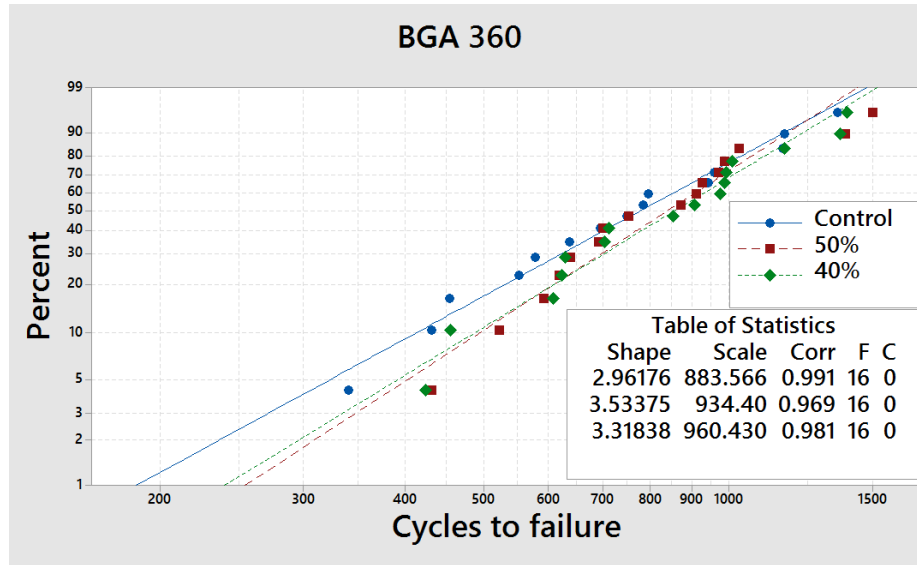
Figure 76 Weibull plot comparing solder joint reliability of control BGA144 samples with Target T.E 50% and Target T.E 40% BGA 360 samples.
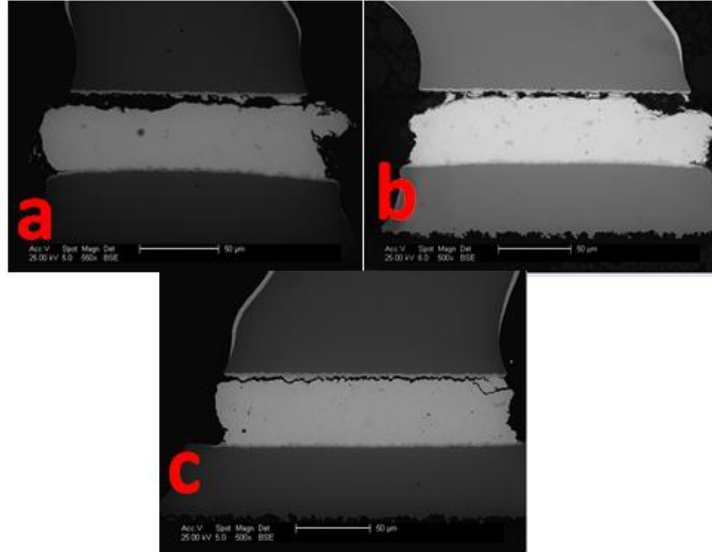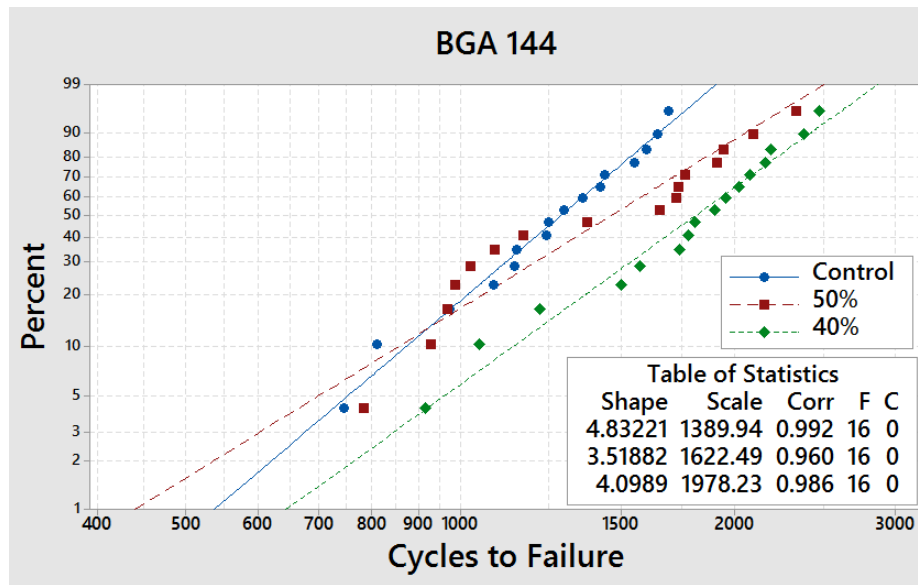
From Figure 76 it is evident that target TE 40% samples and target TE 50% performed better than the Control samples. Target TE 40% samples shows 8% and target TE 50% samples show 5% improvement in failure life time than control samples the numbers are not statistically significant. Suggesting paste volume outliers at a corner joint had no significant effect on the reliability of BGA 360 samples.
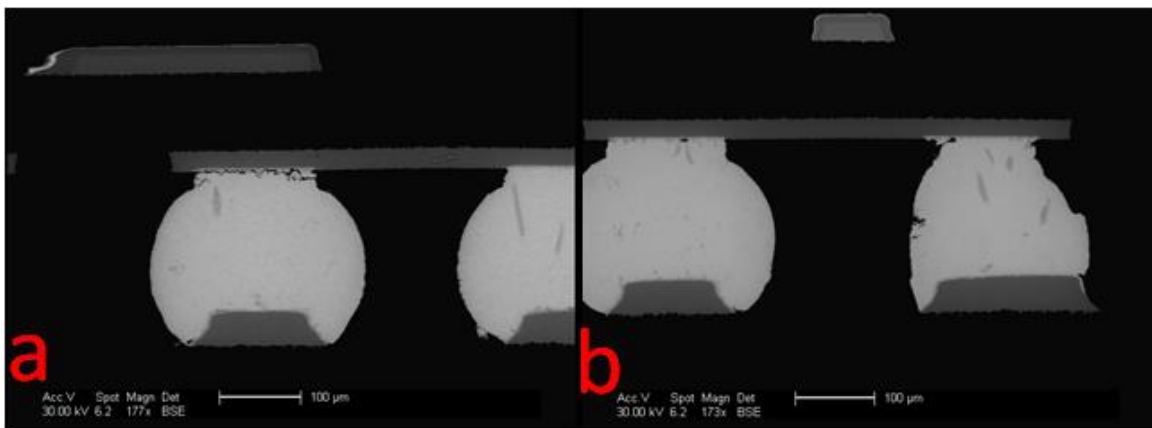
Figure 77 a. Corner joint failure of standard joint of target 40% TE sample; b. Undersized functional joint of the sample in adjacent figure.

From the X-ray images in Figure 77, it is observed that the sample which had an undersized joint did not fail at the undersized joint location but failed at a corner location which had a good sized standard joint. Out of 32 samples which had undersized joints, 20 samples failed at a good standard joint location when the undersized joint was still electrically functional.

4.3 Conclusion

From the assembly and reliability results it is evident that outliers in solder paste printing process will affect the assembly yield and reliability of bottom terminated components (BTC) and BGA's had no reduction in reliability due to low volume paste deposits, this can be expected because the volume of the solder paste printed is very little when compared to the volume of the BGA ball in this experiment the total volume of the solder paste printed is about 10% of the volume of the solder ball. But for BTC the entire joint should be formed based on the solder paste deposited during stencil printing process. Therefore a precise tolerance limit for the solder paste volume deposited is needed for these BTC package types to achieve good assembly yields and reliability.

From this experiment it is observed that LGA's and QFN's deliver better reliability for joints formed with higher TE paste deposits when compared to joints formed with low TE.

We have up to this point deduced the consequences of undersized paste deposits through comparison of the characteristic lives as indicated in the Weibull fits to the failure rate distributions. This would not necessarily be a meaningful metric for product populations

in the field however. There, product reliability perception (and warranty cost) is determined principally by the early life regime of the failure rate distribution. In the event that the shapes of the failure rate distributions are relatively unchanged when the undersized deposits are introduced into the population, any observed reduction in characteristic life will be replicated in the early life fails. This appears to be the case for the packages evaluated in this study. Compare for instance the failure rate distributions produced with various reduced TE populations on the LGA208 (*Figure 78*).
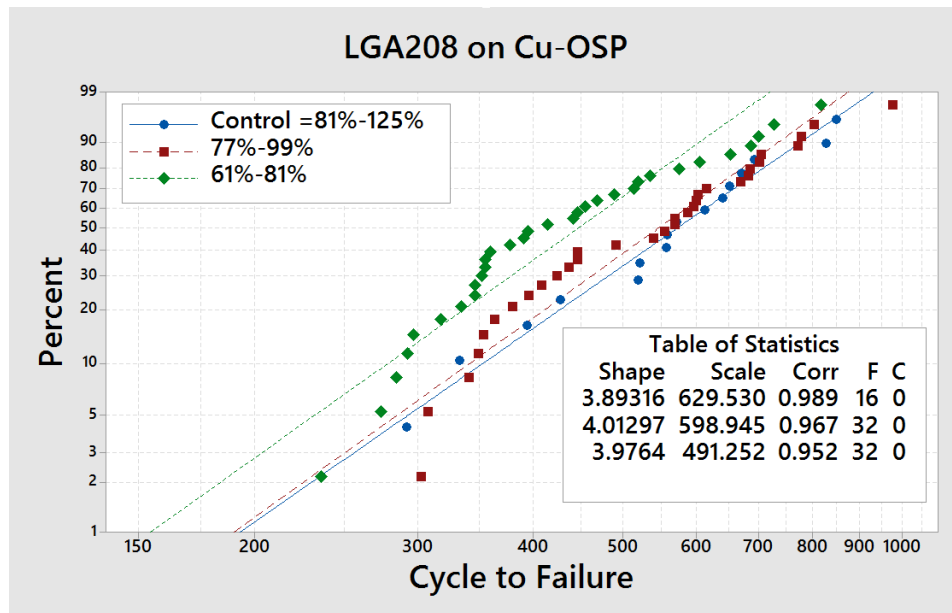
Figure 78 Weibull analysis of LGA 208 on Cu-OSP

The Weibull shape factors stay very near 3.9 regardless of the imposed lower TE level. And even where the Weibull fit is less than ideal for the early failures, the fit deviations are observed to be similar for each different level of TE reduction. Thus, the reduction in thermal cycle lifetime indicated by the characteristic lives will similarly be observed in the early life failure regime.

Similarly for the QFN156 (*Figure 79*), the Weibull shape factor remains relatively unchanged (3.5±0.2) across a range of print transfer efficiencies.
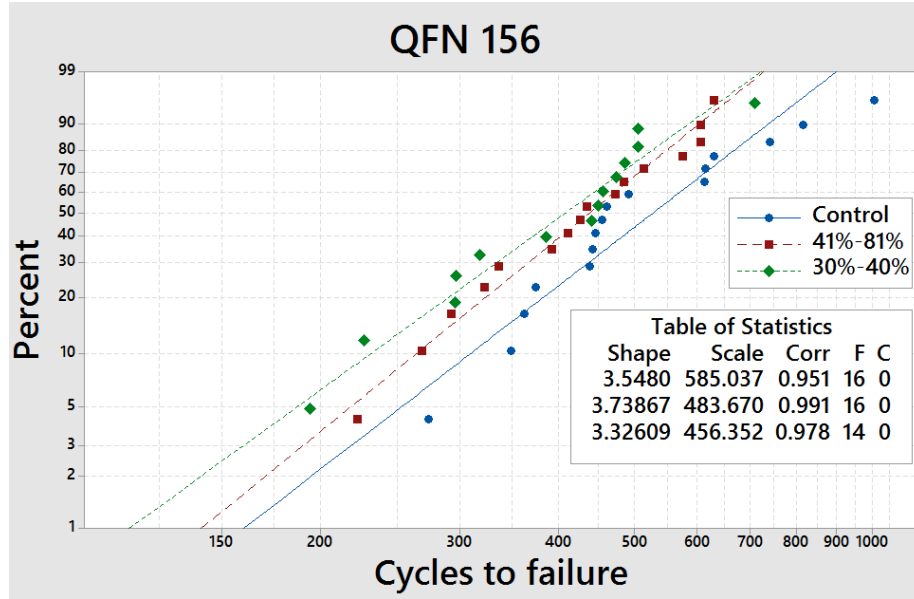
Figure 79 Weibull analysis of QFN 156

The reduction in characteristic life with reduced paste print TE produces a similar reduction in cycles to first failure. These and similar examinations on other BTC package types included in this study indicate that the reduced TE paste printing is very likely to produce a measurable increase in early field failures. And if the low TE paste deposits are generated at corner location of the package it effect on early field failures is significantly increased.

Good assembly yield is defined as an assembly which always resulted in an electrically functional joint after reflow. And good reliability is defined as anything greater than 15% reduction from the characteristic life time of the control samples.

Device	TE for Good Assembly Yield	TE for Good Reliability
LGA 208	60%	80%
LGA 97	50%	70%
QFN 100	30%	50%
QFN 156	30%	50%
BGA 144	30%	30%
BGA 360	30%	30%

Table 6 Acceptable lower limits of transfer efficiencies for good assembly yield and reliability.

Based on the experimental results Table 6 lists the TE tolerance limits to obtain high assembly yields and good reliability for the components under test. For BGA's it was observed low solder paste volume deposits at corner locations improved reliability of the package, but lowering the solder paste deposits may not be practical and a nitrogen atmosphere is used for reflow which most of the high volume manufacturers do not use to save cost. So, based on the results it was decided a 30% TE cutoff would be ideal for BGA's for both assembly yield and reliability.

References

Amalu, E. H., Ekere, N.N., Mallik.S. 2011. "Evaluation of rheological properties of lead-free solder pastes and their relationship with transfer efficiency during stencil printing process." *Materials and Design* 32: 3189-3197.

Biemans. 2011. "5D solder paste inspection merits beyond 3D technology." *Gobal SMT and Packaging* 8-13.

Burr, D.C. 1998. "Printing Guidelines for BGA and CSP Assemblies." *Surface Mount International.* San Diego, CA: SMTA. 417-424.

Burr, D.C. 1997. "Solder Paste Inspection: Process Control for Defect Reduction." 1036-1037.

Chen, J., et al,. 2011. "Method Of Determining Solder Paste Inspection Tolerance Settings." *SMTA International.* Fort Worth, TX. 799-813.

CyberOptics. 2013. "Importance of True Heights Measurement." http://www.cyberoptics.com/pdf/WhitePapers/True_Heights_White_Paper_Oct_2013.pdf.

Durairaj, R., Nguty.T.A., and Ekere.N.N. 2001. "Critical factors affecting paste flow during the stencil printing of solder paste." *Soldering & Surface Mount Technology* 12 (2): 30-34.

Electronics, Marantz Business. 2012. *SPI warps into the fifth dimension.* Accessed December 2015. http://www.dataweek.co.za/43654n.

Gunn, R., and Ries, B. 2001. "Selecting and Implementing Solder Paste Inspection for SMT Process Control." *IPC SMEMA Council APEX* 31-38.

Haslehurst.L., Ekere.N.N. 1996. "Parameter interactions in stencil printing of solder pastes." *Journal of Electronics Manufacturing* 6 (4): 307-316.

Huang C, Lin Y, Ying K, Ku C. 2011. "The solder paste printing process: critical parameters, defect scenarios, specifications, and cost reduction." *Soldering & Surface Mount Technology* 211-223.

Jianbiao Pan, Gregory L.Tonkay, Robert H.storer, Ronald M.sallade, David J.Leandri. 1999. "Critical Variables of Solder Paste Stencil Printing for Micro-BGA and Fine Pitch QFP." *IEEE/CPMT International Electronics Manufacturing Technology Symposium* 94-100.

Johnson, S.K. 2003. *Realizing the Benefits of 3D Inline Solder Paste Inspection.* Accessed january 2016. www.keysight.com.

Kim, K., Huh, S., Suganuma, K. 2003. "Effects of Intermetallic compounds on properties of Sn-Ag-Cu lead-free soldered joints." *Journal of alloys and compounds* 352 (4): 226-236.

Kulkarni, S., Langbridge, S., Johnson, D. 2014. "Inspection strategies for more accurate, faster and smarter inspection." *SMTA International Conference.* Rosemont, IL. 43-47.

Ladani, L.J., Dasgupta, A., Cardoso, I., Monlevade, E. 2008. "Effects of Selected Process Parameters on Durability and Defects in Surface-Mount Assemblies for Portable Electronics." *IEEE Transactions on Electronics Packaging Manufacturing* 31 (1): 51-60.

Lau, F.K.H., Yeung, V.W.S. 1997. "A hierarchical evaluation of the solder paste printing process." *Journal of Materials Processing Technology* 69 (1-3): 79-89.

Lee, N.C. 2001. "Reflow Soldering Process and Troubleshooting: SMT, BGA, CSP and Flip Chip Technologies (2nd ed.)." *Newnes.* New Delhi.

Liu, Y., and Johnson.R.W. 2006. "Optimization of lead free solder 01005 component assembly." *Soldering & Surface Mount Technology* 19 (1): 15-27.

Mallik, S., Scmidt, M., Bauer, R., Ekere, N.N. 2008. "Influence of solder paste components on rheological behavior." *Electronics System Integration Technology Conference.* Greenwich, NY. 1135-1140.

Mohanty R, and Haugen, P. 2008. " Solder paste inspection using 2D and 3D technique." *SMTA International.* New York City, NY. 63-69.

Nguty, T.A., Ekere, N.N., and Adebayo. A. 1999. "Correlating solder paste composition with stencil printing performance." *Electronics Manufacturing Technology Symposium.* Austin, TX. 304-312.

Riddle, M.E. 2007. *ascinternational.* Accessed January 2016. http://www.ascinternational.com/index.php/content/yield_improvement_strategy.

Sekharan, G., Rohani. J.M., Yusof, S.M., and Bakar, Z.A. 2006. "Optimization Of Solder Paste Printing Parameters Using Design Of Experiments (DOE)." *Jurnal Teknologi* 43(A): 11-20.

Yang, T., Tsai, T.N, Yeh, J. 2005. "A neural network-based prediction model for fine pitch stencil-printing quality in surface mount assembly." *Engineering Application of Artificial Intelligence* 18 (3): 335-341.