Electro-Static-Discharge (ESD) Protection in Touch and Display Driver Integrated (TDDI) Systems

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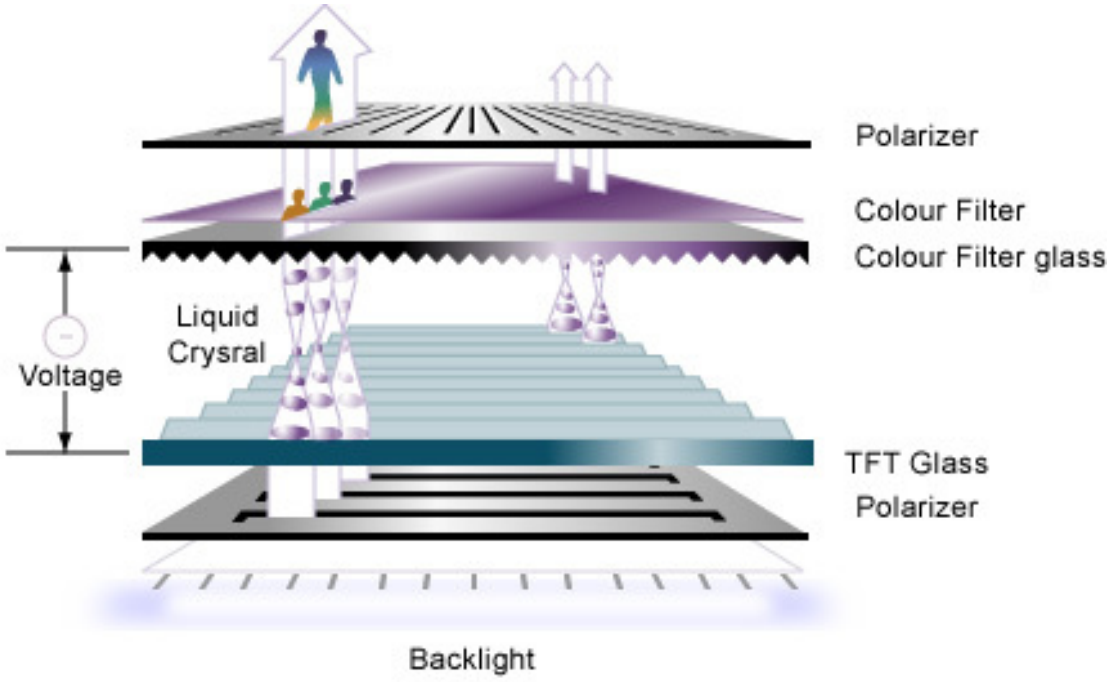
What is TDDI?

- TDDI is a Synaptics Inc. product that merges a standard display driver integrated circuit (DDIC) with a capacitive touch controller on a single chip.
- A DDIC is responsible for converting a digital image into the analog voltages required to drive a liquid crystal display (LCD).
- A capacitive touch controller detects changes in the electric field around electrodes built into the display.

LCD Displays



- LCD displays operate by applying an electric field to the liquid crystal material, forcing it into a certain orientation.
- The orientation will determine how much polarized light passed through the material controlling the brightness of each pixel.

Image: http://www.neowin.net/news/guide-to-smartphone-hardware-47-displays

Capacitive Multi-Touch Screen

- A capacitive touch screen operates by driving a signal out on electrodes (driving lines) in the screen, creating an electric field.
- Separate capacitive coupled electrodes (sensing lines) react to that electric field.
- An object near the touchscreens surface will changing the electrical field and modify the resulting signal on sensing lines.
- This signal gets interpreted by a processor to determine the 2D location of up to 10 objects.

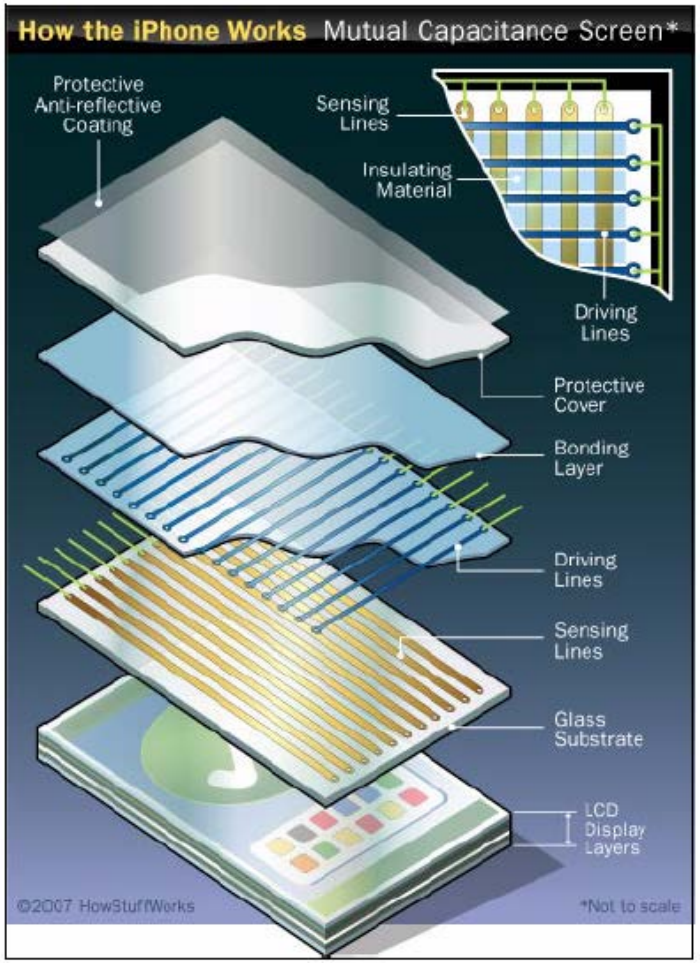


Image: http://electronics.howstuffworks.com/iphone2.htm

How is ESD protection integrated on a system level?

- The TDDI integrated circuit (IC) component is assembled into a system.
- The component is expected to meet certain component level ESD requirements while the system is expected to meet system level ESD requirements.
- Normally the system is responsible for ensuring the ESD stress seen by all components does not exceed their rating.

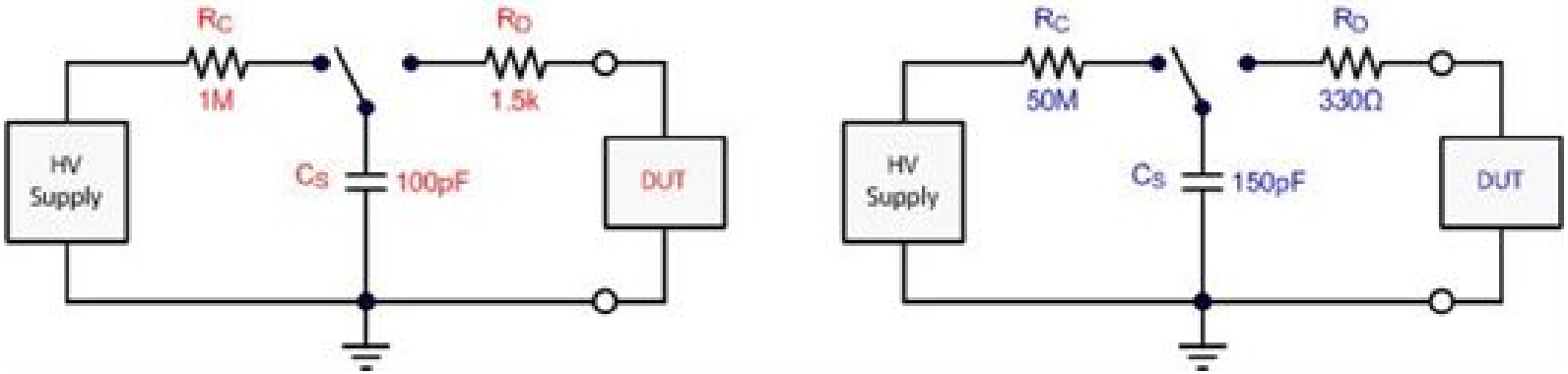
ESD Testing

Component Level Testing

- Simulated discharge through skin of an inadequately grounded person
- Intended to protect a component during manufacturing processes
- Component level testing is done to the Joint Electron Device Engineering Council (JEDEC) Human Body Model (HBM) and Charged Device Model (CDM) standards.

System Level Testing

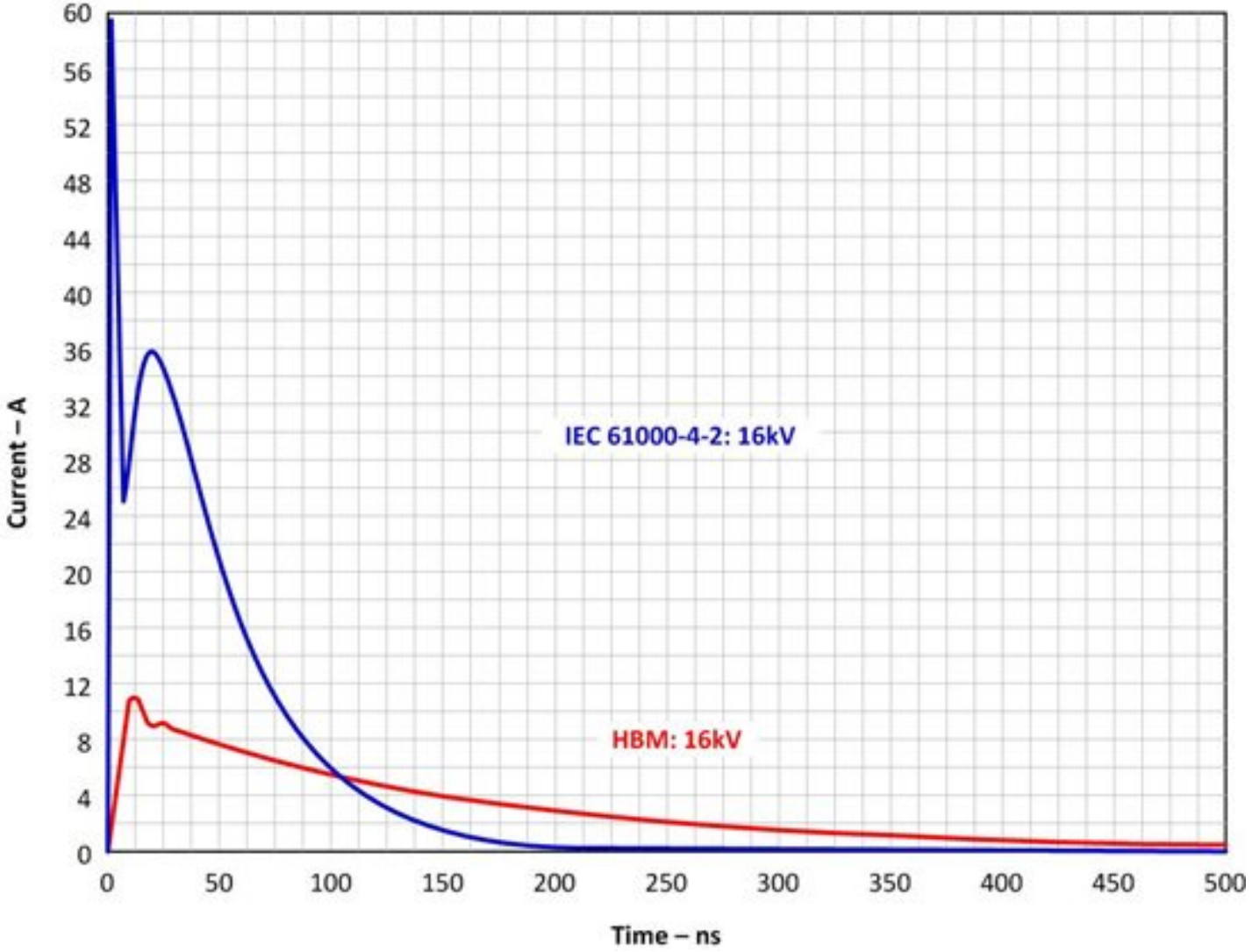
- Simulated discharge of an ungrounded person through a metal object (such as a tool or a connector)
- Intended to protect the end item from normal usage ESD stress
- System level testing is done to the International Electrotechnical Commission (IEC) 61000-4-2 standards.



Comparison of ESD generator models for HBM and IEC

Image Texas Instruments : http://e2e.ti.com/support/interface/industrial_interface/f/142/t/359524

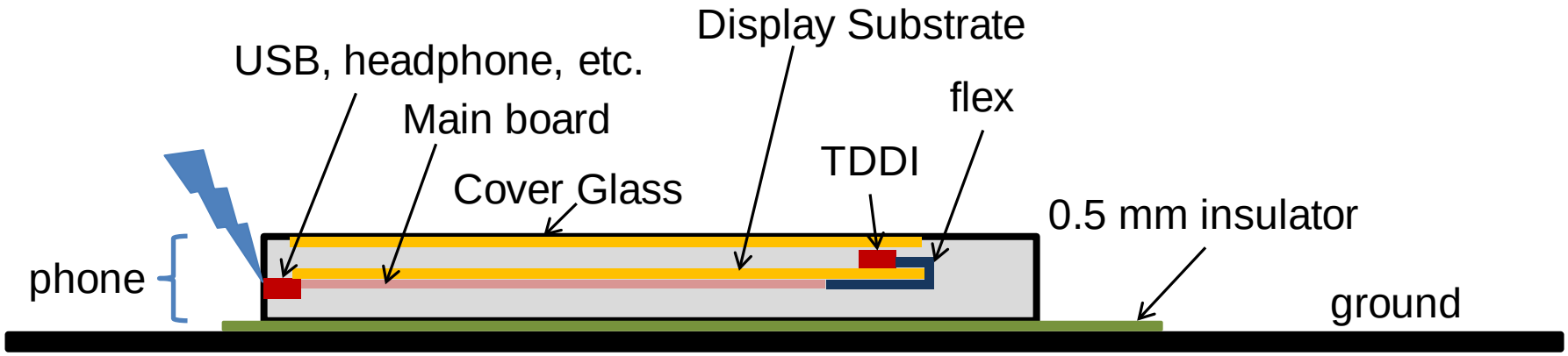
Current Profile of IEC Event vs. HBM

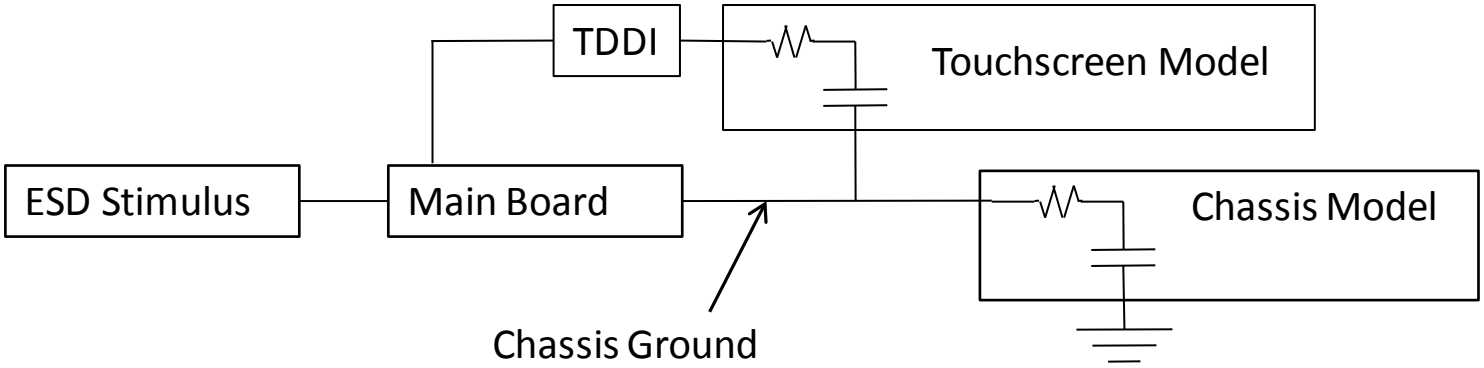


Comparison of current profiles for IEC and HBM of equal voltage

Image Texas Instruments : http://e2e.ti.com/support/interface/industrial_interface/f/142/t/359524

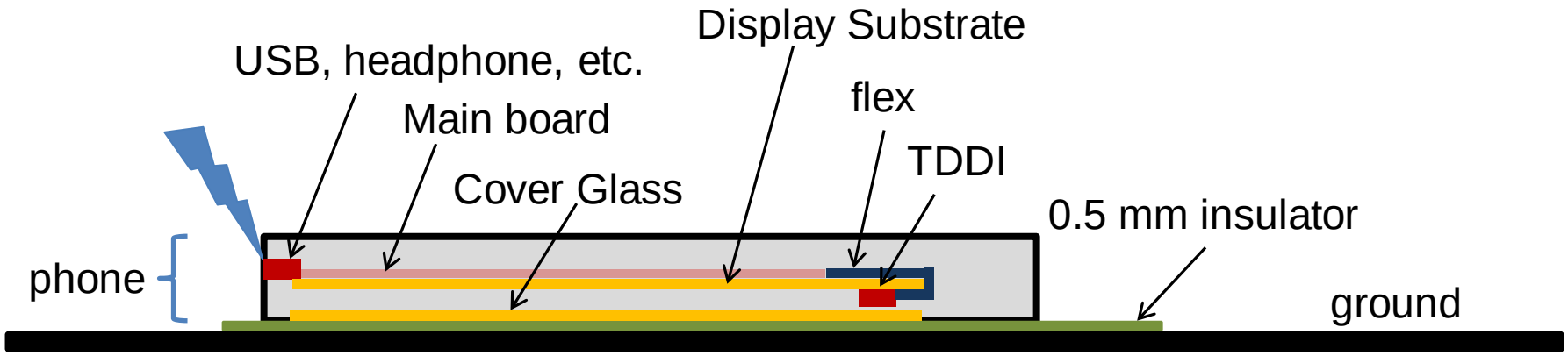
Display Side Up IEC Testing

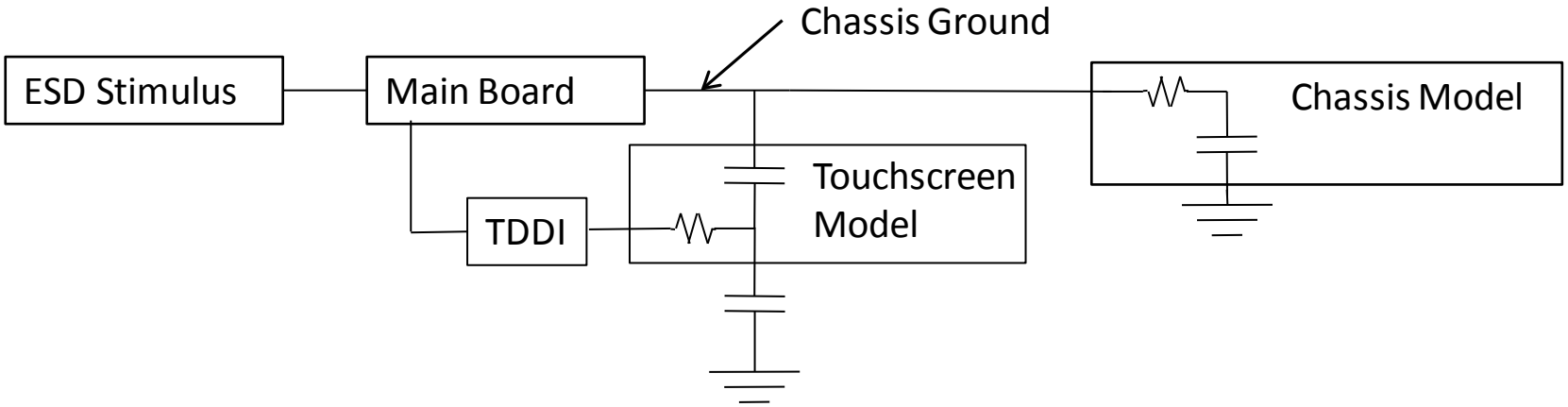




In this configuration, the primary discharge path is through the main board and the chassis. There is no significant discharge path through the TDDI IC and the display.

Display Side Down IEC Testing

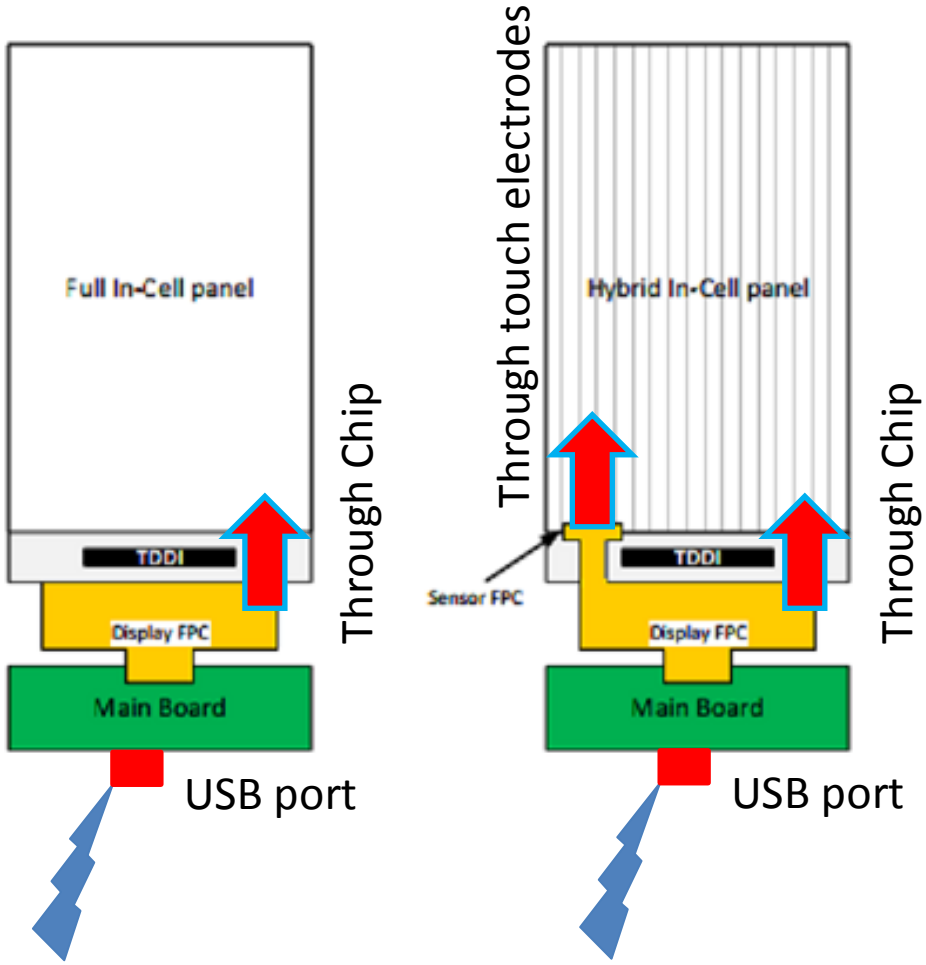




In this configuration, the display has a large capacitance to ground which can put the TDDI IC directly in a discharge path, causing both hard and soft failures.

TDDI Flexible Printed Circuits (FPC)

- The assembled display is connected to main board through an FPC .
- As component suppliers, we have no control over the FPC design, aside from providing a reference design.
- FPC design plays a major role in system level ESD performance.
- In certain system architectures, there is no low impedance path for current to flow around the TDDI IC to reach the display.

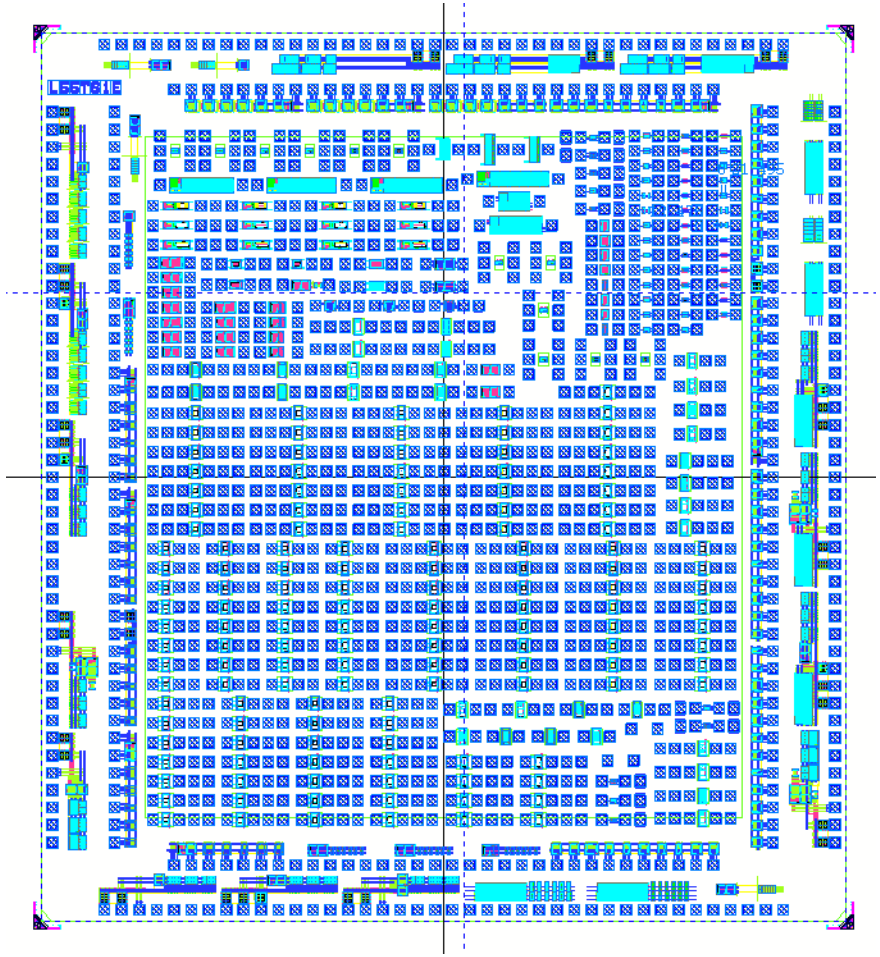


TDDI Specific Design Considerations

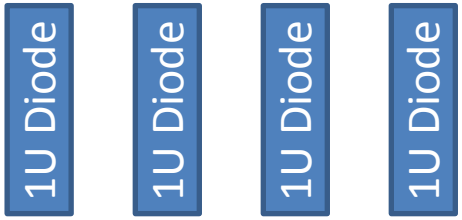
- The ESD stress seen by the TDDI IC during system level testing are inadequately modeled using an HBM test condition.
- As a result, transmission line pulse (TLP) characterization will be added to all ESD devices to better model the stress seen during an IEC ESD event [1].
- The highly coupled and resistive thin film transistors (TFTs) in the display dissipate the energy of the ESD event over multiple pins.
  - 576 touch pins and 2400 display pins on the TD4191 IC
  - Current will not divide evenly over all pins, therefore each pin must have a relatively high current sink specification
- Most recent designs have a target handling 4A of TLP current per output pin.
- Multiple active clamps along the chip have been designed with a combined current capability of 10A of TLP current for power supplies.

ESD Test Chip

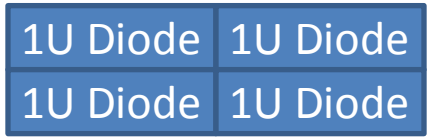
- Primarily ESD focused test chip with over 200 device variations
- Includes individual devices for evaluating the effects the primary parameters associated with ESD devices
- Includes full ESD scheme for variations of external I/O pins
- Also includes structures for evaluating ballasting strategies, metallization, and layout



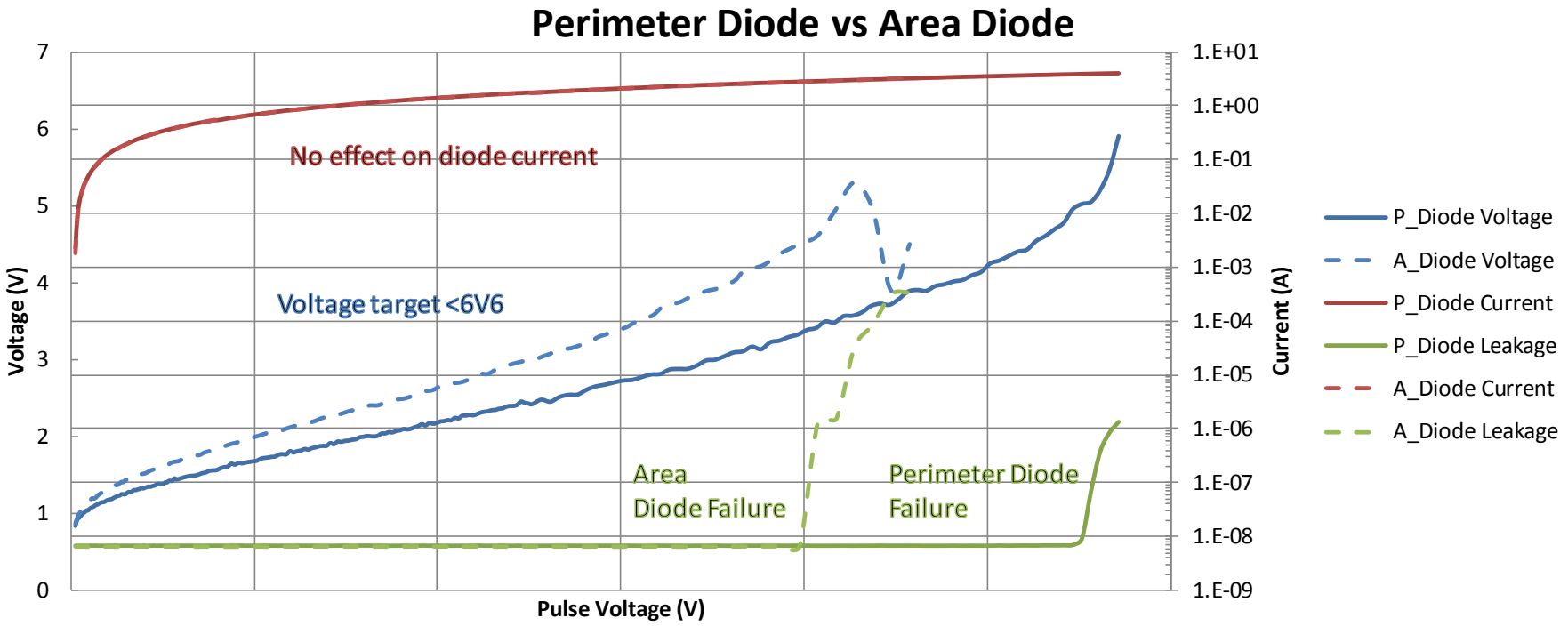
Diode Design



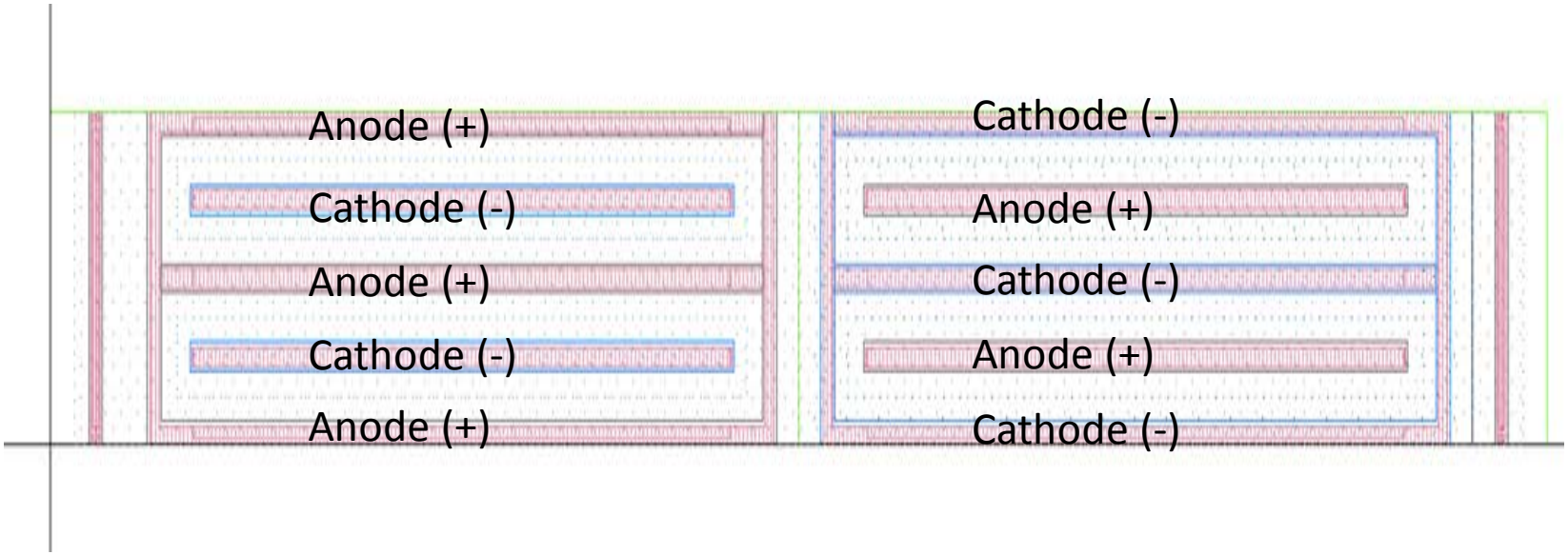
Perimeter Diode Configuration

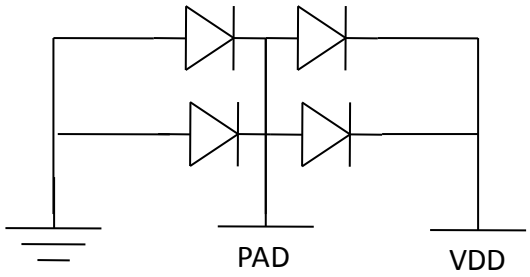


Area Diode Configuration

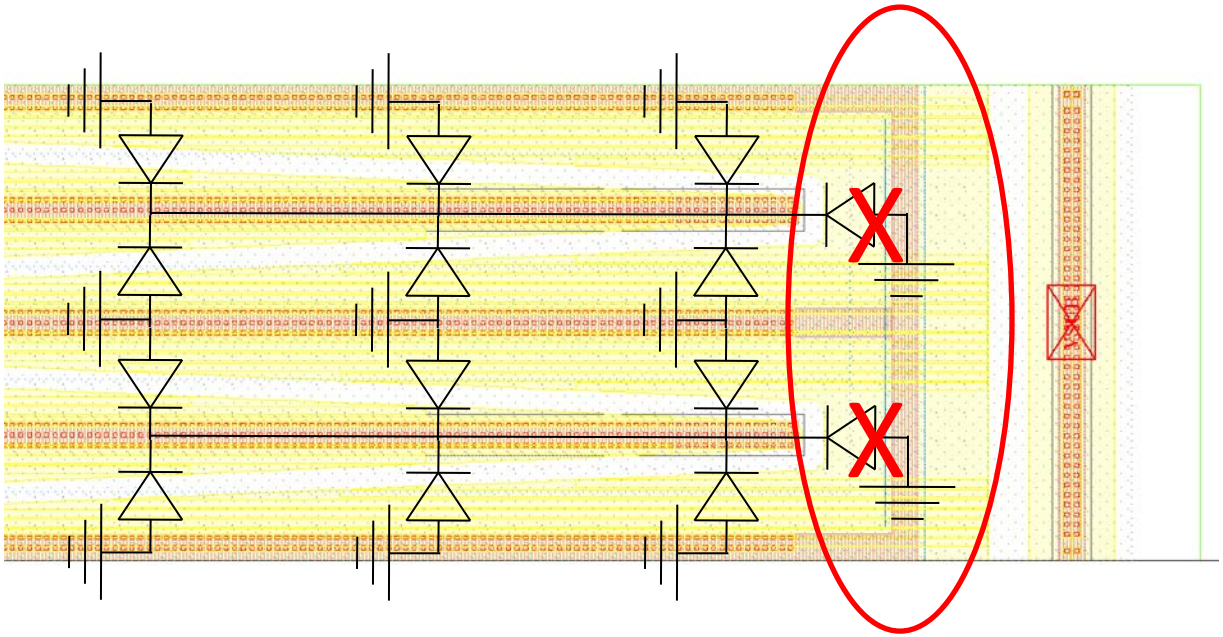


Diode Design



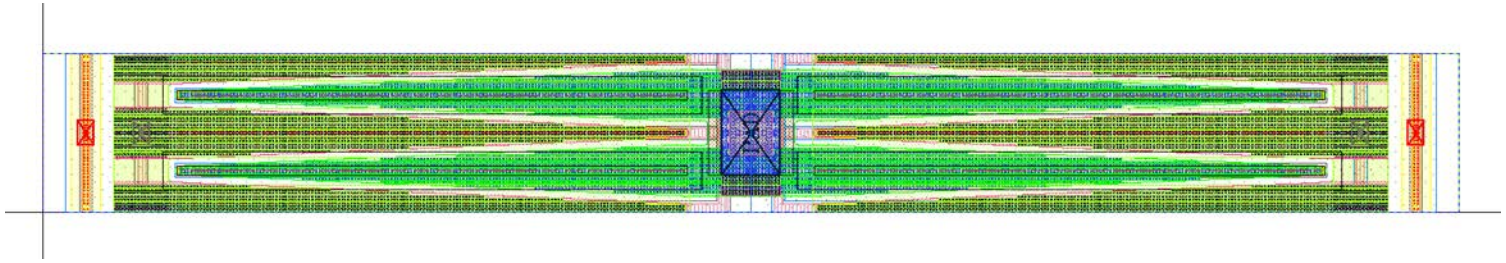


Current Density



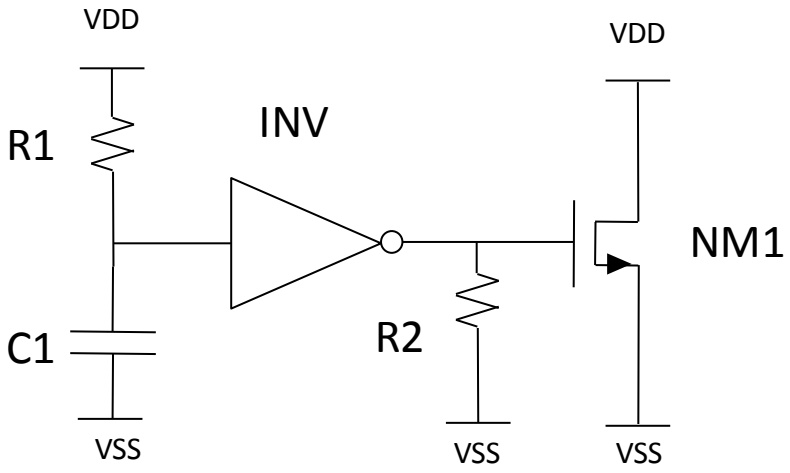
- Contact distribution is one of the primary reasons for improved performance of perimeter based diodes.
- Perimeter diodes less variation in impedance from one area to another, which gives all points of the diode a consistent current density.
- Inconsistent current density in ESD devices will cause localized failure and degrade device performance over time.

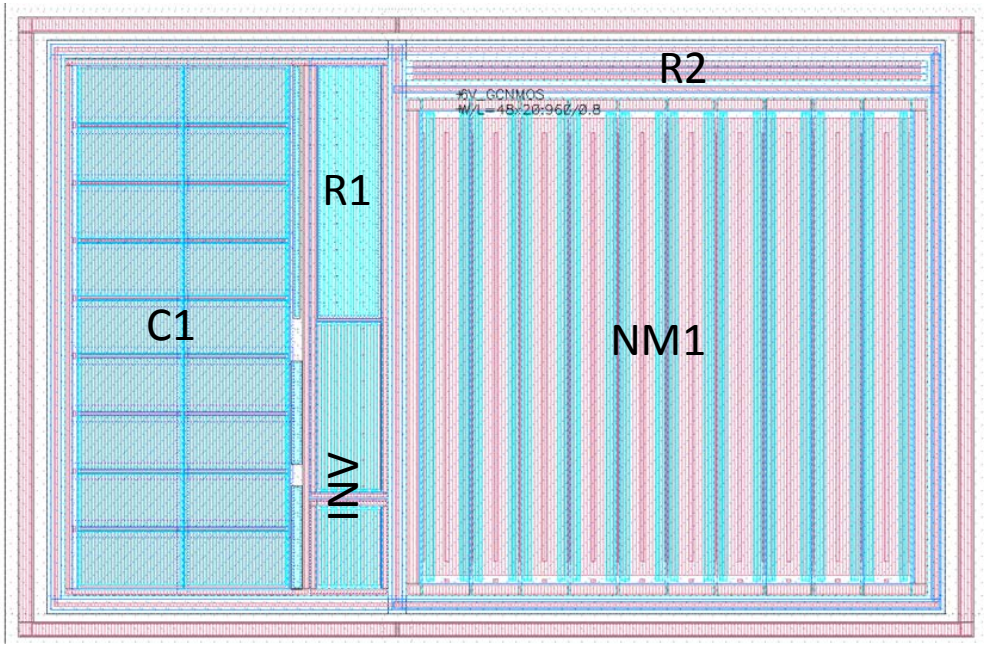
Diode Metallization



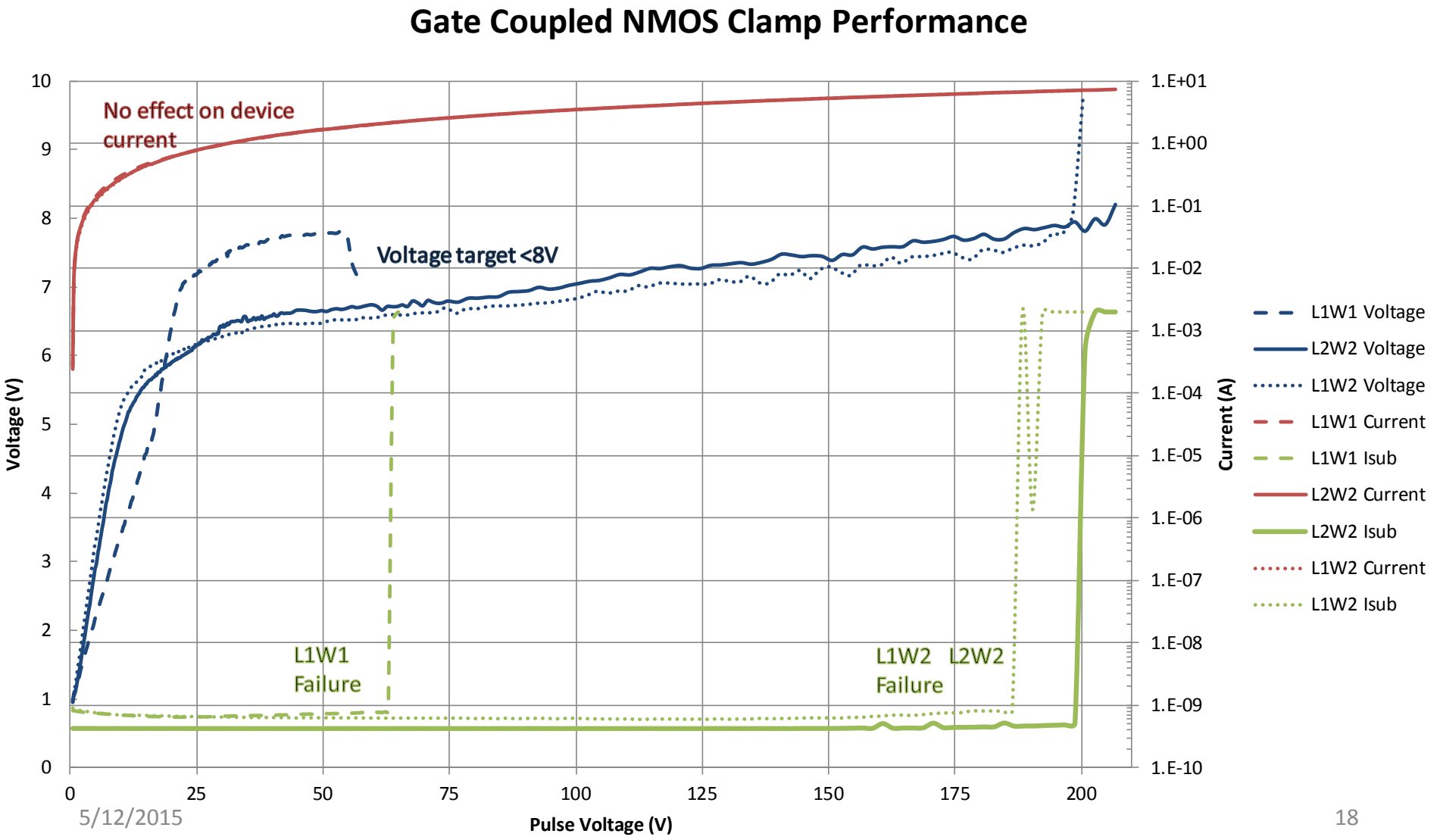
- Stacking multiple metal layers reduces overall impedance of the device.
- A tapered metal design improves heat dissipation in the areas subjected to the highest currents.
- Pad connection is a straight line through all metal layers from Pad to Metal 1 to ensure the ESD device is the lowest resistance path to a diode.

Gate Coupled NMOS Clamp Design

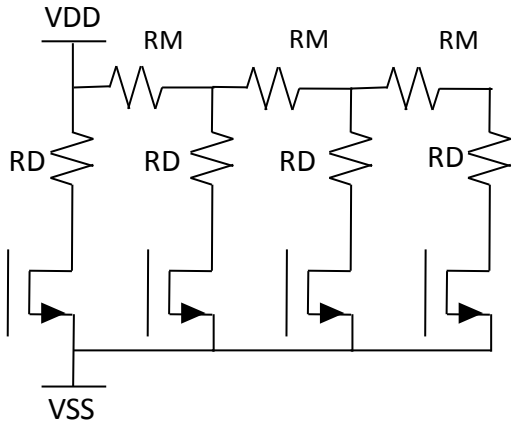




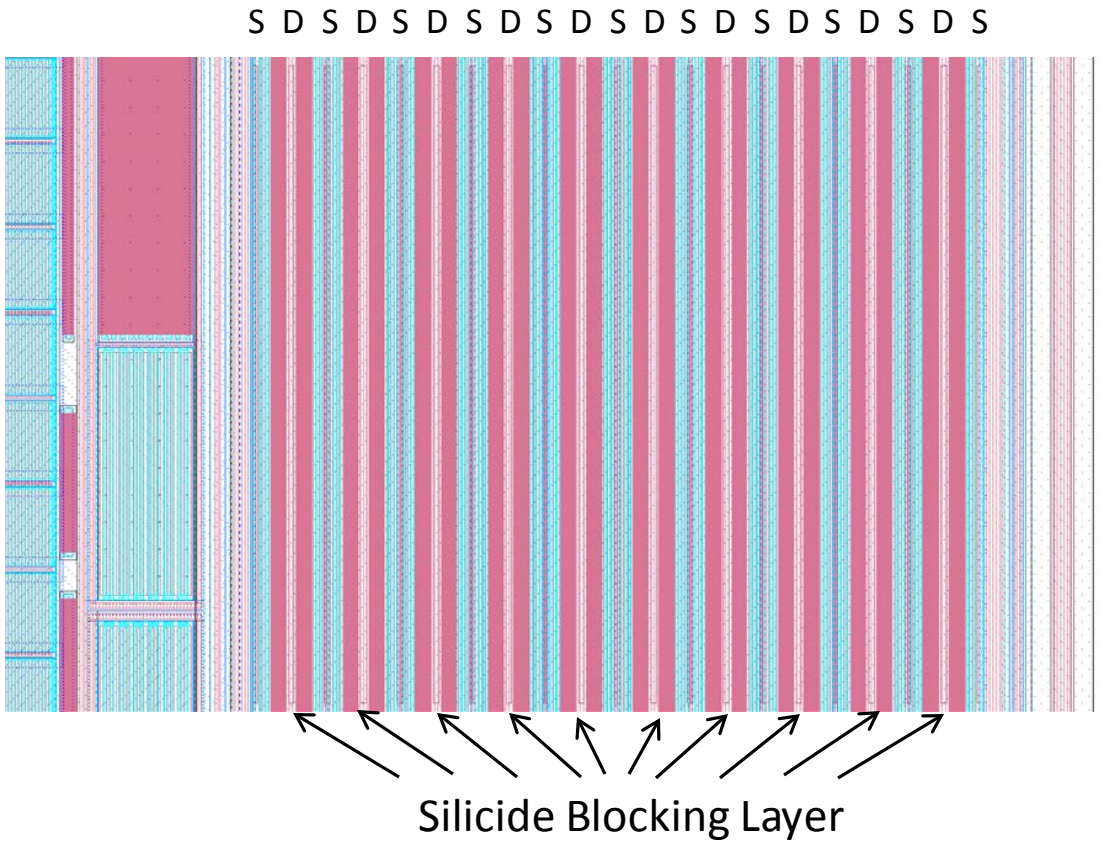
GCNMOS I-V Response



GCNMOS Clamp Drain Ballasting

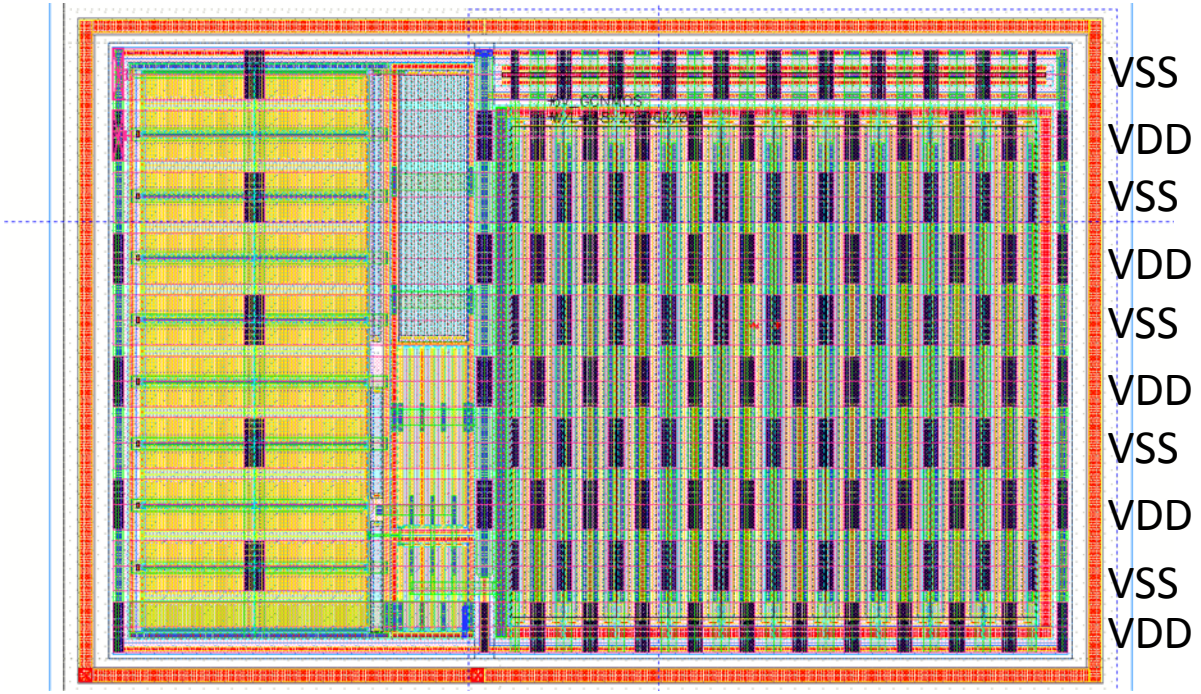


Drain ballasting ensures metal resistance (RM) between device fingers is negligible when compared to the resulting drain resistance (RD).



N-type diffusion also has a positive temperature coefficient of resistance which prevents current from concentrating in a localized region [2].

GCNMOS Metallization



- Continuous Metal1 used for guard bands to reduce risk of latch up during an ESD event.
- No internal connections made above Metal2 to preserve higher level metals for robust supply connections
- Redundant grid of supplies to all locations of the NMOS device to prevent current crowding in metal

Conclusions

- TLP characterization of ESD devices should provide a better metric for determining IC performance in the end item.
- The design impact of IEC considerations results in approximately 4X area increase for ESD devices as opposed to the previous 2kV Human Body Model specification.
- Development of silicon controlled rectifiers could reduce the area requirement for ESD protection under IEC conditions, but may require multiple stages due to high trigger voltages and process variations.

Acknowledgements

- Synaptics Inc.
- Dr. Robert Pearson
- Dr. Dale Ewbank

References

[1] S. H. Voldman, "The state of the art of electrostatic discharge protection: Physics, technology, circuits, design, simulation, and scaling," Ieee Journal of Solid-State Circuits, vol. 34, pp. 1272-1282, Sep 1999.

[2] Jung-Hoong Chun. “ESD Protection Circuits for Advanced CMOS Technologies” Dissertation for the degree of Doctor of Philosophy at Stanford University. June 2006