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Towards integrating chalcogenide based phase change memory with silicon microelectronics

Archana Devasia

TOWARDS INTEGRATING CHALCOGENIDE BASED PHASE CHANGE MEMORY WITH SILICON MICROELECTRONICS

by

ARCHANA DEVASIA

A DISSERTATION

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Towards Integrating Chalcogenide based Phase Change Memory with Silicon Microelectronics

By

Archana Devasia

Submitted by Archana Devasia in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microsystems Engineering and accepted on behalf of the Rochester Institute of Technology by the dissertation committee.

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ABSTRACT

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The continued dominance of floating gate technology as the premier non-volatile memory (NVM) technology is expected to hit a roadblock due to issues associated with its inability to catch up with CMOS scaling. The uncertain future of floating gate memory has led to a host of unorthodox NVM technologies to surface as potential heirs. Among the mix is phase change memory (PCM), which is a non-volatile, resistance variable, memory technology wherein the state of the memory bit is defined by the resistance of the memory material. This research study examines novel, bilayer chalcogenide based materials composed of Ge-chalcogenide (GeTe or Ge_2Se_3) and Sn-chalcogenide (SnTe or SnSe) for phase change memory applications and explores their integration with CMOS technology. By using a layered arrangement, it is possible to induce phase change response in materials, which normally do not exhibit such behavior, and thus form new materials which may have lower threshold voltage and programming current requirements. Also, through the incorporation of a metal containing layer, the phase transition characteristics of the memory layer can be tailored in order to obtain in-situ, a material with optimized phase change properties. Using X-ray diffraction (XRD) and time resolved XRD, it has been demonstrated that stacked phase change memory films exhibit both structural and compositional dependency with annealing temperature. The outcome of the structural transformation of the bottom layer, is an annealing temperature dependent residual stress. By the incorporation of a Sn layer, the phase transition characteristics of Ge-chalcogenide thin films can be tuned. Clear evidence of thermally induced Ge, Sn and chalcogen inter-diffusion, has been discerned via transmission electron microscopy and parallel electron energy loss spectroscopy. The presence of Al_2O_3 as capping layer has been found to mitigate volatilization and metallic Sn phase separation at high temperatures. Two terminal PCM cells employing these bilayers have been designed, fabricated and tested. All devices exhibit threshold switching and memory switching behavior. By the application of suitable voltage programming pulses, RESET state switching can be accomplished in these devices, thus demonstrating single bit memory functionality. A process for integrating bilayer PCM technology with 2 μm CMOS has been designed and developed. The baseline RIT CMOS process has been modified to incorporate 12 levels of photolithography, 3 levels of metal and the addition of PCM as a BEOL process. On electrical testing, NMOS connected PCM devices exhibit switching behavior. The effect of the state (SET/RESET) of the series connected PCM cell on the drain current of the NMOS has also been investigated. It is determined that threshold switching of the PCM cell is essential in order to observe any change in MOS drain current with variation in drain voltage. Thus, successful integration of bilayer PCM with CMOS has been demonstrated.

Abstract Approval: Committee Chair _____

Program Director _____

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To Mama and Papa with much love

I solemnly swear that I am up to no good….

- J. K. Rowling
Harry Potter and the Prisoner of Azkaban

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List of Abbreviations

CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
FeRAM	Ferroelectric RAM
GDM	Growth dominated material
Ge-Ch	Germanium chalcogenide
GST	$Ge_2Sb_2Te_5$
ILD	Inter-level dielectric
MIM	Metal-insulator-metal
MLC	Multilevel cell technology
MOSFET	Metal oxide semiconductor field effect transistor
MRAM	Magnetoresistive RAM
NDM	Nucleation dominated material
NDR	Negative differential resistance
NSLS	National synchrotron light source
NVM	Non-volatile memory
PCB	Phase change bridge
PCM	Phase change memory
PECVD	Plasma enhanced chemical vapor deposition
PEELS	Parallel electron energy loss spectroscopy
PF	Poole-Frenkel
PR	Photoresist
PRAM	Phase change memory RAM
PVD	Physical vapor deposition

RIE	Reactive ion etch
RRAM	Resistive RAM
Sn-Ch	Tin chalcogenide
TEM	Transmission electron microscopy
XRD	X-ray diffraction

Chapter 1: Introduction

The arena of Non-Volatile Memory (NVM) technology is a flourishing industry due to an inundation of portable electronic devices such as smart phones, digital cameras, MP3 players, global positioning systems and electronic readers in the market. NVM has the unique combination of non-volatility, in-system rewritability, ruggedness, high density, affordable cost, low power consumption and small factor which has enabled it to revolutionize information storage technology [1]. Today, EEPROM and floating gate technology, which includes NOR Flash and NAND Flash are the principal silicon NVM products. Fig. 1.1 illustrates the quantity trends of EEPROM, NOR Flash and NAND Flash.

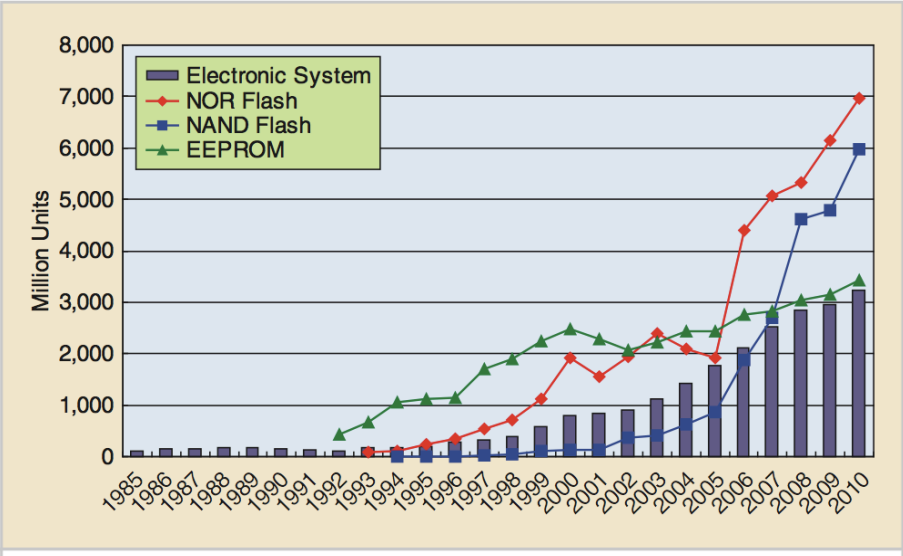

Figure 1.1: Quantity trend of EEPROM, NOR Flash, NAND Flash and electronic system [1]

It is observed that from 1992 to 2009 a total of 105 billion units of Si NVM (EEPROM, 1 NOR, 1 NAND) have been shipped while during the same time, 23 billion units of electronic systems were shipped [1]. From Fig. 1.2 it is ascertained that the NVM penetration rate in electronic systems, has been more than 90% post 2004. This means that almost every electronic system with any intelligence

needs NVM to perform its function, either as a standalone nonvolatile memory or as an embedded memory onto the system core chips [1].

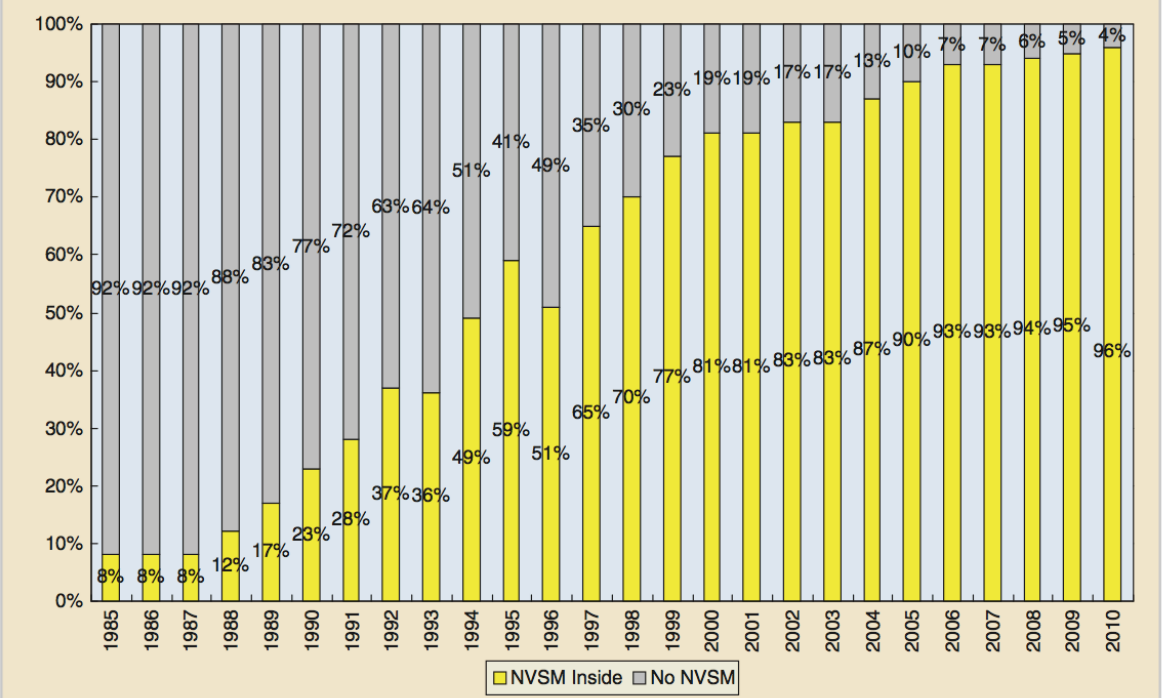

Figure 1.2: NVM penetration rate in electronic systems [1]

Unlike the hard disk drive, optical drive or tape, NVM units do not require mechanical parts such as motor or drive for operations. The read, programming and erase operations for NVM are executed electronically in place as a result of which it requires lower power, less RAM in system, reduced reliability concern and smaller form factor which makes it friendly to a host of applications [1]. As a result NVM has become ubiquitous and the application units enabled by it exceed any other storage solutions by one to three orders of magnitude [1] as illustrated in Fig. 1.3. Figure 1.4(a) shows a qualitative comparison between the different NVM technologies on the basis of flexibility and cost. Here, flexibility refers to the possibility of being programmed and erased many times on the system with minimum granularity (whole chip, page, byte, bit), while cost means process complexity and in particular silicon occupancy, i.e., density or, in simpler words, cell size [2]. From the flexibility-cost

plane it is determined that Flash offers the best compromise between these two parameters, since it has the smallest cell size (one transistor cell) with a very good flexibility (10^6 read/write cycles are possible). As a result Flash has dominated the NVM technology market, originating from a small beginning in 1987 to over $23.8B in revenue in 2007 (Fig. 1.4(b)) [3].

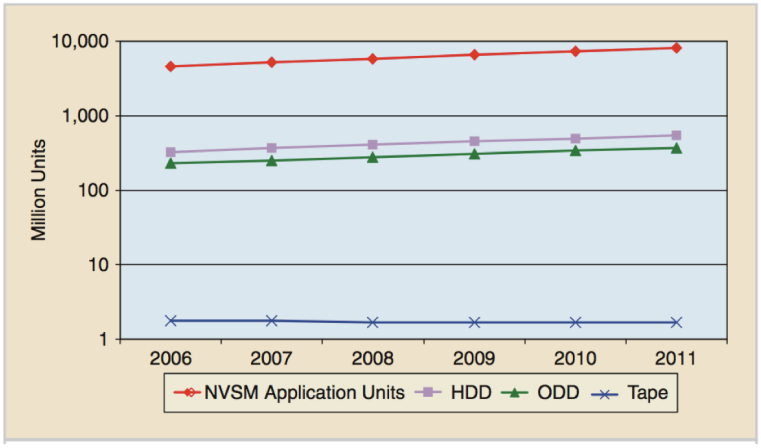

Figure 1.3: Quantity trend of storage application units (Source: Web-Feet Research, iSuppli.)

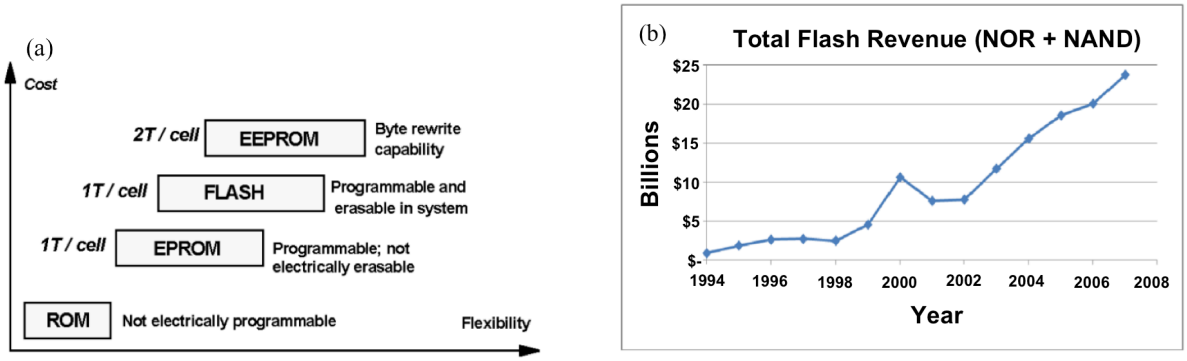

Figure 1.4: (a) Cost-flexibility plane comparison of NVM technologies [2], (b) NOR+NAND Flash revenue [3]

A brief discussion of this current NVM mainstay is carried out in the ensuing section.

1.1 Floating Gate Technology

A cross section of a typical Flash memory device is illustrated in Fig. 1.5. Different types of Flash

cells and architectures have been proposed in [2]. They can be categorized on the basis of access type i.e. serial or parallel, or on the basis of the mechanism utilized for programming and erasure viz. Fowler–Nordheim tunneling (FN), channel hot electron (CHE), hot-holes (HH) and source-side hot electron (SSHE). Among these architectures, the two that can be considered as the industry standard are the NOR Flash and the NAND Flash [1-4]. NOR Flash is optimized for program code and execution. As illustrated in Fig. 1.6, each NOR flash memory cell has two gates, stacked vertically. The cell is connected to the common drain connection called a bitline and can be read from directly, giving the fast read performance that is essential for fast program execution [5].

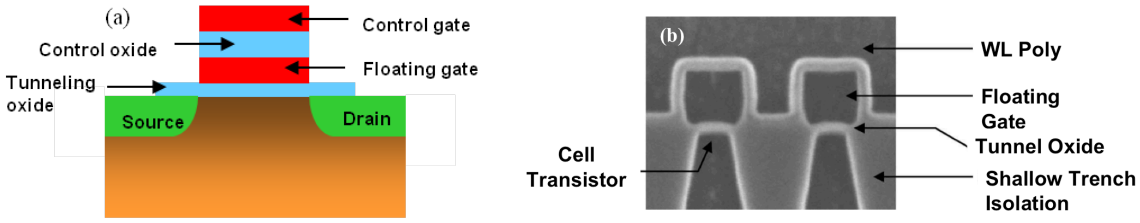

Figure 1.5: (a) Cross section of a typical Flash memory cell, (b) SEM cross section of 65 nm NOR Flash cell [4]

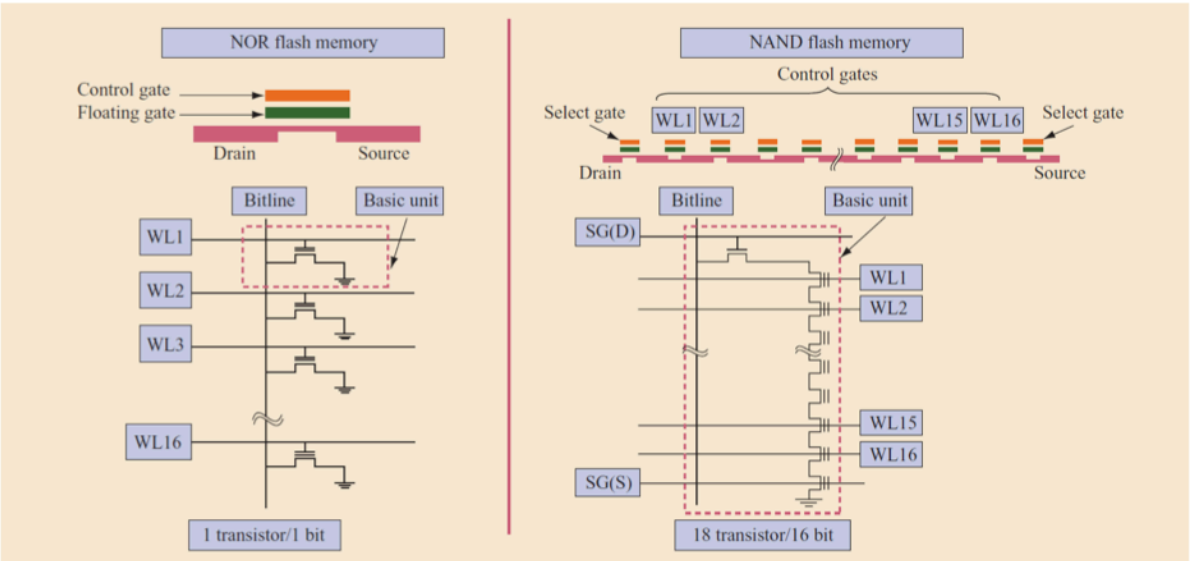

Figure 1.6: Schematic cross-sections and circuit diagrams for NOR and NAND flash memory [5]

With a view to decrease the cost, the NAND flash memory was invented [5]. In this type of memory, the cells are connected in series, with 16 or 32 memory cells connected to the bitline and the source line through two select transistors. This approach results in a smaller cell size and lower die cost compared to NOR memory. However, reduction in size is achieved at the expense of a slower read performance due to the use of serial transistors. The NAND memory business has flourished with the growth in the popularity of digital cameras, where slow read speed is not an issue and for which NAND memory cards provide a convenient low-cost media for picture storage [5].

Flash has enjoyed great success due to its scaling capability, which has allowed a rapid improvement in storage density at decreasing prices. The scaling rate in the last decade has been around a factor of 2 per year with an associated 40% price decrease [3, 6]. This success can be attributed to the improvement in lithography capability and the ability to dominate reliability issues by accurate process optimization and software-level system management [6]. However, the continued dominance of Flash as the premier NVM technology is expected to hit a roadblock due to significant challenges associated with future scaling. Three main areas of concern may be identified as (1) physical scaling, (2) electrical scaling, and (3) reliability scaling [5].

1.1.1 Physical Cell-Scaling Challenges

For NAND memory, techniques such as self-aligned double patterning [7] can be used which enable the reduction in the physical size of the cell to dimensions close to 20 nm. At the 65 nm technology node, the layout of the NOR memory cell has 45˚ angle structures around source contacts that are not conducive to optical enhancement techniques [8]. To improve NOR scaling, a self-aligned contact technology has been developed at the 45 nm lithographic node [8], which not only enables the reduction in contact area but also comprises of a new layout similar to that of NAND, making it easier to implement optical enhancement techniques. However, the true limiters of cell size reduction involve electrical and reliability requirements which will be discussed in the following section [5].

1.1.2 Electrical Cell-Scaling Challenges

The major scaling limitation for NOR Flash is the requirement of a high programming voltage. A voltage higher than 4 V from drain to source is required to achieve hot carrier channel programming in order to produce electrons of sufficient energy to overcome the 3.2 eV Si to SiO_2 barrier height [9]. Hence, the minimum gate length is limited to the channel length that can withstand the required programming voltage. On the other hand, in NAND Flash, the transistor channel is used for read only, thus requiring a lower drain to source voltage and hence shorter channel length limit.

A high coupling ratio between the control gate and the poly gate is essential in order to provide adequate control of the channel used for reads. This becomes difficult as the cell scales in size and self aligned techniques are used for the floating gate. Maintaining control of the channel requires a thinner inter-poly dielectric between the control and floating gates, which has to be optimized for no leakage current under low-field storage.

Another scaling limitation is the capacitance associated with the coupling of two adjacent cells. As the spacing between the floating gates decreases, the coupling between them increases. Thus data stored in one cell can influence the operation of an adjacent cell [5].

1.1.3 Reliability Scaling Challenges

Due to the analog nature of charge storage in floating gate, the amount of stored charge can be subdivided into small increments, thus enabling multilevel cell (MLC) technology i.e. storage of more than one bit per cell in both NOR and NAND Flash memories. MLC technology is highly sensitive to cell degradation mechanisms due to the limited separation between charge states as compared to single level cell technology. As the memory cell is scaled, the cell capacitance is decreased, resulting in the decrease of charge stored [9, 10]. For NOR Flash [9], which has a larger memory cell layout as compared to NAND, the number of stored electrons at the 45 nm node is about 1000, while that for NAND is less than 500 [10]. For a two bit per cell MLC technology, the number of electrons per level is slightly more than 100. While the number of stored electrons decreases with each technology node,

the defect charge leakage mechanisms causing charge loss remain the same [5]. Hence the impact of each defect on the threshold voltage of the cell is proportionally larger at each new node, manifesting as faster voltage drops and an increase in error rates [5].

In order to facilitate further scaling of Flash, several innovative methods can be applied. However, in most cases they will involve significant increase in complexity or use of expensive new manufacturing tools thus causing future scaling to depend more on economics than on purely technical issues [5]. As a result, a host of unorthodox non-volatile memory (NVM) technologies are being explored to overcome the ultimate limitations of MOS-based memory devices. These will be very briefly reviewed in the following section.

1.2 Non-Conventional Memory Technologies

Among the mix of emerging memory technologies is Ferroelectric RAM (FeRAM), Magnetoresistive RAM (MRAM), and Resistive RAM (RRAM) technologies such as Phase Change Memory (PCM), and Nanoionic Memory which comprises of Valence Change or Mixed Valence Memory and Electrochemical Metallization Memory (i.e. Program Metal Cell) [11-17].

FeRAM utilizes the permanent polarization of a ferroelectric material such as PZT (Lead-Zirconate-Titanate), SBT (Strontium-Bismuth-Tantalate) or BLT (La substituted-Bismuth-Tantalate) as the storing mechanism. It has a DRAM like cell structure for a 1-transistor, 1-capacitor cell [11, 12].

The MRAM technology is mostly magnetic tunnel junction based and constitutes a pinned magnetic layer (e.g. CoFe or NiFe/CoFe) and a free magnetic layer (e.g. CoFe or NiFe/CoFe) separated by an insulating barrier [11, 13]. Information is stored in the magnetization direction of the free layer. By employing a magnetic field, the orientation of the free magnetic layer can be flipped in order to make the two layers parallel or anti-parallel with each other. These two conditions correspond to high or low barrier conductance respectively, and thus define the state of the memory bit.

In the case of RRAM, the memory cell is a metal-insulator-metal (MIM) structure. Resistance switching in the Valence Change or Mixed Valence Memory is accomplished by changing the conductivity of the insulator layer by employing redox electrochemistry, as discussed in [16]. Consider an MIM structure comprising of an insulating TiO_2 layer sandwiched between two Pt electrodes. When a voltage is applied to the structure, a forming process occurs wherein the insulating layer separates into two components defined by the generation of O^{2-} anions and oxygen vacancies denoted by Vo^{++}. The O^{2-} anions flow toward the positively biased electrode and oxidize the TiO_2 insulating layer to form Ti_2O_5. This causes an increase in its bulk resistivity and Schottky barrier height with respect to the Pt electrode, thus enhancing the structure's resistance. Similarly, Vo^{++} oxygen vacancies flow toward the negatively biased electrode on the right, thereby reducing the TiO_2 insulating layer to form TiO_{2-X}, which reduces its resistivity. The boundary between the insulating TiO_2 layer and the conducting TiO_{2-X} layer moves towards the former, until it approaches the positively biased contact, thus reducing the resistance of the cell. Application of a voltage of the opposite polarity removes the tunneling gap between the negatively biased right Pt electrode and the insulating TiO_2 / Ti_2O_5 layer [16].

The ionic conduction of chalcogenide glasses forms the basis of Electrochemical Metallization Memory. As described in [17], the high resistance OFF state consists of a small volume of metal-doped chalcogenide sandwiched between two electrodes, one of them being a soluble metallic anode. The transition toward the low resistance ON state is induced by a voltage pulse. A negative potential applied to the inert cathode leads to the electro-migration of dissolved positives ions and hereafter electro-deposition of a metallic dendrite on the cathode, thus resulting in the growth of a metallic conductive pathway between the two electrodes. The erasing process involves the dissolution of the metallic pathway under the application of a reversed polarity voltage pulse [17].

PCM on the other hand, is a variable resistance memory technology wherein the resistance of the memory material determines the state of the memory bit [18]. A comparison between these memory technologies, based on the 2009 ITRS roadmap, is summarized in Table 1.1.

Table 1.1: Comparison between Flash and Emerging NVM Technologies [15, 16]

		Floating Gate		**FeRAM**	**MRAM**	**PCM**	**Ionic**	
		NOR	**NAND**					
Storage Mechanism		Charge on floating gate		Remnant polarization of a ferroelectric capacitor	Magnet-ization of ferro-magnetic layer	Reversibly changing amorphous and crystalline phases	Ion transport and redox reaction	
Cell Elements		1T		1T1C	1(2)T1R	1T1R	1T1R or 1D1R	
Feature size F (nm)	2009	90	90	180	130	65	min. required	<65
	2024	18	18	65	16	8	best projected	5-10
							demonstrated	90
Cell Area	2009	10 F^2	5 F^2	22 F^2	45 F^2	16 F^2	min. required	10 F^2
	2024	10 F^2	5 F^2	12 F^2	10 F^2	6 F^2	best projected	8/5 F^2
							demonstrated	8 F^2
Read Time (ns)	2009	10	50	45	20	60	min. required	<15
	2024	1.5	8	<20	<0.5	<60	best projected	<10
							demonstrated	<50
W/E Time	2009	1 µs/ 10 ms	1 ms/ 0.1 ms	10 ns	20 ns	50 ns/ 120 ns	min. required	Application dependent
	2024	1 µs/ 10 ms	1 ms/ 0.1 ms	1 ns	<0.5 ns	<50 ns	best projected	<20 ns
							demonstrated	5 ns/5 ns
Retention Time (y)	2009	>10	>10	>10	>10	>10	min. required	>10
	2024	>10	>10	>10	>10	>10	best projected	>10
							demonstrated	>10
Write Cycles	2009	1E5	1E5	1E14	58E12*	1E9	min. required	1E5
	2024	1E5	1E5	>1E16	>1E16	1E15	best projected	1E16
							demonstrated	1E9
Write operating voltage	2009	12 V	15 V	0.9 - 3.3 V	1.5 V	3 V	min. required	Application dependent
	2024	12 V	15 V	0.7 - 1 V	<1.5 V	<3 V	best projected	<0.5 V
							demonstrated	0.6/-0.2 V
Read operating voltage	2009	2 V	2 V	0.9 - 3.3 V	1.5 V	3 V	min. required	2.5 V
	2024	1 V	1 V	0.7 - 1 V	<1.8	< 3 V	best projected	<0.2 V
							demonstrated	0.15 V
Write energy (J/bit)	2009	>1E-14	>1E-14	3E-14	1.5E-10	6E-12	min. required	Application dependent
	2024	>1E-15	>1E-15	7E15	1.5E-13	<2E-13	best projected	1E-15
							demonstrated	5E-14
Multiple-bit potential		Yes	Yes	No	No	Yes	Yes	

*Measured value reported by Evespin Technologies, Inc. (Source: http://www.hotchips.org/uploads/archive22/HC22.22.130-Tehrani-MRAM.pdf)

1.3 Phase Change Memory

Among the emerging NVM technologies, PCM is the only one demonstrating the capability to enter the broad NVM market. With the April 2010 announcement of Numonyx's 128 Mb Omneo™ line of 90 nm [19] PCM RAM (PRAM) and Samsung's multi-chip package containing 512 Mb PRAM [20], there exists a very real possibility of PCM technology becoming the next NVM mainstay.

From the application point of view, PCM can be exploited by all the memory systems, especially the ones resulting from the convergence of consumer, computer and communication electronics [21]. In particular PCM can be used in [22]:

(a) Wireless systems for the storage of directly executed code, semi-static data structures, and files. PCM is bit alterable i.e. like DRAM it has direct-write capability. This significantly reduces DRAM requirements, lowering the cost of the memory subsystem.

(b) Embedded applications, in particular as Flash replacement. However, in smaller embedded applications the use of PCM allows eliminating the need for DRAM, where its requirements may be so small as to fit within the microcontroller cache itself.

(c) Solid state storage subsystem to store frequently accessed pages and to store those elements, which are more easily managed when manipulated in place. Moreover, in this application, a small amount of PCM could be used to enhance the manageability of NAND. This caching with PCM will improve the performance and reliability of the subsystem. Another advantage is the bit alterable nature of PCM that solves the issue of increased write cycles when the device is full. Higher endurance on PCM addresses the needs of these systems when heavy use is expected.

(d) In computing platforms, exploiting the non-volatility to reduce the power. While idle DRAM banks consume significant refresh power, inactive PCM banks can simply be turned off. This results in significant power reduction for large memory arrays in enterprise computing applications and battery life improvement in relatively inactive arrays in mobile computing applications.

Thus, PCM provides a new set of features interesting for applications combining components of NVM and DRAM and is at the same time a sustaining and disruptive technology [22]. As a result it forms the topic of discussion of this research.

1.4 Scope and Novelty of this Study

Integrated Circuit (IC) technology has witnessed an explosive growth during the past four decades not only in scaling but also in the incorporation of innovative materials in both logic and memory technologies. The modern day complementary metal oxide semiconductor (CMOS) technology is an ensemble of a variety of materials such as, high permittivity dielectrics, metal gates, polymer dielectrics, copper interconnects, along with silicon as the primary substrate. As discussed previously, novel materials are also finding their way into the dominion of memory technology. Magnetic materials such as CoFe, ferroelectric materials such as PZT, phase change materials such as chalcogenides, are all emerging from the shadows to claim a place of their own. The integration of such disparate technologies may lead to innovative solutions that yield a unique technology, which may result in substantial improvements in circuit functionality. This is the underlying philosophy of the work presented here. This research is aimed towards integrating PCM technology with CMOS technology with a view to develop a robust phase change semiconductor memory system.

Metal oxide semiconductor field effect transistor (MOSFET) is the conventional microelectronic device and it mainly utilizes the charge properties of electrons to manipulate information. In CMOS technology, the modulation of current flow is controlled by applying a voltage bias to the gate electrode to either allow or inhibit charges to flow in the channel region. This research will utilize CMOS as a test bed for integration with PCM devices.

The PCM device employs the phenomena of phase transition in order to create a variable resistance memory technology. Electrically initiated, reversible and rapid amorphous to crystalline phase change process can be achieved in multi-component chalcogenide alloy materials. The two different phases are stable, thus providing the technology its non-volatile flavor. In this particular

study, bilayers of metal and germanium chalcogenide PCM structures will be designed, fabricated and characterized.

This research seeks to utilize basic physical phenomena viz. flow of charge and change of phase to build PCM cells. Together with CMOS, they become components necessary to construct a sub-system level circuitry, a single memory cell. An addressable array of these cells will form a memory system. The integration will be conducted using a silicon platform. The novelty of this research lies in the fact that it consists of heterogeneous technologies integrated on a silicon platform which are very fast, very small, and easy to fabricate. The goal of this research is to realize a fully compatible PCM–CMOS technology. The proposed technologies utilize different state variables - electric charge and change of phase – to create a novel form of information processing. By the convergence of these functionalities, these technologies are expected to outperform the current state-of-the-art memory architectures in terms of cell size, signal-to-noise ratio, ease of fabrication and cost. This research will provide a major step towards the development of such memory technology.

1.5 Organization of Thesis

The rest of this dissertation is organized as follows.

Chapter 2 provides an overview of phase change memory. It discusses the basic device operation, the physical principles behind phase transition and the switching mechanism. It also presents a brief description of the materials used in phase-change applications and concludes by an examination of the characteristics of PCM vis-à-vis the features of the next generation non-volatile memory technology.

Chapter 3 is divided into two sections. The first half is devoted to the rationale behind the investigation of bilayer chalcogenides as potential PCM memory materials, and the second part lists out the goals of the presented research.

Chapter 4 describes the application of techniques such as X-ray diffraction, transmission electron microscopy and parallel electron energy loss spectroscopy to examine phase transition, residual stress and material inter-diffusion in the bilayers.

Chapter 5 details the design, fabrication and electrical testing of two terminal phase change memory devices. Depending upon the materials forming the bilayer, three major device types are fabricated and tested.

Chapter 6 deals with the integration of bilayer PCM cells with a 2 μm CMOS process. Details of circuit design, SPICE simulation, fabrication and electrical testing results of integrated devices and circuits are presented. A brief discussion on MOSFET parameter extraction pertaining to the PMOS and NMOS devices fabricated using the 2 μm CMOS process is provided in Appendix A. The netlist employed for SPICE simulations is reproduced in Appendix B.

Chapter 7 concludes this dissertation by listing out the contributions made by research study to the field of bilayer, chalcogenide based phase change memory. It also makes recommendations for future extensions to this work.

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Chapter 2: Background of Phase Change Memory

This chapter provides an overview of phase change memory. It discusses the basic device operation, the physical principles behind phase transition and the switching mechanism, particularly the threshold switching phenomenon, which is fundamental to the operation of a PCM cell. It also presents a brief description of the materials used in phase-change applications. The chapter concludes with an examination of the characteristics of PCM vis-à-vis the features of the next generation non-volatile memory technology.

2.1 Introduction

The essence of the PCM technology is the memory material, which is composed of elements belonging to group VI A of the periodic table viz. sulfur, selenium and tellurium [1]. These elements, referred to as chalcogens, form compounds called chalcogenides. PCM devices, based on reversible memory switching in chalcogenides, are the result of the seminal work carried out by J. F. Dewald and S. R. Ovshinky in the 1960s [2-4]. Chalcogenides are very attractive as memory materials since they can form a wide range of glasses and have a correspondingly wide variety of glass transition temperatures [1]. These materials exhibit a change in resistance during phase transition - a feature that can be exploited to create fast, highly scalable, reliable, radiation resistant memory cells having high endurance and retention capability [5-7].

2.2 PCM Device Operation

The most widely studied PCM material is an alloy of Germanium-Antimony-Tellurium (GST) with $Ge_2Sb_2Te_5$ being one of the most popular stoichiometries [5, 8-13]. A typical cell employing GST as the PCM material is illustrated in Fig. 2.1(a). This particular design constitutes a lance like structure due to the shape of the heater element and the vertical flow of current. The programmable volume

represents the phase transition region. It is sandwiched between a top electrode and a resistive heater through which the programming current flows.

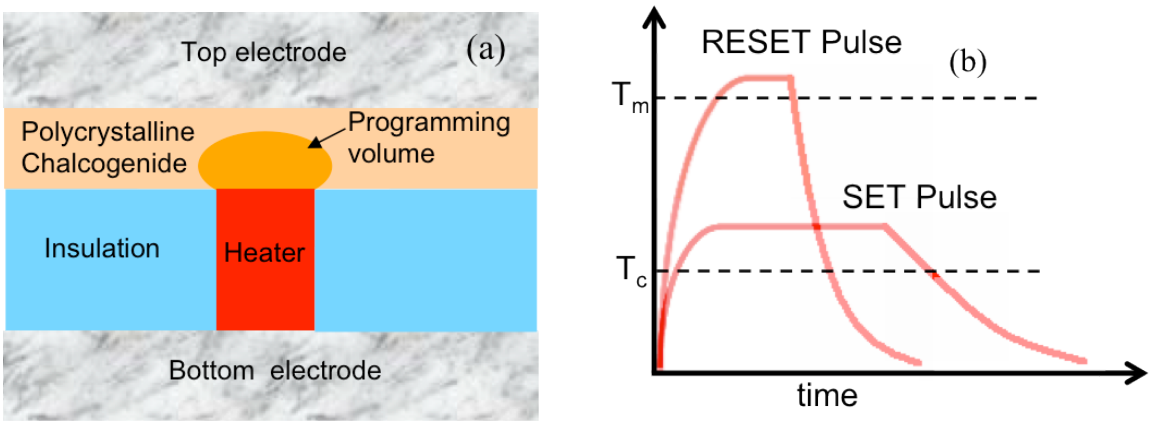

Figure 2.1: (a) Typical phase change memory cell employing GST [8], (b) Schematic temperature–time relationship during programming in a PCM cell

The current concentration at the heater-GST interface results in local heating of the GST in a semi-hemispherical volume where the amorphous/crystalline phase change occurs [3]. The thermally induced phase change is realized via application of current pulses of varying amplitude and time intervals as shown in Fig. 2.1 (b). When a current pulse lasting less than 100 ns [3, 8] is driven into the device, the GST temperature close to the heater rises above the melting point (T_m =620 ˚C [8]) and then the device gets swiftly quenched by the nanosecond trailing edge of the current pulse. The molten material has no time to rearrange its bonds and it is left in the amorphous phase. For recovery of the crystalline state, the cell is driven by a similar current pulse but with lower amplitude. The pulse heats the GST close to the heater to a temperature of about 550 ˚C [8]. This temperature is less than the melting temperature but high enough to speed up the spontaneous amorphous-to-crystalline transition: the crystalline phase builds up in about 100 ns by nucleation and growth processes [3].

The typical *I-V* curve of a PCM cell is illustrated in Fig. 2.2. For crystalline GST, the characteristics appear practically ohmic. By increasing the bias, the local temperature rises because of

Joule heating and the crystalline GST eventually melts. If the current is now swiftly quenched, the GST is left in the amorphous state.

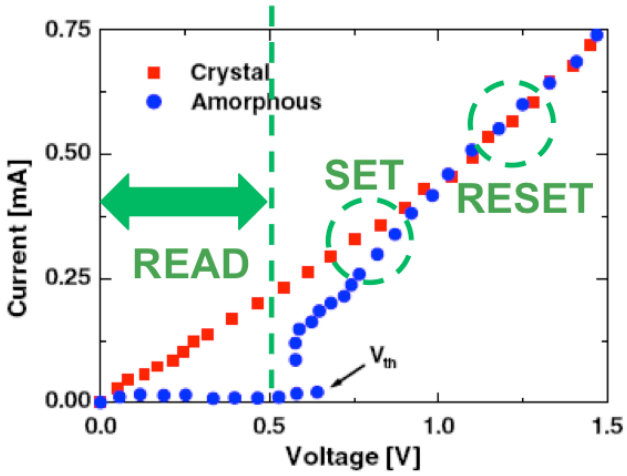

Figure 2.2: *I-V* characteristics of a PCM cell [8]

The amorphous state *I-V* curve shows two different regimes. At low bias, the resistance is fairly high. However as the voltage reaches a threshold value V_t, the amorphous material switches from a highly resistive to a highly conductive state. The current rapidly rises with this voltage snap-back. Even after switching, the material is still amorphous. Phase transition to the crystalline state occurs only by further increasing the current. In this region, Joule heating is high enough to cause the temperature to exceed the glass transition temperature (T_g) but not T_m. Now if the current is reduced at a slow enough rate to allow the material to cool, it crystallizes into a low resistance state. (It should be noted that the use of the term threshold voltage in this context is different from that used to turn on a MOSFET).

The overlap of the curves for crystalline and amorphous states is indicative of the fact that the current in that region has become independent of the initial memory state. This gives the direct write characteristic of the memory. Thus the cell can be re-written without any intermediate erase step and hence can be referred to as bit-alterable. Such a direct write capability simplifies writing to the memory and improves the write performance of the memory.

The electrical resistivity, ρ of the two phases differs by orders of magnitude. The resistance of the two memory states ranges from a few kΩ in the low resistance ON state, referred to as SET state to some MΩ in the high resistance OFF state also know as RESET state [3].

In order to read the memory bit, a very low voltage, which essentially causes no joule heating, is used. In the SET state, a few mV of voltage applied across the cell generates 50-100 μA of current [8]. This evaluates to logic 1. However if the same bias is applied across the cell in RESET state then the resulting current generation in not enough to trigger the amplifier used to sense the current flowing through the cell. Hence this evaluates to logic 0. The read operation is possible in 50 ns [8].

2.3 Physical Principles Underlying PCM

As discussed in the preceding section, PCM device operation comprises of two major processes: amorphous-crystalline phase transition and threshold switching. The underlying physics is summarized in the sections below.

2.3.1 Amorphous-Crystalline Phase Transition

Consider a crystalline chalcogenide material. When it is heated, the material will start to melt at the solidus temperature T_{sol} illustrated in Fig. 2.3 and become completely molten at T_m. As the material cools from the liquid state, it may transform back into the lower energy crystalline state and undergo a sharp change in volume. On the other hand, if the characteristic time constants of the crystallization process are slow compared to the cooling rate, the material may bypass crystallization and become a supercooled liquid. On further cooling the material enters into a glassy state at the glass transition temperature T_g. For temperatures below T_g, the ability of the system to rearrange itself becomes long, compared to experimentally accessible times and the material thus freezes into an amorphous solid [14]. Unlike, the crystalline state, the amorphous solid undergoes no sharp changes in volume and is in a metastable state whose volume and free energy depend on the cooling rate; the value of T_g thus

also changes with the cooling rate as illustrated in Fig. 2.3. Conversely, when the amorphous material is heated to a temperature between T_g and T_m, it will start to crystallize. This is because; the speed of the crystallization process is determined by a combination of the mobility of the atoms and the free energy difference between the starting and ending phases [14]. At T_m, the liquid and crystalline states are in equilibrium and hence the free energy difference is zero. This implies that the maximum crystallization rate will occur at an intermediate temperature between T_g and T_m.

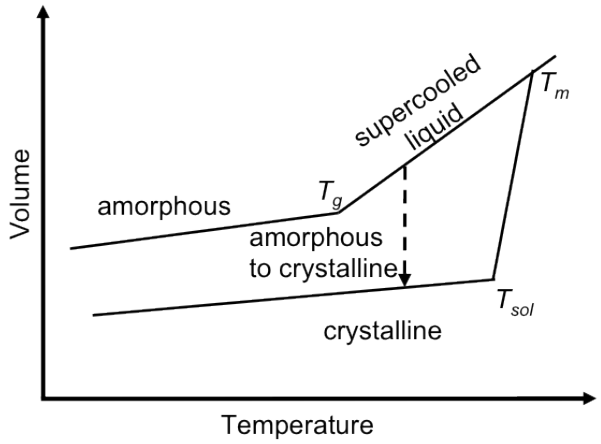

Figure 2.3: Schematic of volume-temperature variation of a PCM material showing different possible phase transitions [14]

2.3.2 Band Structure for Chalcogenide Semiconductors

The band diagrams for a chalcogenide semiconductor are illustrated in Fig. 2.4(a) and (b) [15]. It is observed that the amorphous phase (Fig. 2.4(a)) has a relatively large energy gap and is characterized by a large concentration of localized states in the gap, which contribute significantly to the density of states. On the other hand, a conventional semiconductor picture applies to the crystalline phase (Fig. 2.4(b)), resulting in well-defined conduction and valence bands and a forbidden gap [15]. The energy gap in an amorphous semiconductor is generally referred to as a *mobility gap*, namely an energy range with insufficient mobility of states, rather than a forbidden range with no states, as in standard

crystalline semiconductors [16]. This is because deep states tend to be highly localized, while mobility increases for energies approaching the conduction or valence bands. The large concentration of localized states causes the Fermi level to be pinned at about midgap in the amorphous chalcogenide. This results in a relatively large activation energy and high effective resistivity [17].

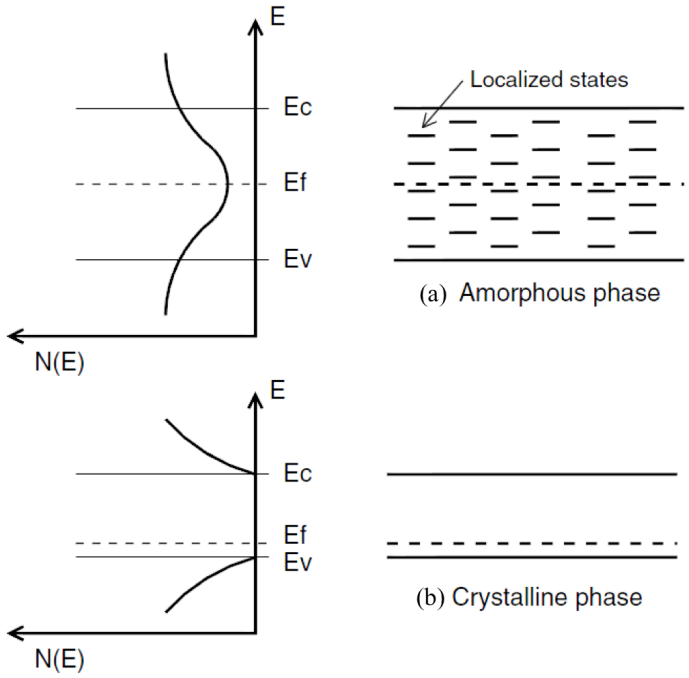

Figure 2.4: Schematic band diagrams and density of states as a function of energy of chalcogenide material for (a) amorphous phase, (b) crystalline phase [15]

Crystalline chalcogenides such as $Ge_2Sb_2Te_5$, GeTe, generally display small activation energy for conduction, which is compatible with a selfdoping behavior, probably due to point defects (e.g., vacancies) in some Te compounds [16].

2.3.3 Conduction in the Crystalline Phase

In the crystalline phase, $Ge_2Sb_2Te_5$ appears as a relatively low band gap, doped semiconductor, consistent with the band diagram illustrated in Fig. 2.4(b). Hence the drift-diffusion equation can be

used to describe electrical conduction in the crystalline phase, by applying the standard semiconductor theory [16]. This accounts for the behavior exhibited by the *I-V* curve in the crystalline phase as shown in Fig. 2.2.

In order to completely describe electrical conduction in phase change memory, it is essential to consider conduction in states, which display resistance values between the SET and RESET states. These intermediate states comprise of a mixed amorphous crystalline phase. Electrical conduction in this mixed-phase volume can be explained by percolation of carriers through dispersed low-resistivity crystalline grains [16]. Figure 2.5 shows two different mixed-phase states. State A is characterized by an incomplete percolation path, while state B is distinguished by a complete percolation path through low-resistivity crystalline grains. In state A, a small amorphous barrier limits the electrical current, and this accounts for the relatively large values of resistance and activation energy. For the case of state B, no amorphous barrier exists. Hence the activation energy for this state is the same as that of the bulk crystalline phase (SET state). However, the resistance still remains higher than the SET state due to geometrical effects, namely a small cross section and a relatively large percolation length through the mixed phase [16].

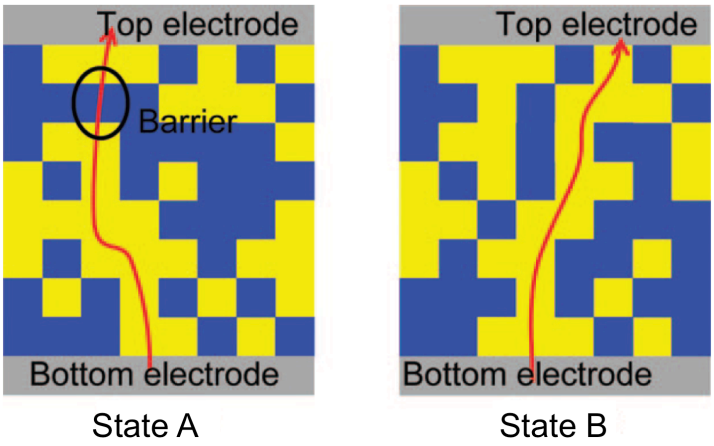

Figure 2.5: Schematic of two different mixed-phase configurations, characterized by an incomplete (State A) or complete (State B) percolation path through low-resistivity grains [16]

2.3.4 Conduction in the Amorphous Phase

Figure 2.6 shows *I-V* characteristics as a function of temperature, for a PCM cell with TiN bottom contact and GST phase-change layer [17].

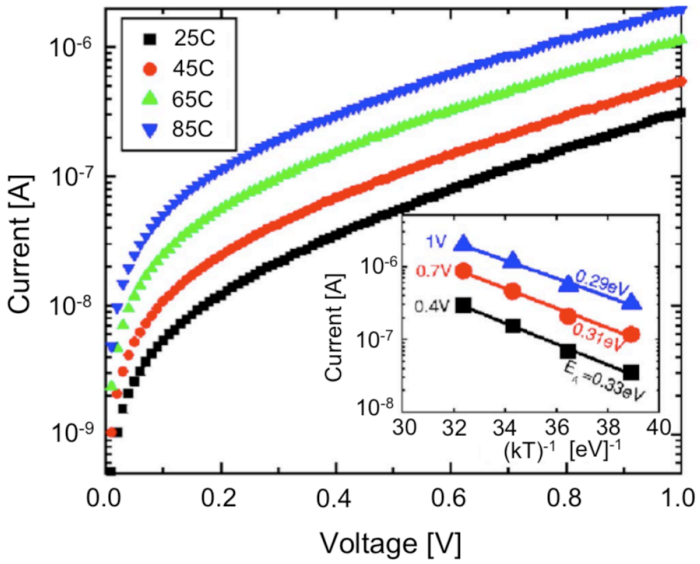

Figure 2.6: Measured *I-V* characteristics for amorphous GST at temperature T = 25, 45, 65 and 85˚C [17]

During the *I-V* measurement, the voltage sweep is always stopped below the threshold voltage V_t to avoid threshold switching and consequent phase transformation due to Joule heating. It is observed that the *I-V* curves are linear for small applied voltages (< 0.3 V), and exhibit an exponential behavior at higher voltages. For the device in Fig 2.6, the threshold voltage is observed to be around 1.6 V (not illustrated) [17], and hence the region of the *I-V* curve shown in the figure is referred to as the sub-threshold region. It is ascertained that for increasing temperature, the current strongly increases due to the relatively large activation energy E_A of conduction in chalcogenide glasses [17]. However, the current appears to be differently activated for different applied voltages. In order to characterize the activation energy in these samples, the current values at different voltages are plotted as a function of $1/kT$. This is illustrated in the inset in Fig. 2.6. The activation energy is estimated by a least-mean-square linear fit in the Arrhenius plot, and values E_A = 0.33, 0.31, and 0.29 eV are obtained for

V = 0.4, 0.7, and 1 V, respectively. This behavior is commonly observed for trap-limited conduction such as the Poole-Frenkel (PF) mechanisms, where the applied electric field lowers the potential barriers, hence the activation energy for conduction [16-18]. As schematically shown in Fig. 2.7(a) and (b), Poole-Frenkel conduction is due to carriers (electrons in the figure) being thermally emitted from one trap to the conduction band and then captured by another trap [17]. In this figure, the energy barrier between two localized states, equal to $\Delta\phi(0)$ for zero applied voltage (Fig. 2.7(a)), is lowered to a value $\Delta\phi(V)$ by the application of a voltage V (Fig. 2.7(b)).

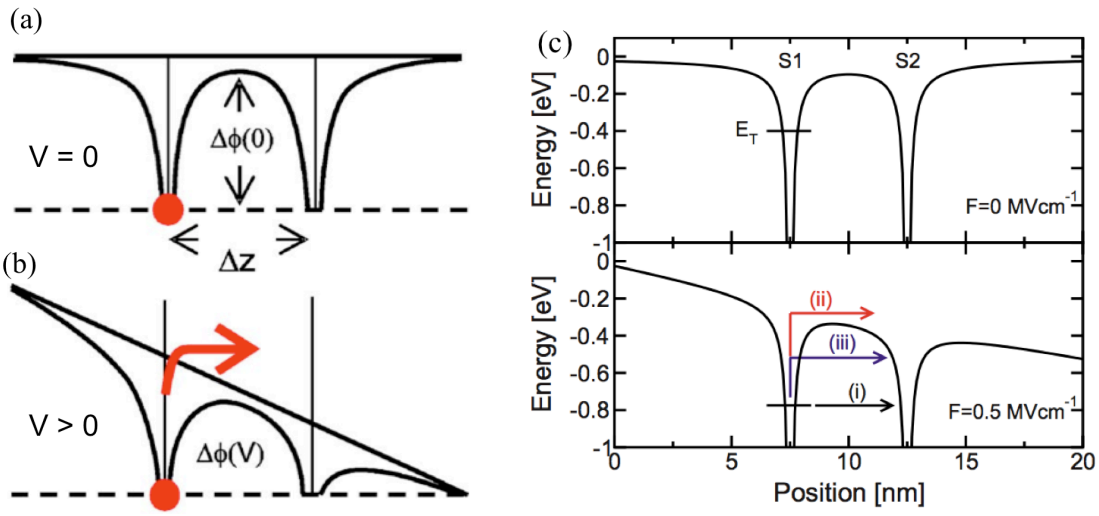

Figure 2.7: Schematic for sub-threshold conduction via localized states. (a) Electrons trapped at donor-type traps confined by potential *Δϕ(0)* at zero bias, (b) drop in potential barrier to *Δϕ(V)* with application of voltage, $V > 0$ [17]. (c) Profile of electron potential energy along minimum path between localized sates S1 and S2, with electric field F = 0 (top) and F = 0.5 MV cm^{-1} (bottom) [19]

It has been noted that not only pure thermal emission above the conduction band edge but also thermally activated tunneling below the conduction band contribute significantly to conduction [16, 19]. As shown in Fig. 2.7(c), the tunneling mechanism denoted by (i) occurs by transmission through the potential barrier from S1 to S2 [19]. The PF transport, discussed previously is illustrated

by (ii). Also shown is a third mechanism (iii), obtained by a combination of thermal emission and tunneling, namely thermally assisted tunneling. This consists of a thermal excitation within S1 to an energy level E below E_C, followed by tunneling through the potential barrier seen at E [19]. While the probability of reaching E is exponentially decreasing with E, the probability of tunneling through the barrier may be significantly higher than the tunneling probability for a 'cold' electron at the trap level E_T indicated in Fig. 2.7(c) [19]. The combined transport due to thermally activated PF and tunneling accounts for the strong temperature dependence of the current in Fig. 2.6 [16]. For PF conduction, the voltage dependence of the current can be expressed as [18],

$$I = I_{\mathrm{PF}} e^{\beta_{\mathrm{PF}} V^{1/2}} \tag{2.1}$$

where I_{PF} and β_{PF} are constants. However (2.1) applies to emission from an isolated trap to the conduction band and assumes that the nearest neighbor traps are still far enough from the trapped electron so that their contribution to the potential profile can be neglected [18]. This situation is therefore completely different from the physical picture in Fig. 2.7(a), (b) and (c), where traps are closely interacting as a result of a large density of traps in the glassy material. In order to analyze the impact of a different distances between traps on the shape of the $I-V$ curve, Ielmini and Zhang [18] calculated the potential profile between two traps with variable intertrap distance Δz. They determined that the change of the barrier height (barrier lowering) for a trapped electron depends linearly on the applied electric field F for small Δz while a transition to a square root dependence on the field is found for increasing Δz as the traps become more and more independent. Since the electron thermal emission current is exponentially dependent on the barrier lowering, it is concluded that, for sufficiently high trap density and a correspondingly short intertrap distance the current will obey [18],

$$I = I'_{PF} e^{\beta'_{PF} V} \tag{2.2}$$

where I'_{PF} and β'_{PF} are constants. The linear dependence of barrier lowering on the applied voltage can be viewed as the result of the position of the potential maximum between the two traps being nearly

constant and experiencing a negligible shift upon a voltage increase [18]. As a result, the barrier change can be approximated as [18],

$$\Delta U \approx -qF\frac{\Delta z}{2} = -qV\frac{\Delta z}{2u_a} \tag{2.3}$$

where q is the elementary charge and u_a is the amorphous chalcogenide thickness. Thus, the energy barrier $\Delta\phi(V)$ can be expressed as [16],

$$\Delta\phi(V) = \Delta\phi(0) + \Delta U = E_C' - E_{F0} - qV\frac{\Delta z}{2u_a} \tag{2.4}$$

where E_C' is the conduction band mobility edge and E_{F0} is the equilibrium Fermi level. The mobility edge is used instead of the proper band edge in order to take into account the tunneling contribution [19].

The average electron velocity can be expressed as the intertrap spacing divided by the average transfer time between two traps under the enhancement of the applied electric field. The transfer time in the same direction of the electrostatic force (i.e. forward time) is estimated as [18],

$$\tau_{\rightarrow} = \tau_0 \exp\left(\frac{\Delta\phi(V)}{kT}\right) = \tau_0 \exp\left(\frac{E_C' - E_{F0} - qV(\Delta z/2u_a)}{kT}\right) \tag{2.5}$$

where τ_0 is the characteristic attempt-to-escape time for the trapped electron (typically in the range of 10^{-13} - 10^{-14} s). The corresponding forward current $dI_{\rightarrow}$ can be obtained as [16],

$$dI_{\rightarrow} = qAn_T(E)\frac{\Delta z}{\tau_{\rightarrow}}dE = qAn_T(E)\frac{\Delta z}{\tau_0}\exp\left(-\frac{E_C' - E_{F0} - qV(\Delta z/2u_a)}{kT}\right)dE \tag{2.6}$$

where A is the area of cross section of the amorphous region, and $n_T(E)dE$ is the concentration of electrons in traps between E and $E + dE$. This expression can be used to describe the exponential behavior of the sub-threshold $I-V$ curves in Fig. 2.6. In order to account for the linear behavior of these $I-V$ curves at small applied voltages, the reverse current has to be considered. This is because, a trapped electron may have a non negligible probability of jumping back to a trap in the direction

opposite to the electrostatic force [18]. The reverse flow of electrons will be significant at small fields. The reverse current $dI_{\leftarrow}$ can be obtained as [16],

$$dI_{\leftarrow} = qAn_T(E)\frac{\Delta z}{\tau_0}\exp\left(-\frac{E_C' - E_{F0} + qV(\Delta z/2u_a)}{kT}\right)dE \tag{2.7}$$

where the barrier lowering is replaced by a barrier increase, by the same amount but opposite sign. Therefore, the net current is given by [18],

$$dI = 2qAn_T(E)\frac{\Delta z}{\tau_0}\exp\left(-\frac{E_C' - E_{F0}}{kT}\right)\sinh\left(\frac{qV}{kT}\frac{\Delta z}{2u_a}\right)dE \tag{2.8}$$

Here the density of localized electrons is expressed by the Maxwell- Boltzmann statistics as [18],

$$n_T(E) = N_T(E)\exp\left(-\frac{E - E_{F0}}{kT}\right) \tag{2.9}$$

where N_T is the trap density. Thus from (2.8), the current I can be obtained by integrating over the entire distribution of electron traps, i.e., above E_{F0}, resulting in [16],

$$I = 2qAN_{T,\text{tot}}\frac{\Delta z}{\tau_0}\exp\left(-\frac{E_C' - E_{F0}}{kT}\right)\sinh\left(\frac{qV}{kT}\frac{\Delta z}{2u_a}\right) \tag{2.10}$$

where $N_{T,\text{tot}}$ is the density of states integrated in the energy range E_{F0} to E'_{C}.

For small voltages, the sinh function in (2.10) can be replaced by its linear approximation [18],

$$I \approx \frac{q^2AN_{T,\text{tot}}\Delta z^2}{kT\tau_0 u_a}\exp\left(-\frac{E_C' - E_{F0}}{kT}\right)V \tag{2.11}$$

which accounts for the linear I–V region at low voltage.

For larger applied voltages, the sinh function approaches an exponential function and the conduction mechanism corresponds to the forward emission, thus $I = I_{\rightarrow}$.

For the entire sub-threshold regime, the activation energy can be obtained as [18],

$$E_A = -\frac{\partial \log I}{\partial(1/kT)} = E_C' - E_{F0} - \frac{qV}{kT}\coth\left(\frac{qV}{kT}\frac{\Delta z}{2u_a}\right) \tag{2.12}$$

which for sufficiently large voltages converges to [16],

$$E_A = -\frac{\partial \log I_{\rightarrow}}{\partial(1/kT)} = E_C' - E_{F0} - qV\frac{\Delta z}{2u_a} \tag{2.13}$$

Figure 2.8 shows the activation energy E_A extracted from data in Fig. 2.6, as a function of voltage. Equation (2.12) can account for both the linear decrease of E_A with voltage at sufficiently large voltage and for the saturation at low voltage. The decrease of E_A with voltage is consistent with data in Fig. 2.6 and is due to the lowering of the potential barrier between two trapped states for increasing voltage. The activation energy saturates to $E_C' - E_{F0} - kT$ in the ohmic regime, due to the competition between forward and reverse conduction [16].

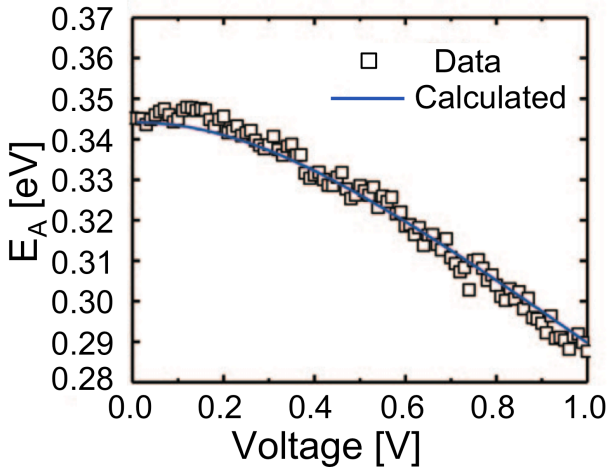

Figure 2.8: Activation energy as a function of voltage, obtained from experimental *I-V* curves at variable temperature and from calculations using Eq. (2.12) [16, 18]

2.3.5 Mechanism of Threshold Switching

Threshold switching in chalcogenide glasses appears as a sudden increase in conductivity with a negative differential resistance (NDR) behavior, leading to a characteristic snapback of the voltage at the threshold voltage V_t [19] as shown in Fig. 2.2. If the phase change material is in the highly resistive amorphous phase and a certain electrical field is applied to the material, it will suddenly (within nanoseconds) become highly conductive. This process does not necessarily lead to a phase

change; it is reversible if the current pulse is so short that it does not heat the material above the crystallization temperature for long enough time to cause crystallization [16]. *Threshold switching defines* V_t *and hence can be considered as fundamental to PCM as hot carrier injection or Fowler Nordheim tunneling is to floating gate based memory technology* [20]. This phenomenon has attracted scientific interest since the first proposal of chalcogenide materials for electronic devices [2] and its physical explanation is still largely debated today. Initial explanations included microscopic phase change [2], thermally induced instabilities [21], and carrier generation by impact ionization [22, 23]. Although switching has been recognized to be an electronic process [20], its details are still not completely understood, and a consistent explanation of the mechanisms for sub-threshold conduction and threshold switching is today missing.

The PF transport model at high electric fields, discussed previously, can be used to explain the NDR behavior [16-19]. Figures 2.9(a) and (b) schematically show the mobility gap of a chalcogenide glass, defined by mobility edges E_C' and E_V'. Here the equilibrium Fermi level E_{F0} is pinned at midgap. It is observed that (Fig. 2.9(a)), electrons at relatively low fields obey the equilibrium conduction model, i.e. Fermi statistics where approximately all the states below (above) E_{F0} are filled (unfilled) by electrons. Application of a large voltage (Fig. 2.9(b)) can lead to an energy gain of the carriers by the electric field, thus establishing a non-equilibrium carrier distribution in the amorphous semiconductor [19]. Due to the exponential energy dependence of the escape time in (2.5), even a small increase of energy, e.g. in the range of few *kT*, can result in a huge enhancement of conductivity, thus resulting in significant instability of conduction [16].

The energy gain effects can be described by employing the concept of *quasi Fermi energy* E_F [16, 19]. Since the current is mainly due to carriers lying around the Fermi level, E_F can also be viewed as the average energy of electrons mostly contributing to the current. This description is equivalent to considering the effect on the electron temperature [18], which increases under an applied electric field.

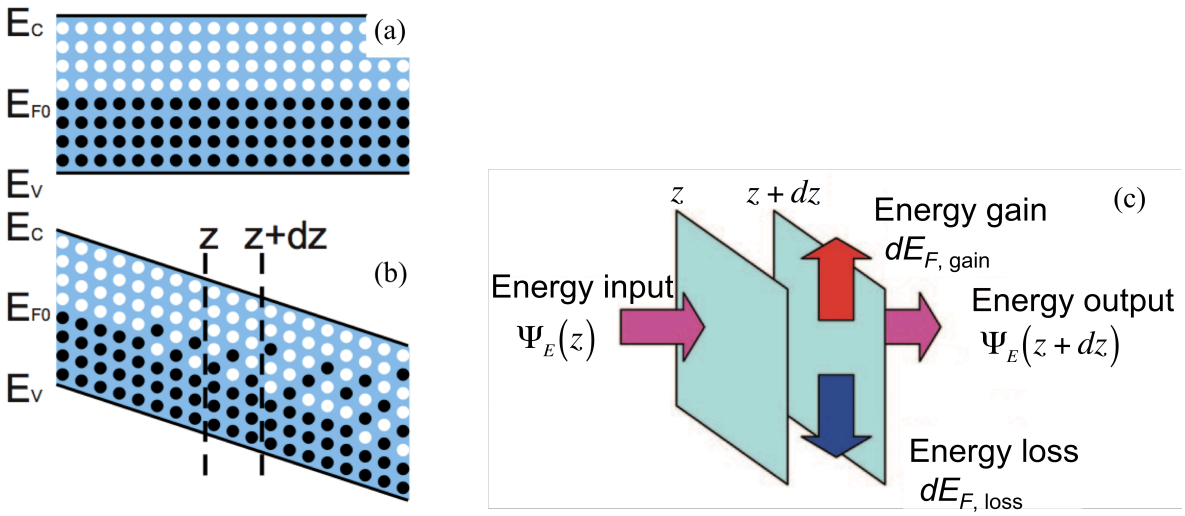

Figure 2.9: Schematic for (a) energy distribution of electrons in amorphous chalcogenide at equilibrium (no applied electric field), (b) energy distribution of electrons in amorphous chalcogenide under off-equilibrium conditions at high electric field [19], (c) energy balance in a thin slice *dz* along the direction of the current in the amorphous region [16]

Consider Fig. 2.9(c) representing the energy balance in a thin slice dz along the direction of the current in the amorphous region. The electrons entering the slice at z correspond to the input flow of energy given by [16],

$$\Psi_E(z) = \frac{J(z)E_F(z)}{q} \tag{2.14}$$

Similarly, the electrons exiting the slice at $z+dz$ result in an output flow of energy given by [16],

$$\Psi_E(z+dz) = \frac{J(z+dz)E_F(z+dz)}{q} \tag{2.15}$$

where J is the hopping current density. The energy gain in the slice due to the electric field is given by [16],

$$dE_{F,\text{gain}} = qF(z)dz \tag{2.16}$$

While the electric field tends to raise E_F, inelastic scattering processes reduce the excess energy. The effect of inelastic scattering can be modeled as a first-order energy relaxation rate, given by [19],

$$\left.\frac{dE_F}{dt}\right|_{\text{loss}} = -\frac{E_F - E_{F0}}{\tau_{\text{rel}}} \tag{2.17}$$

where the energy relaxation time τ_{rel} can be associated to electron-phonon interaction at localized states [19]. The energy loss $dE_{F,\text{loss}}$ can be obtained by dividing (2.17) by the average electron velocity, thus yielding [16],

$$dE_{F,\text{loss}} = \left.\frac{dE_F}{dt}\right|_{\text{loss}} \frac{qn_T}{J(z)}dz \tag{2.18}$$

where the concentration n_T [cm^{-3}] of trapped electrons contributing to the current has been used.

$$n_T = N_{T,\text{tot}} \frac{kT}{E_C' - E_{F0}} \tag{2.19}$$

Here it is assumed that the trap distribution $N_{T,\text{ tot}}$ is uniform in energy and that only traps within an energy range kT are populated, which is equivalent to integrating the exponentially decreasing Maxwell-Boltzmann distribution [19]. The balance between energy gain and relaxation in the slice between z and $z+dz$ thus reads [19],

$$\frac{J(z+dz)E_F(z+dz)}{q} - \frac{J(z)E_F(z)}{q} = \frac{J(z)}{q}\left(E_{F,\text{gain}} - E_{F,\text{loss}}\right) \tag{2.20}$$

$$\therefore \quad \frac{J(z)E_F(z)}{q} - \frac{J(z+dz)E_F(z+dz)}{q} + J(z)F(z)dz - \frac{E_F - E_{F0}}{\tau_{rel}} n_T(z)dz = 0 \tag{2.21}$$

For continuity $J(z+\mathrm{d}z) = J(z)$, and after some simplification [16],

$$\frac{dE_F}{dz} = qF - \frac{qn_T}{J}\frac{E_F - E_{F0}}{\tau_{\text{rel}}} \tag{2.22}$$

Equation (2.22) can be solved in conjunction with the analytical model in (2.10), corrected by the replacement of E_{F0} by the more general quasi-Fermi level E_F [16], thus allowing to describe off-equilibrium conditions at threshold switching, and with the basic relationship between electrostatic potential and electric field [16]:

$$F = \frac{dE_C'}{qdz} \tag{2.23}$$

Figure 2.10 illustrates the *I-V* curves obtained by solving the coupled equations (10) and (22) and using the relation (23). Different values for the thickness u_a of the amorphous region are assumed, and the best agreement with experiments is obtained for u_a = 40 nm, which is consistent with direct transmission electron microscopy (TEM) observation of the amorphous region in the memory cell [19]. The difference between the experimental and calculated *I-V* curves above the switching point is due to circuit-induced current spiking due to NDR [19] and consequent crystallization. As a result, experimental and calculated results should be compared limitedly to the sub-threshold/threshold regimes.

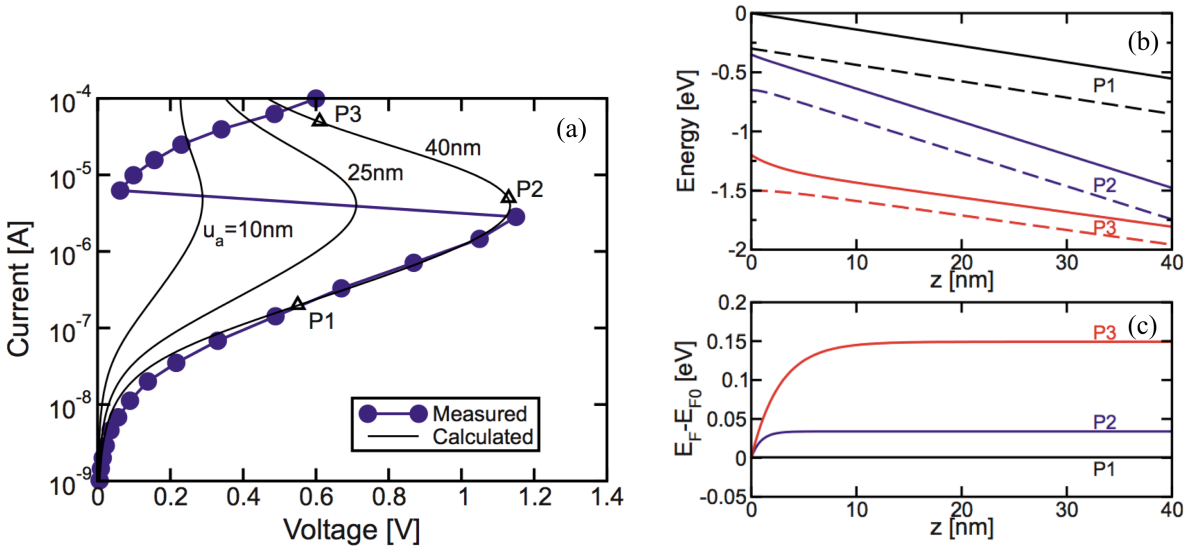

Figure 2.10: (a) Measured *I-V* curve for a PCM cell with amorphous GST and calculation results obtained from the coupled solution of eqs. (2.10) and (2.22) for different values of amorphous chalcogenide thickness. The three bias points P1, P2 and P3 are utilized in (b) and (c) to explain physical origin of NDR [19]. Calculated profiles for three bias points P1, P2 and P3 for (a) conduction band mobility edge E'_C (solid line) and quasi-Fermi level E_F, (b) average excess energy E_F - E_{F0} [19]

As discussed in [16, 19], the physical origin for the NDR can be understood by considering the profiles for E'_C, E_F (Fig. 2.10(a)), and the average excess energy E_F - E_{F0} (Fig. 2.10(b)) as a function

of the position along the amorphous layer z, obtained from the solution of (2.22). In these plots, P1, P2 and P3 represent three bias points denoting the sub-threshold region, the threshold point, and the ON state in the NDR region respectively. At P1, the excess energy is almost negligible, since the electric field is still insufficient to originate substantial energy gain. As a result, the field profile is flat and the potential profile E_C' is almost linear. At P2, the energy increases far from the cathode up to a value of about kT, which corresponds to an increase of current density J at constant field by a factor of e. Since the current must remain continuous at steady state and since there is no conductivity enhancement close to the injection electrode, a redistribution of the electric field is essential, thus resulting in a nonlinear potential profile. At even higher current levels, in the ON state at point P3, E_F - E_{F0} further increases to about 150 meV (Fig. 2.10(b)), thus causing a large non-uniformity of the field and a stronger bending of E_C'. The relatively large excess energy strongly enhances conductivity, thus allowing a large current to be sustained with a relatively small voltage drop across the amorphous layer. This results in a significant voltage with respect to the threshold switching point. Therefore, based on this model, NDR can be explained by taking into account, (i) the energy gain due to the high electric field in the proximity of the negative electrode and (ii) the consequent low voltage drop in the so-called ON region [16].

2.4 Materials Used for Phase Change Memory

Theoretically every material has the potential to undergo reversible structural changes between amorphous and crystalline states [14]. However, not all materials can undergo this change easily. Materials that can be utilized for practical PCM applications should exhibit the following properties:

(a) joule heating caused by current injection to produce structural changes modulated by the magnitude of the injected current,

(b) a large change in the electrical resistivity accompanied by the structural changes,

(c) stable existence of both amorphous and crystalline phases, for a long period of time at the operating environmental conditions.

In the case of metals, condition (b) is not satisfied because of the presence of many free electrons. For dielectrics, conditions (a) and (b) are not satisfied. Semiconductors such as Si and Ge have high T_m and high viscosity in the molten state. As a result, crystalline Si or crystalline Ge are difficult to amorphize because of high T_m while amorphous Si or amorphous Ge are difficult to crystallize because of high viscosity causing slow atomic diffusion.

Chalcogens such as Te and Se on the other hand, are two-fold coordinated, forming coil like structures. In the case of Te, the atoms form strong covalent bonds with two adjacent Te atoms resulting in a –Te-Te-Te- coil which is bound to another by a weak van der Waal force [14]. This is responsible for the low T_m (450 ˚C) of Te. When Te is heated above T_m, it easily melts by breaking the van der Waals bonds between the –Te-Te-Te- coils and these coils remain in the melt. Te is partially three fold coordinated in the molten state, and hence forms a random network structure. By rapid quenching, the network structure is frozen to form the amorphous solid [14]. The three-fold coordination in amorphous Te is not stable at room temperature and hence amorphous Te rapidly and automatically crystallizes by removing the cross-linking bonds. This means that stable, amorphous materials can be obtained by adding some cross-linking elements e.g. P, As and Sb have three-fold coordination with Te while, Si, Ge and Sn have four- fold coordination with Te. Thus, the fragile, amorphous Te was the starting point for the discovery and development of fast phase change materials [14].

A significant number of phase change materials can be found on the ternary phase diagram of the elements Ge, Sb and Te. This illustrated is in Fig. 2.11. These materials can be distinguished into two classes with slightly different compositions based on their crystallization mechanisms [14]. They have been described in the ensuing sections.

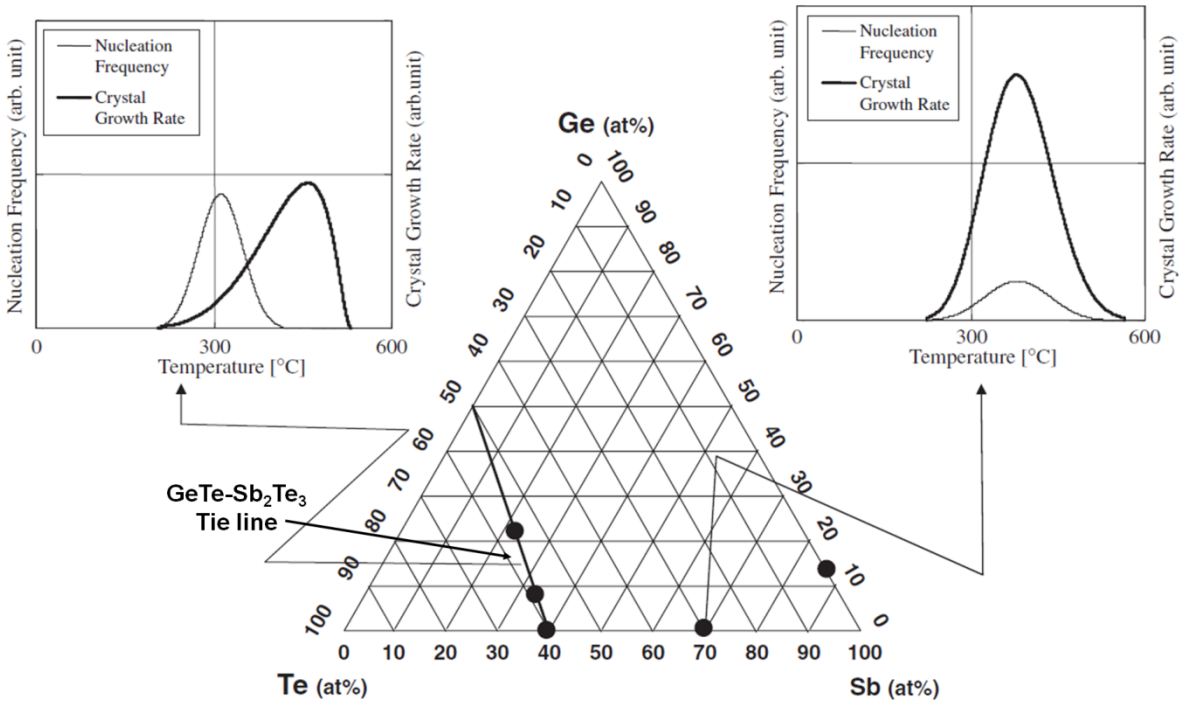

Figure 2.11: Typical compositions of phase change materials [14]

2.4.1 The Pseudo-Binary GeTe-Sb_2Te_3 Compositions – Class I

These materials lie on the GeTe-Sb_2Te_3 tie line. The widely researched $Ge_2Sb_2Te_5$ composition lies in this category. In these materials, crystallization is characterized by nucleation followed by growth of the nuclei over a small distance until they impinge on other crystallites [14]. These materials are called nucleation-dominated materials (NDMs). Along the tie-line, the properties change from GeTe with high crystallization temperature (i.e. high stability) and low crystallization speed to Sb_2Te_3 with high crystallization speed and low stability [24].

2.4.2 The Compositions Around the Eutectic Point $Sb_{69}Te_{31}$ – Class II

These materials are called growth-dominated materials (GDMs), in which crystallization starts from the amorphous-crystalline interface and proceeds inwards. GDMs are interesting options to achieve high data rates in high density formats [14]. They have better high temperature retention and low threshold field for conductivity switching in the amorphous phase [3]. The properties of these class II

materials such as crystallization rate and archival life stability can be adjusted by slight variations in their compositions [25].

Additionally, two other categories of phase change materials can be chronicled as follows,

2.4.3 Doped GST

Nitrogen or oxygen doping of GST results in grain growth suppression, leading to smaller grain size and a correspondingly enhanced resistivity resulting in lower value of RESET current I_{RESET}. Using this technique, the I_{RESET} has been reported to have reduced from 2 mA at the 240 nm technology node to 600 μA at the 120 nm technology node [26].

By employing SiO_2 as a dopant, crystallization temperature can be increased which helps in suppressing undesired SET operation of the cell. T_m also reduces with increase in SiO_2 concentration, which may lead to reduction in the I_{RESET} [27].

Sn doped GST has a lower ρ in the as-deposited state as well as a correspondingly lower RESET state resistance compared to undoped GST. Sn in GST may substitute Ge in GST resulting in the formation of lower energy Sn-Te bonds (bond energy = 76 kcal/mol), which may accelerate the crystallization in Sn-GST as compared to pure GST, which contains the stronger Ge-Te bond (bond energy = 93 kcal/mol) [28].

Addition of Si to GST reduces T_m. Hence low thermal energy is required for the amorphization process. However phase separation of Si may occur. ρ of Si-GST is an order of magnitude greater than that of undoped GST. V_t also increases with increased Si content [29].

2.4.4 Other Materials

Se based chalcogenide materials such as $SnSe_2$ have been reported to be amorphous in the as-deposited state, crystallize into a single crystalline phase above 200 °C, and have a reasonably high activation energy for crystallization of 1.93±0.07 eV [30]. All of these attributes indicate that $SnSe_2$ is

a good candidate for phase change memories. Bilayer PCM devices employing a thin film of Ge-chalcogenide with an overlying layer of metal-chalcogenide have also been proposed [1] and form the basis of discussion of this dissertation. Further details of the suitability of these materials for PCM applications will be furnished in the ensuing chapters.

2.5 Characteristics of GST based PCM cells vis–à-vis requirements of next generation NVM

This section presents an evaluation of the suitability of current GST based PCM technology as a successor to floating gate technology. Various key features have been examined and existing challenges have been identified as discussed below.

2.5.1 Read/Write Times

Fast read and write capability is a necessary prerequisite for any NVM technology that desires to become the industry mainstay. In case of PCM, read time of less than 50 ns has been reported [31]. On complete crystallization of the PCM material, a resistance window of almost three orders of magnitude between SET and RESET states can be achieved. This enables easy identification of the state (0 or 1) and hence very fast read circuitry can be employed. However, this is achieved at the cost of very long write times – complete crystallization of GST entails a write pulse of 10 μs. On the other hand if the SET pulse is reduced to 20 ns, the SET state will have a higher resistance thereby drastically reducing the resistance window between SET and RESET states. Thus, in order to exploit PCM technology for high-performance applications, the trade-off between fast write times and read noise margin is a key concern. With the SET pulse width reduced to 20 ns and the RESET pulse is decreased to 10 ns, a 10x resistance change has been observed between the two programmed states, and this is still suitable for read out operations [14].

2.5.2 Data Retention

The most important requirement for NVM is the capability to retain the stored information for a long time, a typical specification being 10 years at a minimum of 85˚C [3]. GST based PCM devices have been reported to exhibit the desired retention characteristics [8]. However, in high-volume manufacturing it is expected that extrinsic defect mechanisms such as non-uniformity of the contact surface of the electrode and composition distribution of the phase change layers will dominate retention characteristics [4]. The failure mode associated with data retention is the retention loss of amorphous cells. This results from the fact that amorphous GST is unstable with respect to crystalline GST, limited only by the kinetics of the crystallization process [14]. On the other hand, SET cells do not drift as they are already crystalline and hence their resistance is stable with time. Data loss in this state is therefore not a significant risk [14].

2.5.3 Endurance

Endurance of a PCM cell is determined by factors such as precipitation of chalcogenide material, diffusion of the electrode and insulating material into the chalcogenide and interface separation [4]. Single bit GST devices have been reported to show stable behavior upto 10^{12} cycles [3]. Integrated cells on the other hand exhibit a slightly reduced endurance of 10^{8}-10^{10} cycles [14]. This is still higher than the 10^{6} write cycles exhibited by floating gate technology [31]. There are two failure modes associated with cycling viz. stuck SET and stuck RESET. Stuck SET is caused by compositional changes occurring in the active volume of GST via its interaction with the surrounding electrode materials. Voiding or delamination at the heater chalcogenide interface on the other hand, causes stuck RESET. It has also been observed that ‘overcurrent’ or energy per pulse larger than that required for switching has a significantly deteriorating effect on the endurance of PCM cells [3]. In fact, it has been reported that cycling endurance scales inversely with the applied write energy [32].

2.5.4 Scalability

In order to be competitive with floating gate technology, PCM technology must exhibit excellent scalability particularly beyond the 45 nm technology node. In this section, several aspects of PCM scalability will be addressed.

2.5.4.1 Temperature profile distributions

For the proper operation of PCM memory, it is crucial that the heating remains very localized and does not affect the neighboring cells. It has been reported that, for a scaling factor of α, if two cells in the original device, at a distance d, do not suffer from cross talk then, in an isotropically scaled device, two cells at a distance d/α will be immune to thermal disturbances [3]. However, crosstalk immunity is no more granted in a more aggressive scaling scheme, where only the contact area of the cell is scaled down without changing the thickness of the different layers. Simulation results have shown that even without using additional thermally insulated layers, thermal cross-talk is not expected to slow down scaling till the 45 nm node [3].

2.5.4.2 Scaling of dissipated power and I_{RESET}

By using an isotropic scaling approach, as the technology node scales, the cell surface area decreases as $1/\alpha^2$ and the distance to the heat sink decreases as $1/\alpha$. As a result the electrical resistance increases by α and thus I_{RESET} and power dissipated scale as $1/\alpha$. A more aggressive reduction of the programming current can be achieved by scaling the contact area but not the other dimensions (such as PCM thickness). This causes the electrical resistance to scale faster i.e. by α^2 and hence both I_{RESET} and power dissipated scale as $1/\alpha^2$. Aggressive scaling has the potential to cause some manufacturability problems since the aspect ratio of some cell features (e.g. the thickness to the cell, size of the PCM material) will increase [3]. Even though the scaling result is independent of the

adopted cell architecture, it has to be optimized by an accurate design of the geometry and material engineering to minimize the programming current and the dissipated power.

2.5.4.3 Scaling of Voltage

The programming voltage for a PCM cell is determined by its threshold voltage. In addition to scaling with the PCM layer thickness, V_t is a strong function of the material. It has been shown that the minimum value of V_t depends upon the bandgap and/or the contact characteristics [3]. This may pose a constraint on the maximum voltage, which should be sustained by the bipolar selectors or by the gate oxide of the MOSFETs across the unselected cells of the array [3].

2.5.4.4 Scaling of Cell Size

The projection of the PCM scaling trend is illustrated in Fig. 2.12.

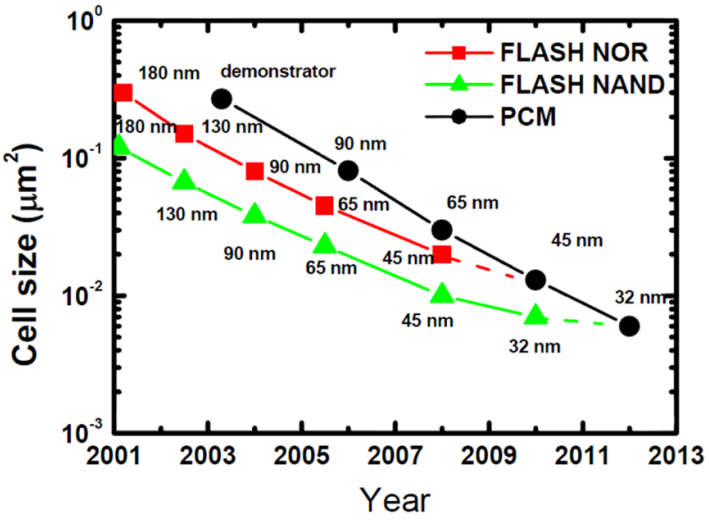

Figure 2.12: Scaling trends of NOR and NAND Flash and PCM technologies [11]

It is observed that the PCM cell size is expected to reach the NOR cell size around the 45 nm node and possibly reach the NAND cell size around the 32 nm node.

2.5.4.5 Physical Limits of Scaling

For optical memory applications, it has been found that very thin films of 6 nm Sb_2Te_3 and GeTe exhibit excellent recording properties. For PCM applications, doped $Ge_{15}Sb_{85}$ bridge type structures employing films as thin as 3 nm and 20 nm in width have been proposed. These devices could be switched repeatedly and showed very good thermal stability [33]. A storage density of 3.3 Tb/in^2 has been demonstrated using a heated atomic force microscope (AFM) tip on an 18 nm thick GST film [34]. From thin film research [14], it has been observed that at a certain thickness in the range of 1-2 nm, phase change materials will not crystallize any more. With shrinking dimensions, properties such as crystallization temperature, activation energy for crystallization, incubation time and crystallization speed will change. The crystallization speed for NDMs (sandwiched between electrodes) will be reduced while that for GDMs (sandwiched between electrodes) will first increase until it reaches a maximum at an optimum thickness in the 10 nm thickness range. Phase change nanowires and nanoparticles [14] have also been attempted. It has been proposed that as nanowires scale, the T_m, incubation time and activation energy for re-crystallization and the switching currents and powers will be reduced. From phase change nanoparticle research, good crystallization behavior has been observed for dimensions down to 15 nm with crystallization temperatures that are not too dramatically different from bulk [14].

2.5.5 Low Power

Low power essentially translates to low programming current, the upper limit of which is determined by I_{RESET}. This is crucial to achieve competitive memory density. I_{RESET} is determined by the contact area between the memory material and the heater and scales naturally with scaling in lithography. As discussed earlier, one proposed remedy to decrease I_{RESET} is to dope GST with N_2 or O_2 or SiO_2, all of which result in an increased resistivity in the RESET state.

Another solution is to engineer the PCM cell structure i.e. use an innovative approach to cell design. Examples of three major schemes used in cell engineering are elucidated in the following sections.

2.5.5.1 Reducing the Electrode Contact Area

A novel μ trench PCM cell has been proposed by Pellizzer *et al.* in [35]. A schematic cross section of such a device is illustrated in Fig. 2.13(b). To keep the programming current low while still maintaining a compact vertical integration, the definition of the contact area between the heater and the GST element is achieved by the intersection of a thin vertical semi-metallic heater and a trench in the heater-to-GST dielectric, referred to as the 'μ trench', in which the GST alloy is deposited. The trench approach allows defining the PCM active region as the intersection of a sub-litho feature and the deposited heater thickness.

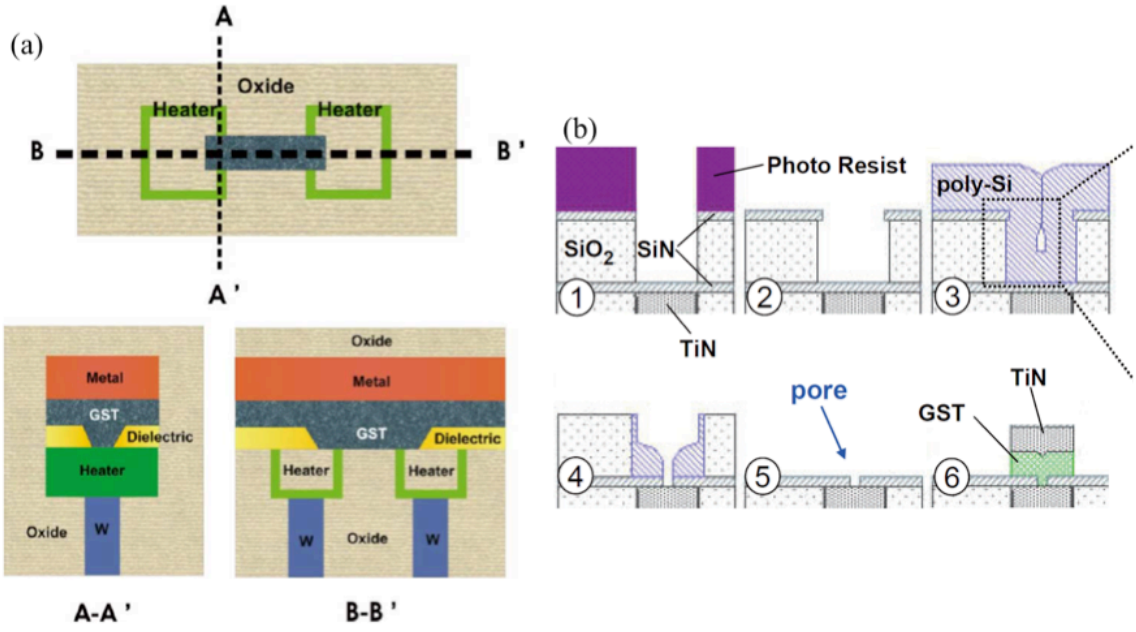

Figure 2.13: Cell engineering, (a) 'μ' trench PCM cell [35], (b) Fabrication of a 'pore' PCM cell [37]

This architecture has been demonstrated to achieve superior results in terms of programming current and dimensional control of the sub-lithographic features. For example, a 90 nm phase change process developed using the μ trench cell has been successful in reducing the programming current to 400 µA from 700 µA required by an equivalent cell employing a lance like heater [36]. However, the integration of the μ trench process in an array architecture demands additional lithographic

requirements, in particular the alignment tolerance with the word-line plugs to avoid short-circuits in the array [14]. Moreover, these constraints are expected to become increasingly important with the scaling of the technology node, thus becoming a potential yield detractor in next-generation PCM products [14].

2.5.5.2 Reducing the Phase Change Material Volume

Breitwisch *et al.* [37] have demonstrated a novel 'pore' phase change memory cell whose critical dimension is independent of lithography. As illustrated in Fig. 2.13(b), the pore diameter is accurately defined by intentionally creating a 'keyhole' with conformal deposition. First, a lithographically defined hole is etched into a SiN-SiO_2-SiN stack stopping on the bottom SiN. Next, a selective wet etch is used to recess the SiO_2 layer with respect to the SiN layer resulting in an overhang in the SiN layer. This is followed by a highly conformal polysilicon deposition, which results in the formation of a void or keyhole in the polysilicon whose diameter is equal to the recess of the SiO_2 layer. Further, this keyhole is transferred to the bottom SiN using an RIE process, resulting in the formation of a pore in the SiN layer. The SiO_2 and the polysilicon are removed using selective wet etches. Finally the PCM and top electrode materials are deposited. I_{RESET} less than 250 μA has been reported by using this technique. In addition to the increased number of processing steps and tight process control required, a crucial concern is that the pore must be filled without producing unwanted seam or void within the phase change material [14]. However, the steeper the sidewall, the more difficult it is to fill the pore with a physical vapor deposition (PVD) process. Combining this process with a chemical vapor deposition (CVD) phase change material deposition process would create a very efficient memory element, however CVD of phase change material is still in its infancy and requires extensive research for successful implementation [3].

Researchers from IBM, Macronix, Qimonda and Infineon have developed an ultra-thin PCM cell employing a novel phase-change bridge (PCB) using doped GeSb [33]. The PCB device consists of a narrow line of ultra-thin phase-change material bridging two underlying electrodes as shown in

Fig. 2.13(c). The electrodes are formed very close together to obtain a reasonable threshold voltage, separated by a small oxide gap that defines the bridge length *L*. The thickness of the phase-change material deposited on this planarized surface defines the bridge height *H*, and the width *W* is defined with a subsequent patterning step. In a PCB cell, the lithographic patterning has only a linear impact on the effective cross-sectional area. This offers both reduced sensitivity to variations in critical dimension, and an alternative path to rapid scaling via ultra-thin films. The doped GeSb is not a commonly used material system in phase change memory because it is not a chalcogenide. The material is chosen because it allows very good scalability. I_{RESET} of less than 100 µA has been demonstrated using such a design.

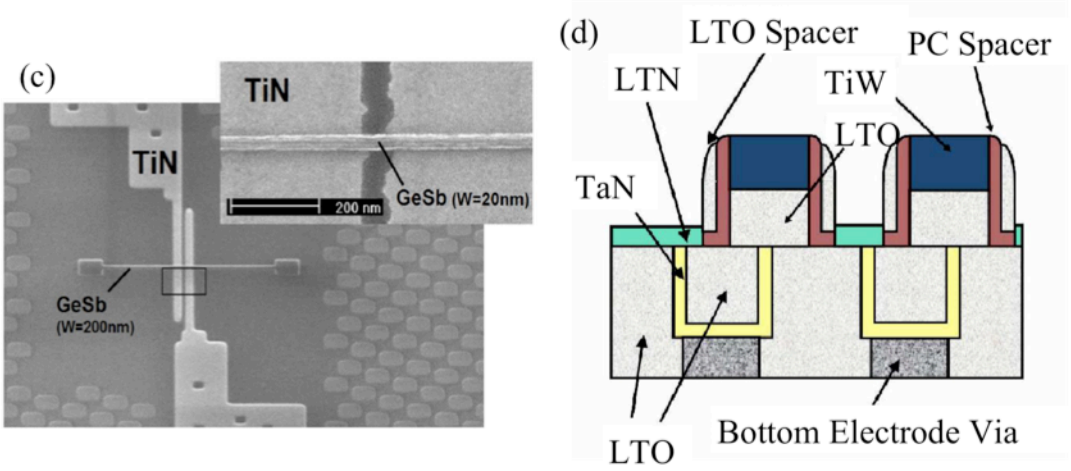

Figure 2.13: Cell engineering, (c) TEM of a phase change bridge [33], (d) Cross sectional view of cross-spacer structure [38]

2.5.5.3 Reducing Both the Material and the Contact

A cross-spacer structure illustrated in Fig. 2.13(d), has been reported by Chen *et al.* [38]. In this device a thin TaN layer is deposited in a via and then filled with oxide. The bottom electrode is formed after planarization by back etching. To ensure only one contact between the electrode and the phase change material, half of the bottom electrode is covered by a thin SiO_2 layer. After the

formation of a straight edged LTO and TiW top electrode, GST and SiO_2 are sequentially deposited on the SiO_2/TiW stack, followed by a blanket etch back to form the spacer. In this way an orthogonal contact between the phase change material and the bottom electrode can be made. Thus, the contact area between the phase change material and the bottom electrode is defined by the thickness of the TaN film and the phase change spacer and is not affected by lithography. Using this approach, an I_{RESET} of 80 μA has been reported for a contact area of 500 nm^2. One of the major concerns with this approach is that the GST film formed on the sidewall may cause reliability issues, especially since it is the key layer. Also, as discussed previously it is a serious challenge to obtain a smooth and uniform thin film on a vertical sidewall using a PVD process.

2.6 Need for Material Engineering

The PCM cell prototypes that have been evaluated in the preceding sections demonstrate that while I_{RESET} may be reduced by making clever modifications in cell design, it comes at the cost of increased process complexity and integration complexity, material deposition challenges and reliability issues. In addition to I_{RESET} reduction, moderating variation in switching voltages and ON/OFF resistance ratios, lowering thermal stresses on materials and improving their adhesion to the electrodes –all of which are crucial for high density memory development – are not addressed by mere cell engineering. On the other hand, material engineering which involves modification of existing materials e.g. doped GST or exploration of new materials e.g. GeSb, offers a much wider scope. In this spirit of exploration, Campbell *et al.* have proposed device structures with layered or stacked chalcogenide films in [1]. These structures comprise of Ge-chalcogenide and an overlying layer of Sn-chalcogenide – an arrangement that offers the possibility of creating a phase change memory device with tunable electrical properties. This forms the rationale of the work described in this dissertation.

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Chapter 3: Motivation and Research Objectives

This chapter is divided into two sections. The first half is devoted to the rationale behind the investigation of bilayer chalcogenides as potential PCM memory materials, and the second part lists out the goals of the presented research.

3.1 Motivation

A bilayer structure, as proposed by Campbell *et al.* [1], is illustrated in Fig. 3.1. It utilizes a layer of germanium chalcogenide (Ge-Ch), which may be GeTe or Ge_2Se_3, and a layer of tin chalcogenide (Sn-Ch), which may be SnTe or SnSe.

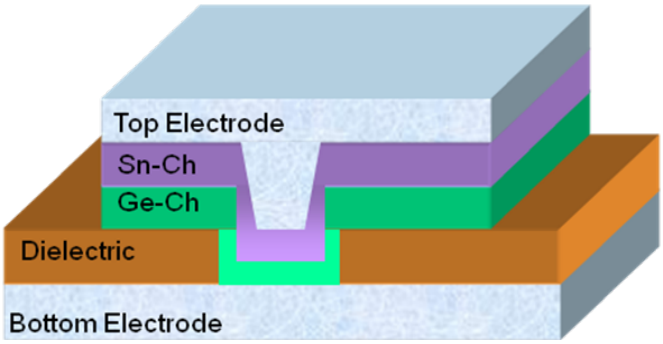

Figure 3.1: Bilayer chalcogenide based PCM structure [1]

The rationale behind the choice of materials employed is discussed below [1]:

3.1.1 Choice of Memory Material

The Ge-chalcogenide layer serves as the memory material. The potential of GeTe as a PCM material has been well documented [2, 3]. On the other hand, Campbell *et al*. were the first to examine Ge_2Se_3 for PCM applications. Both GeTe and Ge_2Se_3 contain homopolar Ge-Ge bonds, which may provide nucleation sites for crystallization during the phase-change operation, thus improving the phase-

change memory response. Also, Ge_2Se_3 offers the advantage of higher glass transition temperature over Te-based glasses, thus providing more temperature tolerance during manufacturing.

3.1.2 Merits of Using a Tin-Chalcogenide Layer

(a) The contact between the Ge-Ch and the electrode is essentially a Schottky barrier. The insertion of a metal-chalcogenide layer between the two, results in an Ohmic contact which allows for the application of a lower voltage to the memory cell in order to achieve the current necessary for phase-change switching.

(b) The Sn-chalcogenide layer provides a better adhesion of the Ge-Ch layer to the electrode. Thus delamination issues arising from repeated thermal cycling may be circumvented or minimized.

(c) The inclusion of an Sn-Ch layer may provide a region with graded chalcogenide concentration between the Sn-Ch and Ge-Ch layers due to the ability of the chalcogenide to form bridging bonds between the Sn and Ge atoms in the Sn-Ch and Ge-Ch layers respectively.

(d) The Sn-Ch layer may donate Sn ions to the Ge-Ch layer during operation thereby allowing chalcogenide materials that do not exhibit phase change response to be chemically altered into an alloy that is capable of such a response. Thus, the Sn-Ch layers assists in PCM switching by electrically tuning the characteristics of the Ge-Ch material.

Thus, research in layered chalcogenide PCM devices is of consequence because:

(a) By using a layered arrangement, it is possible to induce phase change response in materials which normally do not exhibit such behavior and thus form new materials which may have lower V_t and programming current requirements.

(b) Through the incorporation of a metal containing layer, the phase transition characteristics of the memory layer can be tailored in order to obtain a material with optimized phase change properties.

(c) Due to an improved contact between the chalcogenide material and the electrode via insertion of a metal-chalcogenide film, layered devices show an enhanced capacity to withstand thermal cycling

thus precluding adhesion issues. This is a key factor in improving endurance; particularly in eschewing stuck RESET issues.

(d) Stacked structures show promise of multi-state behavior - a feature that a single GST layer is incapable of exhibiting [4]. Thus improvement in memory density can be achieved without compromising on cell size.

The features exhibited by bilayer structures, highlighted above, are the key ingredients in fashioning a low power, highly reliable non-volatile memory technology with high endurance and possibility of multi-bit operation, thus making layered chalcogenide PCM devices a leading contender for the future commercialization of PCM technology. This forms the motivation of the work discussed in this dissertation.

3.2 Research Objectives

Based on the rationale described in the preceding section, the major goals of this research are as presented below:

(1) Perform a materials study of layered structures

As discussed previously, the switching behavior observed in layered structures is due the interaction between the top and bottom films resulting in a material with optimized properties for phase change operation. A comprehensive materials characterization of these bilayer structures has not been carried out so far. It is the goal of this research to investigate phase transition, analyze residual stress and examine possible Sn migration in these stacked structures by means of X-ray diffraction (XRD), time resolved XRD and parallel electron energy loss spectroscopy (PEELS), in order to gain further insight into the functioning of devices built using such layers.

(2) Design and fabricate a two terminal PCM cell employing stacked chalcogenide layers.

This is the first step towards developing a memory array. The two terminal cells will be fabricated using techniques and materials compatible with the RIT 2 μm CMOS process.

(3) Integrate the two terminal device with CMOS, using the RIT 2 μm process as a baseline.

The final goal of this research is to integrate the two terminal PCM cell designed in step (2) with a 2 μm CMOS process. This will serve as a proof of concept for developing a prototypical memory array in the future.

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Chapter 4: Material Characterization

A comprehensive material characterization of the chalcogenide stacks is carried out prior to PCM device fabrication. This chapter describes the application of techniques such as X-ray diffraction, transmission electron microscopy and parallel electron energy loss spectroscopy to investigate phase transition, residual stress and material inter-diffusion in the bilayers.

4.1 Introduction to X-ray Diffraction

X-ray diffraction can be employed to examine the crystal structure of a solid. The X-rays used in diffraction experiments have wavelengths lying approximately in the range of 0.5 – 0.25 Å, which is of the same order as the distance between crystal lattice planes [1].

Consider a perfectly parallel and perfectly monochromatic beam of X-rays incident on the (*hkl*) planes of a crystal as shown in Fig. 4.1. The incident X-rays will be scattered in all directions by the crystal. A diffracted beam will result if the reflected beam is composed of a large number of scattered rays mutually reinforcing one another.

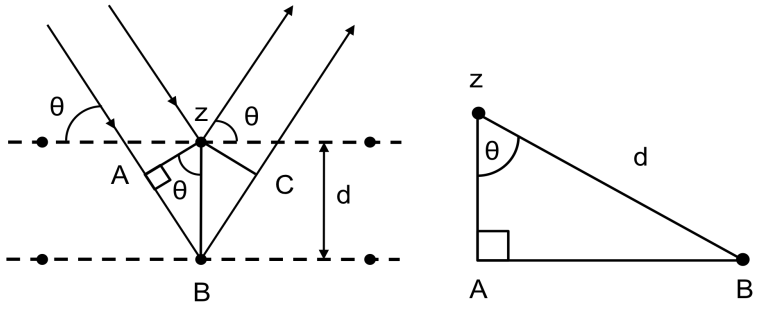

Figure 4.1: Diffraction of X-rays by a crystal using Bragg's law [1]

Such reinforcement will occur only in those directions in which the scattered beams are completely in phase. This is possible only if the path difference between the scattered rays is an integer multiple of

the wavelength λ of the incident X rays. This condition can be mathematically expressed by Bragg's Law as,

$$n\lambda = 2d' \sin\theta_B \tag{4.1}$$

Here n is the order of reflection, d' is the interplanar spacing of the (hkl) planes under consideration and θ_B is called the Bragg angle. A more convenient variant of Bragg's Law is given in (4.2).

$$\lambda = 2\frac{d'}{n}\sin\theta_B$$
$$\text{i.e.} \quad \lambda = 2d\sin\theta_B \tag{4.2}$$

Since the coefficient of λ is now unity, a reflection of any order can be considered as a first order reflection from planes (real or fictitious) spaced at a distance of $1/n$ of the previous spacing [1].

The crystal structure of a solid determines the diffraction pattern of that solid. Specifically, the size of the unit cell determines the angular positions of the diffraction lines and the arrangement of the atoms within the unit cell determines the relative intensities of the lines. Since it is impossible to obtain a perfectly monochromatic beam for XRD, characteristic K lines can be employed. These characteristic lines are very narrow and exhibit a tight wavelength distribution and hence are used for practical diffraction experiments.

4.2 Amorphous-Crystalline Spectrum of Chalcogenides under Investigation

Based on the literature, the amorphous-crystalline spectra of individual chalcogenide layers, employed in the PCM devices discussed in this research, are presented below.

(a) GeTe

Thin films of GeTe deposited using techniques such as sputtering or evaporation are typically amorphous [2, 3]. At ~170 ˚C, GeTe crystallizes to a rhombohedral state [4]. At higher temperatures in the range of 350 ˚C – 432 ˚C, a rhombohedral to cubic transformation occurs [3-5]. GeTe melts at ~725 ˚C [6].

(b) SnSe

SnSe is crystalline upon deposition and typically exhibits an orthorhombic crystal structure [7]. Its melting temperature is around 880 ˚C [8].

(c) Ge_2Se_3

Ge_2Se_3 is an alloy equivalent to $(GeSe)_{0.33}(GeSe_2)_{0.67}$ [9]. In the as-deposited state, it is amorphous [2]. Ge_2Se_3 has been reported to crystallize into orthorhombic GeSe and monoclinic $GeSe_2$ at around 450 ˚C [9]. Ge_2Se_3 glasses prepared using the melt quench technique [10] have been found to melt at around 600 ˚C [11].

(d) SnTe

SnTe is also crystalline upon deposition and exhibits a cubic crystal structure [12]. Its melting temperature is around 806 ˚C [8].

4.3 Residual Stress Analysis

In order to gain insight into phase transitions at elevated temperatures, chalcogenide thin film stacks of Ge_2Se_3/SnTe and GeTe/SnTe are analyzed for residual stress using XRD. For the purpose of this study, the as-deposited film stacks are annealed at different temperatures and the thermal dependence of stress is investigated. Stress evaluations are performed by employing the $\sin^2\psi$ technique [1, 13] using a 2D area detector system.

4.3.1 Sample Preparation

Silicon (100) wafers, 100 mm in diameter are cleaned in order to strip them of organics, native oxide and ionic contaminants. This is followed by thermal oxidation at a temperature of 1172 ˚C for 45 minutes in O_2. The resulting oxide thickness is measured optically and is found to be approximately 50 nm. Pressed Ge_2Se_3 or GeTe powder is thermally evaporated on the oxidized wafers. During the evaporation, the wafers are rotated at a speed of approximately 11 RPM. The

deposition is carried out at a base pressure of 2×10^{-6} Torr in order to obtain a film thickness of 30 nm. SnTe (from Alfa Aesar, 99.999% purity) is also evaporated in a similar fashion resulting in a 50 nm thick layer. Thickness measurement for the chalcogenide films is done in-situ using a crystal monitor. Detailed chalcogenide evaporation descriptions are provided in Chapter 5.

The wafers are cut into smaller samples having typical dimensions of 1 cm^2. A Bruker D8 Diffractometer equipped with an Anton-Paar DHS900 domed hot stage is used to obtain the diffraction profiles. Within the dome, samples are heated to various annealing temperatures under flowing nitrogen at a rate of 30 ˚C/min, held for 10 minutes, cooled at the same rate and then subjected to XRD. *Thus, all XRD profiles acquired using the Bruker D8 Diffractometer are obtained at room temperature unless specified otherwise.*

4.3.2 Stress Measurement Technique

In the XRD method of stress determination, the strain is measured in the crystal lattice by examining the shift in the position of a selected diffraction peak for different tilt angles (ψ), and the residual stress producing the strain is calculated assuming a linear elastic distortion of the crystal lattice [13]. Equation (4.3) relates the *d*-spacing corresponding to the stress and tilt angle.

$$d_{\phi\psi} = d_n + d_n\left(\frac{1+\nu}{E}\right)\sigma_\phi \sin^2\psi \tag{4.3}$$

Here, σ_ϕ is the surface stress, making an arbitrary angle ϕ with the principal stress σ_{11}, d_n is the plane spacing of selected *hkl* planes when the sample is in stressed condition with the surface normal $\boldsymbol{N}_s$ coinciding with the plane normal $\boldsymbol{N}_p$ (i.e., tilt angle $\psi = 0^\circ$). $d_{\phi\psi}$ is the spacing between the lattice planes measured in the direction defined by ϕ and ψ, and ν and E are the Poisson's ratio and Young's modulus respectively. The theoretical ψ is related to the experimental setup through an angle defined as ω, which is the angle between the incident X-ray beam and the sample surface. The

tilt angle ψ can be computed using the relation $\psi = \omega - (2\theta_B/2)$, where θ_B represents the Bragg angle of the peak under consideration.

A Vantec 2000 2D area detector is used to measure the 2θ -γ (Debye ring) position and intensity of the diffracted beams. The use of this detector allows a wide 2θ measurement without moving the diffraction beam detector. Hence highly resolved and repeatable results can be obtained [14]. As opposed to a point detector or a position sensitive detector, the diffraction information measured by a 2D detector is not restricted to the diffractometer plane. Point and position sensitive detectors do not capture the material structure information outside the diffractometer plane. Hence additional sample rotations and time are essential in order to obtain the complete measurement. With Vantec 2000, there is no such limitation. Faster measurement capability enables multiple peaks to be studied at the same time.

For high precision strain measurements, high angle diffraction lines are desirable. However, such lines are low in intensity and hence relatively difficult to measure. Consequently, as a tradeoff between the two, the (420) and (422) peaks of SnTe, having reasonable 2θ and intensity values are chosen in this work. In fact, the intensity of the (420) peak is toward the lower end, which makes an area detector ideally suited to observe it because intensity can be integrated over a portion of the Debye ring. Instead, if a point detector were used then, due to low intensity this peak would almost blend in with the background.

In order to obtain the relation between $d_{\phi\psi}$ of a particular peak and ψ, different values of ω are selected in accordance with the $\sin^2\psi$ method. These values are listed in Table 4.1. This variation of $d_{\phi\psi}$ with ψ is determined for in-plane sample orientation angles (ϕ) of 0˚, 45˚ and 90˚. Once ω and ϕ are selected, XRD profiles are obtained by fixing the area detector at 2θ = 78˚ so that a wide range of 64˚-90˚ can be covered. This enables the (420) and (422) peaks to be obtained simultaneously. The scan step size for intensity integration is set to 0.02˚. The sample-to-detector distance is fixed at

20 cm and a pin hole slit of 0.5 mm is used. A resolution of 0.02˚ can be achieved according to [14]. The incident beam, conditioned with a Göbel mirror, is Cu Kα radiation of wavelength 1.5418 Å.

Table 4.1: Tilt angles used for residual stress measurement

2θ (degrees)	$\sin^2 \psi$	
	420 Peak, $\theta_B = 32.98^\circ$ (Cu Kα1, λ=1.54056Å)	422 Peak, $\theta_B = 36.63^\circ$ (Cu Kα1, λ=1.54056Å)
36.6	0.0039	0.00
23.7	0.0261	0.0498
18.2	0.0653	0.0996
13.8	0.1082	0.1508
10.1	0.1527	0.2005
6.6	0.1977	0.2500

Samples of Ge_2Se_3/SnTe and GeTe/SnTe in the as-deposited state as well Ge_2Se_3/SnTe stacks annealed at 240 ˚C, 270 ˚C, 360 ˚C and 450 ˚C and GeTe/SnTe bilayers annealed at 170 ˚C, 200 ˚C, 270 ˚C and 450 ˚C are investigated using the procedure described above.

4.3.3 Extraction of 1D profile from 2D data

The 2D diffraction frames of Ge_2Se_3/SnTe as-deposited and annealed at 450 ˚C are shown in Fig. 4.2.

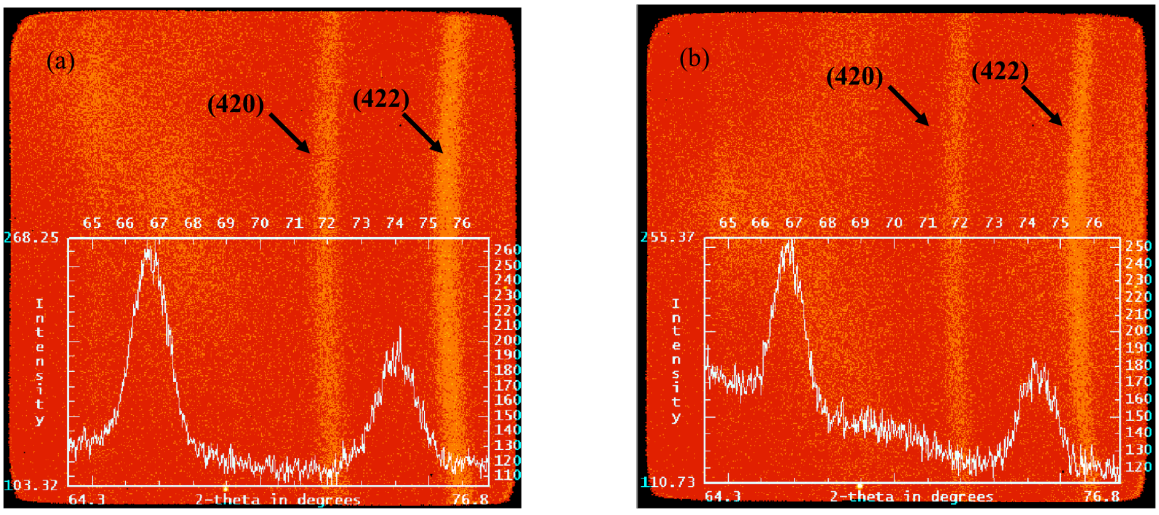

Figure 4.2: 2D diffraction frames showing (420) and (422) Debye rings in (a) as-deposited Ge_2Se_3/SnTe sample and (b) Ge_2Se_3/SnTe sample annealed to 450 ˚C

The Debye rings represent the (420) and (422) SnTe lines respectively. The presence of these Debye rings is indicative of the polycrystalline nature of the film. In order to convert the 2D data into 1D form (inset) integration over a γ range of 10˚ is performed. It is possible to achieve a high integrated intensity even with a small X-ray beam size due to the fact that there are a large number of grains, which are contributing to each Debye ring.

4.3.4 Results and Discussion

Results pertaining to Ge_2Se_3/SnTe and GeTe/SnTe are discussed separately in the ensuing sections.

4.3.4.1 Ge_2Se_3/SnTe Stack

The XRD profiles of the different samples for a 2θ range of 14˚–70˚ are shown in Fig. 4.3(a). The diffraction pattern of as-deposited sample, exhibits peaks only due to the top SnTe layer (PDF# 461210 [15]) signifying that the bottom Ge_2Se_3 film is amorphous. When the sample is annealed to about 240 ˚C, a slight right shift in the SnTe peak positions is observed as is seen by the displacement of the (420) peak from the dotted line. For the sample annealed at 270 ˚C the diffraction pattern shows the appearance of new peaks. These peaks have been found to correspond to a new phase viz. SnSe (PDF# 530527 [15]). Also, the SnTe peaks appear to have shifted further to the right as compared to the previous case. The samples annealed at 360 ˚C and 450 ˚C exhibit stronger SnSe peaks. In the diffraction profile of the latter, the peak shift observed is now towards the left.

Stress measurements are performed in order to understand the origin of these peaks shifts. XRD peak profile fitting is carried out using the Pearson Type VII function [16] and the principal stresses σ_{11} and σ_{22} are determined. The invariant sum of principal stresses (σ_{11} + σ_{22}) is plotted against annealing temperature in Fig. 4.3(b). Table 4.2 lists the measured values of d spacing and principal stresses as a function of annealing temperature.

From Fig. 4.3(b) it is seen that in the as-deposited state SnTe experiences a low compressive stress. Since the bottom Ge_2Se_3 film is amorphous, strains resulting due to lattice mismatch between

the two films are absent. This accounts for the small value of residual stress. In the case of the sample annealed at 240 ˚C, the slight right shift in the SnTe peak positions can be related to the fall in the value of d_n, as is evident from Table 4.2. It is suggestive of an increase in tensile stress experienced by the top layer.

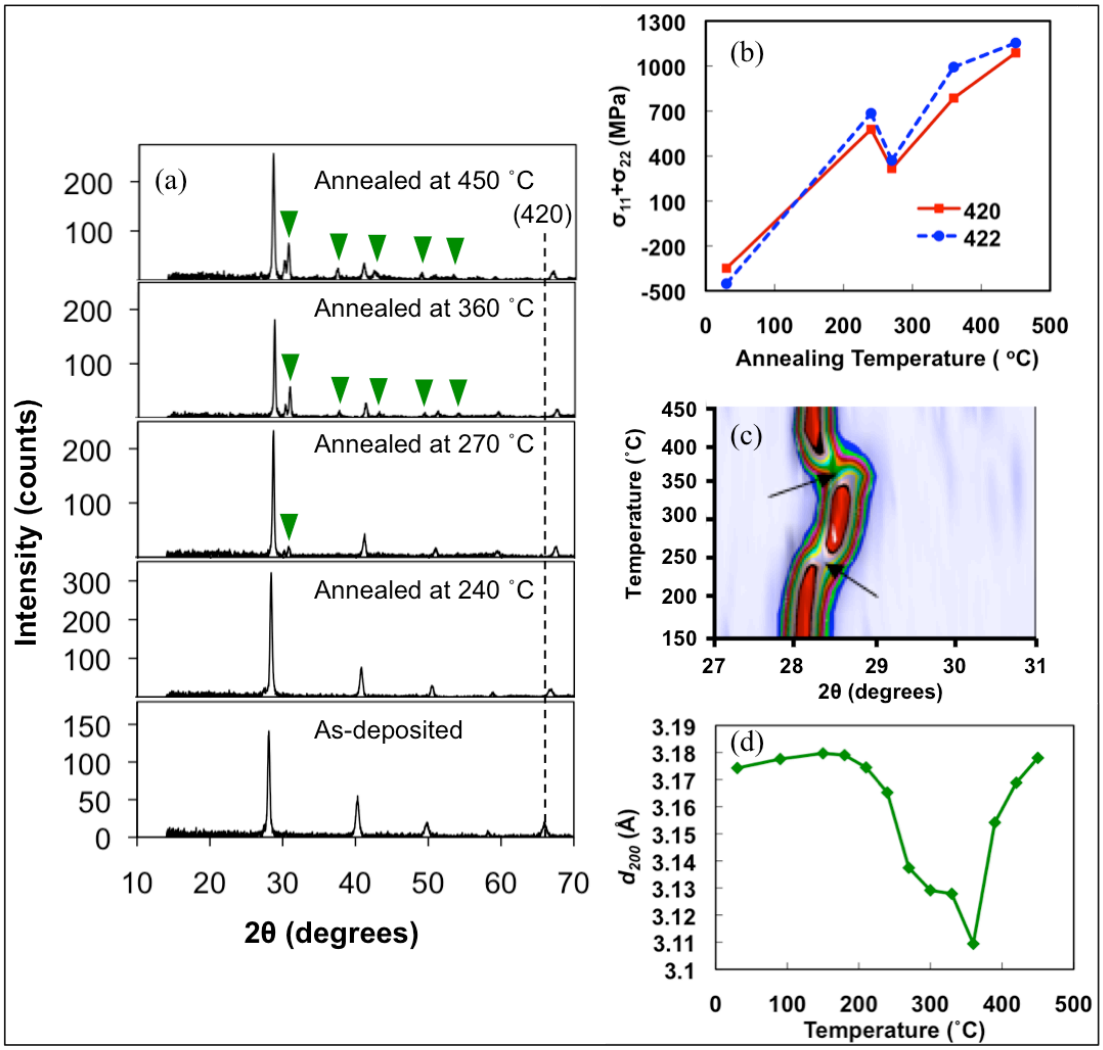

Figure 4.3: (a) Diffraction profiles of Ge_2Se_3/SnTe samples annealed at various temperatures (temperature increases from bottom to top), (b) Annealing temperature dependence of in-plane residual stress, (c) Level view of SnTe (200) peak upon heating. The arrow at ~250 ˚C corresponds to separation of SnSe phase. The arrow at ~350 ˚C represents possible crystallization of Ge_2Se_3, (d) Variation of d_{200} with temperature

As discussed previously, Fig. 4.3(b) indicates a noticeable decline in the stress level at around 270 ˚C. This behavior can be attributed to the crystallization of the SnSe phase, possibly due to migration of Sn ions to the bottom Ge_2Se_3 layer. This is validated by the appearance of SnSe peaks in the corresponding diffraction pattern. A volume reduction is associated with such a phase transition and the top SnTe layer experiences an increased compressive stress.

Table 4.2: Measured values of *d*-spacing and principal stresses for Ge_2Se_3/SnTe

Annealing Temperature	d_n **(Å)**		$\sigma_{11} \times 10^6$ **(Pa)**		$\sigma_{22} \times 10^6$ **(Pa)**	
	(420)	(422)	(420)	(422)	(420)	(422)
As-deposited	1.413	1.291	-112	-175	-237	-277
240 ˚C	1.396	1.273	387	405	191	280
270 ˚C	1.385	1.262	270	409	464	-38
360 ˚C	1.383	1.259	490	610	296	383
450 ˚C	1.394	1.270	709	672	379	482

As the bottom layer begins to crystallize, peaks due to Ge_2Se_3 are anticipated in the diffraction pattern. However they are not observed in the profiles of the samples annealed at 360 ˚C and 450 ˚C. The diffraction patterns of these samples are similar to that of the sample annealed at 270 ˚C except that the SnSe peaks have become more prominent at these higher annealing temperatures and further peak shifting has occurred. The stronger SnSe peaks are an indication of an enhanced level of crystallization. The peak shift on the other hand, can be attributed to two factors viz. residual stress developed due to crystallization of the bottom layer and compositional variation of the stack with annealing temperature. From Table 4.2 it is seen that for the (420) peak of the sample annealed at 360 ˚C, the change in *d* spacing is approximately 2%. However the calculated strain accounts for only 0.4% of it. Similarly for the (422) peak of the same sample, the change in *d* spacing is approximately 2.5% but the calculated strain accounts for only 0.5% of it. The remainder can be attributed to the possible diffusion of Sn or Te or both into the bottom Ge_2Se_3 layer resulting in the formation of a Ge_2Se_3-SnTe solid solution. Since ionic inter-diffusion has visually manifested itself at lower

annealing temperatures (270 ˚C) through the separation of the SnSe phase, it may be considered to be at work even at higher annealing temperatures (≥ 360 ˚C).

XRD studies performed on single layer Ge_2Se_3 films have revealed that Ge_2Se_3 sublimes easily. Even though Ge_2Se_3 crystallizes in the range of 270 ˚C – 360 ˚C as evidenced by the sharp drop in stress in Fig. 4.3(b), the absence of Ge_2Se_3 peaks may be attributed to its sublimation during the step when the sample is held at the annealing temperature for 10 minutes. It has been reported that employing a capping layer over the chalcogenide can inhibit sublimation [17]. The effect of Al_2O_3 as a capping material is discussed in sections 4.4 and 4.5.

The effect of compositional alterations is also observed in the case of sample annealed at 450 ˚C. The peaks in the profile of this sample appear to have shifted left as compared to that of the previously discussed one. However the stress seems to have become more tensile than in the previous case. If residual stress were considered to be solely responsible for change in *d* spacing then the measured peak shift would be toward the right. Thus the direction of the shift is an indication that the change in *d* spacing is being driven by a second factor, which is identified as the variation in composition of the stack with annealing temperature.

To study compositional changes in the stack, the SnTe (200) peak is monitored during heating. Fig. 4.3(c) shows the level view of SnTe (200) peak as a function of temperature in a Ge_2Se_3/SnTe stack. A broad *d*-spacing change can be observed, initiating from ~180 ˚C until 450 ˚C. The d_{200} versus temperature is plotted in Fig. 4.3(d). Phase transitions can be described by three stages: (i) the first stage occurs from 180 ˚C to 240 ˚C, accompanying a gradual d_{200} decrease; (ii) the second stage occurs from 240 ˚C to 330 ˚C, characterized by a sharp decrease of d_{200} and (iii) the third stage occurs from 330 ˚C to 450 ˚C, where a first decrease then sharp increase of d_{200} is observed. According to the diffraction profile illustrated in Fig. 4.3(a), the second stage should correspond to the separation of the SnSe phase.

In the third stage, no new peaks can be identified; however, the sharp increase in d_{200} shown by the top arrow in Fig. 4.3(c), may indicate a second phase transition. This phase transition occurs near

360 ˚C, much lower than the crystallization temperature of Ge_2Se_3. It is known that the glass transition temperatures of both Ge-Se-Sn and Ge-Se-Te glasses decrease with increasing Sn or Te content due to a continuous reduction of activation energy and connectedness [18, 19]. In the case of Ge-Sn-Se-Te system, SnSe can serve as a network modifier to adjust the glass transition temperature [20]. It is therefore reasonable to conclude that the transition temperature of Ge_2Se_3 is lowered because of interlayer diffusion of either Sn or Te or both into Ge_2Se_3.

TEM and PEELS analysis of variously annealed bilayer samples is carried out in order to provide evidence of such interlayer diffusion and the results are presented in Section 4.5.

4.3.3.2 GeTe/SnTe Stack

Figure 4.4(a) shows the XRD profile of as-deposited GeTe/SnTe stack. Only the peaks of SnTe (PDF# 461210 [15]) are identified indicating that the underlying GeTe layer is amorphous. Crystallization of GeTe (PDF# 471079 [15]) begins after annealing at 170 ˚C. This is consistent with the literature reported value of the crystallization onset temperature of GeTe [6]. However, these GeTe peaks disappear after the annealing temperature is increased above 200 ˚C. Additionally, all SnTe peaks shift to larger 2θ values after annealing. In the sample annealed at 270 ˚C, d_{420} is 2.1% smaller than in as-deposited sample. In conjunction with the disappearance of GeTe peaks, this large change in d_{420} can be attributed to either the development of residual stress in SnTe or composition change in the stack or both during annealing.

Similar to the case of Ge_2Se_3/SnTe stack, the as-deposited GeTe/SnTe film is under a small compressive stress due to absence of lattice mismatch during deposition. However, samples exhibit increasing tensile stress with increasing annealing temperature. Fig. 4.4(b) shows the invariant sum of the measured principal stresses as a function of annealing temperature. Initially, as the temperature is increased, the tensile stress increases. At around 200 ˚C there is a sharp dip in the stress and this can be attributed to the transition of the underlying GeTe layer from amorphous to crystalline.

Consequently there is a reduction in the volume of the bottom layer, which is responsible for the decrease in tensile stress.

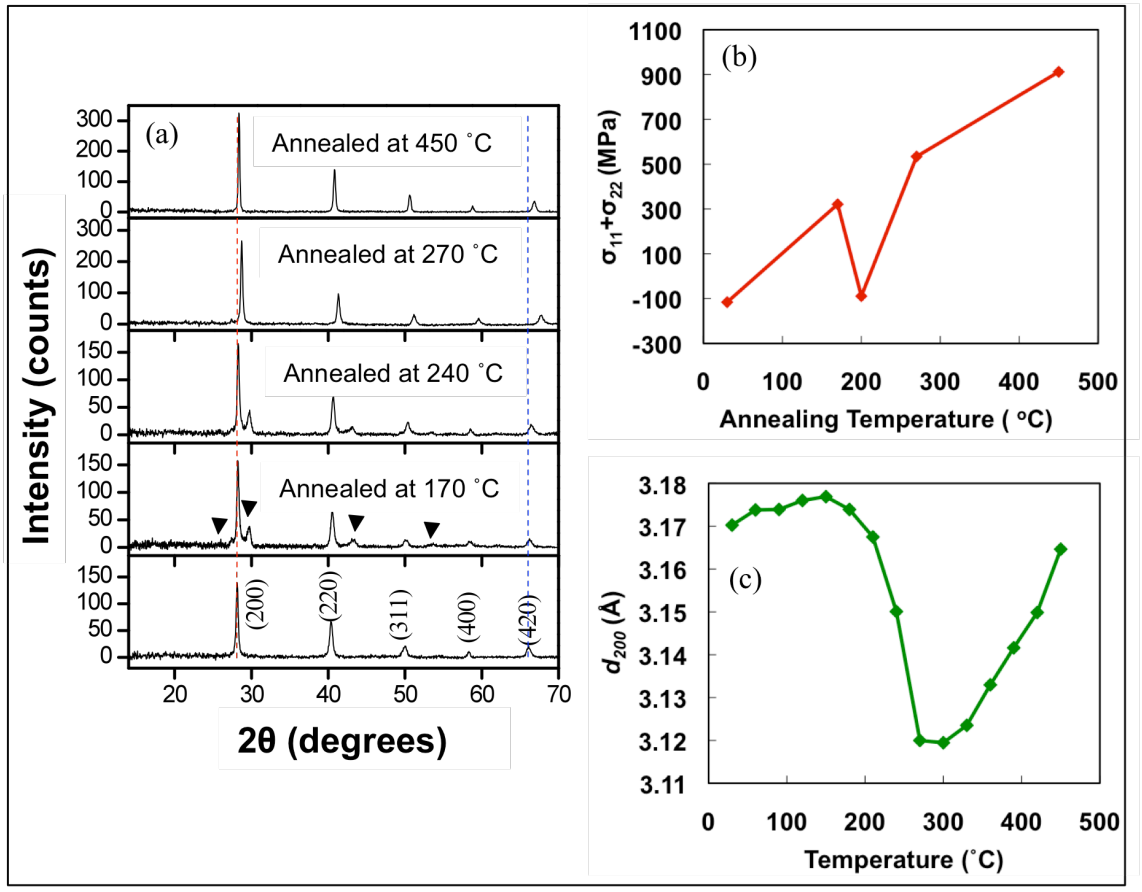

Figure 4.4: (a) Diffraction profiles of GeTe/SnTe samples annealed at various temperatures, (b) Annealing temperature dependence of in-plane residual stress, (c) Variation of d_{200} with temperature

It is observed that the change in d_{420} at 270 ˚C is approximately 2%, however the out of plane strain, which is given by $\varepsilon_{33} = \frac{-\nu}{E}(\sigma_{11} + \sigma_{22})$, accounts for only 0.25% of it. The remainder may be attributed to the change in composition of the SnTe layer during annealing above 200 ˚C.

Again, in order to obtain insight into the phase transition, the variation of d_{200} with temperature is examined as shown in Fig. 4.4(c). The observed behavior can be distinguished into two stages: (i) The first stage occurs from 170 ˚C to 210 ˚C, in which there is a gradual decrease in d_{200}.

(ii) In the second stage, which occurs from 210 ˚C to 400 ˚C, there is at first a sharp decrease and then an increase in d_{200}. From the diffraction profiles it is seen that the first stage corresponds to the crystallization of the GeTe phase. In the second stage, the (200) peak of GeTe first shifts to smaller 2θ and then merges into the (200) peak of SnTe, followed by a remarkable increase in the breadth of (200) SnTe, signifying the formation of a solid solution. Previously, it has been reported that GeTe has a face-centered rhombohedral structure, whereas SnTe has a cubic rocksalt structure [4]. These two structurally different constituents can form solid solutions of $Ge_xSn_{1-x}Te$ in a continuous phase transformation from rhombohedral to cubic configuration.

4.4 Examination of Phase Transition using Time-resolved XRD

In this study, phase transition in response to application of heat, which involves examining structural changes with temperature variation in bilayers of GeTe/SnSe is explored. Also, as discussed in the previous section, sublimation issues have been encountered in studies on residual stress analysis of Ge_2Se_3/SnTe bilayers. In order to preclude such a possibility, in the present study, phase transition in this stack is analyzed using Al_2O_3 as a capping layer. Time-resolved XRD experiments are employed for these investigations.

4.4.1 Time-resolved XRD using Synchrotron Radiation

Time-resolved XRD is carried out at the National Synchrotron Light Source (NSLS) at Brookhaven National Laboratory, NY, in order to examine in-situ crystallization of bilayers during thermal annealing. Synchrotron radiation is used for this purpose. This is the radiation emitted by electrons moving with nearly $9/10^{th}$ of the velocity of light, constrained to move in a curved path. An electron gun is used to send bunches of electrons circulating around an electron storage ring (in the shape of a polygon) which is at vacuum. As the electrons round each bend in the ring, guided by bending magnets, they give off energy in the form of synchrotron light. Several factors give synchrotron radiation an advantage over tube sources for XRD. The intensity of X-rays delivered to a sample is

far greater than that of other sources, and the synchrotron radiation can be tuned to the most advantageous X-ray wavelength [1]. The relativistic character of the synchrotron radiation process confines radiation to directions very close to the plane of electron orbit and the resulting divergence of the X-ray beam is very small. Therefore this source of very high flux X-rays has an even higher brightness (intensity per unit area of source) and spectral brightness (intensity per unit area per unit solid angle per unit energy bandwidth) [1]. Synchrotron light from the NSLS is composed of a range of wavelengths, including X-rays, UV, visible wavelengths and infrared light.

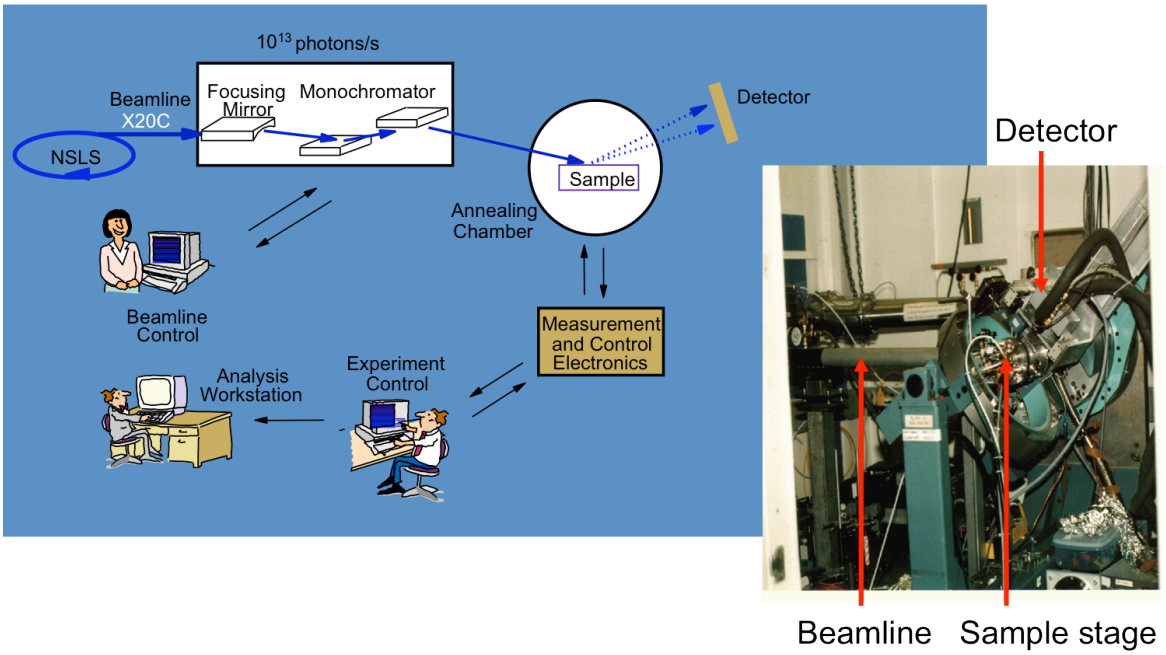

Figure 4.5: Block diagram of beamline X20C at NSLS [21]

The NSLS operates two electron storage rings viz. the X-ray Ring and the Vacuum Ultra Violet Ring. The X-ray Ring is used for the purpose of this study. This ring is split in several beamlines (at the corners of the polygon). At the end of each beamline is an experimental station where equipment directs and focuses the synchrotron light and where experiments are conducted. When light is delivered from the storage ring, it consists of several wavelengths. Special mirrors, lenses and filters are used to select specific wavelengths and to focus the light. The block diagram [21] of such an

experimental station is illustrated in Fig. 4.5. In the context of this research, experiments have been carried out at beamline X20C using an incident beam wavelength of 1.797 Å.

4.4.2 Sample Preparation

Tantalum of 100 nm thickness, which serves the purpose of a bottom electrode, is DC sputter deposited and patterned on oxidized silicon substrate. 100 nm of PECVD Si_xN_y is employed as the inter-level dielectric. Thermal evaporation of Ge-chalcogenide (GeTe or Ge_2Se_3, Alfa Aesar, 99.999% purity) of 30 nm thickness is carried out, followed by 50 nm thick Sn-chalcogenide (SnSe or SnTe, Alfa Aesar, 99.999% purity). The thickness is verified using cross-sectional SEM. Detailed descriptions of Ta, Si_xN_y and Ge-chalcogenide/Sn-chalcogenide depositions are furnished in Chapter 5. Samples of Ge_2Se_3/SnTe bilayers are capped with 10 nm Al_2O_3 by means of atomic layer deposition (ALD). The deposition is performed at a base pressure of 0.28 Torr and at a temperature of 150 ˚C in the presence of 15 sccm of N_2 carrier gas. The precursors used are Trimethylaluminum (TMA) and H_2O. The ALD process has been carried out the IBM, T. J. Watson Research Center, Yorktown Heights, NY.

4.4.3 Experiment

GeTe/SnSe and Ge_2Se_3/SnTe stacks are subjected to time-resolved XRD measurements. For this purpose, the samples are heated at the rate of 1 ˚C/s, under flowing He, to different temperatures using an in-situ heater. The detector employed comprises of a fast linear diode array, which monitors the intensity of the peaks over a 2θ range of ±7˚ [3]. Some samples are also subjected to θ - 2θ scans over a 2θ range of 20˚ – 60˚ before or after a specified temperature ramp to obtain XRD peak profiles.

4.4.4 Results and Discussion

Results pertaining to GeTe/SnSe and Ge_2Se_3/SnTe are discussed separately in the following sections.

4.4.3.1 GeTe/SnSe

In the as-deposited state, the bottom GeTe layer is amorphous and only orthorhombic SnSe (PDF# 481224 [15]) is observed as is evidenced from Fig. 4.6.

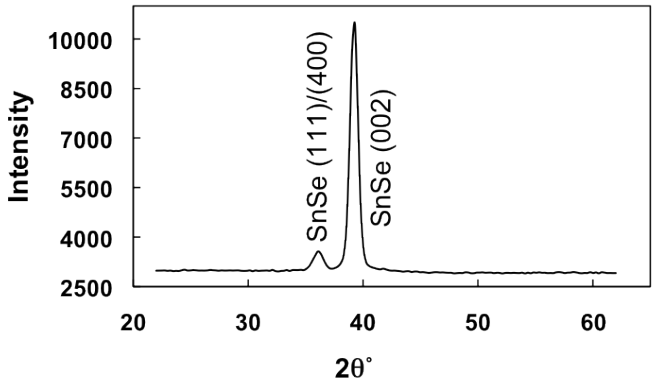

Figure 4.6: XRD profile of as-deposited GeTe/SnSe

The exceedingly intense peak at $2\theta = 39.18^{\circ}$ corresponds to (002) Ta (PDF# 891545 [15]) indicating that the bottom electrode material is highly textured.

Figure 4.7(a) shows the intensity of the XRD peaks as a function of temperature during heating to 230 ˚C with the detector centered at $2\theta = 37^{\circ}$ and (b) during heating to 270 ˚C with the detector centered at $2\theta = 50^{\circ}$.

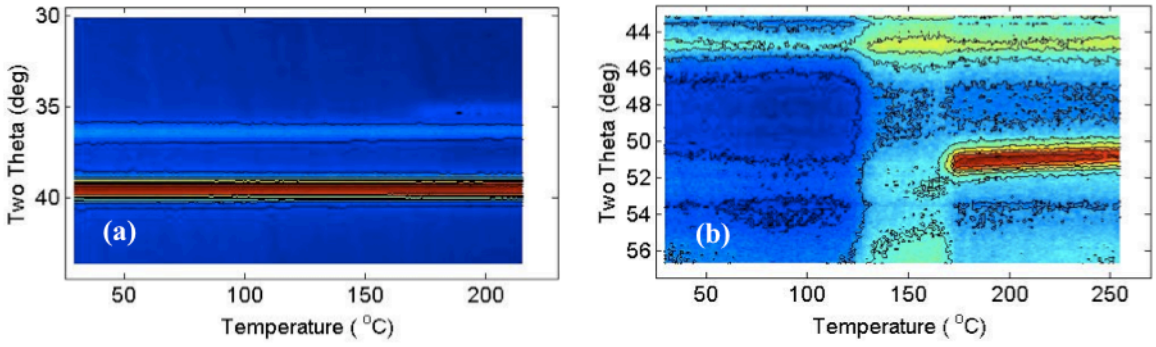

Figure 4.7: Peak intensity variation with temperature when sample is heated to, (a) 230 ˚C, and detector centered at $2\theta = 37^{\circ}$, (b) 270 ˚C, and detector centered at $2\theta = 50^{\circ}$

At 170 ˚C, the onset of a new phase is discerned at $2\theta = 35.14^{\circ}$ and $2\theta = 51.69^{\circ}$. These peaks match rhombohedral low temperature phase of GeTe corresponding to PDF# 471079 [15]. The crystallization temperature $T_x = 170$ ˚C is in agreement with that found in literature [3, 6].

A sample heated to 350 ˚C is illustrated in Fig. 4.8(a). A noticeable shift in the position of the GeTe peak at $2\theta = 35.14^{\circ}$ is observed at 290 ˚C.

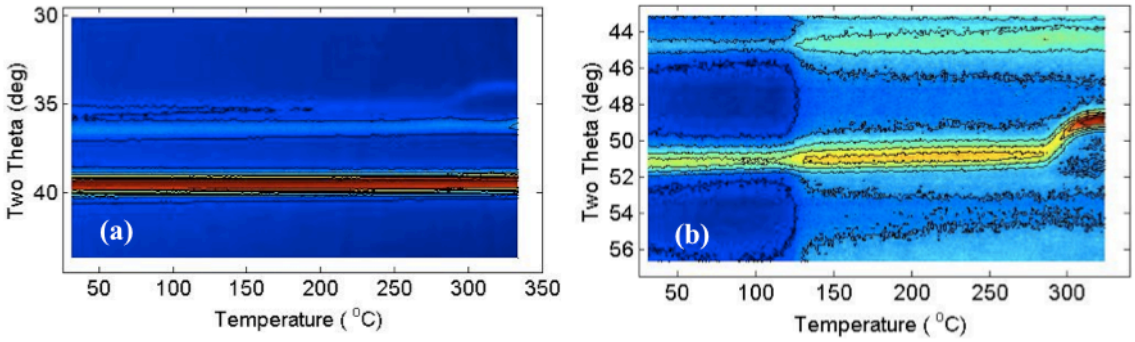

Figure 4.8: Peak intensity variation with temperature when sample is heated to, (a) 350 ˚C, and detector centered at $2\theta = 37^{\circ}$, (b) 340 ˚C, and detector centered at $2\theta = 50^{\circ}$. In both cases GeTe peaks exist at room temperature because the samples were previously heated above 170 ˚C

A similar change is detected at 300 ˚C for the peak at $2\theta = 51.69^{\circ}$ for the sample heated to 340 ˚C shown in Fig. 4.8(b). This is indicative of a structural phase transition. On heating, GeTe undergoes a transformation from rhombohedral symmetry (R3m) to rocksalt cubic symmetry (Fm3m). The transition temperature, T_c, has been determined by various investigators as 350 ˚C, 400 ˚C, 427 ˚C, 430 ˚C, 432 ˚C [3-5]. When Ge atoms are partially replaced by atoms of elemental analogs such as Sn or Pb, T_c decreases [4, 22]. It has been found that in GeTe-SnTe solid solution, increasing SnTe content inhibits the thermal stability of the rhombohedral phase with T_c reducing to room temperature at 68 mole % SnTe [4].

The driving mechanism of the phase transition in GeTe is the softening of the zone-centre transverse optic phonon mode, which causes a relative shift in the anion and cation sublattices [5]. To

form a rock-salt structured lattice, the ratio of the effective cation to anion radii should be greater than the equivalent of the Hume-Rothery 0.41, which as argued by Bierly *et al*. [4], is stimulated by an increase in temperature, which increases the effective size of Ge more rapidly than Te due to the former being lighter than the latter. On substitution of Sn, the temperature necessary to produce the required ratio of radii would be lowered since Sn cation $\left(r_{Sn^{2-}} = 1.02 \text{ Å } [22]\right)$ is larger than Ge cation $\left(r_{Ge^{2+}} = 0.65 \text{ Å } [22]\right)$.

As discussed in the section 4.3.3.2, migration of Sn to the GeTe layer during heat treatments has been observed in GeTe/SnTe bilayers. In addition, switching behavior in PCM devices employing stacks of Ge-chalcogenide and Sn-chalcogenide has been attributed to Sn migration to the Ge-chalcogenide layer [2]. Thus, in the sample under investigation, the Sn can be supplied by the top SnSe layer of the stack resulting in the formation of $Ge_{1-x}Sn_xTe$ solid solution. The addition of Sn facilitates the lowering of the temperature of the rhombohedral to cubic transition to 290 ˚C – 300 ˚C, and a substantial shift in lattice constant. Thus, beyond 300 ˚C, the (202) rhombohedral peak at $2\theta = 35.14^\circ$ becomes the (200) cubic peak at $2\theta = 33.95^\circ$ and the (220) rhombohedral peak at $2\theta = 51.69^\circ$ becomes the (220) cubic peak at $2\theta = 49.49^\circ$.

4.4.3.2 Ge_2Se_3/SnTe

As discussed in section 4.3.4.1, in an attempt to examine the crystallization of GeSe and $GeSe_2$, bilayers of Ge_2Se_3/SnTe are capped with 10 nm Al_2O_3. When this sample is annealed to 350 ˚C, several peaks are ascertained in the profile shown in Fig. 4.9(a). Peaks at $2\theta = 36.12^\circ$, $2\theta = 43.9^\circ$ and $2\theta \approx 58^\circ$ can all be indexed to SnSe (PDF# 530527 [15]) signifying the migration of Sn from top SnTe layer to the bottom Ge_2Se_3 layer. The peaks at $2\theta = 29.65^\circ$ and $2\theta = 32.14^\circ$ correspond to $GeSe_2$ (PDF# 421104 [15]) while the peak at $2\theta = 30.14^\circ$ is attributed to GeSe (PDF# 731802 [15]). Thus, the Ge_2Se_3 specimen crystallizes into two phases viz. orthorhombic GeSe and monoclinic $GeSe_2$. These findings are in agreement with the fact that Ge_2Se_3 is an alloy equivalent to

$(GeSe)_{0.33}(GeSe_2)_{0.67}$ [9]. The crystallization onset (T_x) for the Ge_2Se_3 under investigation is found to be between 300 ˚C and 350 ˚C and is lower than the bulk T_x of 450 ˚C [9]. It has been reported that when Sn atoms are incorporated in a Ge-Se system, the tetravalent Sn combines only with Se [20]. As discussed previously, Sn is bigger than Ge. Also the Sn-Se bond has a larger ionicity than the Ge-Se bond. This causes lack of flexibility of the bond angle between Se and Sn atoms and thus, addition of Sn introduces a strain in the network structure, which gets reflected as a decrease in T_x [20].

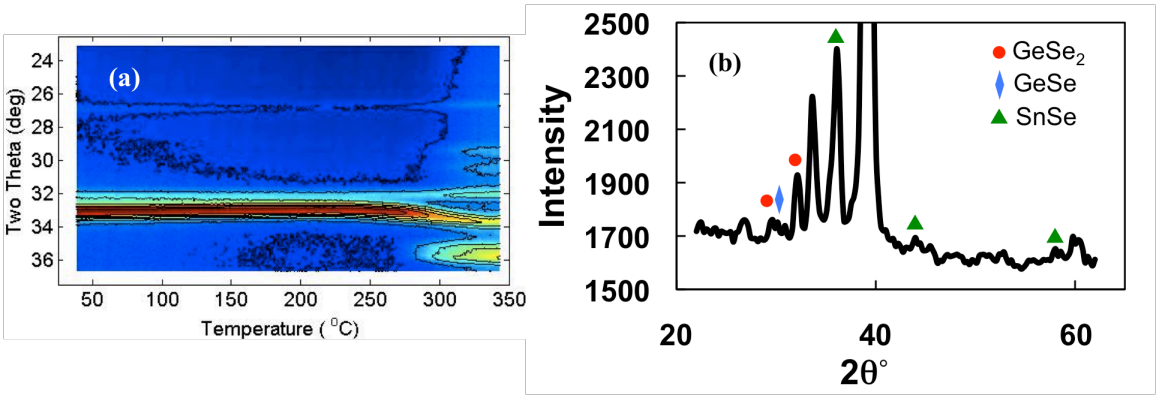

Figure 4.9: (a) Peak intensity variation with temperature for sample heated to 350 ˚C and detector centered at $2\theta = 30^{\circ}$, (b) Zoomed in XRD profile of sample after ramp to show detail

When a Ge_2Se_3/SnTe sample is heated to 450 ˚C, several existing peaks vanish. Fig. 4.10(a) shows that the GeSe and $GeSe_2$ phases have dissolved while the (200) SnTe peak has become visibly weaker and the (220) and (222) peaks have disappeared. In a $GeSe_2$-SnTe system, the existence of at least two intermediate phases has been reported as a result of complex physico-chemical interactions [23], and this may be responsible for the peak disappearances. On the other hand, the $GeSe_2$-SnSe system shows neither the existence of solid solutions nor any intermediate compounds [24].

Figure 4.10(b) illustrates the XRD profile of the sample after ramp, at room temperature. Two new peaks are determined in this profile. The peak at $2\theta = 36.22^{\circ}$ which appears at ~320 ˚C and

grows strongly at ~400 ˚C corresponds to SnSe. The peak at $2\theta = 37.44^{\circ}$ at ~440 ˚C may correspond to a metallic Sn peak.

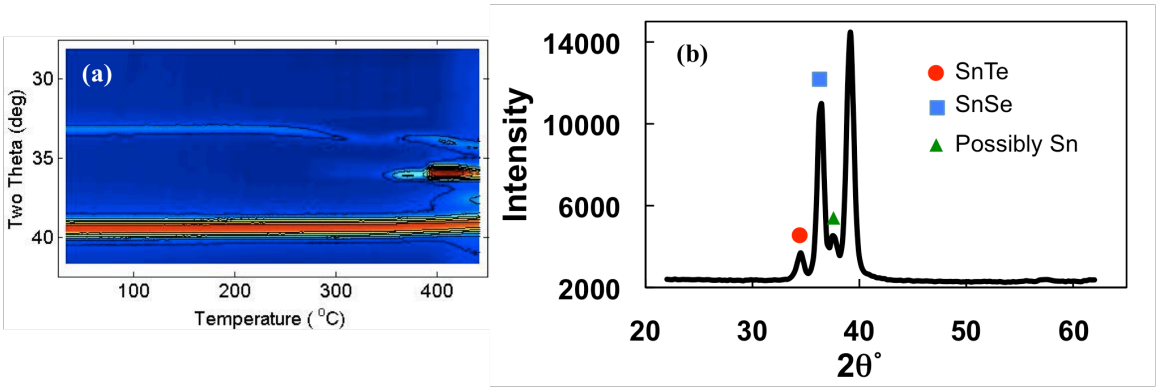

Figure 4.10: (a) Peak intensity variation with temperature for sample heated to 450 ˚C and detector centered at $2\theta = 35^{\circ}$, (b) XRD profile of sample after ramp

In order to investigate the origin of this peak TEM and PEELS analysis is performed and is discussed in the following sections.

4.5 Investigation of Material Inter-diffusion via Time-resolved XRD, TEM and PEELS

In this study, material inter-diffusion in response to heat treatments and corresponding phase transitions in bilayers of GeTe/SnSe are examined. The efficacy of Al_2O_3 as a capping layer to counter potential film volatilization issues is also investigated. Prior to discussion of the results, a brief introduction to the PEELS technique is provided in following sub-section.

4.5.1 Overview of PEELS Technique

While performing a TEM analysis, it is possible to measure the energy loss due to scattering within the material. Various scattering mechanisms contribute to this energy loss. One of the mechanisms involves a transmitting electron scattering off an inner-shell electron within the atom. The resulting

energy loss due to collision is a direct measure of the energies of the outer shells of the atom, including those of the bonding orbitals. This information is a valuable tool for determining the nature of the elemental species with which the electron has scattered, and also for discerning the nature of the bonding that the element possesses with the other atoms. In this technique, a very fine beam of electrons, of the order of 2 Å in diameter, is incident upon the sample. A position dependent analysis can be accomplished by varying the scan direction of the beam. Ineleastically scattered electrons are passed through an energy analyzer, which separates the electrons having different energy in spatial positions. When electrons having different energies are collected in parallel, it is called Parallel Electron Energy Loss Spectroscopy. A scanning-transmission electron microscope (STEM) is illustrated in Fig. 4.11.

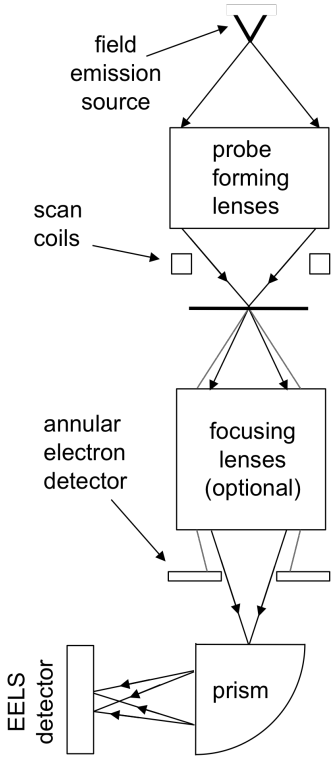

Figure 4.11: Scanning-transmission electron microscope system [25]

In this system, a field-emission source and strong electromagnetic lenses are used to form a small probe that can be raster-scanned across the specimen. A dark-field image, representing transmitted electrons scattered through relatively large angles, is formed by feeding the signal from a ring-shaped (annular) detector to a display device scanned in synchronism with the probe scan. Electrons scattered through smaller angles enter a single-prism spectrometer, which produces an energy-loss spectrum for a given position of the probe on the specimen. Inserting a slit in the spectrum plane then gives an energy-filtered image, obtained this time in serial mode. Alternatively, the whole spectrum is read out at each probe position (pixel), resulting in a large spectrum-image data set that can be processed off-line. A comprehensive review of the EELS technique is furnished in [25].

PEELS studies are carried out by employing a Hitachi HD-2300A STEM fitted with a Gatan Enfina PEELS Spectrometer at Micron Technology's Manassas, VA facility.

For the purpose of this research, PEELS line and area scans have been utilized in order to obtain information about the various elements present either at a particular point or in a given area of the sample.

4.5.2 Sample Preparation

Samples are created using exactly the same method as that described in section 4.4.2. Only bilayers of GeTe/SnSe are prepared. In the following sub-sections, samples with no Al_2O_3 capping are referred to as 'uncapped' samples while those with Al_2O_3 capping are referred to as 'capped' samples.

4.5.3 Experiment

For different annealing temperatures, the bilayer is first examined using time-resolved XRD as discussed in section 4.4.3. Next, temperature induced material inter-diffusion is investigated by employing TEM and PEELS on samples prepared by focused ion beam technique. A TEM fitted with a PEELS spectrometer is used to provide a probe diameter of 4–5 Å, a probe current of ~150 pA, a convergence semi- angle of 10.6 mrad, and a PEELS acceptance semiangle of 21.8 mrad. An energy

resolution ~1 eV is achieved by setting the spectroscope dispersion to 0.5 eV per channel with a total of 1340 parallel channels.

4.5.4 Results and Discussion

The as-deposited sample exhibits amorphous GeTe, orthorhombic SnSe (PDF# 481224 [15]) and the (002) peak of the highly textured Ta (PDF# 891545 [15]) bottom electrode as previously illustrated in Fig. 4.6. Clearly defined GeTe and SnSe layers are distinguished from the PEELS line scan shown in Fig. 4.12.

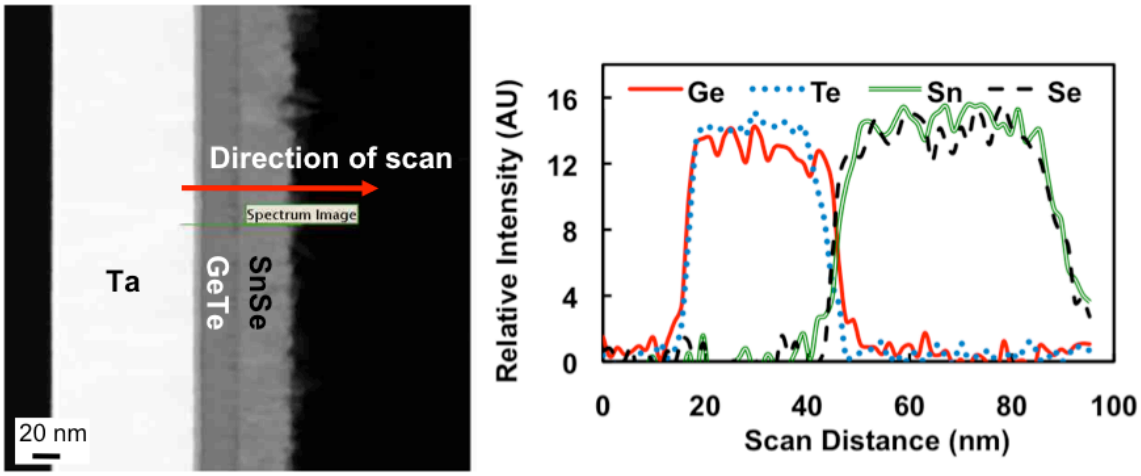

Figure 4.12: PEELS scan on as-deposited GeTe/SnSe sample

When an uncapped sample is annealed to 340 ˚C, GeTe crystallizes into its low temperature rhombohedral phase at 170 ˚C. The time-resolved XRD results discussed in the previous section have demonstrated a reduction in the GeTe rhombohedral to cubic transition temperature to 300˚C. This has been attributed to incorporation of Sn from the top SnSe layer. In this study, direct visual evidence of Sn inter-diffusion is provided via PEELS area scan illustrated in Fig. 4.13(a). It is ascertained that Ge and Sn cations are most mobile. Since GeTe starts out as amorphous, it contains homopolar Ge-Ge bonds [2, 26], which are known to be thermodynamically unstable [9] and break

easily, thus allowing diffusion of Ge into the SnSe layer. The Ge diffusion mechanism is presumably vacancy driven since SnSe is a p-type semiconductor [27] and it has been reported that Ge diffuses predominantly via cation vacancies in chalcogen rich lead and tin chalcogenides [28, 29]. In crystalline GeTe, the most energetically favorable intrinsic defect is the Ge vacancy due to its very low energy of formation [30]. The Sn ions are observed to diffuse into the bottom layer by means of occupation of these substitutional sites resulting in the formation of a $Ge_xSn_{1-x}Te$ solid solution, which de-stabilizes the rhombohedral phase causing the peak shift from $2\theta = 51.69^{\circ}$ to $2\theta = 49.49^{\circ}$ as seen in Fig. 4.13(b).

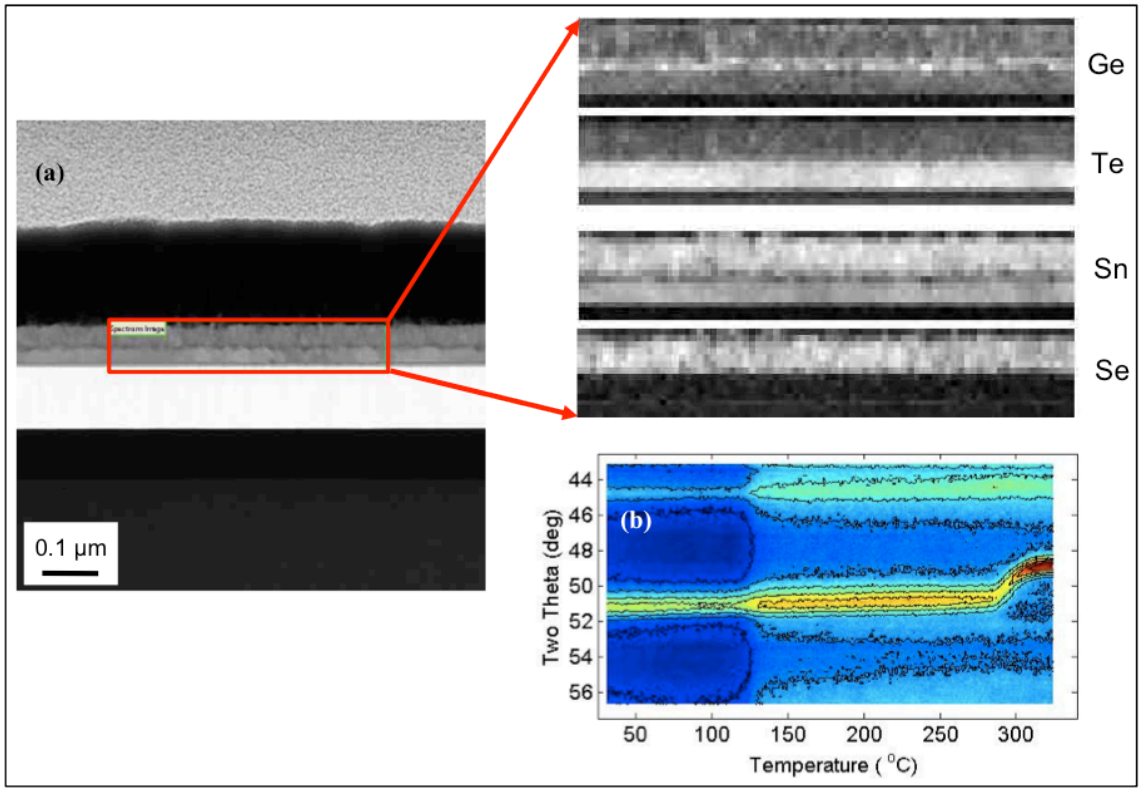

Figure 4.13: GeTe/SnSe sample without Al_2O_3 capping, annealed to 340 ˚C, (a) PEELS area scan, (b) Peak intensity variation with temperature, when detector is centered at $2\theta = 50^{\circ}$, showing rhombohedral to cubic transition. GeTe peaks exist at room temperature because the sample was previously heated above 170 ˚C

Evidence of Te and Se diffusion is clearly discerned in the PEELS area scan of an uncapped sample annealed to 550 ˚C (Fig. 4.14(a)). P-type chalcogenides have a low concentration of anion vacancies. Previous studies have shown that the diffusion of Se and Te in lead chalcogenide and tin telluride is a strong function of the concentration of excess anions in the crystal [31, 32]. Hence, despite the large ionic radii of these anions ($r_{Se^{2-}} = 1.96\text{Å}, r_{Te^{2-}} = 2.11\text{Å}$), they are reported to exhibit an interstitial diffusion mechanism.

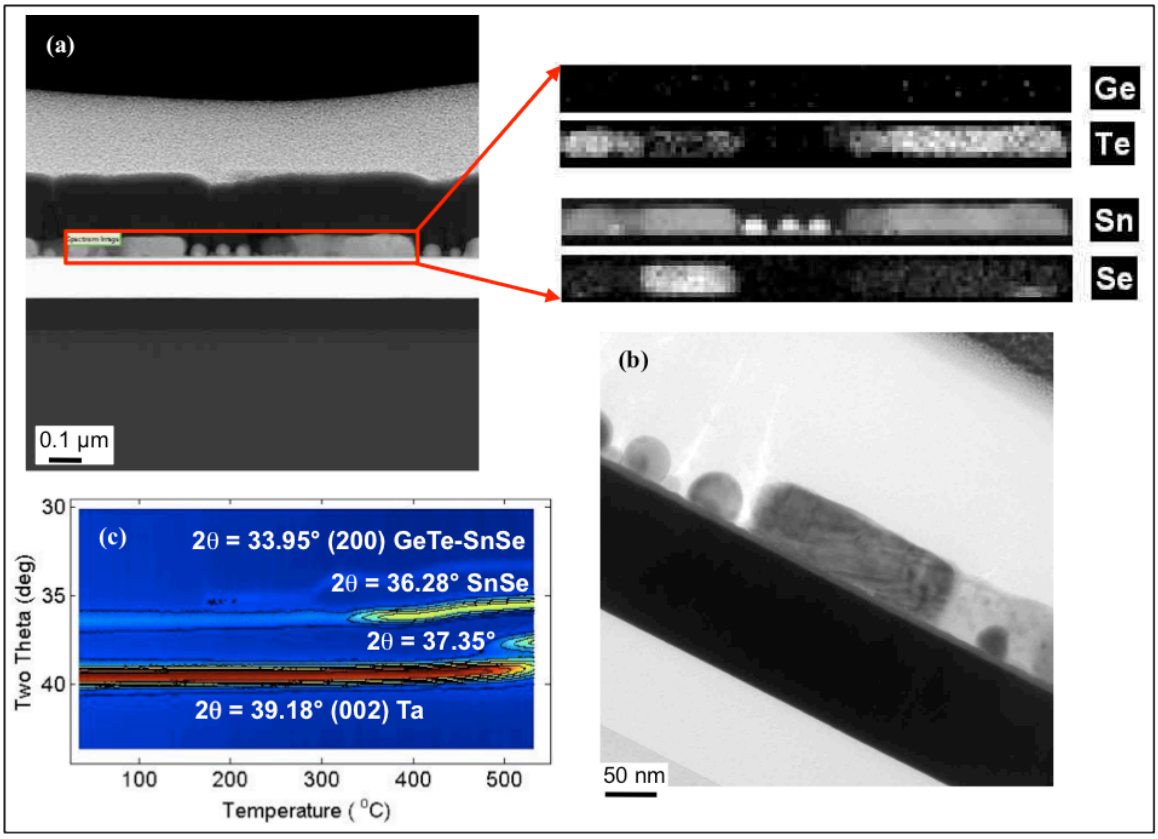

Figure 4.14: GeTe/SnSe sample without Al_2O_3 capping, annealed to 550 ˚C, (a) PEELS area scan, (b) TEM image, (c) Peak intensity variation with temperature, when is detector centered at $2\theta = 37^{\circ}$

At 550 ˚C, the TEM image in shown in Fig. 4.14(b), reveals severe decomposition of the film. It is seen that the bilayer begins to volatilize below the melting temperatures of the individual layers. Se vaporizes noticeably and regions where the film has balled up can be mapped directly to the Sn

clusters detected via PEELS. The appearance of the peak at $2\theta = 37.35^{\circ}$ at 500 ˚C in Fig. 4.14(c) represents the separation of the metallic Sn phase (PDF# 650297 [15]). This is evidence of incongruent SnSe sublimation. On annealing an uncapped sample of a single layer SnSe of thickness 76.5 nm to 700 ˚C, it is observed that, the SnSe peaks disappear after 620 ˚C. The resulting XRD profile reveals the presence of only tetragonal Sn (PDF# 650297 [15]) and the corresponding PEELS spectrum exhibits only the Sn-M edge. By employing the Knudsen cell – mass spectrometry methods [33, 34], it has been reported that the composition of the vapor phase of SnSe does not match that of the crystal. The vapor above solid SnSe has been found to be predominantly comprising of SnSe, Se_2, $SnSe_2$ and Sn_2Se_2 molecules indicating that the vapor is enriched in Se as compared to solid SnSe [34].

Fig. 4.14(a) exhibits significant vaporization of Ge and that of Te to a lesser degree. There have been conflicting reports in literature as to whether GeTe sublimes congruently or incongruently [35, 36]. For the sample under investigation, no separation of Ge or Te phases have been distinguished in the post-anneal XRD profile. For a single layer, uncapped GeTe film annealed to 600 ˚C, it is seen that, GeTe peaks disappear after 520 ˚C. The post-anneal XRD profile is devoid of any peaks and the corresponding PEELS spectrum is characterized by the absence of Te-M and Ge-L edges indicating that both Ge and Te have volatilized.

The SnSe peak at $2\theta = 36.28^{\circ}$ grows very strongly at ~340 ˚C. This is not a consequence of material inter-diffusion since a similar increase in intensity is also observed for a single layer SnSe film when subjected to heat treatments.

When an Al_2O_3 capped sample is annealed to 600˚C, it is observed that the degree of thermal decomposition of the bilayer is reduced as illustrated in the TEM image in Fig. 4.15(a). Several regions are detected where the integrity of the film is maintained. A PEELS line scan, as shown in Fig. 4.15(b), along such a region, reveals a uniform distribution of Te, Sn and Ge. The oxygen ‘peak’ detected below a depth of 20 nm indicates oxidation of Ta. Hence the ~8 nm interfacial layer perceived between Ta and GeTe, in the TEM image, can be attributed to Ta_xO_y.

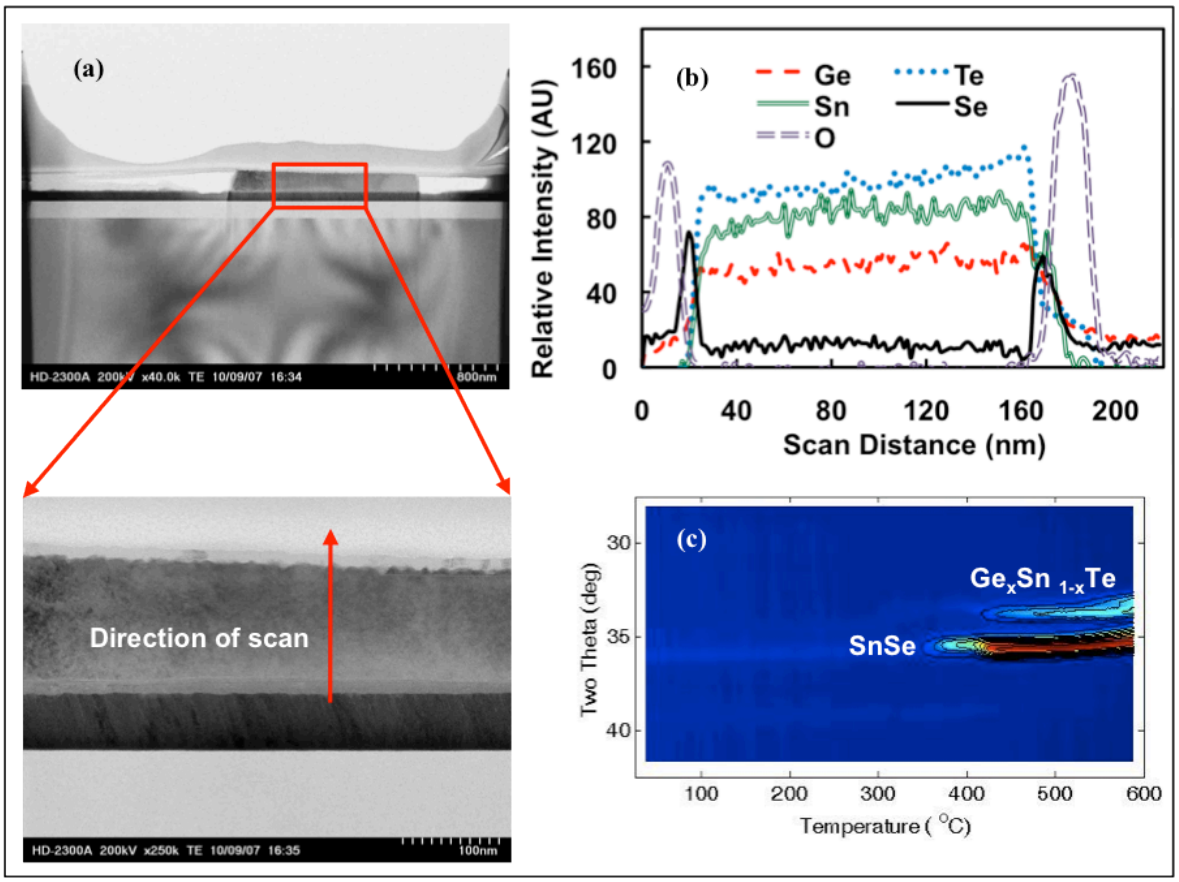

Figure 4.15: GeTe/SnSe sample capped with Al_2O_3, annealed to 600 ˚C, (a) TEM image, (b) PEELS line scan, (c) Peak intensity variation with temperature, when detector is centered at $2\theta = 35^{\circ}$

From Fig. 4.15(b) it appears that Se has preferentially segregated to the oxide interfaces. The inference drawn from this observation can be misleading. Se is highly susceptible to segregation to grain boundaries and free surfaces [37]. However, the low level of Se within the bilayer is an indication of volatilization, which may occur from neighboring areas that is not captured in the line scan or from along the width of the sample where no capping is present.

From the post-anneal XRD profile of the capped sample, shown in Fig. 4.15(c), it is seen that separation of the Sn phase does not occur presumably because the presence of Al_2O_3 inhibits the degree of volatilization of Te and Se. As such, Fig. 4.15(c) exhibits only the orthorhombic SnSe peak at $2\theta = 35.89^{\circ}$ and the cubic $Ge_xSn_{1-x}Te$ peak at $2\theta = 33.88^{\circ}$.

An increase in the intensity of the peak at $2\theta = 33.88^{\circ}$ is observed at ~ 420 ˚C. This does not represent the separation of the SnTe phase, which also has a cubic peak at the same location. This is because the Ge-Sn-Te system forms a continuous series of solid solutions [4]. A similar observation is not made in the case of the uncapped sample due to an enhanced level of sublimation of Ge and Te and the separation of the Sn phase.

4.6 Summary of Results

The major findings of the various material characterization experiments discussed in this chapter are tabulated as shown below.

Table 4.3: Summary of Results

Stack	Observations and Results
GeTe/SnTe	• in the as-deposited state, GeTe is amorphous and SnTe has a cubic crystalline structure • at 170 ˚C GeTe crystallizes into a rhombohedral phase • at higher temperatures, migration of Sn from top to bottom layer results in the formation of a $Ge_xSn_{1-x}Te$ solid solution resulting in a rhombohedral to cubic structural transition
Ge_2Se_3/SnTe	• in the as-deposited state, Ge_2Se_3 is amorphous and SnTe has a cubic crystalline structure • after heating to 270 ˚C, separation of the orthorhombic SnSe phase is observed indicating migrating of Sn from top to bottom layer • no GeSe or $GeSe_2$ peaks are observed due to sublimation of Ge_2Se_3 at high temperatures • on capping with 10 nm Al_2O_3, Ge_2Se_3 begins to crystallize in the 300-350 ˚C range and orthorhombic GeSe and monoclinic $GeSe_2$ peaks appear
GeTe/SnSe	• in the as-deposited state, GeTe is amorphous and SnSe has an orthorhombic structure • at 170 ˚C GeTe crystallizes into a rhombohedral phase • migration of Sn from top to bottom layer results in the formation of a $Ge_xSn_{1-x}Te$ solid solution • at ~300 ˚C a rhombohedral to cubic transition is observed, which is ~100 °C lower than that of pure GeTe due to Ge cations being partially replaced by larger Sn cations • after heating to 550 ˚C, incongruent sublimation of GeTe and SnSe is observed • at ~500 ˚C volatilization of Se results in the separation of the tetragonal Sn phase • after heating to 600 ˚C, sample capped with 10 nm Al_2O_3 exhibits lesser degree of volatilization and no separation of Sn phase

4.7 Resistivity v/s Temperature Measurements of Single Layers

These measurements are performed with an aim to examine the change in resistivity (ρ) of single layer chalcogenides with temperature. The samples are prepared by thermally growing dry oxide of thickness 50 nm on 100 mm (100) Si wafers. GeTe or SnTe or SnSe or Ge_2Se_3 is evaporated on separate substrates using the technique discussed in Chapter 5. ρ versus T measurements are carried at IBM Almaden Research Center, CA, by using a custom-made setup that makes contact with two large Al pads with a small gap. Measurements are performed in a nitrogen atmosphere at a heating rate of 1 °C/s and during subsequent cool down. Due to the high volatility of Ge_2Se_3 meaningful data for this particular film is not obtained.

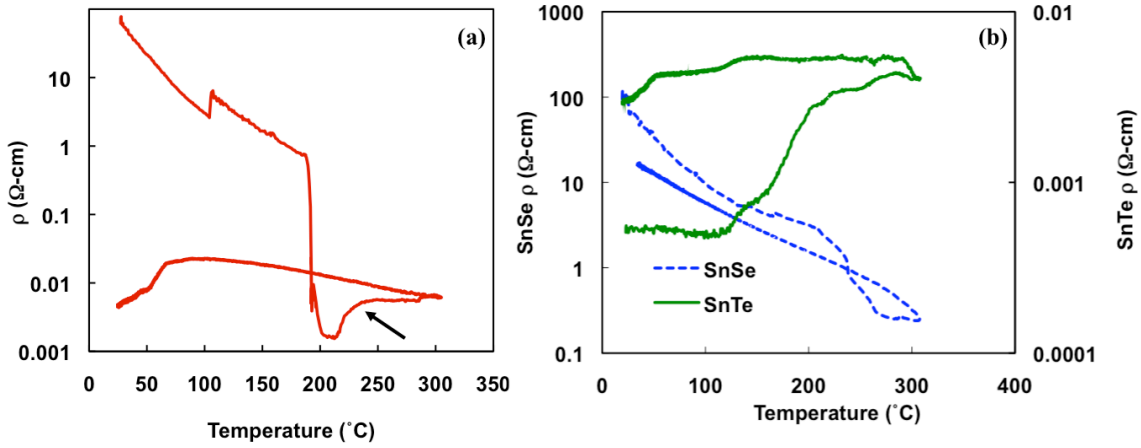

Figure 4.16: Resistivity v/s temperature measurements for (a) GeTe (The arrow represents anomalous behavior possibly due to film evaporation), (b) SnSe and SnTe

4.7.1 GeTe

The ρ versus T measurements for a 45.6 nm thick GeTe film are illustrated in Fig. 4.16(a). It is observed that upon heating the ρ decreases since the conductivity in amorphous (as-deposited state of GeTe) phase change materials can be described by a thermally activated hopping transport [3]. ρ drops very sharply at around 180 ˚C, which corresponds to the crystallization temperature of this

GeTe film. The sharp increase in ρ observed from ~100 ˚C is an artifact due to a change in the value of the measurement resistance. Upon cooling it is observed that the resistivities remain low. The strange loop seen in the high temperature region is attributed to the loss in film due to evaporation.

4.7.2 SnSe

Figure 4.16(b) shows the change in ρ versus T for an SnSe sample of 76.5 nm thickness. This film also shows a continuous decrease in ρ upon annealing till a temperature of about 220 ˚C where a sudden drop in resistivity occurs. On cooling it is seen that the ρ increases. From these observations it may be inferred that both as-deposited (partially crystalline) SnSe and crystalline SnSe exhibit semiconductor like behavior [7]. Again, the strange loop is seen at high temperature, which is attributed to film evaporation.

4.7.3 SnTe

The ρ versus T plot for a 45.9 nm thick SnTe sample is shown in Fig 4.16(b). It is observed that with increase in temperature, the ρ remains practically constant at a low value of approximately 0.55 mΩ-cm. On cooling however, ρ decreases indicating a metallic behavior.

4.8 Conclusions

Extensive material characterization of bilayers employed in the fabrication of PCM devices has been carried out. It is demonstrated that stacked Ge_2Se_3/SnTe and GeTe/SnTe phase change memory films exhibit both structural and compositional dependency with annealing temperature. The outcome of the structural transformation of the bottom layer is an annealing temperature dependent residual stress. By the incorporation of a Sn layer the phase transition characteristics of Ge-chalcogenide thin films can be tuned. Sn ions play a major role in reducing the crystallization temperature (T_c or T_x) of the Ge-chalcogenide layer, and this property can be exploited for low power PCM applications. Clear

evidence of thermally induced Ge, Sn and chalcogen inter-diffusion, has been discerned via TEM and PEELS studies. Severe film decomposition, volatilization and metallic Sn phase separation has been observed at high temperatures (> 500 ˚C) in the absence of Al_2O_3 as a capping layer. The presence of Al_2O_3 has been found to mitigate some of these effects.

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Chapter 5: Two Terminal Phase Change Memory Devices

This chapter describes the design, fabrication and electrical testing of two terminal phase change memory devices. As discussed previously, a typical device employs a bilayer (also referred to as a stack) of germanium chalcogenide and tin chalcogenide. The Ge-Ch layer may be GeTe or Ge_2Se_3 while the Sn-Ch layer may be SnTe or SnSe. Depending upon the materials forming the bilayer, three major device types are fabricated and tested. A fourth bilayer comprising of Ge_2Se_3/SnSe is also fabricated and subjected to preliminary electrical testing.

5.1 Concept

A two terminal PCM cell is devised with the intention of demonstrating single cell memory functionality. The cross-section and top view of the proposed design is illustrated in Fig. 5.1. As can be seen from the figures, bilayers of Sn-Ch (SnTe or SnSe) and Ge-Ch (GeTe or Ge_2Se_3) are sandwiched between tantalum electrodes.

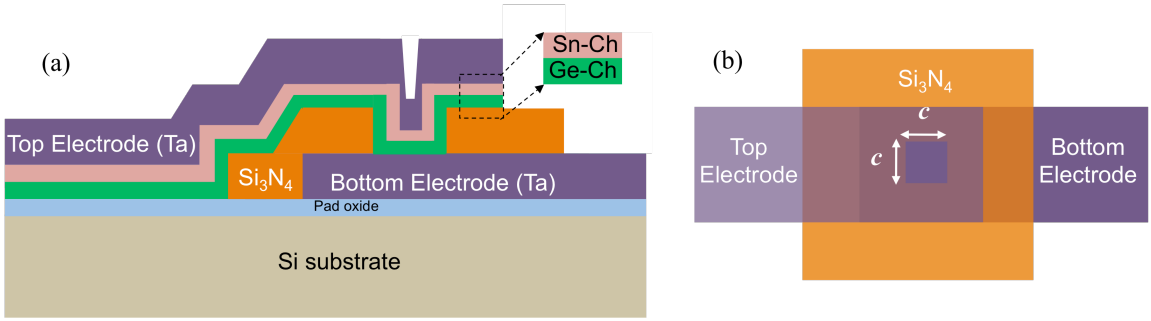


Figure 5.1: Two terminal PCM cell employing bilayers of Ge-Ch and Sn-Ch, (a) Cross-sectional view, (b) Top view illustrating size of contact area is c^2

The ability of Ta to withstand high temperatures, frequently seen in PCM cell operation, makes it an ideal candidate for electrode material. Silicon nitride (Si_3N_4) is the inter-level dielectric. Si_3N_4 is chosen over the commonly used SiO_2 due to the possibility of oxidation of the overlying chalcogenide

material on using the latter. In order to obtain a low stress dielectric, a low temperature plasma enhanced chemical vapor deposition (PECVD) nitride process has been developed. The cross sectional area of the programmable volume is determined by the Si_3N_4 etch step. The proposed design eliminates the need for an additional heater element, as on electrical switching, the resultant material formed, is resistive enough to cause adequate Joule heating. Such a design reduces the number of processing steps. Simplicity of design and ease of fabrication are the hallmarks of the proposed two terminal structure.

5.2 Mask Layout

A layout of the device is created using the IC Station layout editor from Mentor Graphics®. It involves 3 levels of lithography and can be accomplished in less than 20 processing steps. It is comprised of two terminal PCM cells of varying feature sizes and different test structures, such as resistors, serpentines, Vander Pauw structures and comb structures. Fig. 5.2 illustrates selected sections of the layout.

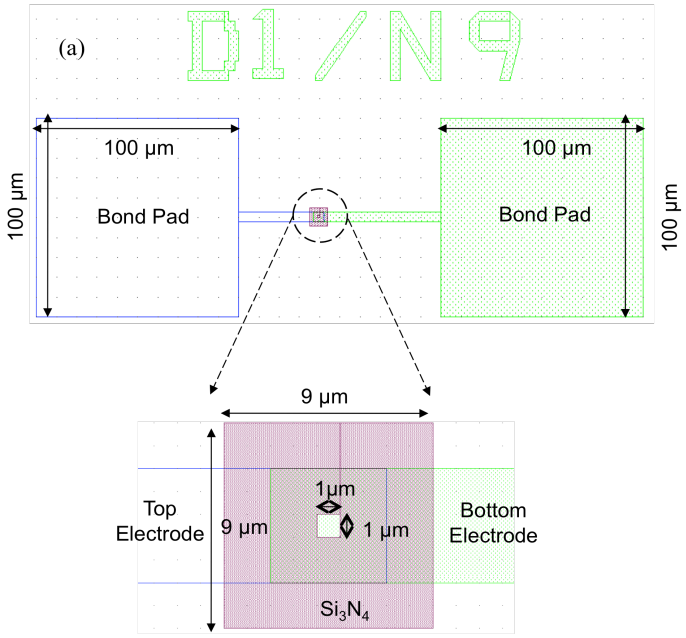


Figure 5.2(a): Top view of a two terminal PCM cell with a programming cross sectional area of 1 μm^2

Fig. 5.2(a) shows the top view of a typical two terminal PCM device with a 1 μm^2 programming cross sectional area (c^2 from figure).

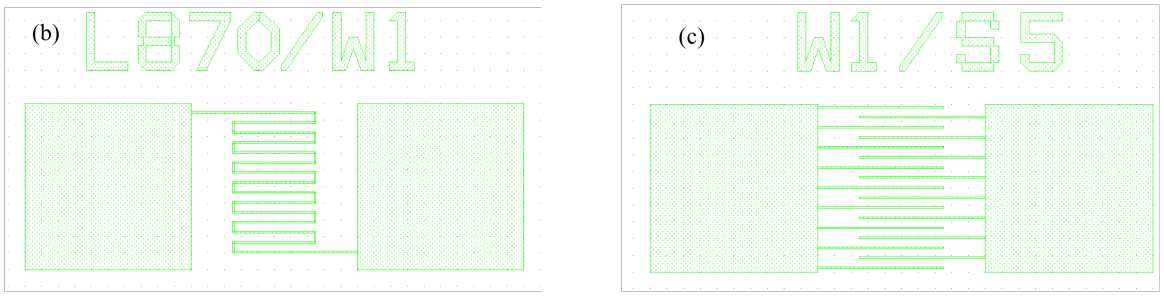


Figure 5.2: (b) Serpentine connected between two bond pads with L = 870 µm and W= 1 µm, (c) Comb structure with 1 µm wide (W) fingers separated by a distance of 5 µm (S) from each other

The serpentines/resistors illustrated in Fig. 5.2 (b) have been designed with a view to investigate the resistance of the bottom electrode and chalcogenide/top electrode stack for various lengths (L) and widths (W). The comb structure shown in Fig. 5(c) is suitable for evaluating the efficacy (resolution) of the Reactive Ion Etch (RIE) and ion milling techniques used for etching the bottom electrode and chalcogenide/top electrode stack respectively. Once the layout is created, it is converted into a GDSII file format and transferred to the Computer Aided Transcription Software system for fracturing and performing other data manipulations such as rotation etc. and for conversion to e-beam format. The masks are generated using the Perkin Elmer MEBES II electron beam writer.

5.3 Fabrication

The process flow for the two terminal PCM device is summarized in Fig. 5.3. The patterning and etch of the bottom electrode, nitride and top electrode lithography is carried out at the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT. Evaporation of the chalcogenide bilayers and the consequent ion-milling of the top electrode/chalcogenide stack is performed at the Idaho

Microfabrication Laboratory at Boise State University (BSU), ID. The key process steps are highlighted below.

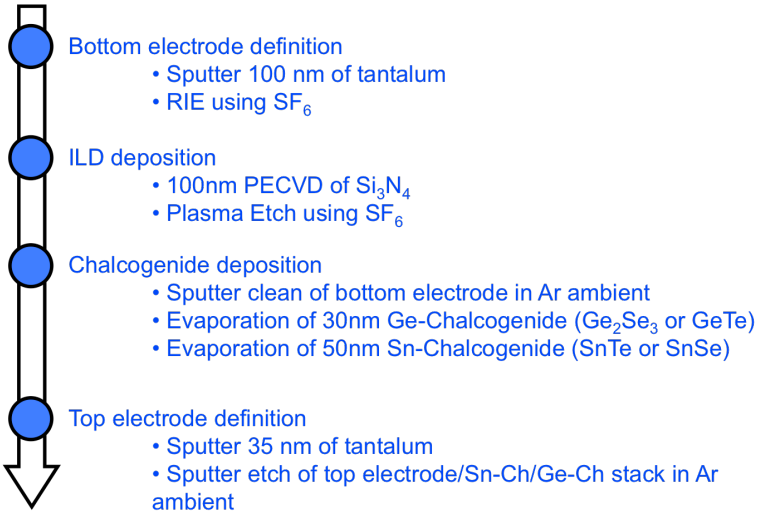


Figure 5.3: Process flow for fabricating two terminal PCM cell

5.3.1 Substrate Preparation

Silicon wafers, 150 mm in diameter are subjected to a 240 s spin/rinse/dry in DI water and nitrogen ambient. Since the surface of the wafer is not a part of the device and is used merely as a substrate, a more sophisticated clean such as an RCA clean may be eschewed. This is followed by a 100 nm dry oxide growth at 1000 ˚C in order to electrically isolate the device from the substrate.

5.3.2 Bottom Electrode Formation

Tantalum, 100 nm thick, which serves as the bottom electrode, is DC sputter deposited by flowing 20 sccm of Ar at a deposition pressure of 5 mTorr and 250 W power. In order to pattern the bottom electrode, first HMDS priming is carried out at 140 ˚C for 60 s to enhance adhesion between the photoresist (PR) and wafer surface. Wafers are spin coated with ~1 µm of OIR 620-10 PR at 3250 RPM for 30 s. This is followed by a soft bake at 90 ˚C for 60 s to drive the solvent out of the spun on resist. Next, wafers are exposed by means of a Canon *i*-line stepper using a dose of

200 mJ/cm^2. Following exposure, the wafers were subjected to a 60 s, 110 ˚C post exposure bake. The resist film is then developed for 48 s in CD-26 developer, rinsed and then hard baked at 120 ˚C for 60 s in order to improve its mechanical robustness. The Ta is subsequently etched by means of RIE via the action of 125 sccm of SF_6 at a power of 125 W and a pressure of 125 mTorr. Residual PR is ashed using O_2 plasma.

5.3.3 Inter-level Dielectric Deposition

As discussed in section 5.1, PECVD Si_xN_y serves as the dielectric between the top and bottom electrodes. Prior to nitride deposition, a de-scum is required in order to remove organic contaminants which may otherwise introduce pinholes in the dielectric. For this purpose, a Piranha clean is carried out by submerging the samples in a heated bath containing a 4:1 mixture of H_2SO_4 and H_2O_2 respectively. Following this, PECVD Si_xN_y of thickness 100 nm is deposited at 400 ˚C, by flowing 130 sccm of SiH_4 and 60 sccm of NH_3 at 4.5 Torr and at a power of 600 W. The Si_xN_y is patterned using a photolithographic process similar to that described in section 5.3.2. Since both Si_xN_y and the underlying Ta can be etched using SF_6, in order to maintain selectivity, a less aggressive (in comparison to RIE), timed plasma etch is performed by flowing 200 sccm of SF_6 at 200 W and 200 mTorr pressure. Residual PR is ashed in O_2 plasma.

5.3.4 Sputter clean

Over a period of time, the exposed Ta surface gets oxidized. Hence, before chalcogenide deposition, it is essential to remove this native oxide layer in order to preserve the integrity of the contact between the chalcogenide and the bottom electrode. For this purpose, sputter clean using an ion mill is carried out. Bombarding the surface of the Ta with argon atoms helps remove the oxide monolayers and exposes a fresh Ta surface, resulting in a clean contact with the chalcogenide. Each sample is subjected to a 6 s sputter clean by placing it at an angle of 45˚ to the incoming beam of 550 eV, 0.3 A current and 500 V supply.

5.3.5 Chalcogenide Evaporation

Ge_2Se_3, SnSe, SnTe and GeTe are thermally evaporated separately in 4 different runs by means of a CHA600 thermal evaporator. The tool uses resistive energy to evaporate thin films and is equipped with a rotating planetary system for uniform deposition [1]. Evaporation is performed using appropriate tooling factor (TF) values. The TF adjusts for the difference in the material deposited on the crystal (thickness) monitor versus the substrate. Four different types of devices (based upon the materials forming the stack) are fabricated. For each type of device, first the 30 nm thick Ge-Ch layer is deposited, followed by a break in vacuum and then the 50 nm thick Sn-Ch layer is evaporated.

Table 5.1: Chalcogenide Material Parameters for Evaporation

Material	Density (g/cm^3)	Z ratio	Tooling Factor
Ge_2Se_3	6	1.0	95%
SnSe	6.18	1.0	86%
SnTe	6.48	1.0	88%
GeTe	6.20	1.0	94%

The material to be deposited is in the form of a coarse powder and is held in an alumina crucible, which is placed inside a tungsten basket to be heated. The material parameters are listed in Table 5.1.

Table 5.2: Chalcogenide Deposition Parameters

Device Type	Run	Initial Crucible Mass (g)	Mass of material (g)	Initial Power (%)	Initial Dwell (min:s)	Max. Power (%)	Max. dep. rate (Å/s)	Dep. time (min:s)	Post dep. crucible mass (g)
1	GeTe	2.2715	0.1252	60	2:00	90	4.8	1:14	2.307
	SnTe	2.798	0.1496	60	2:00	90	2.7	4:56	2.8215
2	GeTe	2.2718	0.1786	60	2:00	90	4.1	1:32	2.3632
	SnSe	2.8421	0.1312	60	2:00	90	2.6	5:31	2.8663
3	Ge_2Se_3	3.0209	0.2102	60	2:00	90	3.8	2:10	3.035
	SnTe	2.7996	0.127	60	2:00	90	2.8	4:33	2.8056
4	Ge_2Se_3	3.021	0.1275	60	2:00	90	5.1	1:40	3.0725
	SnSe	2.8421	0.1373	60	2:00	90	2.5	3:43	2.8761

In Table 5.2, the columns describing the initial power, initial dwell time and maximum power, specify the heating profile of the deposition. At the beginning of the evaporation, the power is quickly

ramped up to 60% and the shutter is kept closed for 2 minutes (referred to as the dwell time). At the end of this dwell time, the power is ramped up to 90% and the shutter is opened so that deposition on the substrate can occur. When the reading on the crystal monitor is equal to the desired thickness value, the deposition is stopped and the shutter is closed.

5.3.6 Top Electrode Formation

DC sputter deposited Ta of 35 nm thickness is used as the top electrode material. Lithography is performed using the same method employed for the bottom electrode. The top electrode and the underlying Sn-Ch/Ge-Ch stack are all ion-milled in the same step via Ar bombardment using the sputter clean technique described previously. The etch is carried out until the sample visually appears clear of metal from undesired locations. Fig. 5.4 shows an optical image of a fabricated two terminal bilayer PCM device.

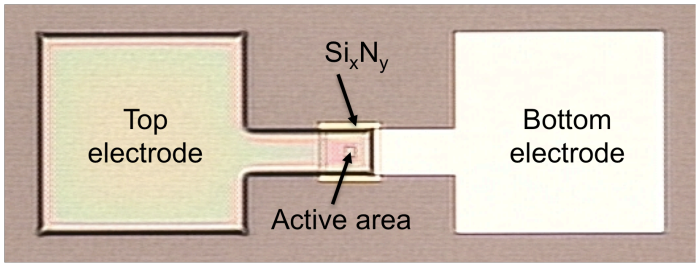


Figure 5.4: Optical image of PCM cell with 5 μm^2 contact area. Active area represents region of chalcogenide between top and bottom electrodes

5.4 Electrical Testing

Only devices with 1 μm^2 contact area are tested due to the inability of larger devices to exhibit switching. Two different types of tests are carried out in order to characterize their electrical behavior. They are as described in the ensuing sections.

5.4.1 Determination of *I-V* Characteristics

In this test, the two terminal cell under consideration is subjected to a DC current sweep using an HP 4145 Parameter Analyzer. The bottom electrode is grounded and current is forced through the top electrode. The chosen range of current is stack specific. For devices with SnTe as the top stack, the current is varied from 0 to 100 µA in steps of 0.25 µA, using short integration time, while for devices employing SnSe as the top stack, the current is swept from 0 to 1 mA (for RESET state) (or 500 µA for SET state) in steps of 10 µA, again using short integration time. Representative *I-V* characteristics for the four different types of devices are illustrated in Fig. 5.5.

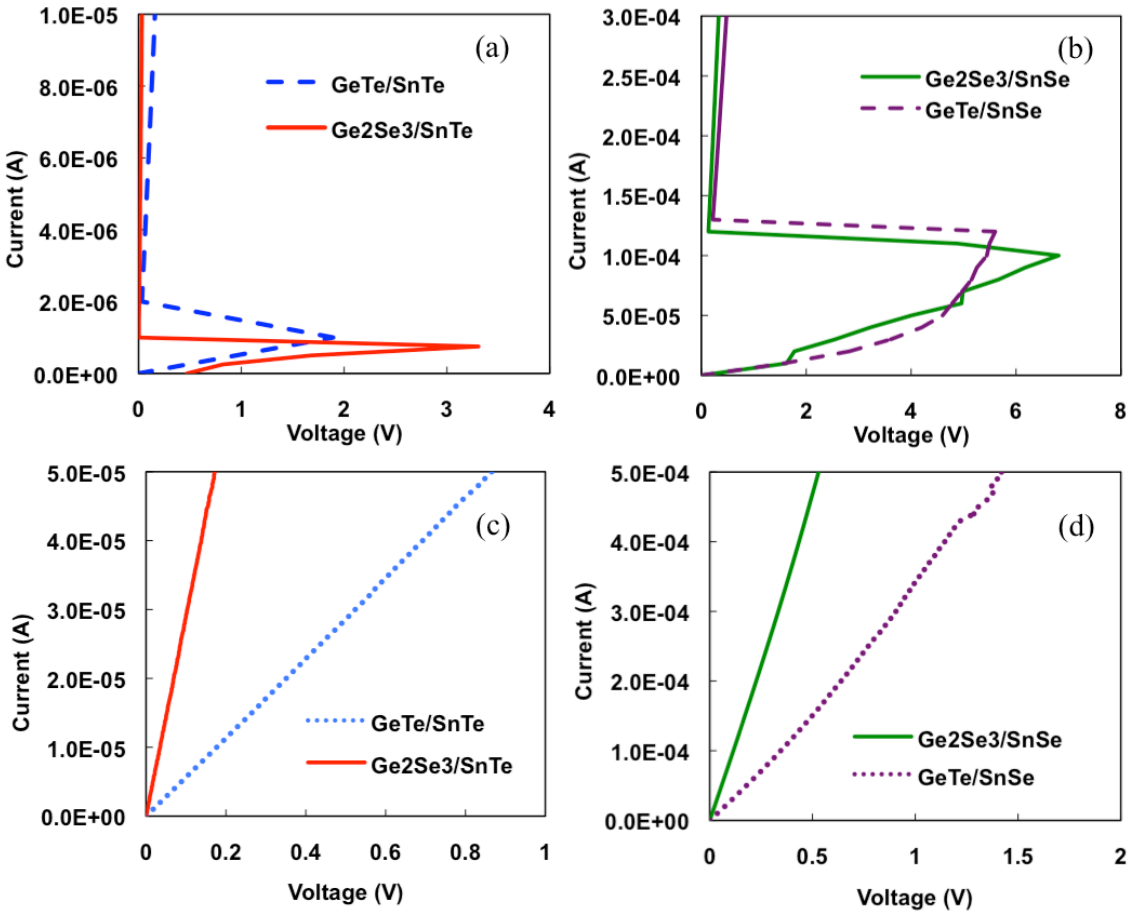


Figure 5.5: RESET state *I-V* characteristics of PCM cells employing bilayers of, (a) GeTe/SnTe and Ge_2Se_3/SnTe, (b) GeTe/SnSe and Ge_2Se_3/SnSe , SET state *I-V* characteristics of PCM cells employing bilayers of, (c) GeTe/SnTe and Ge_2Se_3/SnTe, (d) GeTe/SnSe and Ge_2Se_3/SnSe

All four types of devices show threshold switching, which as discussed in Chapter 2 is a characteristic of a PCM cell. The starting material is amorphous which is evident from the shallow slope of the initial portion of the *I-V* curve. As current is increased, voltage also increases until V_t is reached, at which point it snaps back and the curve becomes ohmic with a steep slope indicating an increased conductivity. As the current is increased further, phase transition from the amorphous to the crystalline state occurs. This is substantiated by a second *I-V* sweep performed on the same device as shown in Fig. 5.5 (c) and Fig. 5.5 (d). The characteristics are ohmic. This confirms that Ovonic memory switching has occurred and the devices have switched to the SET state.

Table 5.3 lists the average values of V_t and current at V_t for the four bilayers, measured for several devices over the surface of the wafer.

Table 5.3: Parameters extracted from RESET *I-V* characteristics

Bilayer	**Average V_t (V)**	**Average current at V_t (μA)**
GeTe/SnTe	1.79	4.11
Ge_2Se_3/SnTe	3.20	0.77
GeTe/SnSe	5.51	117
Ge_2Se_3/SnSe	5.87	98.5
Note: SnTe based devices are measured by varying the current from 0 to 100 μA in steps of 0.25 μA, using short integration time. SnSe based devices are measured by sweeping the current from 0 to 1mA in steps of 10 μA, using short integration time. HP 4145 parameter analyzer is used for both types of measurements		

From the RESET *I-V* characteristics and parameters listed in Table 5.3 it is observed that devices employing SnSe as a layer exhibit higher values of V_t and current at V_t. This may be explained as follows. The threshold voltage of a phase change material is a very strong function of the material bandgap [2]. SnSe has a noticeably higher bandgap of 0.95 eV as compared to SnTe (0.18 eV [3]). From the temperature v/s ρ measurements of SnTe and SnSe elucidated in Chapter 4, it is seen that, the ρ of as-deposited, partially crystalline SnTe does not change with increase in temperature. After complete crystallization beyond 300˚C, as the temperature is reduced, ρ also reduces slightly. This is demonstrative of a metallic behavior. SnSe on the other hand, exhibits a continuous reduction in ρ with increase in temperature till a transition temperature is reached at which point, a sudden drop in ρ

occurs. This decrease in ρ with rising temperature just before the onset of the transition temperature indicates a semiconductor like behavior [4]. Thus the Ta-SnSe contact is more of a Schottky barrier than an ohmic contact like that of Ta and SnTe, resulting in the requirement of a higher voltage/current in order to achieve switching.

5.4.2 Programming the PCM Devices

In order to demonstrate single bit memory functionality, the fabricated two terminal PCM cells are programmed using voltage pulses. The technique adopted is summarized below:

(1) From section 5.4.3, it is gleaned that, an as-deposited PCM device exhibits RESET state *I-V* characteristics as evidenced by the presence of a voltage snap-back in the curve. The initial *I-V* sweep has the effect of switching the device to the SET state. As long as the current is maintained below that required for melting, any subsequent current sweep will result in ohmic characteristics.

(2) The SET device may be switched to the RESET state by application of a programming pulse. This is a write operation. The pulse parameters such as amplitude (V_{amp}), pulse width (t_{RESET}), rise time (t_r) and fall time (t_f) depend upon the materials constituting the bilayer.

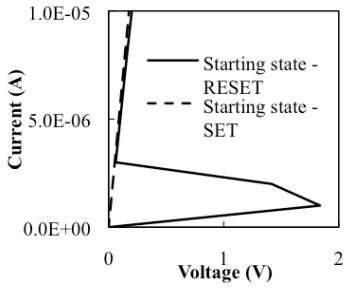
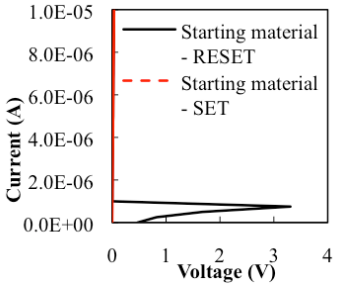
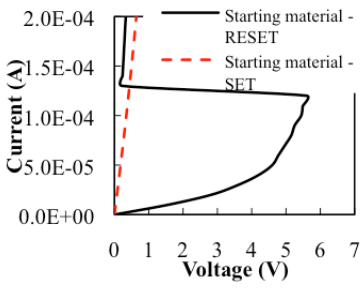
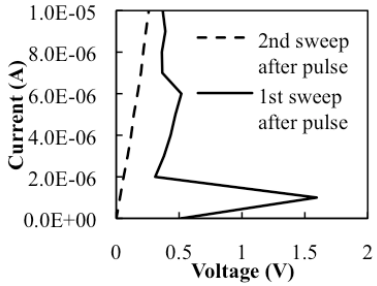
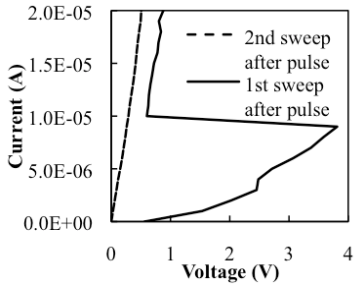
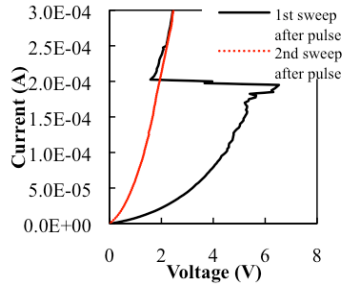
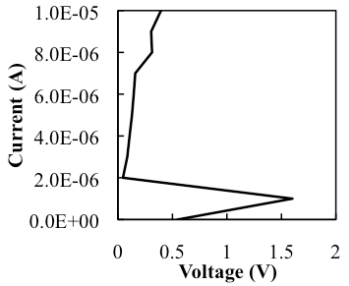
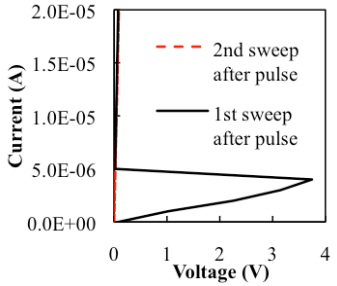
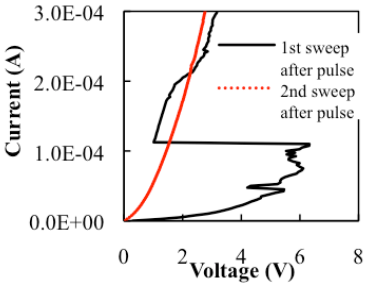
(3) The state of the device, after application of the programming pulse is read via a current sweep. The snap-back observed in the resulting *I-V* characteristics is evidence of the fact that the applied programming pulse was successful in switching the device from SET to RESET state.

(4) At the end of the current sweep, the device switches back from RESET to SET state.

(5) Again, in order to program the device into the RESET state, a programming pulse may be applied and this process can be repeated till the cell fails either due to stuck SET or stuck RESET.

Programming of devices employing three different stacks viz. GeTe/SnTe, Ge_2Se_3/SnTe and GeTe/SnSe has been accomplished using the method outlined above. The results are discussed in Table 5.4.

Table 5.4: RESET state Programming of Bilayer PCM Devices

	GeTe/SnTe	Ge_2Se_3/SnTe	GeTe/SnSe
Initial *I-V* sweep - As-deposited device is in RESET state and exhibits Ovonic threshold switching - At the end of sweep Ovonic memory switching occurs and device switches to SET state	 V_t = 1.84 V	 V_t = 3.31 V	 V_t = 5.49 V
I-V sweep after 1st pulse - Programming voltage is applied to RESET the device - Post RESET pulse *I-V* sweep exhibits threshold switching - At the end of sweep device switches back to SET state.	 V_{amp} = 6 V, t_{RESET} = 100 ns, $t_r = t_f$ = 20 ns	 V_{amp} = 6 V, t_{RESET} = 100 ns, $t_r = t_f$ = 20 ns	 V_{amp} = 10 V, t_{RESET} = 100 ns, $t_r = t_f$ = 20 ns
I-V sweep after 2nd pulse - The second pulse is identical to the first and is applied to determine repeatability of programming	 V_{amp} = 6 V, t_{RESET} = 100 ns, $t_r = t_f$ = 20 ns	 V_{amp} = 6 V, t_{RESET} = 100 ns, $t_r = t_f$ = 20 ns	 V_{amp} = 10 V, t_{RESET} = 100 ns, $t_r = t_f$ = 20 ns

From Table 5.4 it is observed that for bilayers of GeTe/SnTe and Ge_2Se_3/SnTe, the V_t for switched devices is not significantly different from that of as-deposited devices. On the other hand, the V_t of as-deposited GeTe/SnSe device increases by approximately 0.5 V from its average value on switching. Using the technique described above, the devices can be switched to two stable states. The corresponding distribution in SET and RESET state resistances for consecutive measurements is illustrated in Fig. 5.6.

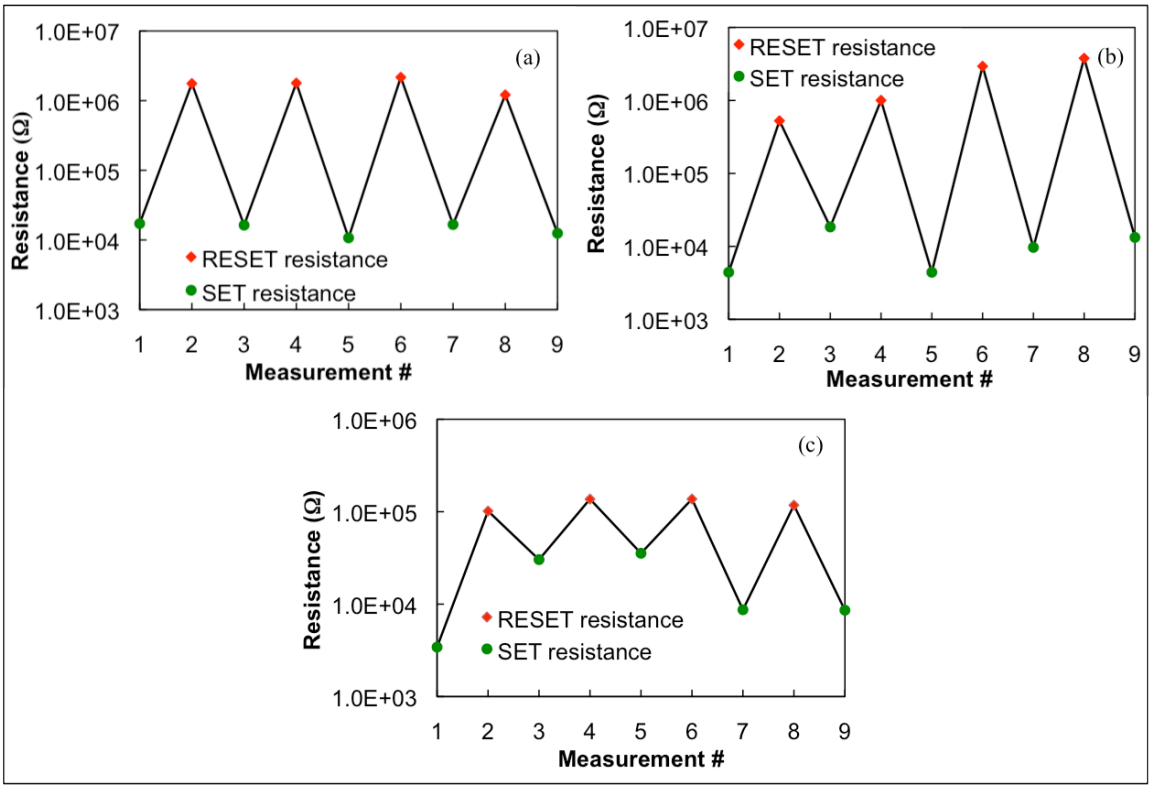


Figure 5.6: Variation in RESET and SET state resistance values with measurement for, (a) GeTe/SnTe, (b)Ge_2Se_3/SnTe and (c) GeTe/SnSe devices

The resistance margin between SET and RESET states for GeTe/SnTe devices is almost three orders of magnitude and they demonstrate the tightest control in terms of the distribution of RESET and SET state resistance values. GeTe/SnSe devices on the other hand exhibit significant variability with respect to SET state resistance and a correspondingly lower resistance margin.

Two terminal devices with Ge_2Se_3/SnSe bilayers could not be programmed back into the amorphous phase after the initial *I-V* sweep. It is observed that a voltage pulse as high as 15 V is not successful in switching the cell from the SET state to the RESET state. This is attributed to the large cross-sectional area of the active material. Further investigations employing active area reduction techniques similar to those discussed in Chapter 7 are warranted in order to examine single bit memory functionality of this bilayer.

5.5 Conclusions

Two terminal PCM cells employing bilayers of GeTe/SnTe, Ge_2Se_3/SnTe, GeTe/SnSe and Ge_2Se_3/SnSe have been designed, fabricated and tested. All devices exhibit threshold switching and memory switching behavior. Devices composed of stacks of GeTe/SnTe, Ge_2Se_3/SnTe and GeTe/SnSe have been subjected to programming pulses to examine their memory functionality. By the application of suitable voltage pulses, RESET state switching can be accomplished in devices of all three bilayers. It is observed that SnTe based devices exhibit lower V_t, lower current at V_t, higher resistance margin and less variability in SET state resistance as compared to SnSe based devices.

References for Chapter 5

[1] Idaho Microfabrication Laboratory, CHA Thermal Evaporator Operation, Boise State University, Boise, ID. [Online]. Available: http://coen.boisestate.edu/IMFL/Equipment/ThermalEvap.html.

[2] A. L. Lacaita and D. J. Wouters, "Phase-change memories," *Phys. Stat. Sol.*, vol. 205, pp. 2281-2297, 2008.

[3] K. A. Campbell and C. M. Anderson, "Phase-change memory devices with stacked Ge-chalcogenide/Sn-chalcogenide layers," *Microelectron. J.*, vol. 38, no. 1, pp. 52-59, 2007.

[4] K. Chung, D. Wamwangi, M. Woda, M. Wuttig and W. Bensch, "Investigation of SnSe, $SnSe_2$, and Sn_2Se_3 alloys for phase change memory applications," *J. Appl. Phys.*, vol. 103 p. 083523, 2008.

Chapter 6: Integration of Bilayer PCM cells with CMOS

The integration of bilayer PCM cells with a 2 μm CMOS process is discussed in this chapter. Details of circuit design, SPICE simulation, fabrication and electrical testing results of integrated devices and circuits are presented.

6.1 Introduction

The information obtained from the electrical testing of two terminal devices with no access transistor may not be a reliable reflection of its actual behavior. This is because single bits are not isolated against static build-up or discharge and this can significantly alter the actual current through or the potential across the device, which can in turn vary between devices thus changing the apparent switching conditions as well as the resistance the bit achieves. Secondly the capacitance of the micromanipulator probes in electrical contact with the electrodes of the device can vary. This can cause the device to see an electrical signal with different rise or fall times which can have a significant impact on a phase change device since this technology relies on heating and cooling rates to fix the state of the bit. Without proper isolation from an access transistor, unwanted bit erasing or writing can occur due to spurious electrical signals being picked up by the micromanipulator probes and being randomly applied to the device. All these issues call for the integration of PCM cell, preferably with CMOS technology, which will also serve as a proof of concept for future high density PCM memory arrays.

6.2 Concept

The PCM cell is vertically integrated on top of an NMOS as a back end of the line (BOEL) process. The NMOS is fabricated using a 2 μm twin well CMOS process developed at the SMFL at RIT. The key process steps are illustrated in Fig. 6.1.

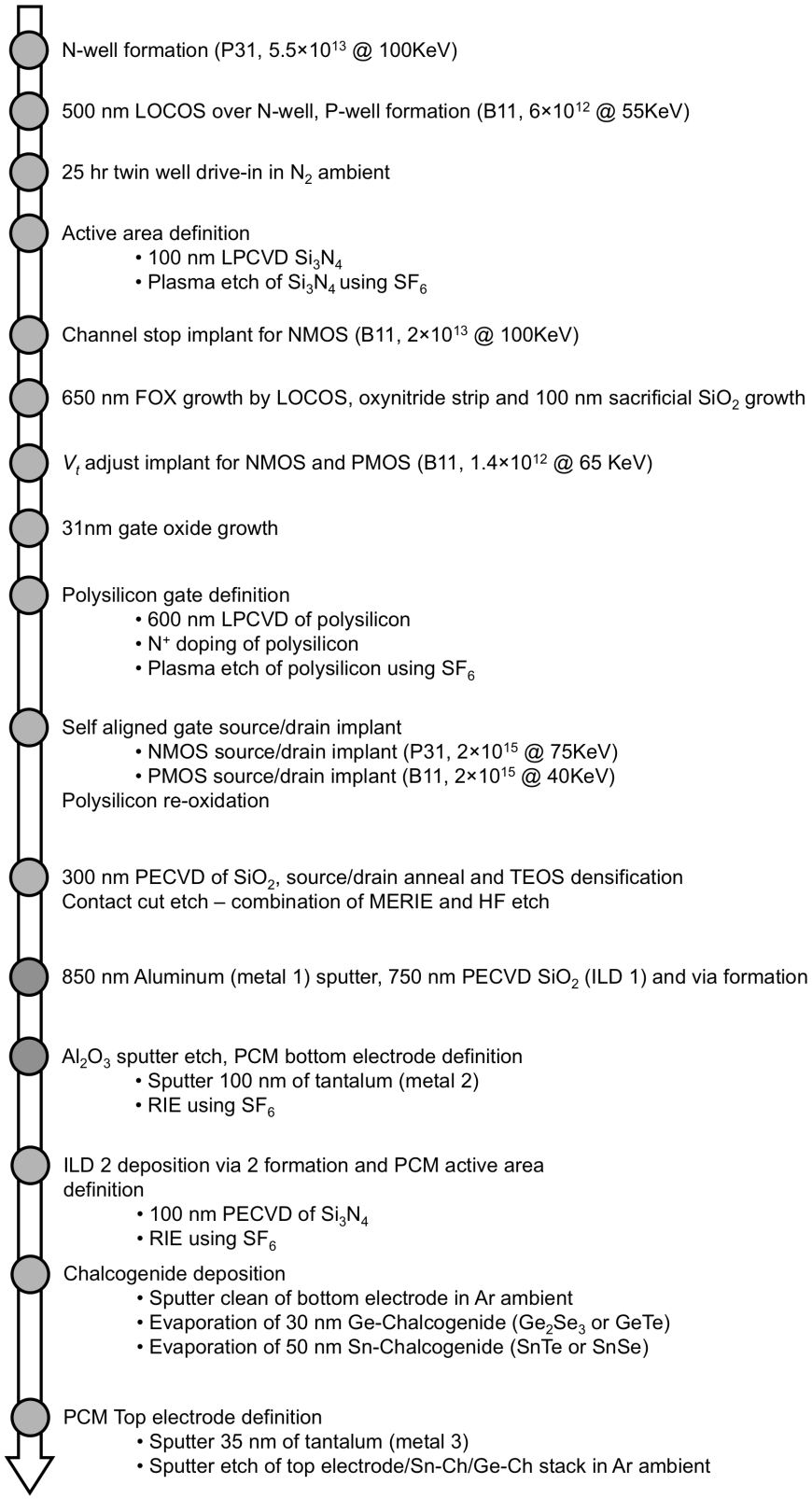


Figure 6.1: Process flow for integrating bilayer PCM with 2 μm CMOS technology

As a proof of concept, one 4 bit by 2 bit and two 8 bit by 2 bit memory arrays have been designed and fabricated. Each memory array comprises of read circuitry with a sense amplifier to sense the state of the cell and an adjustable current source to set the reference current, and write circuitry with drive circuits to SET or RESET the cell. These circuits also serve as a test vehicle for the developed PCM-CMOS process. As discussed previously, since a PCM cell is a direct write memory cell, an erase circuit is unnecessary.

The schematic of a 4 bit by 2 bit memory array is shown in Fig. 6.2. The row decoder is a 1:2 word line decoder and the column decoder is a 2:4 bit line decoder.

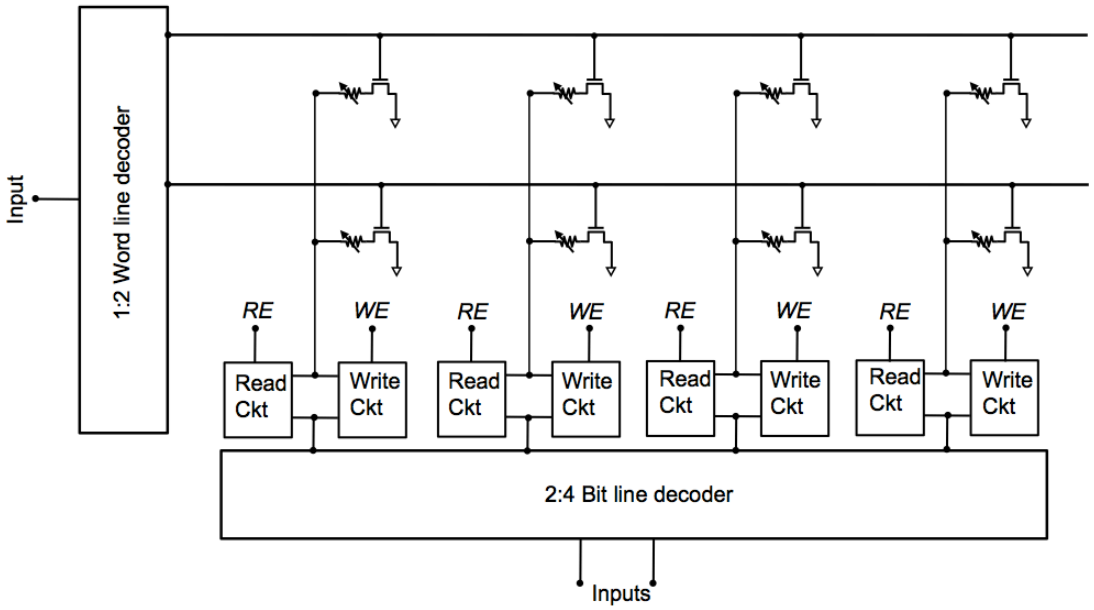


Figure 6.2: Block diagram of 2 by 4 memory array showing key components

After a particular row line is selected, the column address is used to decode which of the PCM cells (bits) from the row are to be addressed. In the figure, a variable resistor connected in series with the drain of an NMOS is used to represent a PCM cell with access transistor. The data can be read into or out of the array through the column decoder, based on the Read Enable (*RE*) or Write Enable (*WE*) signals respectively.

6.3 Design and Mask Layout

All devices and circuits are designed using TSMC 0.35 µm design rules in the IC Station Layout Editor provided by Mentor Graphics® and are simulated using HSPICE (Level 49). Further details can be found in the ensuing sections.

6.3.1 Read Circuitry

The read circuitry is employed to read the state (SET or RESET) of the PCM cell. The schematic shown in Fig. 6.3(a) reveals its major components.

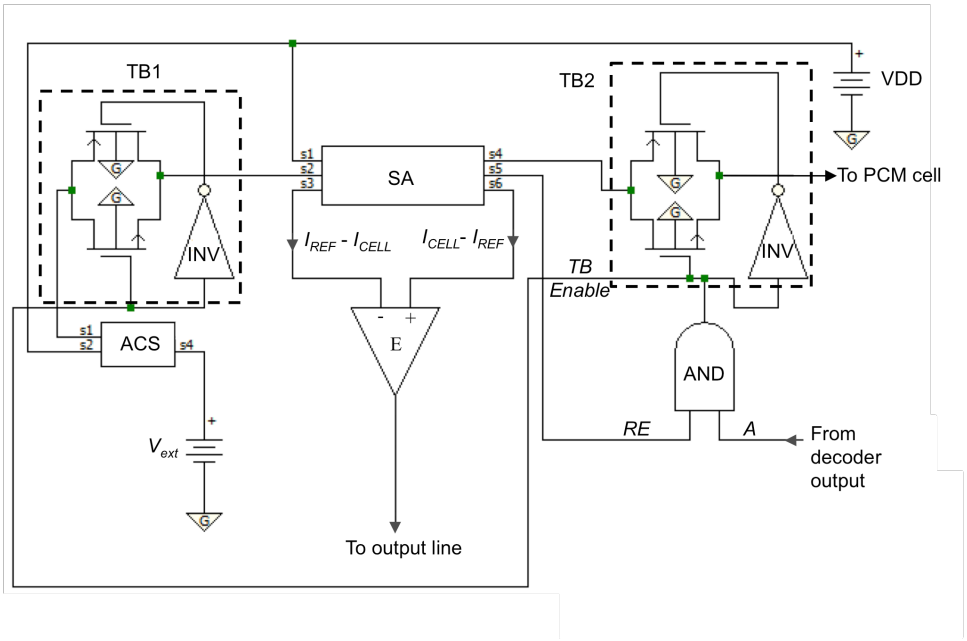


Figure 6.3(a): Schematic of designed read circuitry

SA is a sense amplifier, the left side of which is connected to an adjustable current source ACS supplying the reference current I_{REF}, and the right side of which is connected to the PCM cell through which the current I_{CELL} flows. I_{REF} is fixed to the value of current flowing through the PCM cell when it is in SET state. When the cell under consideration is selected by the access (row and column) decoders i.e. $A = 1$ and the read enable signal is high i.e. $RE = 1$, the tristate buffers, TB1 and TB2

allow I_{REF} and I_{CELL} to flow through the sense amplifier. A comparator circuit E, is used to compare the differential signals I_{REF} - I_{CELL} and I_{REF} - I_{CELL}. If I_{REF} is greater then the output is low and the cell is read to be in RESET state. On the other hand if I_{CELL} is greater, then the output is high and the cell is read to be in SET state.

The behavior of the read circuitry is simulated using HSPICE. The circuit topology is defined in a netlist, which is created using the KDE advanced text editor (Kate). The simulation results are viewed using Synopsys CosmosScope waveform viewer. From the graph shown in Fig. 6.3(b) it is observed that, as the external voltage source V_{ext} is changed from 0 to 5 V, I_{REF} provided by the adjustable current source can be varied from 0 to 340 μA.

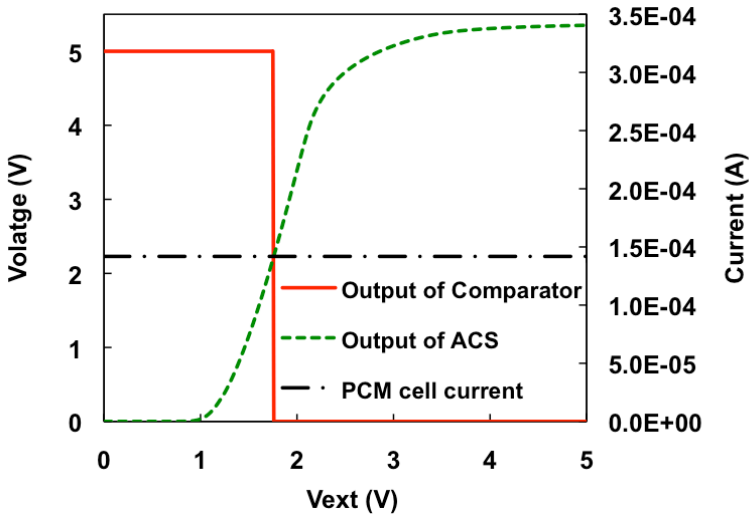


Figure 6.3(b): Behavior of read circuitry simulated in HSPICE

For a bilayer cell with SnTe as the top layer, it has been previously determined that the SET state resistance is in the neighborhood of 11 KΩ, which fixes the current through the PCM cell to 141.19 μA. As I_{REF} becomes greater than I_{CELL}, the comparator output switches from high (5 V) to low (0 V).

A brief description of the component elements of the read circuit is presented in the following sections.

6.3.1.1 Sense Amplifier

The sense amplifier forms the crux of the read circuitry and is used to sense the state of the addressed PCM cell. A schematic of the designed circuit with an external comparator E, is shown in Fig. 6.4(a).

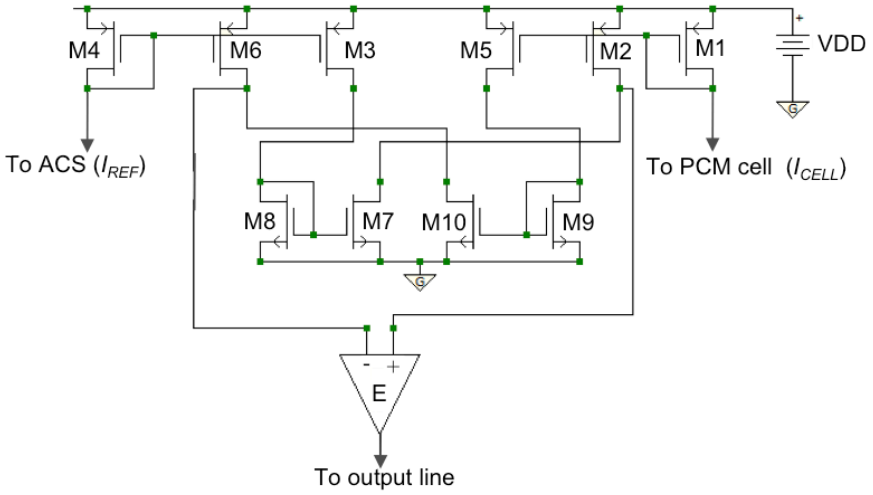


Figure 6.4(a): Schematic of designed sense amplifier with external comparator

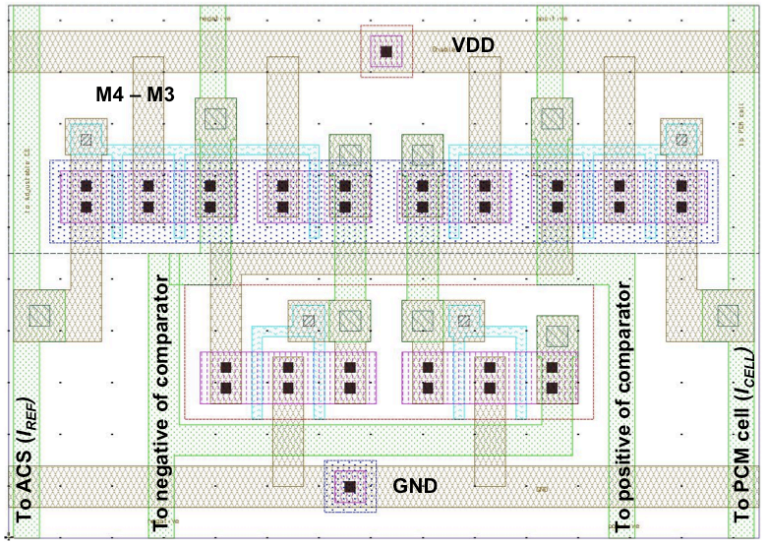


Figure 6.4(b): Layout of sense amplifier

A fully symmetric circuit topology, presented in [1] has been adopted. All mirror factors are set to unity by maintaining the same aspect ratios for PMOS and NMOS transistors respectively. C_C and C_R

are the parasitic capacitances associated with the input nodes of the comparator E. Ideally, C_C and C_R integrate the current differences $I_C = I_{CELL} - I_{REF}$ and $I_R = I_{REF} - I_{CELL}$, respectively. As discussed previously, the ensuing voltages are fed to the negative and the positive input terminals of the comparator, which detects the state of the PCM cell. When current mirror mismatches are taken into account I_C and I_R can be represented as [1],

$$I_C = \alpha_{C1} I_{CELL} - \alpha_{R2} I_{REF} \tag{6.1}$$

$$I_R = \alpha_{R1} I_{REF} - \alpha_{C2} I_{CELL} \tag{6.2}$$

Here α_{C1} and α_{R2} are the current mismatches introduced by current mirrors M1 – M2 and M4 – M6, respectively, and α_{R1} and α_{C2} are the current mismatches due to the pair of current mirrors M4 – M3, M8 – M7 and M1 – M5, M9 – M10 respectively. The effective current signal that produces the input signal of the comparator, can therefore be expressed as [1],

$$I_C - I_R = K_1 I_{CELL} - K_2 I_{REF} \tag{6.3}$$

where $K_1 = \alpha_{C1} + \alpha_{C2}$ and $K_2 = \alpha_{R1} + \alpha_{R2}$.

If only systematic mismatch is considered [1],

$$K_1 = \frac{\left(1 + \lambda_p \Delta V_{DS,sat2}\right)\left(1 + \lambda_n \Delta V_{DS,sat9}\right) + \left(1 + \lambda_p \Delta V_{DS,sat5}\right)\left(1 + \lambda_n \Delta V_{DS,sat10}\right)}{\left(1 + \lambda_p \Delta V_{DS,sat1}\right)\left(1 + \lambda_n \Delta V_{DS,sat9}\right)} \tag{6.4}$$

$$K_1 = \frac{\left(1 + \lambda_p \Delta V_{DS,sat6}\right)\left(1 + \lambda_n \Delta V_{DS,sat8}\right) + \left(1 + \lambda_p \Delta V_{DS,sat3}\right)\left(1 + \lambda_n \Delta V_{DS,sat7}\right)}{\left(1 + \lambda_p \Delta V_{DS,sat4}\right)\left(1 + \lambda_n \Delta V_{DS,sat8}\right)} \tag{6.5}$$

In the above equations, λ_n and λ_p are the NMOS and the PMOS channel length modulation parameters respectively, and $\Delta V_{DS,sati} = V_{DSi} - V_{Dsat}$, V_{DSi} and V_{Dsat} being the drain-to-source voltage of transistor T_i and the drain-to-source saturation voltage respectively.

In the absence of any process mismatch, all PMOS and all NMOS transistors have the same channel length modulation parameter, respectively. In addition, when $I_{REF} = I_{CELL}$, the drain-to-source voltages of the corresponding devices are identical and hence, *K1 = K2*. Therefore, no systematic current offset is present, which leads to zero systematic voltage offset at the comparator input.

Due to the perfect symmetry of the circuit topology, the inverting and the non-inverting inputs of the comparator are driven with identical impedance. Any disturb coming from sources such as capacitive coupling with noisy substrate, VDD, or ground, is treated as a common-mode signal and is therefore rejected.

6.3.1.2 Adjustable Current Source

By employing an adjustable current source the reference current can be conveniently set to the desired value. As observed from the schematic illustrated in Fig. 6.5(a), I_{REF} is the drain current of M7 which mirrors the current in M6. The bias current through M6 is set using the PMOS current mirror comprising of M2 and M3. The external voltage source V_{ext} governs the current through M1 and through the series connected M2. Thus, V_{ext} provides a handle on the value of I_{REF}.

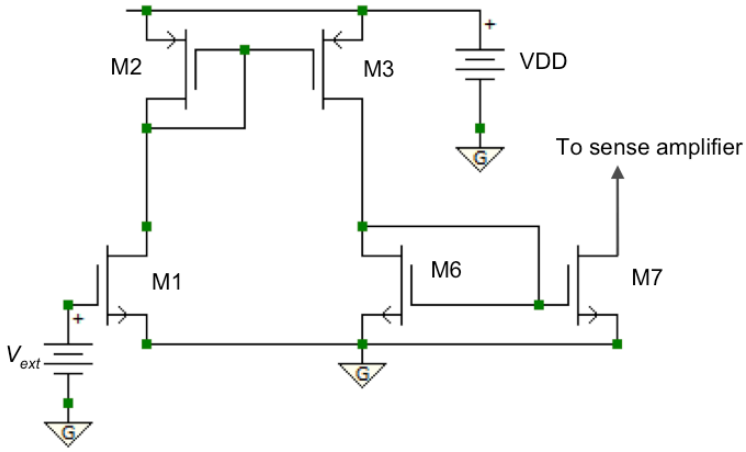


Figure 6.5(a): Schematic of designed adjustable current source

By using a common-centroid layout technique, the current matching in a mirror can be improved [2, 3]. This is particularly suitable for devices with large *W/L*. The layout of the PMOS current mirror designed using this arrangement is shown in Fig. 6.5(b). Each MOSFET of size 48/2 has been split up

into four parallel devices, each of size 12/2. Splitting the two MOSFETs into parallel devices and interdigitizing them distributes process gradients across both devices and thus improves matching [2].

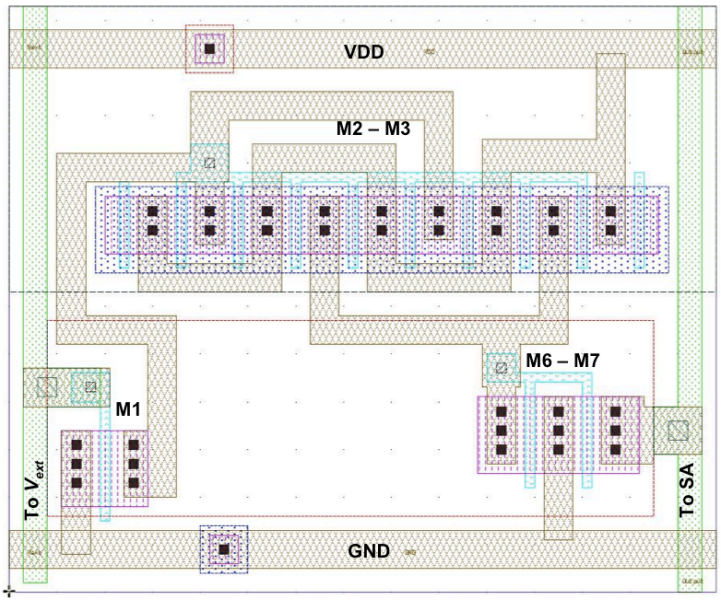


Figure 6.5(b): Layout of adjustable current source

The overall parasitic capacitance associated with the reverse-biased implant substrate diode i.e. the drain or source depletion capacitance to substrate (C_{db} and C_{sb}) can also be lowered by splitting a device into parts. The values of C_{db} and C_{sb} are proportional to W. If n is the number of devices in parallel and is odd, the split device reduces these parasitics by a factor of $(n+1)/2n$. For an even number of devices in parallel, C_{sb} is reduced by one half and C_{db} is reduced by $(n+2)/2n$. Another advantage of placing devices in parallel is that such an arrangement reduces the parasitic resistance in series with both the source and drain.

Figure 6.5(b) also shows the presence of dummy polysilicon strips, which have been included on either sides of the device. This helps in minimizing effects of polysilicon undercut on the outer edges after patterning. In the absence of dummy strips, the polysilicon would be etched out more under the outermost gates resulting in a mismatch between the parallel devices [1].

6.3.1.3 Tri-state Buffer

The tri-state buffer comprises of a transmission gate and an inverter, shown enclosed within the dashed region in Fig. 6.3. When *Enable* (*TB Enable*) is high, *input* is passed to *output*. The NMOS passes logic 0 and the PMOS passes logic 1. When *Enable* is low, *output* is in high impedance state.

6.3.1.4 Comparator

A general-purpose comparator 3 stage comparator, designed and presented in [2] is used to compare the outputs of the sense amplifier and thus read the state of the addressed PCM cell. It comprises of a pre-amplification stage wherein the input signal is amplified to improve the comparator sensitivity and isolated from the switching noise coming from the next stage. The second stage is the decision stage that determines which of the input signals is larger. The final stage is called the output buffer or post amplification stage. It amplifies the signal from the decision circuit and converts it into a digital signal. Additional details are furnished in [2].

6.3.2 Write Circuitry

The addressed PCM cell is programmed into the SET or RESET state using the write circuitry.

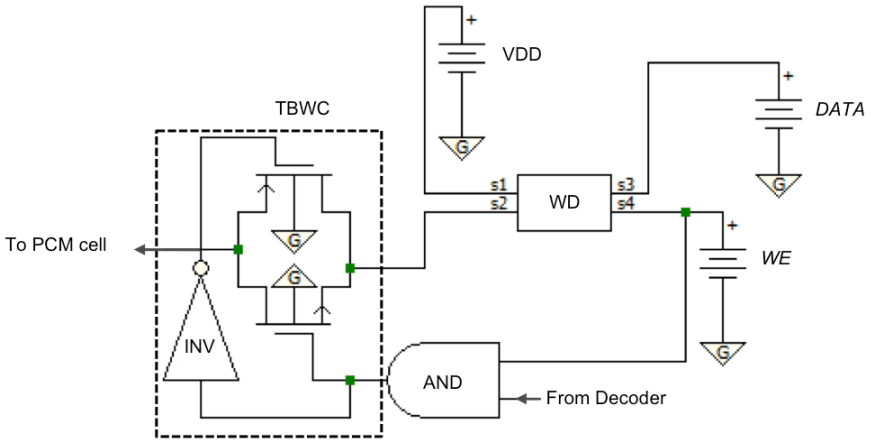


Figure 6.6: Schematic of designed write circuitry

Its key elements are presented in Fig. 6.7. WD is the write drive circuit, which provides the drive current to program the cell. Depending upon the value of *DATA*, the cell is SET (*DATA* = 0) or RESET (*DATA* = 1). When the write enable signal is high, *WE* = 1 and the cell under consideration is selected by the bit and word line decoders, *A* = 1, the tri-state buffer TBWC allows the write current from WD to reach the PCM cell.

6.3.2.1 Write Drive Circuit

This circuit generates the drive current to SET or RESET the addressed PCM cell. When the externally applied voltage, *DATA* is low, the current mirror M3-M4 is active. This mirror is used to multiply current and hence functions as a current amplifier. The current through the multiplier MOSFET M4 is four times that through the reference MOSFET M3 and is used to program the PCM cell into the SET state. Similarly, the mirror M7 – M8, which is active when *DATA* is high, also works as a current amplifier. In this case, the current through M8 is eight times that through M7 and serves to RESET the cell.

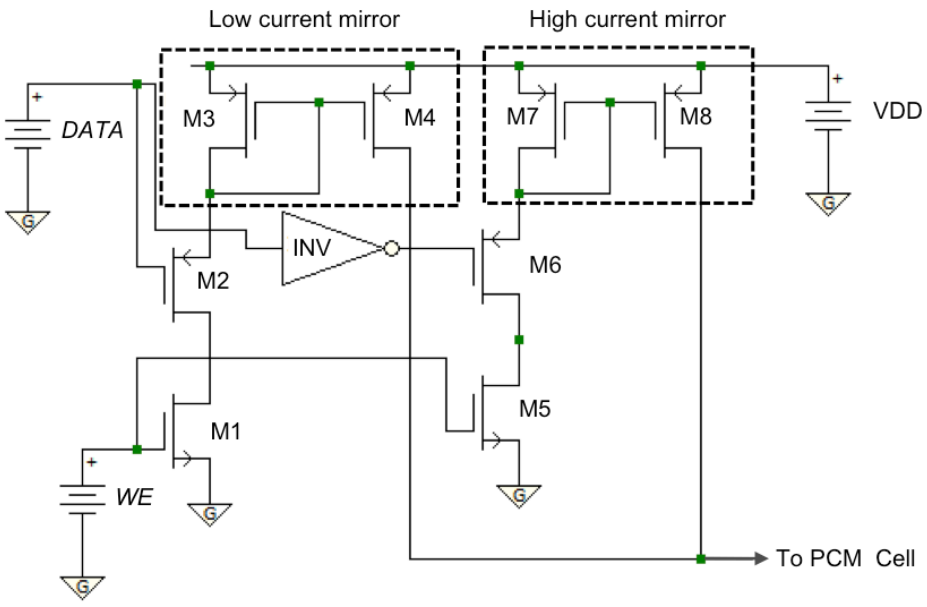


Figure 6.7(a): Schematic of designed write drive circuit

When laying out a mirror with different widths (M3 (32/2) – M4 (128/2) and M7 (32/2) – M8 (256/2)) oxide encroachment - due to the FOX not being precisely patterned as specified by the active layer mask - may reduce the actual width of the MOSFETs thus affecting the mirror's ratio. In order to preclude these issues, a width compensation technique is employed while designing the high-current and low-current mirrors as shown in Fig. 6.7(b).

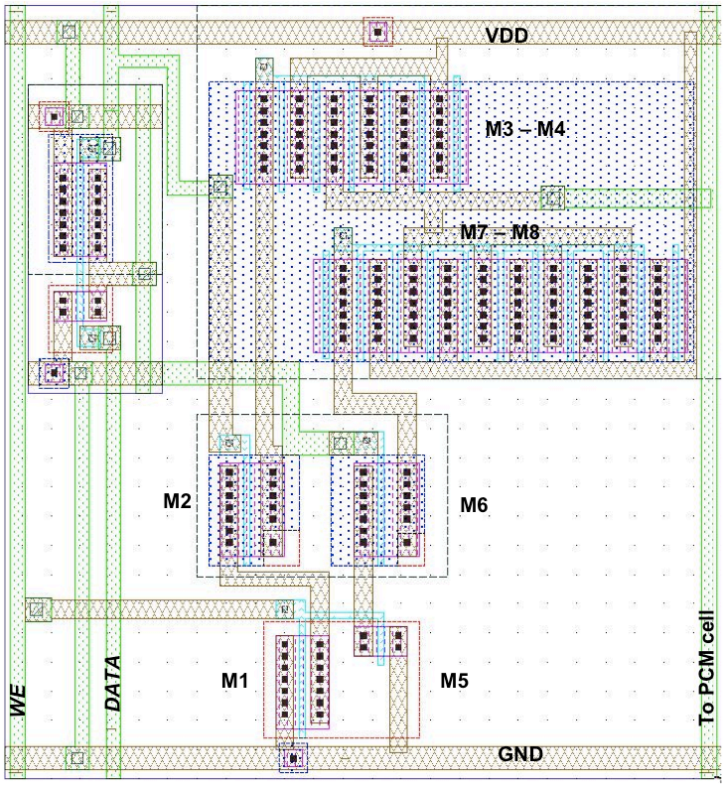


Figure 6.7(b): Layout of write drive circuit

Using this approach, M4 is split up into four parallel MOSFETs each of size 32/2 and M8 is split up into eight parallel devices, again each of size 32/2.

The behavior of the write-drive circuit is also simulated using HSPICE. From the graph shown in Fig. 6.7(c) it is observed that when *DATA* is low (0 V – 2.5 V) a current as high as 1.1 mA is available to SET the addressed PCM cell. On the other hand, when *DATA* is high (2.5 V – 5 V), the PCM cell can be RESET with a current as large as 3.17 mA.

Two different write-drive circuits have been designed based on the width of M8 in the high current mirror. They are, small (W = 256) with an output current of 1.5 mA and medium (W = 4096) with an output of 3.17 mA.

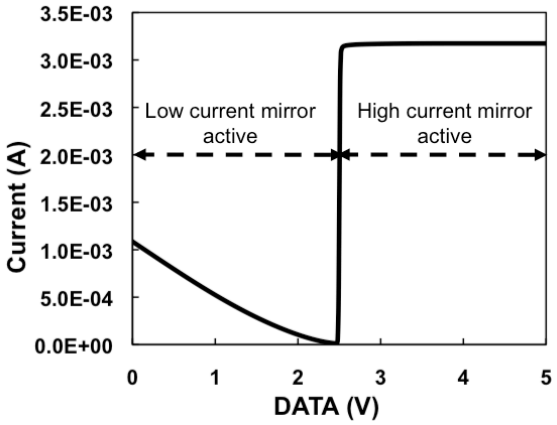


Figure 6.7(c): Output of write-drive circuit based on applied DATA, simulated in HSPICE

6.3.3 Word Line Decoder

The world-line decoder is a 2:1 row decoder. It is simply a string of two invertors connected in series. As shown in the schematic, when *i/p* is high, row 1 goes high and when *i/p* is low, row 2 is selected.

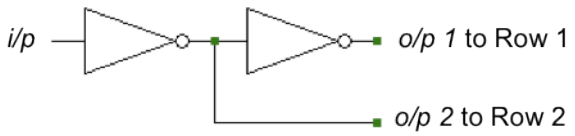


Figure 6.8: Schematic of designed world line decoder

6.3.4 Bit Line Decoder

The bit line decoder is a 3: 8 column decoder. It comprises of eight, 3 input NOR gates fed through inverting and non-inverting inputs. Similarly, a 2:4 decoder has also been designed consisting of four, 2 input NOR gates. The schematic is illustrated in Fig. 6.9.

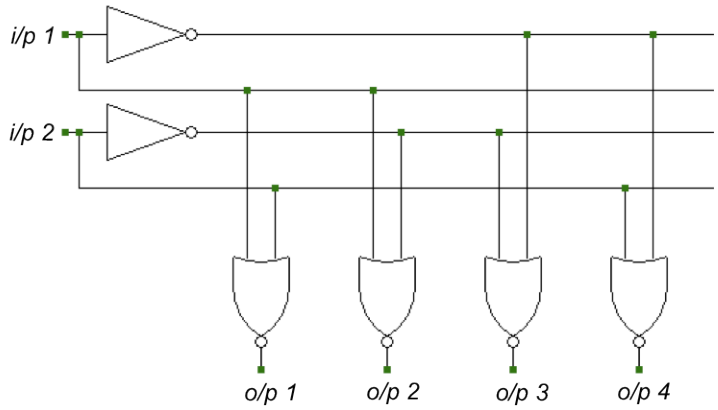


Figure 6.9: Schematic of designed 2:4 bit line decoder

6.4 Fabrication

The integration of bilayer PCM cells with a 2 μm CMOS process involves 3 levels of metal and a total of 12 levels of photolithography. The CMOS is defined by twin well formation, LOCOS isolation, 31 nm n^+ polysilicon gate, 5 V power supply and $V_{Tn} = |V_{Tp}| = 1$ V. Fig. 6.1 summarizes the major steps in the process flow. A brief description of the key processes can be found in the following sections.

6.4.1 Substrate Acquisition and Preparation

The starting wafer used is 150 mm (100) p type Si with an initial resistivity of 15-25 Ω-cm. Sixteen wafers are designated as device samples and are scribed as D1 – D16. Two n type control wafers are included for the purpose of p-well and p^+ source/drain characterization. Initial sheet resistance, R_s, measurement is carried out on the device samples using the Resmap and is determined to be in the range of 290-304 Ω/□. Following this, the wafers are subjected to standard RCA clean (10 min SC-I at 75˚C in 15:1:3 H_2O:NH_4OH:H_2O_2, 60 s 50:1 HF, 10 min SC-II at 75˚C in 15:1:3 H_2O:HCl:H_2O_2) to remove organic contaminants, native/chemical oxide and metallic contaminants respectively.

6.4.2 N-well Formation

In order to create the n-well, 150 nm of LPCVD Si_3N_4 is used as the implant mask. Prior to the deposition of Si_3N_4, 50 nm of dry SiO_2 is grown at a temperature of 1000˚C as a stress release layer. Si_3N_4 is deposited by flowing 60 sccm of $SiCl_2H_2$ and 152 sccm of NH_3 at 810˚C and at a pressure of 400 mTorr.

The first level lithography is done in order to open the n-well area for phosphorus implant. HMDS priming is carried out at 140˚C for 60 s to enhance adhesion between the PR and wafer surface. Wafers are spin coated with ~ 1 μm of OIR 620-10 PR at 3250 RPM for 30 s. This is followed by a soft bake at 90˚C for 60 s to drive the solvent out of the spun on resist. Next, wafers are exposed by means of the Canon *i*-line stepper using a dose of 180 mJ/cm^2. Following exposure, the wafers were subjected to a 60 s, 110˚C post exposure bake. The resist film is then developed for 48 s in CD-26 developer, rinsed and then hard baked at 120˚C for 60 s in order to improve its mechanical robustness.

The Si_3N_4 is plasma etched using the LAM 490 by flowing 200 sccm of SF_6 at a pressure of 260 mTorr at 125 W for 2 min 40 s.

The n-well is created by implanting 5.5×10^{12} /cm^2 of phosphorus P31 species at 100 KeV using phosphine gas diluted in hydrogen as the source. In order to quantify the effect of the implant, rapid thermal anneal (RTA) of the n-well monitor is done to activate the dopant. The anneal is carried out for 60 s at 1000˚C in N_2 ambient. The resulting R_s is measured to be 962.36 Ω/□.

The residual PR is stripped off in O_2 plasma using the Branson Asher and a standard RCA clean is carried out on the wafers.

6.4.3 P-well Formation

Localized oxidation of silicon (LOCOS) is performed over the n-well to block the boron implant required for the p-well. This is the reason why the n-well is created prior to the p-well. If the situation is reversed and the p-well is created first then, during the subsequent LOCOS, there would be

significant loss of boron from the p-well to the oxide due to it segregation constant being < 1. LOCOS is carried out at 1000˚C in steam ambient to grow 500 nm of wet SiO_2.

The residual Si_3N_4 on the wafers has to be etched in order to open up the area for the p-well. Prior to this nitride etch, a 45 s 10:1 BOE dip is performed to ensure that any layer of SiO_2 that may have been formed on the nitride during LOCOS is removed. This is essential because oxide on nitride will prevent the nitride from being (wet) etched thereby blocking subsequent implant. Following the oxynitride strip, Si_3N_4 on the device wafers is etched in hot phosphoric acid at 175˚C.

To create the p-well, a dose of 6×10^{12} /cm^2 of Boron B11 species is implanted into the samples at an energy of 55 keV using a BF_3 source. Again, to quantify the effect of the implant, RTA of the p-well monitor (starting R_s = 294.92 Ω/□) is done to activate the dopant. After a 60 s anneal at 1000˚C in N_2 ambient the R_s is measured to be 4497.62 Ω/□.

6.4.4 Twin Well Drive In

A 25 hr twin well drive in process is performed at 1100˚C in N_2 ambient for dopant diffusion and activation. After the drive in, any existing oxide on the wafer surface is etched in 5.2:1 BOE bath for 5 min 23 s.

6.4.5 Active Area Definition

This is the 2nd level of lithography and is performed in order to delineate the field regions from the active areas and ready them for the ensuing channel stop implant. To define the active areas, 100 nm LPCVD Si_3N_4 deposited on 50 nm thick dry SiO_2 is employed. The nitride deposition pressure is lowered to 250 mTorr for improved film uniformity. To open up field areas, lithography is carried out using the process discussed in section 6.4.2.

The Si_3N_4 covering the field regions is plasma etched using the LAM 490 by flowing 200 sccm of SF_6 at a pressure of 260 mTorr at 125 W for 2 min 47 s. Residual PR on the wafers is ashed in O_2 plasma.

6.4.5 Channel Stop Implant

In order to prevent the formation of a field transistor between adjacent NMOSFETs, a boron channel stop implant is provided in the field region. Level 3 photolithography thus involves masking the n-well and the NMOS active area with PR using the same process discussed in Section 5.4.2. The PR covering the active region of the NMOS is given a 1 μm shrink on each side in order to account for the worst case misalignment. If such a shrink is not provided then any misalignment would result in the PR covering one of the edges of the nitride thereby preventing the channel stop implant from getting into the field region near the nitride edge i.e. along the width dimension of the transistor.

It is essential for the channel stop implant to be fairly deep, otherwise when the field oxide is grown in the subsequent step, the boron will segregate into the oxide causing loss of dopant thereby defeating the purpose of the implant. For this reason a dose of 2×10^{13} /cm^2 of Boron B11 species is implanted at a high energy 100 KeV. The masking PR is then ashed and the wafers are subjected to a standard RCA clean.

6.4.6 Field Oxide Growth

LOCOS is carried out in a steam ambient at 950˚C in order to grow 650 nm thick field oxide (FOX).

Prior to stripping away the nitride covering the active regions, a 35 second oxynitride strip is done in 5:1 BOE. The nitride is etched for 25 min in hot phosphoric acid heated to 175˚C.

6.4.7 Kooi Oxide Growth

During the FOX growth, which is a steam oxidation, H_2O will react with the nitride over the active region and liberate ammonia. This ammonia may pass into the FOX through the region near the bird's beak, which is the most vulnerable region due to the encroachment of the oxide into the nitride. The ammonia may give rise to nitride pockets in the FOX, which act as potential getter sites and cause device problems. In order to remedy this, oxide of thickness equal to that present on the active region has to be stripped away and new oxide has to be grown which will consume the defects at the

interface. This is done by growing a sacrificial oxide called the Kooi oxide. It serves the purpose of consuming the nitride pockets and thus ensures integrity of the active border.

First, oxide of thickness equal to that on the active area (~ 50 nm) is stripped by carrying out a 37 s etch in 5.2:1 BOE bath. Following this, Kooi oxide of thickness 100 nm is grown on the wafers in a steam ambient at 900˚C.

6.4.8 Threshold Voltage Adjust Implant

MOS non-idealities such as metal semiconductor work function difference, interface trap charge, fixed oxide charge, bulk oxide defects and presence of mobile alkali ions in the oxide cause the actual threshold voltage (V_T) of the device to vary considerably from its ideal value. These non-idealities cause a negative shift in the V_T value for both NMOS and PMOS. In order to obtain the desired V_T, a threshold voltage implant is carried out.

For this purpose, a blanket implant of boron B11 species of dose 1.4×10^{12} cm^{-2} is provided to both PMOS and NMOS at an energy of 65 KeV. The Kooi oxide is etched in 5.2:1 BOE bath for 1 min 28 s, following which a standard RCA clean is carried out on the wafers.

6.4.9 Gate Oxide Growth

The gate oxide has to be a very high quality oxide in order to minimize the effect of any fixed oxide charge on the MOS V_T. Before gate oxide growth the furnace is subjected to a high temperature TransLC clean. This clean utilizes 2% Cl which acts a gettering agent. It helps in capturing mobile alkali ions (e.g. Na^+ ions) and renders them immobile. It is also found to react with silicon forming chlorosilane thereby causing Si vacancy creation at the interface. These vacancies act as a sink for the interstitials formed during oxide growth and thus help in reducing stress at the interface. The TransLC clean is done at a temperature of 1050˚C for 40 min. Following the clean, 31 nm of gate oxide is grown at a temperature of 1000˚C in dry oxygen ambient.

6.4.10 Gate Formation

N^+ polysilicon serves as the gate material. For this purpose, 600 nm of polysilicon is deposited using LPCVD at 610˚C at a deposition pressure of 288 mTorr by flowing 50 sccm of SiH_4. The polysilicon is doped by spin coating wafers with phosphorus spin on glass (SOG) - N250 Emulsitone solution, followed by a 15 min bake at 200˚C to drive out the solvents from the SOG. After curing, n^+ diffusion is carried out in N_2 ambient at 1000˚C for 15 minutes. Post diffusion, the remaining SOG on the surface of the wafers is etched in 5.2:1 BOE for 5 minutes.

Level 4 photolithography is performed using the same process described in Section 6.4.2 in order to define the gate region. The polysilicon is plasma etched using the LAM 490 through the action of 15 sccm of O_2 and 140 sccm of SF_6 at a power of 140 W and a pressure of 325 mTorr. Residual PR is stripped off using the Branson Asher.

6.4.11 N^+ Source/Drain Formation

The polysilicon gate created in this process is a self aligned gate since it defines the source and drain regions of the MOSFET. No separate lithography level is required to define these regions. The gate is aligned in such a way that it acts as a mask to the source/drain (S/D) implant and thus prevents the implant from entering the channel region.

However n^+ S/D lithography (level 5) is essential to mask the n-well area to prevent the n^+ implant from entering the PMOS active region.

For creating the S/D regions, a dose of 2×10^{15} /cm^2 of phosphorus P31 species is implanted at an energy of 75 keV. The high dose entails a long implant time which hardens the PR. Hence a combination of Baker PRS 2000 solvent strip heated to 90˚C and O_2 plasma is employed to ensure that all the residual PR is removed.

6.4.12 P^+ Source/Drain Formation

Similarly a p^+ S/D lithography (level 6) is carried out to mask the p-well areas with PR to prevent the p^+ implant from entering the NMOS active regions.

The p^+ S/D regions are created by implanting a dose of 2×10^{15} /cm^2 of boron B11 species at an energy of 40 keV. Again, the hardened residual PR is removed using a hot solvent strip followed by O_2 plasma. Finally, the wafers are cleaned in a standard RCA clean.

6.4.13 Polysilicon Re-oxidation

The polysilicon re-oxidation is not the final S/D anneal but it is essential for two main purposes. Firstly it helps to restore the integrity of the gate oxide at the channel edge, which gets fairly worn out when the implant is done. Secondly, it helps to reduce the overlap capacitance associated with the source and drain. This re-oxidation is carried out at a low temperature of 850˚C for about 15 minutes in a steam ambient, in order to reduce stress and prevent any out diffusion from the S/D to the oxide.

6.4.14 Pre-metal Dielectric Deposition

Due to issues associated with the uniformity of low temperature LPCVD oxide, PECVD SiO_2 is used as the pre-metal dielectric (PMD) between polysilicon and metal 1. PECVD oxide of thickness 300 nm is deposited at 390˚C by flowing 285 sccm of O_2 and 400 sccm of Tetraethylorthosilicate (TEOS) at a working pressure of 9 Torr and a power of 270 W.

6.4.15 Source/Drain Anneal

An anneal is performed at 1000˚C for 30 minutes in N_2 and steam ambient in order to activate the dopant in the source and drain regions. This anneal also serves to densify the PECVD SiO_2.

6.4.16 Contact Cut Formation

Level 7 photolithography is carried out to create the contact cuts. The wafers are coated with HMDS and PR using the same recipe discussed in section 6.4.2. The contact cuts are of size 2 μm^2 and hence for reliable pattern transfer, the exposure dose is increased to 260 mJ/cm^2. After a 60 s post-exposure bake at 110˚C, the wafers are developed in CD-26 developer for 200 s followed by a 30 s DI water rinse and spin dry. Finally, the PR is hard-baked at 140˚C for 60 s.

A combination of magnetically enhanced RIE (MERIE) and wet-etch techniques are employed to create the contact cuts. To prevent severe under-cutting of oxide due to long wet-etch times, the first 250 nm are etched using MERIE by the action of 100 sccm of CHF_3, 50 sccm of CF_4 and 15 sccm of O_2 at a power of 500 W, a pressure of 250 mTorr and a magnetic field of 40 Gauss. The MERIE is aggressive and this presents a possibility of the S/D regions being etched away if the etch time is not tightly controlled. Hence the remaining 50 nm of SiO_2 is removed in 10:1 BOE with surfactant. Due to the small size of the features, BOE blocking may occur. To prevent this, the wafers are raised completely out of the BOE bath every 15 s during the etch. This approach has been found to give excellent etch uniformity. The residual PR is removed by using hot solvent strip solution and the wafers are subjected to a standard RCA clean.

6.4.17 Metal 1 Deposition

Aluminum of thickness 850 nm is sputtered by flowing of 20 sccm of Argon at a sputter pressure of 5 mTorr and a DC power of 2000 W.

Level 8 photolithography is carried out to pattern Al. Existing topography on the wafers entails a thicker PR for reliable pattern transfer. Hence, 1.5 μm thick PR is spin-coated at 2000 RPM for 30 s. The develop time is increased to 68 s from the baseline value of 48 s to ensure that the thick PR is completely cleared from the exposed regions.

Al is plasma etched in LAM 4600 in 60 sccm of Cl_2, 50 sccm of BCl_3 and 15 sccm of chloroform diluted in 40 sccm of N_2 at 125 W and 300 mTorr pressure for 130 s.

6.4.18 ILD 1 Deposition and Via 1 Formation

PECVD SiO_2 serves as the inter-level dielectric (ILD) between metal 1 and metal 2. For this purpose, 750 nm of SiO_2 is deposited via PECVD at 390˚C by flowing 400 sccm of TEOS and 285 sccm of O_2 at a pressure of 9 Torr and a power of 290 W.

Level 9 photolithography is carried out to define vias in ILD1. Wafers are coated, exposed and developed using the same recipes used for creating the contact cuts. The vias are etched by employing MERIE, through the action of 100 sccm of CHF_3, 50 sccm of CF_4 and 15 sccm of O_2 at a power of 500 W, a pressure of 250 mTorr and a magnetic field of 40 Gauss. The aggressive nature of the etch is not an issue in this case since, the gases employed for etching PECVD SiO_2 do not affect the underlying Al.

6.4.19 Metal 2 Deposition

In addition to connecting the CMOS circuitry to the I/O pads, metal 2 serves as the bottom electrode for the PCM cell. As discussed in Chapter 5, Ta is used for this purpose. Prior to metal 2 deposition, a sputter etch is vital in order to remove Al_2O_3 present on the Al surface and ensure good contact between metal 1 and metal 2. As a result, a 20 min sputter etch is carried out through the action of 20 sccm of Ar at a pressure of 5 mTorr and an RF power of 500 W. Ta of thickness 150 nm is deposited immediately following the sputter etch without a vacuum break. For this purpose, the argon flow and working pressure are maintained at 20 sccm and 5 mTorr respectively while the RF power is increased to 900 W.

Level 10 photolithography is carried out to pattern metal 2 lines using the same recipes used to pattern metal 1.

Ta is etched using RIE in SF_6 based chemistry. First the chamber is cleaned by flowing 30 sccm of O_2 at 400 W at a pressure of 100 mTorr for 10 min in order to remove any polymer contaminants. Next, it is seasoned for 10 min using the recipe employed for performing the etch.

Finally, wafers are etched in 125 sccm of SF_6 at a power of 75 W and a pressure of 125 mTorr. The residual PR is removed in hot solvent strip.

6.4.20 ILD 2 Deposition and Via 2 Formation

ILD 2 is essentially the dielectric between the top and bottom electrodes of the PCM cell. As discussed in Chapter 5, PECVD Si_3N_4 is used for this purpose. Prior to nitride deposition a de-scum is required in order to remove organic contaminants which may otherwise introduce pinholes in the dielectric. This has previously been accomplished by performing a Piranha clean as discussed in Chapter 5. However, due to the possibility of Al being attacked by the H_2SO_4 in the Piranha solution via any pinholes that may be present in ILD1, O_2 plasma de-scum is employed. PECVD Si_3N_4 of thickness 100 nm is deposited at 400˚C by flowing 130 sccm of SiH_4 and 60 sccm of NH_3 at 4.5 Torr and at a power of 600 W.

Level 11 photolithography is carried out to define vias in ILD 2. This level determines the PCM device active area. Wafers are coated, exposed and developed using the same recipes used for creating the contact cuts.

The nitride is plasma etched by flowing 200 sccm of SF_6 at 200 W and 200 mTorr pressure. The residual PR is stripped in hot solvent strip.

6.4.21 Sputter Clean and Chalcogenide Evaporation

Sputter etch of the oxidized Ta monolayers and the ensuing chalcogenide deposition are carried out as detailed in Chapter 5. Depending upon the materials forming the bilayer, three different PCM device types are fabricated viz. GeTe/SnTe, GeTe/SnSe and Ge_2Se_3/SnTe.

6.4.22 Metal 3 Deposition

Metal 3 is the top electrode of the PCM cell. As discussed in Chapter 5, 35 nm of DC sputter deposited Ta is used for this purpose. Again, the Ta/Sn-Ch/Ge-Ch stack is etched via ion milling the details of which have been described previously.

SEM images of some circuits designed using the process described above are illustrated below.

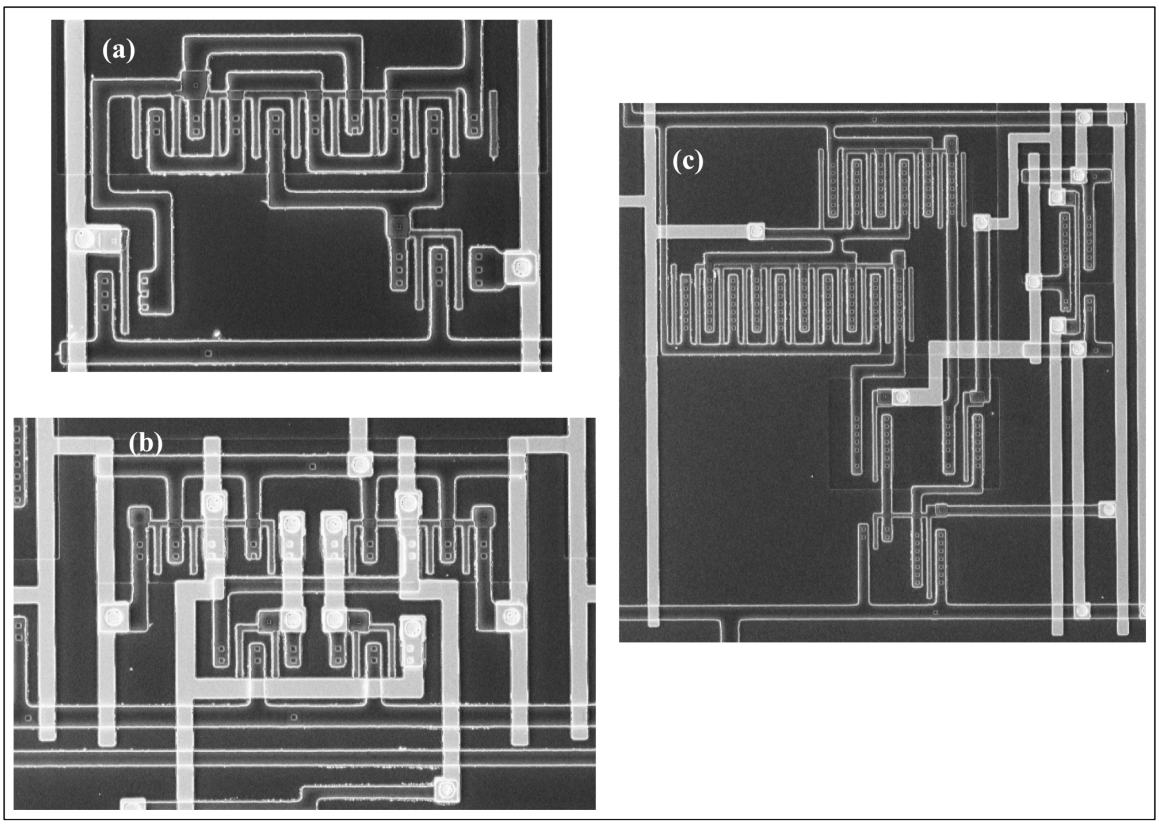


Figure 6.10: SEM images of fabricated circuits, (a) adjustable current source, (b) sense amplifier, (c) write drive circuit

6.5 Electrical Testing of MOS Integrated PCM Devices

Two different types of electrical tests have been carried out in order to characterize the behavior of MOS connected PCM devices. They are as described below:

6.5.1 DC Current Sweep

This test entails forcing current through the PCM top electrode while keeping the NMOS gate at 5 V and grounding the NMOS source and substrate. The set-up is illustrated in Fig. 6.11(a) and Fig. 6.11(b). Thus, this type of measurement is essentially a test of the success of the integration process. The PCM active area is not visible on the SEM image due to the fact that the metal directly over it is covered with 1 µm thick PR.

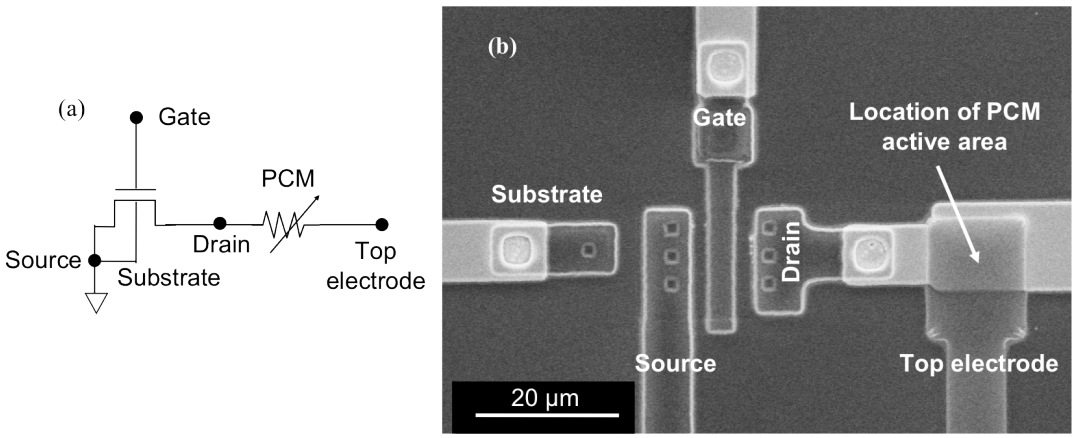


Figure 6.11: NMOS connected PCM, (a) schematic, (b) SEM image

Fig. 6.12(a) – (c) illustrate the *I-V* characteristics of NMOS integrated PCM cell. It is observed that all as-deposited devices demonstrate threshold switching, indicating that the integration has been successful. The GeTe/SnTe cell exhibits ohmic characteristics in the SET state. On the other hand, the SET state *I-V* curve of the Ge_2Se_3/SnTe cell is not completely linear. This is because, the initial *I-V* sweep for this bilayer has been carried out from 0 – 250 µA, a magnitude which may not be high enough to completely crystallize the material. A similar observation is noted for the GeTe/SnSe cell. The SET *I-V* curve for this device features two states: a low current state till ~1 V and a high current state starting at ~1.2 V. In this case, the low current state may define the R_{SET}, while the high current region may determine the resistance when the device is ON.

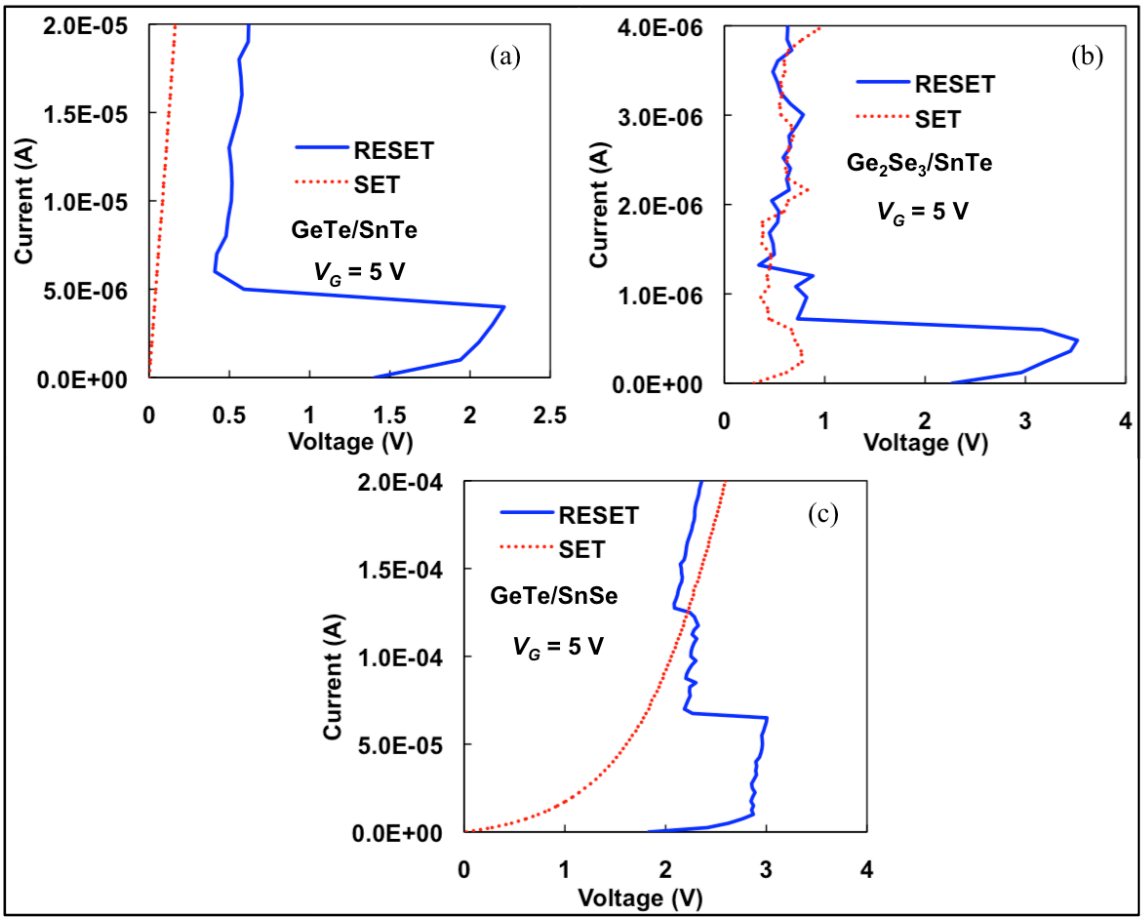


Figure 6.12: *I-V* characteristics of NMOS connected PCM devices employing bilayers of, (a) GeTe/SnTe, (b) Ge_2Se_3/SnTe and (c) GeTe/SnSe

Table 6.1 lists the average values of V_t and current at V_t for the three, bilayer PCM - NMOS integrated cells, measured for several devices over the surface of the wafer.

Table 6.1: Parameters extracted from RESET state *I-V* characteristics of NMOS connected PCM cells

Bilayer	**Average V_t (V)**	**Average current at V_t (μA)**
GeTe/SnTe	2.21	4.45
Ge_2Se_3/SnTe	3.54	0.46
GeTe/SnSe	3.28	52.5

It is observed that as compared to the two terminal devices, the V_t for SnTe based integrated devices is only slightly higher while that for GeTe/SnSe integrated devices is appreciably lower indicating

that, in the absence of an isolation transistor, SnSe based devices are highly susceptible to static buildup or discharge which significantly alters the switching conditions of these devices.

6.5.2 MOSFET Output Characteristics

The variation in the output characteristics of an NMOS with the change in state (RESET or SET) of a series connected PCM cell is illustrated in the figures below.

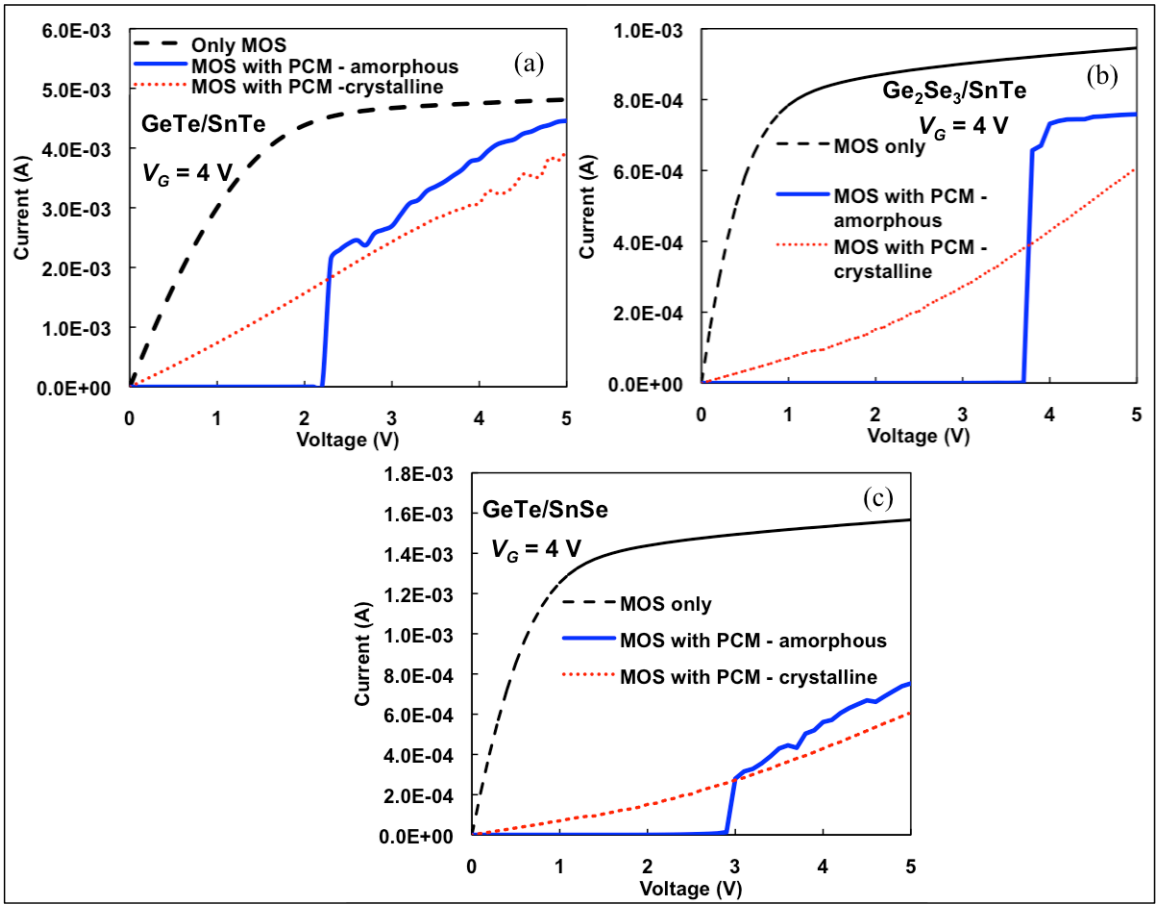


Figure 6.13: I_{DS} v/s V_{DS} characteristics of PCM connected NMOS for bilayers of, (a) GeTe/SnTe, (b) Ge_2Se_3/SnTe, (c) GeTe/SnSe

It is observed that, when the gate voltage V_G is kept constant at a value higher than the NMOS threshold voltage, the drain current I_{DS} is negligible for increasing values of drain voltage V_{DS} till, a

particular voltage is reached, at which, the drain current abruptly increases. It is ascertained that this increase in I_{DS} takes place in the neighborhood of the PCM threshold voltage. On the other hand, when the series connected PCM cell is crystalline, the resulting I_{DS} vs V_{DS} curve exhibits the characteristics of a MOS with a (comparatively) high resistance connected in series with the drain.

6.6 Conclusions

A process for integrating bilayer PCM technology with 2 μm CMOS has been designed and developed. The baseline RIT CMOS process has been modified to incorporate 12 levels of photolithography, 3 levels of metal and the addition of PCM as a BEOL process. On electrical testing, NMOS connected PCM devices exhibit switching behavior. The effect of the state (SET/RESET) of the series connected PCM cell on the drain current of the NMOS has also been investigated. It has been demonstrated that threshold switching of the PCM cell is essential in order to observe any change in MOS drain current with variation in drain voltage.

References for Chapter 6

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Chapter 7: Summary and Conclusions

The main objective of this research study was to examine bilayer chalcogenide based materials for phase change memory applications and explore their integration with CMOS technology. To this end three major research goals were identified. They have been previously listed in Chapter 3. These goals have been achieved as explained below:

1. The first research goal was to perform a material characterization of the behavior of bilayer structures and to identify processing constraints, if any, in their subsequent integration. This task has been accomplished by, (a) employing X-ray diffraction to analyze residual stress in the stacks, (b) using time resolved XRD to examine phase transition and (c) performing transmission electron microscopy and parallel energy loss spectroscopy to investigate material inter-diffusion and volatilization due to thermal treatments.

2. The second research goal was to fabricate a two terminal bilayer PCM cell. For this purpose, cell layouts have been designed and a corresponding mask set has been generated at the SMFL at RIT. Devices with Ta electrodes and low stress PECVD Si_xN_y as inter-level dielectric have been fabricated. The materials have been selected and the processes have been designed in order to be compatible with the CMOS process. Upon electrical testing it has been determined that, all devices exhibit threshold switching and memory switching behavior. Devices composed of stacks of GeTe/SnTe, Ge_2Se_3/SnTe and GeTe/SnSe have been subjected to programming pulses to examine their memory functionality. By the application of suitable voltage pulses, RESET state switching has been accomplished in devices of all three bilayers. These devices have demonstrated a high resistance contrast, of almost three orders of magnitude for SnTe based devices, between RESET and SET states.

3. The third goal of this research was to integrate the fabricated two terminal, bilayer PCM cell with CMOS, using the RIT process as a baseline. This objective has been achieved by developing a 2 μm CMOS process with 3 levels of metal and 12 levels of photolithography, characterized by twin well formation, LOCOS isolation, 31 nm n^+ polysilicon gate, 5 V power supply and $V_{Tn} = |V_{Tp}| = 1$ V. The PCM cell has been vertically integrated on top of an NMOS as a BOEL process. Again, layout design and mask fabrication has been carried out in house. On electrical testing, all NMOS connected PCM devices have been found to exhibit threshold switching and memory switching behavior, thus indicating successful integration.

The items discussed described above provide a broad overview of the accomplishments of this research work. At a finer level, the following original contributions have been made by this work to the knowledge base of bilayer chalcogenide based phase change memory.

1. An in depth analysis using XRD and PEELS has provided substantial new information on the material characteristics of the bilayer chalcogenides. It has been demonstrated that stacked Ge_2Se_3/SnTe and GeTe/SnTe phase change memory films exhibit both structural and compositional dependency on annealing temperature. The structural transformation of the bottom layer results in a temperature dependent residual stress. Clear evidence of thermally induced Ge, Sn and chalcogen inter-diffusion, has been discerned via TEM and PEELS studies. By the incorporation of a Sn layer the phase transition characteristics of Ge-chalcogenide thin films can be tuned. Sn ions play a major role in reducing the crystallization temperature of the Ge-chalcogenide layer, and this property can be exploited for low power PCM applications. Severe film decomposition, volatilization and metallic Sn phase separation has been observed at high temperatures (> 500˚C) in the absence of a capping layer. The presence of Al_2O_3 has been found to mitigate some of these effects.

2. To the best of the author's knowledge, this work has been the first to demonstrate integration of PCM cells comprising of a layered arrangement with CMOS. The process developed, includes 3 levels of metal wherein TEOS is employed as the pre-metal dielectric and the first inter-level dielectric, while low stress PECVD Si_xN_y serves as the second inter-level dielectric. Since the chalcogenide material is surrounded by Si_xN_y instead of SiO_2, oxidation issues are precluded. Successful implementation of a multi-level metal process lies in maintaining a good (low resistivity, ohmic) contact between the different metal levels. In order to achieve this, a magnetically enhanced reactive ion etch technique employing CHF_3, CF_4 and O_2 has been used to etch the contact cuts and via 1. A combination MERIE/wet-etch process is used to facilitate good contact of active and gate regions with metal 1 (Al). An aggressive MERIE process is employed to create the vias between Al and metal 2 (Ta). In order to ensure good contact between them, a sputter etch/deposit process has been developed, which first removes the Al_2O_3 present on the Al surface and then deposits Ta without a vacuum break. The resulting NMOS integrated PCM devices demonstrate both threshold and memory switching.

The following publications and presentations have been disseminated through this study:

Journal

1. A. Devasia, F. Bai, S. Gupta, S. Kurinec, M. Davis and K. Campbell, "Analyzing Residual Stress in Bilayer Phase Change Memory Films", *Thin Solid Films*, vol. 517, pp. 6516-6519, 2009.

2. A. Devasia, S. Kurinec, K. Campbell, S. Raoux, "Influence of Sn Migration on Phase Transition in GeTe and Ge_2Se_3 Thin Films", *Applied Physics Letters*, vol. 96, pp. 1419081-1419083, 2010.

3. A. Devasia, D. MacMahon, S. Raoux, K. Campbell, S. Kurinec, "Material Inter-Diffusion in Bilayer GeTe/SnSe Phase Change Memory Films", to be submitted to *Applied Physics Letters*.

4. A. Devasia, D. McMahon, S. Raoux, K. Campbell, S. Kurinec, "TEM and PEELS investigation of Ge_2Se_3/SnTe bilayers", to be submitted to *Applied Physics Letters*.

Conference Presentations

1. A. Devasia, F. Bai and S. Kurinec, "Residual stress Analysis of Stacked SnTe/Ge_2Se_3 Phase Change Memory Films using VANTEC-2000 Area Detector," *Bruker AXS: Excellence in X-ray Diffraction*, 2007.

2. A Devasia and S. Kurinec, "Modeling the Thermal Behavior of Chalcogenide based Phase Change Memory Cell", presented at the *International Device Research Symposium*, College Park, MD, Dec. 2007.

2. F. Bai, S. Gupta, A. Devasia, S. Kurinec, M. Davis and K. Campbell, "Investigation of phase transition in stacked Ge-chalcogenide/SnTe phase-change memory films", in *Nanophase and Nanocomposite Materials V*, edited by S. Komarneni, K. Kaneko, J.C. Parker, and P. O'Brien (Mater. Res. Soc. Symp. Proc. Volume 1056E, Warrendale, PA, 2008), 1056-HH11-70.

Recommendations for Future Work

1. In this work, the smallest size PCM cell fabricated has an active area of 1 μm^2. Since programming current is a function of PCM-bottom electrode/heater contact area, reducing the PCM cell active area is crucial. To this end, an attempt has already been initiated by the author and others [1, 2] to develop a void transfer process for patterning nm scale features originally introduced by Breitwisch et al. [3].

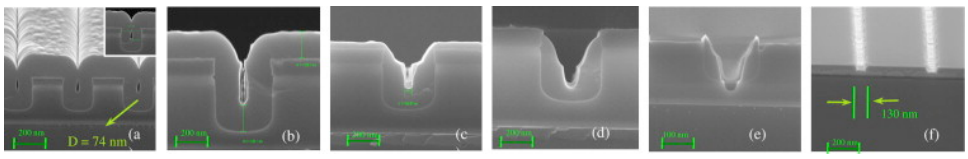

Figure 7.1: Creation of voids and nanoscale pores using the process described in [1]

The technique involves intentional creation of keyhole voids using a conformal chemical vapor deposition followed by a controlled etch-back to form nanoscale pores. This method provides features that are independent of the lithographically defined parent holes and exhibit lower critical dimension

variations. Using this approach, pores with a diameter of 130 nm from an original lithographically defined size of 714 nm have already been demonstrated using *i*-line lithography (Fig. 7.1). The next step would be to incorporate this process as the active area defining step in the two-terminal device fabrication process proposed in this thesis.

The smaller size would make it easier to electrically characterize the devices in terms of switching, endurance and reliability, due to lower requirements of current and voltage. These devices when incorporated with the developed CMOS process may result in achieving competitive memory densities.

2. Modeling the behavior of a PCM device can facilitate a better understanding of the switching operations in the cell and the optimization of cell designs. The author has carried out preliminary modeling of a lance like cell employing Ge_2Se_3/SnSe bilayer and a heater element, which is separate from the electrodes [4].

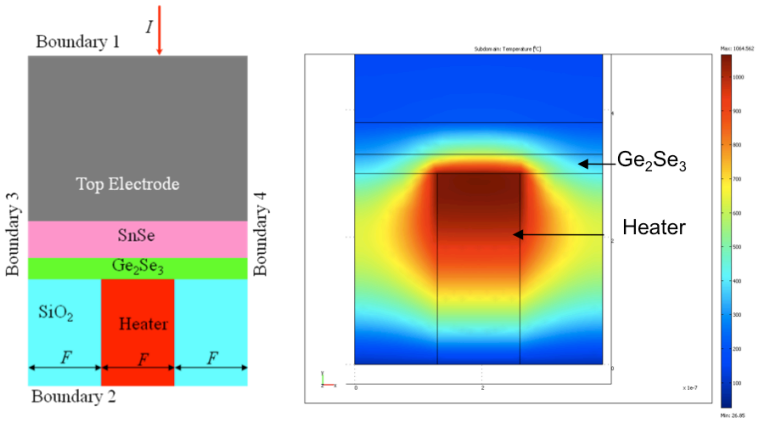

Figure 7.2: Thermal modeling of Ge_2Se_3 based PCM cell employing polysilicon heater [4]

A 2D transient heat diffusion equation using Dirichlet boundary conditions was used to examine the temperature field in the PCM cell required to melt the Ge_2Se_3 layer. The phase change of Ge_2Se_3 was triggered by joule heating. The thermal behavior exhibited by the cell upon melting of Ge_2Se_3 was explored at several technology nodes. In addition, the suitability of doped polysilicon and TiN/W as

potential heater materials was also examined. This model however did not take into consideration any inter-diffusion between the top and bottom layers. A future extension of this work would be to incorporate the information gleaned from material characterization of bilayer PCM structures in order to model, the electrical, thermal and phase change dynamics together, in a bilayer PCM cell.

3. A third extension of this work could be to develop the SPICE model of a bilayer PCM cell. As with any other RAM, PCM cells will include various peripheral circuits and the design of these circuits significantly affects the performance of the memory. Since IC design mostly relies on simulators such as SPICE, which includes effective models of devices, a PCM IC design would require a SPICE model of the PCM element. Thus, the model can be used to test the integrity of the circuit design and predict circuit behavior before committing to manufacturing.

References for Chapter 7

1. G. Josan, A. Devasia, S. Rommel, S. Kurinec, "Simulation and verification of void transfer patterning (VTP) technique for nm-scale features", *Microelectronic Engineering*, doi:10.1016/j.mee.2010.08.020.

2. G. S. Josan, "Design, Development and Simulation of Sub-Lithographic Process for Patterning nm Scale Features," M. S. Thesis, Dept. Elect. Microelectron. Eng., Rochester Inst. Technol., Rochester, NY, 2009.

3. M. Breitwisch, T. Nirschl, C.F. Chen, Y. Zhu, M.H. Lee, M. Lamorey, G.W. Burr, E. Joseph, A. Schrott, J.B. Philipp, R. Creek, T.D. Happ, S.H. Chen, S. Zaidi, P. Flaitz, J. Bruley, R. Dasaka, B. Rajendran, S. Rossnagel, M. Yang, Y.C. Chen, R. Bergmann, H.L. Lung and C. Lam, "Novel Lithography-Independent Pore Phase Change Memory," *Symp. VLSI Technol. Dig. Tech. Papers*, pp. 100-101, 2007.

4. A. Devasia and S. Kurinec, "Modeling the Thermal Behavior of Chalcogenide based Phase Change Memory Cell", presented at the *International Device Research Symposium*, College Park, MD, Dec. 2007.

Appendix A: MOSFET Parameter Extraction

This section provides a brief description of the electrical testing carried out on various PMOS and NMOS devices fabricated using the 2 µm, 3 metal level CMOS process discussed in Chapter 6.

MOSFET Transfer Characteristics

The transfer characteristics illustrate the variation in drain current I_D (I_{DS}) with gate voltage V_G (V_{GS}). They are obtained by maintaining a constant source-drain voltage V_{DS}, varying the gate voltage and measuring the corresponding drain current. The characteristics are indicative of the gate bias required to turn on the transistor and the behavior of drain current with change in gate bias.

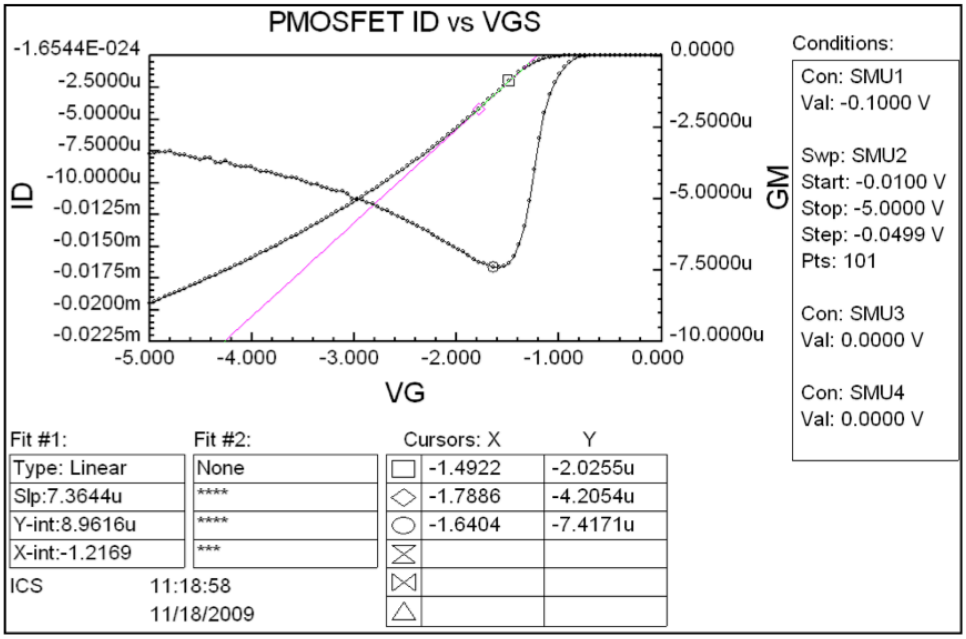

Figure A.1: I_{DS}-V_{DS} characteristics of 4/8 PMOS

The curve in pink represents the ideal I_D-V_G curve, while the overlapping curve in black represents the actual I_D-V_G curve. The initial portion of the black curve is linear. Hence the threshold voltage is extrapolated by extending this line till it intersects the voltage axis. This gives the value of the gate

bias required to turn on the PMOS i.e. the V_T. From the graph shown in Fig. A.1 it is seen that V_T = -1.2169V.

It is observed that after V_T, drain current does not increase linearly with gate voltage but falls off (as exhibited by the leaning over of the black curve - actual characteristic). This is attributed to two factors viz. mobility degradation and source/drain series resistance. Mobility degradation occurs at the semiconductor-oxide interface due to increased scattering caused by the surface roughness and also due to columbic attraction with the fixed charges in the gate oxide. As the voltage on the gate is increased, it draws the carriers closer to the oxide-Si interface where they are most influenced by the interfacial roughness leading to a decrease in mobility and hence reduction in drain current.

The effect of source/drain resistance on the drain current can be understood by considering Fig. A.2.

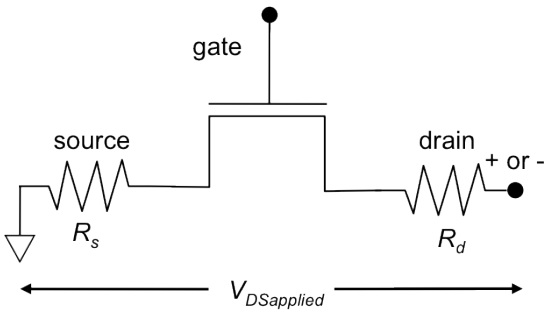

Fig. A.2: Definition of source drain series resistance

It is seen that the applied source drain voltage ($V_{DSapplied}$) is between the external metal contacts. However the source and drain regions have some inherent resistance given by R_s and R_d respectively. Hence the actual V_{DS} is lesser than $V_{DSapplied}$ due to the ohmic drop in the source and drain resistances. As applied gate bias increases, more current will flow and hence there will be a larger drop across R_s and R_d, thus reducing the drain current.

Similar observations are made for an NMOS shown in Fig. A.3. The threshold voltage is determined to be $V_T = 0.3791$ V.

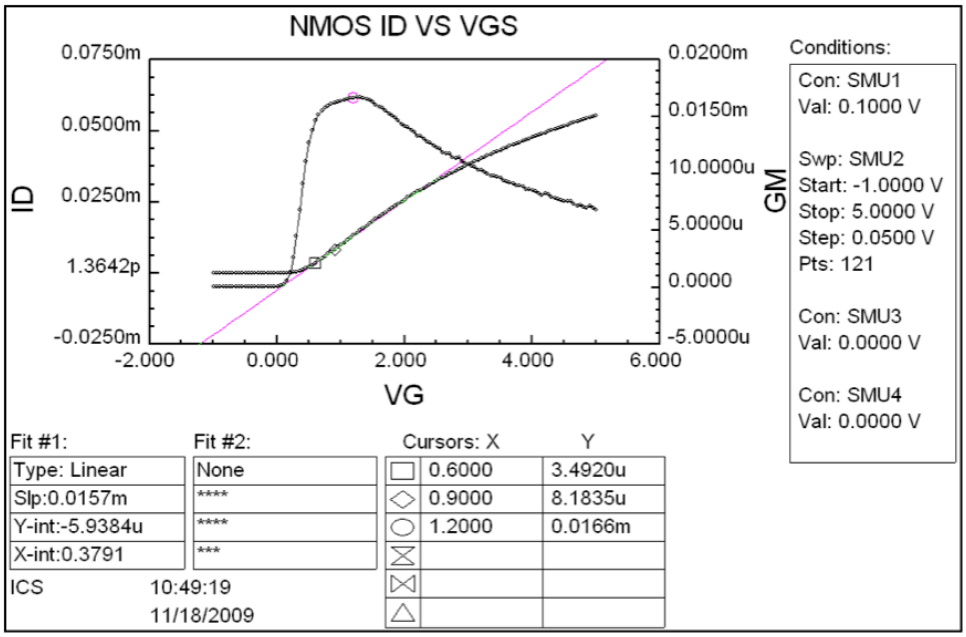

Figure A.3: I_{DS}-V_{DS} characteristics of 4/8 NMOS

Subthreshold Characteristics

The subthreshold characteristics determine how quickly the transistor turns off when the gate voltage is reduced below threshold. This relationship is obtained by plotting the log of the drain current v/s the gate voltage. The sub threshold characteristics for a 4/8 NMOS are illustrated in Fig. A.4. The sub threshold swing is the inverse of the slope of the log (I_D) v/s V_D curve. It is given by,

$$S = \frac{2.3}{B}$$

Here B is the slope and the factor of 2.3 accounts for the conversion from $\log_{10}$ to natural log. The smaller the value of S the faster will the transistor shut off. For the device shown in Fig. A.4, $S = 105.28$ mV/dec.

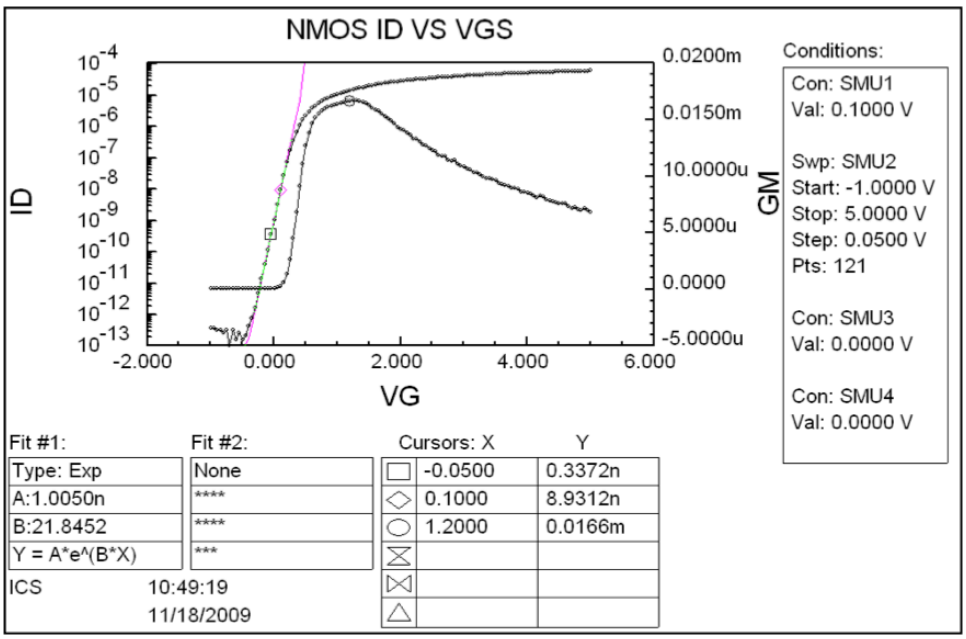

Figure A.4: Determination of subthreshold swing

MOS Output Characteristics

These characteristics consist of a family of curves. Each curve shows the variation in drain current (I_D) with drain voltage (V_D) for a particular value of gate bias (V_{GS}).

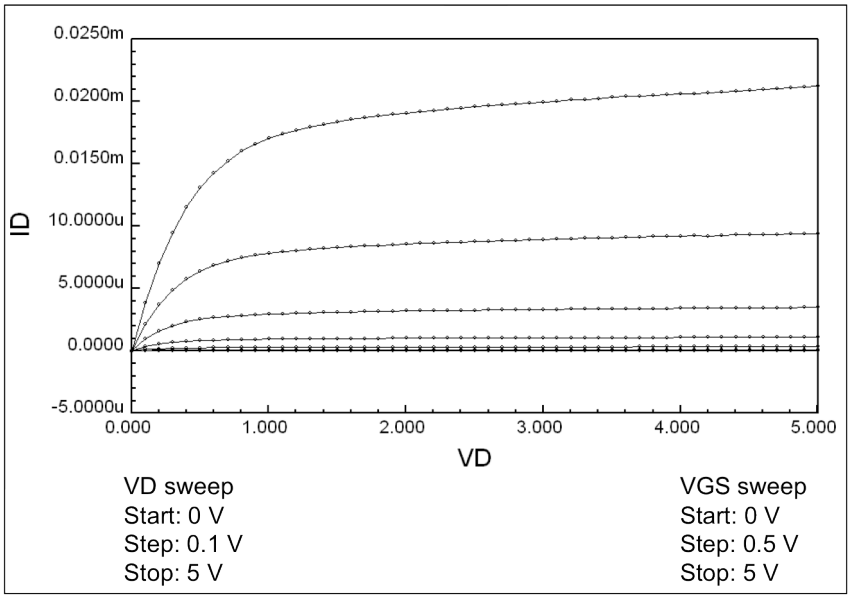

Figure A.5: NMOS family of curves

For $V_G < V_T$, the drain current is zero. As V_G increases beyond V_T, drain current also rises. This increase is linear up to a particular value of drain bias after which saturation sets in. The characteristics for a 4/8 NMOS and a 4/32 PMOS are illustrated in Fig. A.5 and Fig. A.6 respectively.

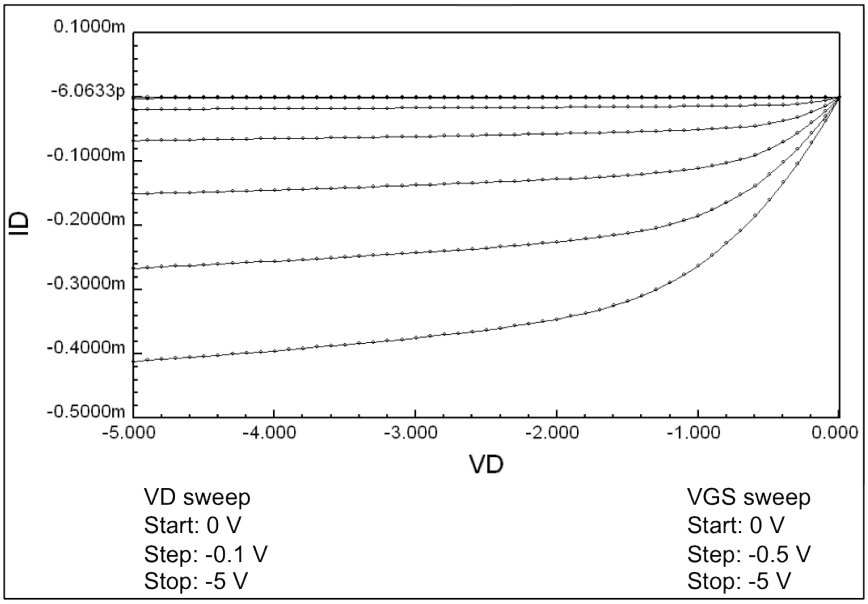

Figure A.6: PMOS family of curves

Appendix B: Netlist used for HSPICE Simulations

The netlist employed for simulating the various circuits discussed in Chapter 6 using HSPICE is presented below.

```
*Include SPICE model files
.include smfl_nmos.cir
.include smfl_pmos.cir

*********Defining sub-circuits*************

*Defining inverter sub-circuit
.SUBCKT INV 11 22 33
*node 11 is supply
*node 22 is input
*node 33 is output
M1 33 22 11 11 RITSMFLP49 L=2U W=32U ad=256e-12 as=256e-12 pd=80e-6 ps=80e-6 nrd=0.001 nrs=0.001
M2 33 22 0 0 RITSMFLN49 L=2U W=10U ad=80e-12 as=80e-12 pd=36e-6 ps=36e-6 nrd=0.001 nrs=0.001
.ENDS


*Defining Tri-state buffer for read ckt
.SUBCKT TBRC 5 1 4 3
*node 5 is VDD
*node 1 is input
*node 4 is enable
*node 3 is output
M1 3 2 1 5 RITSMFLP49 L=2U W=32U ad=256e-12 as=256e-12 pd=80e-6 ps=80e-6 nrd=0.001 nrs=0.001
M2 1 4 3 0 RITSMFLN49 L=2U W=10U ad=80e-12 as=80e-12 pd=36e-6 ps=36e-6 nrd=0.001 nrs=0.001
XINV1 5 4 2 INV
.ENDS


*Defining Tri-state buffer for WRITE ckt
.SUBCKT TBWC 5 1 4 3
*node 5 is VDD
*node 1 is input
*node 4 is enable
*node 3 is output
M1 3 2 1 5 RITSMFLP49 L=2U W=240U ad=1920e-12 as=1920e-12 pd=496e-6 ps=496e-6 nrd=0.001 nrs=0.001
```

```
M2 1 4 3 0 RITSMFLN49 L=2U W=75U ad=600e-12 as=600e-12 pd=166e-6 ps=166e-6 nrd=0.001
nrs=0.001
XINV1 5 4 2 INV
.ENDS


*Defining Sense Amplifier
.SUBCKT SA 1 2 12 5 9
*node 1 will be connected to READ enable
*node 2 will be connected to reference current
*node 12 will be connected to device
*node 5 will be connected to negative input of comparator
*node 9 will be connected to positive input of comparator
M4 2 2 1 1 RITSMFLP49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
M6 3 2 1 1 RITSMFLP49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
VS1 3 5 0
VS3 5 6 0
CR 6 0 0.5P
M3 4 2 1 1 RITSMFLP49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
VS2 4 7 0
M8 7 7 0 0 RITSMFLN49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
VS4 9 8 0
M7 8 7 0 0 RITSMFLN49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
VS5 5 16 0
M10 16 10 0 0 RITSMFLN49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
M9 10 10 0 0 RITSMFLN49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
VS6 11 10 0
M5 11 12 1 1 RITSMFLP49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
M2 13 12 1 1 RITSMFLP49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
VS7 13 9 0
VS8 9 14 0
CM 14 0 0.5P
M1 12 12 1 1 RITSMFLP49 L=2U W=10U ad=100e-12 as=100e-12 pd=40e-6 ps=40e-6 nrd=0.001
nrs=0.001
.ENDS


*Defining beta multiplier circuit
.SUBCKT BMC 1 2 3
*node 1 is VDD
*node 2 is from drain of MSU3
*node 3 is from source of MSU3
```

```
*M3 3 2 1 1 RITSMFLP49 L=2U W=30U  nrd=0.001 nrs=0.001
*M4 2 2 1 1 RITSMFLP49 L=2U W=30U  nrd=0.001 nrs=0.001
*M1 3 3 5 5 RITSMFLN49 L=2U W=10U  nrd=0.001 nrs=0.001
*M2 2 3 4 4 RITSMFLN49 L=2U W=40U  nrd=0.001 nrs=0.001
*VS1 5 0 0
*VS2 4 0 0

M1 2 2 1 1 RITSMFLP49 L=4U W=60U  nrd=0.001 nrs=0.001
M2 3 3 2 1 RITSMFLP49 L=4U W=60U  nrd=0.001 nrs=0.001
M3 3 3 0 0 RITSMFLN49 L=4U W=20U  nrd=0.001 nrs=0.001
.ENDS

*DEfining Pre-amp circuit
.Subckt PREAMP 1 2 3 5 9 6 7
*node 1 is vdd
*node 2  goes to gate of M3 of DECCKT
*node 3 goes to gate of M4 of DECCKT
*node 5 is from gate of M4 of bmc
*node 9 is from gate of M2 of BMC
*node 6 is positive terminal
*node 7 is negavtive terminal
M1 2 2 1 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M2 3 3 1 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M3 2 6 8 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M4 3 7 8 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M5 10 6 4 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M6 11 7 4 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M7 4 5 1 1 RITSMFLP49 L=4U W=20U  nrd=0.001 nrs=0.001
M8 8 9 0 0 RITSMFLN49 L=4U W=20U  nrd=0.001 nrs=0.001
M9 3 10 0 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M10 10 10 0 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M11 11 11 0 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M12 2 11 0 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
.ENDS


*Defining decision circuit
.SUBCKT DECCKT 1 2 3 4 5
*node 1 is VDD
*node 2 is gate of M3
*node 3 is gate of M4
*node 4 is drain of M3
*node 5 is drain of M4
M3 4 2 1 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M4 5 3 1 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M5 4 4 6 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M6 4 5 6 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M7 5 4 6 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M8 5 5 6 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
Mshift 6 6 0 0 RITSMFLN49 L=10U W=10U  nrd=0.001 nrs=0.001
.ENDS
```

```
*Defining output buffer
.SUBCKT OB 1 2 4 5 6
*NODE 1 IS VDD
*node 2 is from vbiasp
*node 4 is from drain of M4 of DECCKT
*node 5 is from drain of M3 of DECCKT
*node 6 is output
M1 3 2 1 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M2 7 4 3 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M3 6 5 3 1 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M4 7 7 0 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
M5 6 7 0 0 RITSMFLN49 L=2U W=20U  nrd=0.001 nrs=0.001
.ENDS

*Defining inverter sub-circuit
.SUBCKT INVC 11 22 33
*node 11 is supply
*node 22 is input
*node 33 is output
M1 33 22 11 11 RITSMFLP49 L=2U W=40U  nrd=0.001 nrs=0.001
M2 33 22 0 0 RITSMFLN49 L=2U W=20U nrd=0.001 nrs=0.001
.ENDS

*Defining Comparator circuit
*XSTUP 1 2 3 STUP
.SUBCKT COMP 1 6 7 11
*node 1 is VDD
*node 6 is positive terminal
*node 7 is negative terminal
*node 11 is output
XBMC 1 2 3 BMC
XPREAMP 1 4 5 2 3 6 7 PREAMP
XDECCKT 1 4 5 8 9 DECCKT
XOB 1 2 9 8 10 OB
XINVC 1 10 11 INV
.ends


*Defining Adjustable current source
.SUBCKT CS 1 2 6 7
*node 1 is vdd
*node 2 is external voltage
*node 6 is connection to M4 of SA
*node 7 is connection to dummy
M1 8 2 9 9 RITSMFLN49 w=16u l=2u nrd=0.001 nrs=0.001
M2 3 3 1 1 RITSMFLP49 w=48u l=2u nrd=0.001 nrs=0.001
M3 10 3 1 1 RITSMFLP49 w=48u l=2u nrd=0.001 nrs=0.001
M6 4 4 12 12 RITSMFLN49 w=16u l=2u nrd=0.001 nrs=0.001
M7 6 4 7 7 RITSMFLN49 w=16u l=2u nrd=0.001 nrs=0.001
VS3 3 8 0
VS4 9 0 0
```

```
VS5 10 4 0
VS7 12 0 0
.ENDS


*Defining AND gate
.SUBCKT AND 1 2 3 6
*node 1 is VDD
*node 2 is 1st input
*node 3 is 2nd input
*node 6 is output
M1 4 2 1 1 RITSMFLP49 L=2U W=32U  nrd=0.001 nrs=0.001
M2 4 3 1 1 RITSMFLP49 L=2U W=32U  nrd=0.001 nrs=0.001
M3 4 2 5 0 RITSMFLN49 L=2U W=14U  nrd=0.001 nrs=0.001
M4 5 3 0 0 RITSMFLn49 L=2U W=14U  nrd=0.001 nrs=0.001

M6 6 4 1 1 RITSMFLP49 L=2U W=32U  nrd=0.001 nrs=0.001
M7 6 4 0 0 RITSMFLn49 L=2U W=10U  nrd=0.001 nrs=0.001
.ENDS


*Defining Write Drive ckt
.SUBCKT WD 1 2 7 13
*node 1 is VDD
*node 2 is Data
*node 7 is WE
*node 13 is output
*****INVERTER*******
XINV 1 2 3 INV
**********************
*****Low-Current Path*****
M1 6 7 0 0 RITSMFLN49 w=32u l=2u nrd=0.001 nrs=0.001
M2 6 2 5 5 RITSMFLP49 w=32u l=2u nrd=0.001 nrs=0.001
M3 4 4 1 1 RITSMFLP49 w=32u l=2u nrd=0.001 nrs=0.001
M4 8 4 1 1 RITSMFLP49 w=128u l=2u nrd=0.001 nrs=0.001
**************************
*****High-Current Path*****
M5 11 7 0 0 RITSMFLN49 w=10u l=2u nrd=0.001 nrs=0.001
M6 11 3 10 10 RITSMFLP49 w=32u l=2u nrd=0.001 nrs=0.001
M7 9 9 1 1 RITSMFLP49 w=32u l=2u nrd=0.001 nrs=0.001
M8 12 9 1 1 RITSMFLP49 w=4096u l=2u nrd=0.001 nrs=0.001
*****************************
******Dummy Sources in WD ckt********
VS1 4 5 0
VS2 8 13 0
VS3 9 10 0
VS4 12 13 0
.ENDS
*******************
```

```
*Defining 3 input NOR for Bit line decoder
.SUBCKT NOR3 1 2 3 4 5
*node 1 is VDD
*node 2 is 1st input
*node 3 is 2nd input
*node 4 is 3rd input
*node 5 is output
M1 6 2 1 1 RITSMFLP49 L=2U W=32U  nrd=0.001 nrs=0.001
M2 7 3 6 6 RITSMFLP49 L=2U W=32U  nrd=0.001 nrs=0.001
M3 5 4 7 7 RITSMFLP49 L=2U W=32U  nrd=0.001 nrs=0.001
M4 5 2 0 0 RITSMFLN49 L=2U W=10U  nrd=0.001 nrs=0.001
M5 5 3 0 0 RITSMFLN49 L=2U W=10U  nrd=0.001 nrs=0.001
M6 5 4 0 0 RITSMFLN49 L=2U W=10U  nrd=0.001 nrs=0.001
.ENDS


*Defining Bit Line Decoder
.SUBCKT BLDEC 1 2 3 4 8 9 10 11 12 13 14 15
*node 1 is VDD
*node 2 is 1st input
*node 3 is 2nd input
*node 4 is 3rd input
*node 8 is Q0
*node 9 is Q1
*node 10 is Q2
*node 11 is Q3
*node 12 is Q4
*node 13 is Q5
*node 14 is Q6
*node 15 is Q7
XINV1 1 2 5 INV
XINV2 1 3 6 INV
XINV3 1 4 7 INV
XNOR1 1 2 3 4 8 NOR3
XNOR2 1 2 3 7 9 NOR3
XNOR3 1 2 6 4 10 NOR3
XNOR4 1 2 6 7 11 NOR3
XNOR5 1 5 3 4 12 NOR3
XNOR6 1 5 3 7 13 NOR3
XNOR7 1 5 6 4 14 NOR3
XNOR8 1 5 6 7 15 NOR3
.ENDS

*Defining word line decoder
.SUBCKT WLDEC 1 2 3 4
*node 1 is supply(VDD)
*node 2 is input
*node 3 is output(inverted input)
*node 4 is output (same as input)
XINV1 1 2 3 INV
XINV2 1 3 4 INV
```

```
.ENDS

*Defining SenseAmp/Read circuitry SAC
.SUBCKT SAC 1 2 13 14 9 12
*node 1 is VDD
*node 2 is read enable
*node 13 is connection from decoder
*node 14 is Vext of adjustable current source
*node 9 is connection to device
*node 12 is output of OPamp
XSA 2 3 4 5 6 SA
XTBRC1 1 7 8 9 TBRC
XTBRC2 1 10 8 11 TBRC
Xcomp 1 6 5 12 COMP
XAND 1 13 2 8 AND
XCS 1 14 11 15 CS
VIREF 15 0 0
VS1 3 10 0
VS2 4 7 0
.ENDS


*Defining Write circuitry WDC
.SUBCKT WDC 1 3 2 5 8
*node 1 is VDD
*node 3 is write enable
*node 2 is data (0 or 1)
*node 5 is connecton from decoder
*node 8 is connection to device
XWD 1 2 3 4 WD
XAND 1 5 3 6 AND
XTBWC 1 7 6 8 TBWC
VS1 4 7 0
.ENDS

*********Defining circuit connections*******************

*******BL Decoder**********
XBLDEC 1 2 3 4 5 6 7 8 9 10 11 12 BLDEC
****************************************

*******Sense Amp # 1**************
XSAC1 1 13 5 14 15 16 SAC
**********************************

*******Word Drive # 1*************
XWDC1 1 17 18 5 15 WDC
**********************************

*******Device-> Row=1 column=1*******
VS1 15 19 0
```

```
VS2 20 21 0
M1 21 22 23 23 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS3 23 0 0
**********************************

**********WL Decoder*********
XWLDEC 1 25 22 24 WLDEC
****************************

*******Device-> Row=2 column=1*******
VS4 15 26 0
VS5 27 28 0
M2 28 24 29 29 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS6 29 0 0
**********************************

**********Sense Amp # 2************
XSAC2 1 13 6 30 31 32 SAC
**********************************

**********Word Drive # 2************
XWDC2 1 17 18 6 31 WDC
**********************************

*******Device-> Row=1 column=2******
VS7 31 33 0
VS8 34 35 0
M3 35 22 36 36 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS9 36 0 0
**********************************

*******Device-> Row=2 column=2******
VS10 31 37 0
VS11 38 39 0
M4 39 24 40 40 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS12 40 0 0
**********************************

********Sense Amp # 3***************
XSAC3 1 13 7 41 42 43 SAC
**********************************

******Word Drive # 3*****************
XWDC3 1 17 18 7 42 WDC
**************************************

********Device-> Row=1 column=3******
VS13 42 44 0
VS14 45 46 0
M5 46 22 47 47 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS15 47 0 0
```

```
**********************************

*********Device-> Row=2 column=3********
VS16 42 48 0
VS17 49 50 0
M6 50 24 51 51 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS18 51 0 0
*****************************************

********Sense Amp # 4***********
XSAC4 1 13 8 52 53 54 SAC
*****************************************

***********Word Drive # 4**************
XWDC4 1 17 18 8 53 WDC
**********************************

*********Device-> Row=1 column=4********
VS19 53 55 0
VS20 56 57 0
M7 57 22 58 58 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS21 58 0 0
*****************************************

************Device-> Row=2 column=4*******
VS22 53 59 0
VS23 60 61 0
M8 61 24 62 62 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS24 62 0 0
**************************************

********Sense Amp # 5***********
XSAC5 1 13 9 63 64 65 SAC
*****************************************

***********Word Drive # 5**************
XWDC5 1 17 18 9 64 WDC
**********************************

*********Device-> Row=1 column=5********
VS25 64 66 0
VS26 67 68 0
M9 68 22 69 69 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS27 69 0 0
*****************************************

************Device-> Row=2 column=5*******
VS28 64 70 0
VS29 71 72 0
M10 72 24 73 73 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS30 73 0 0
```

```
************************************

********Sense Amp # 6**********
XSAC6 1 13 10 74 75 76 SAC
****************************************

**********Word Drive # 6**********
XWDC6 1 17 18 10 75 WDC
**********************************

*********Device-> Row=1 column=6********
VS31 75 77 0
VS32 78 79 0
M11 79 22 80 80 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS33 80 0 0
****************************************

**********Device-> Row=2 column=6*******
VS34 75 81 0
VS35 82 83 0
M12 83 24 84 84 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS36 84 0 0
****************************************

********Sense Amp # 7**********
XSAC7 1 13 11 85 86 87 SAC
****************************************

**********Word Drive # 7**********
XWDC7 1 17 18 11 86 WDC
**********************************

*********Device-> Row=1 column=7********
VS37 86 88 0
VS38 89 90 0
M13 90 22 91 91 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS39 91 0 0
****************************************

**********Device-> Row=2 column=7*******
VS40 86 92 0
VS41 93 94 0
M14 94 24 95 95 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS42 95 0 0
****************************************

********Sense Amp # 8**********
XSAC8 1 13 12 96 97 98 SAC
****************************************

**********Word Drive # 8**********
```

```
XWDC8 1 17 18 12 97 WDC
**********************************

*********Device-> Row=1 column=8********
VS43 97 99 0
VS44 100 101 0
M15 101 22 102 102 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS45 102 0 0
**************************************

***********Device-> Row=2 column=8*******
VS46 97 103 0
VS47 104 105 0
M16 105 24 106 106 RITSMFLN49 L=2U W=32U nrd=0.001 nrs=0.001
VS48 106 0 0
**************************************


*********load capacitances********
CL1 16 0 1P
CL2 32 0 1P
CL3 43 0 1P
CL4 54 0 1P
CL5 65 0 1P
CL6 76 0 1P
CL7 87 0 1P
CL8 98 0 1P
**************************************

****Main power supply********
VDD 1 0 5
******************************

********Selection of device to be read or written into*************
*BL selection
VA 2 0 0
VB 3 0 0
VC 4 0 0
*WL selection
Vin 25 0 0
**********************************************************************

*************************Read Circuitry controls*********************
        VRE 13 0 0 ****read enable*******

        ******Adjustable current sources for Sense amplifiers*******
        VEXT1 14 0 0
        VEXT2 30 0 0
        VEXT3 41 0 0
        VEXT4 52 0 0
        VEXT5 63 0 0
```

```
        VEXT6 74 0 0
        VEXT7 85 0 0
        VEXT8 96 0 0
        ************************************************************
**********************************************************************

**********Write Circuitry Controls**********
VWE 17 0 5 ******WRITE ENABLE******
VDATA 18 0 0 ******selects to write 0 or 1********
**********************************************************************

***********Devices/Resistances**********
R1 19 20 1K
R2 26 27 1K
R3 33 34 1K
R4 37 38 1K
R5 44 45 1K
R6 48 49 1K
R7 55 56 1K
R8 59 60 1K
R9 66 67 1K
R10 70 71 1K
R11 77 78 1K
R12 81 82 1K
R13 88 89 1K
R14 92 93 1K
R15 99 100 1K
R16 103 104 1K
**********************************************************


*.DC VEXT1 0 5 0.01
.DC VDATA 0 5 0.01
*.tran 0.1n 200n
.OPTION POST
.PLOT
.print dc I(VS2)
.END
```