TANOS Charge-Trapping Flash Memory Structures

A Senior Design
by Spencer Pringle

5/8/15

R·I·T
ROCHESTER INSTITUTE OF TECHNOLOGY

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- Planned Devices (Modified Adv_CMOS 150 Process)

Charge Trap Flash (CTF) Basics

- CTF architecture is similar to Floating Gate EEPROM, with one significant difference:
  - The conductive Polysilicon storage layer (floating gate) is replaced with an insulating Silicon Nitride storage layer.

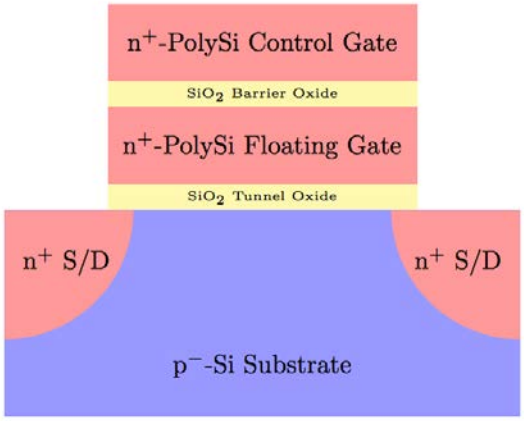


Figure 1. EEPROM

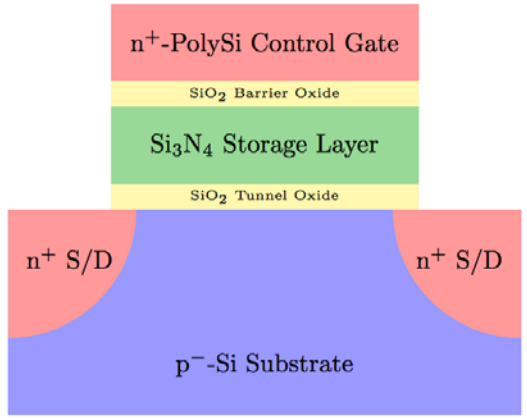


Figure 2. Charge-Trapping Flash (SONOS)

Charge Trap Flash (CTF) Basics

- Technology names are based on a Top-Down acronym of the Gate Stack materials.

SONOS: (Silicon, Oxide, Nitride, Oxide, Silicon

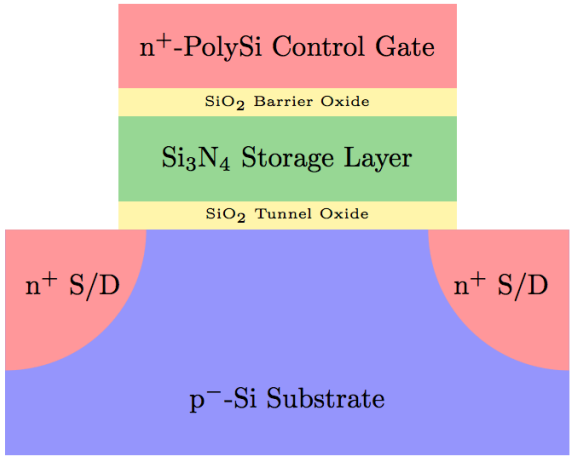


Figure 2. Charge-Trapping Flash (SONOS)

TANOS: (TaN, Alumina, Nitride, Oxide, Silicon)

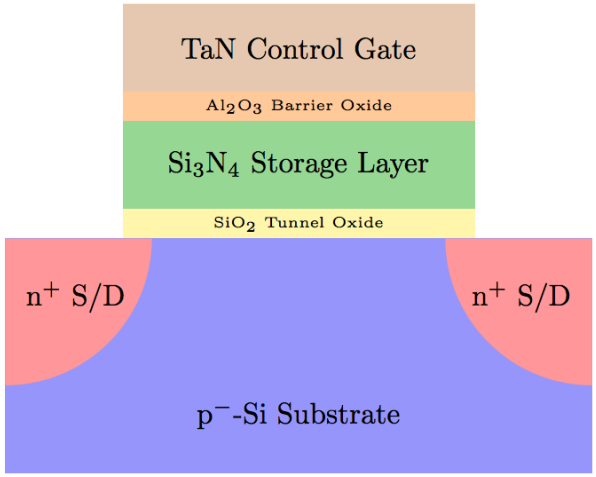


Figure 3. Charge-Trapping Flash (TANOS)

Why TANOS Charge-Trapping Flash (CTF)?

Advantages over Floating Gate EEPROM:

- **Lower Power Consumption**: Charge-Trap requires lower write-erase voltages than EEPROM and consume less power.
- **Faster Speeds:** Samsung has reported a minimum of 20% increase in CTF speed over similar Floating Gate devices.
- **Improved Reliability**: Due to lower voltages, less tunnel oxide stress, and higher data retention in the insulating storage layer.
- **Improved Scalability:** Owing to higher charge density in the storage layer allowing for thinner films and better gate control.

TANOS vs SONOS:

- Tantalum Nitride provides improved gate control
- Alumina improves data retention and suppresses erase saturation.

Objectives

Successfully show charge trapping characteristics by fabricating one or both of:

- C-V Devices of the TANOS Stack on p- well doped Si Wafers
- NMOS Devices using a modification of the Adv_CMOS 150 Process.

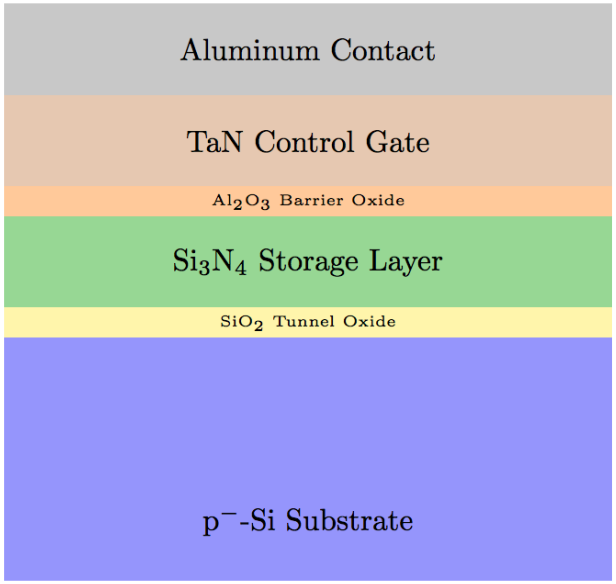


Figure 4. TANOS C-V Structure

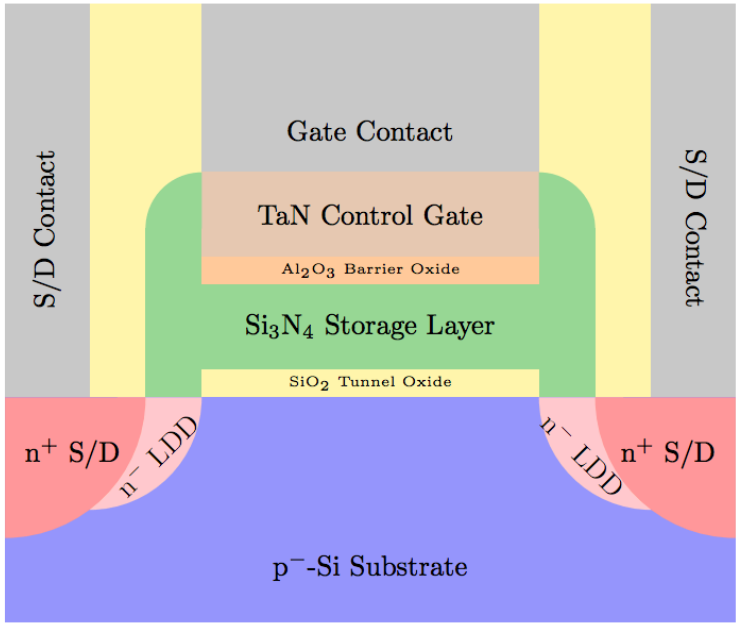


Figure 5. Adv-CMOS 150 Modified TANOS

Process Flow: "Modified AdvCMOS150"

TANOS Charge Trap Flash Device Process Plan

1. Ox05 – Pad Oxide 500Å, Tube 4
2. CV02 – 1500Å Nitride (LPCVD)
3. PH03 – Level 1 – STI (ASML & SSI)
4. ET29 – Nitride Etch (Lam 490)
5. ET07 – Ash (Gasonics)
6. CL01 – RCA
7. OX04 – First STI Oxide Tube 1 (Bruce)
8. ET06 – Oxide Etch (Wet, HF Bench)
9. OX04 - 2nd Oxide Tube 1 (Bruce)
10. ET19 – Hot Phos Nitride Etch (Wet, Phos Bench)
11. PH03 – P-Well Level 3 (ASML & SSI)
12. IM01 – 8E13 B11 80KeV (Varian)
13. ET07 – Ash (Gasonics)
14. OX06 – Well Drive, Tube 1 (Bruce)
15. PH03 – NMOS Vt (ASML & SSI)
16. IM01 – 3E12, P31, 30KeV (Varian)
17. ET07 – Ash (Gasonics)
18. ET06 – Etch 500Å Pad Ox (10:1 BOE, 45Secs, Rinse SRD)
19. CL01 – Pre-Gate RCA Clean
20. ET06 – Pre-Gate HF Etch
21. TANOS GATE
    a. 30, 50, 70Å Oxide, Tube 1 (Bruce) 3 runs, 2 wafers each
    b. 75Å Nitride, (LPCVD) all wafers, equal spacing
    c. 100, 130Å Alumina, (CHA E-Beam) 2 runs, 3 each
    d. 375nm TaN, (CVC 601) all wafers
22. PH03 – Level 6 Poly Gate (ASML & SSI) (Current Device Wafer State)
23. ET08 – Plasma or 4-step Gate Etch (Drytech/LAM490/LAM4600)
24. ET07 – Ash (Gasonics)
25. CL01 – RCA
26. OX05 – Gate Stack Re-Ox, 500Å, Tube 4 (P-5000?)
27. PH03 – Level 8 – N-LDD (ASML & SSI)
28. IM01 – 4E13, P31, 60KeV (Varian)
29. ET07 – Ash (Gasonics)
30. CL01 – RCA Clean
31. CV01 – Nitride Spacer Dep (LPCVD)
32. ET39 – Sidewall Spacer Etch (Drytech)
33. PH03 – Level 9, N+ D/S (ASML & SSI)
34. IM01 – 4E15, P31 60KeV (Varian)
35. ET07 – Ash (Gasonics)
36. PH03 – Level 9, P+ D/S (ASML & SSI)
37. IM01 – 4E15, B11 50KeV (Varian)
38. ET07 – Ash (Gasonics)
39. CL01 – RCA Clean
40. OX08 – DS Anneal, Tube 2, 3 (Bruce)
41. ET06 – Silicide Pad Ox Etch (Wet)
42. ME03 – HF Dip & Ti Sputter (50:1 HF Dip, CVC601 Sputter)
43. RT01 – RTP 1 min, 800C (AG610 RTP TISI1.RCP, 1min, 650C)
44. CV03 – TEOS, (P-5000)
45. PH03 – Level 11 – CC (185mJ/cm^2, DEVFAC.RCP)
46. ET06 – CC Etch (Drytech FACCUT)
47. ET07 – Ash (Gasonics)
48. CL01 – RCA Clean
49. LPCVD Tungsten Plugs?????
50. ME01 – Aluminum Sputter (.5um, CHA Flash Evap)
51. PH03 – Level 12-metal 1 (ASML & SSI) (**C-V Mask for C-V Wafers**)
52. ET15 – Al Etch (Wet Al Etch)
53. ET07 – Ash (Gasonics)
54. CV03 – TEOS P-5000
55. PH03 – Via (ASML & SSI)
56. ET26 – Via Etch
57. ET07 – Ash
58. Tungsten Plugs????
59. ME01 – Al Deposition Metal 2 (CVC601 or PE4400)
60. PH03 - Metal 2
61. ET15 - Al Etch (LAM4600)
62. ET07 – Ash (Gasonics)
63. SI01 – Sinter

C-V Wafers Only:

64. ET16 – TaN Etch (Drytech Quad)
65. ET06 – PRS Strip (PRS2000 Positive Resist Strip – Wet)

"New to RIT" Processes:

- Tantalum Nitride Sputter in CVC 601
  - Tantalum target reactively sputtered in Nitrogen partial pressure ambient (N_2/Ar)
- Tantalum Nitride Etching in Drytech
  - Using pre-existing Tantalum etch – SF_6 reactive ion.
- Very thin Alumina Deposition in CHA E-Beam
  - Correction factor for Film Thickness Monitor
- Very thin Silicon Nitride in ASM LPCVD Tube 2
  - Typical Recipes were designed for ~2500Å, this device requires ~100Å.

Film Optimization:

Silicon Dioxide(SiO_2): Bruce Dry O_2, Drytech Quad

- Test film deposition, 2 wafers, no dummies, separated by 10 slots, with 11 minute N2O and O2 soaks on C-V Stack wafers exhibit very uniform VASE measurements of 57.5Å +- .5Å, with reasonable refractive index measurements.

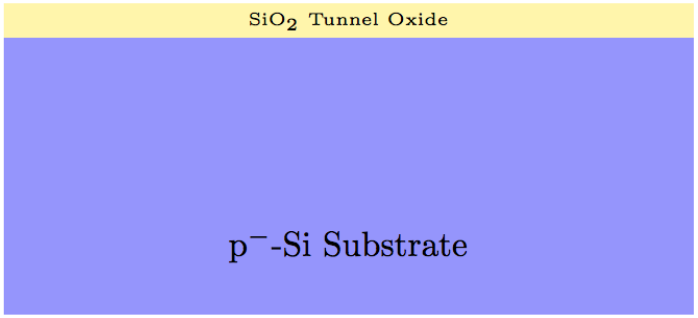


Figure 6. TANOS C-V Structure - Tunnel Oxide

Wafers were processed yielding thicknesses of 38Å, 52Å, and 68Å (1 CV and 2 Device Wafers each).

When etching, Drytech Quad recipes are well known for etching oxide and should be used instead of HF. Such a thin oxide would be easily undercut with a wet etch.

Film Optimization:

Silicon Nitride (Si_3N_4): LPCVD Tube 2 & LAM 490

- Working from the 6” LPCVD Stoichiometric Nitride Recipe, a test film deposition with 1 minute soak reveals appropriate refractive index and very uniform ~110Å film.

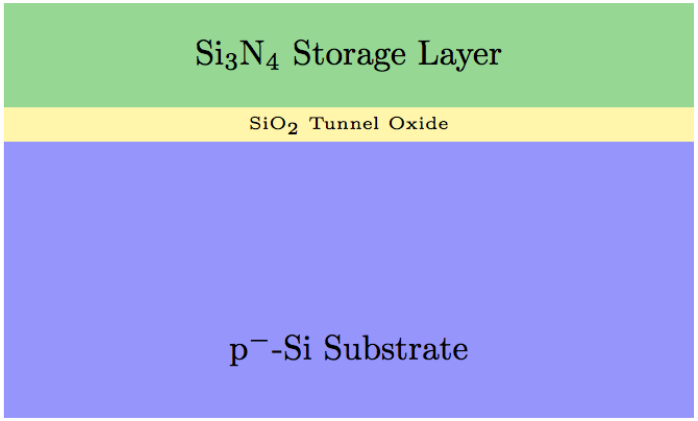


Figure 7. TANOS C-V Structure - Storage Layer

C-V and Device Wafers were coated simultaneously w/ 1 minute soak, yielding very uniform ~75Å film.

Existing LAM 490 nitride etch recipe should be used for etching when patterning Device wafers.

Film Optimization:

Alumina (Al_2O_3): CHA E-beam & HF Wet Etch

- Preliminary films targeting 100Å and 200Å deposited and show promising film properties.

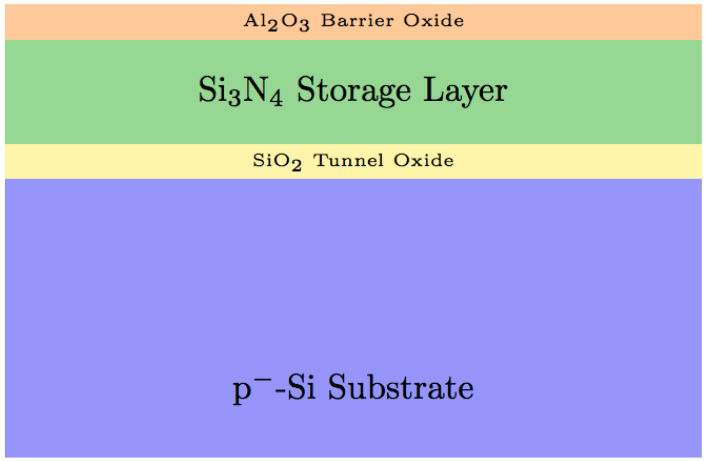
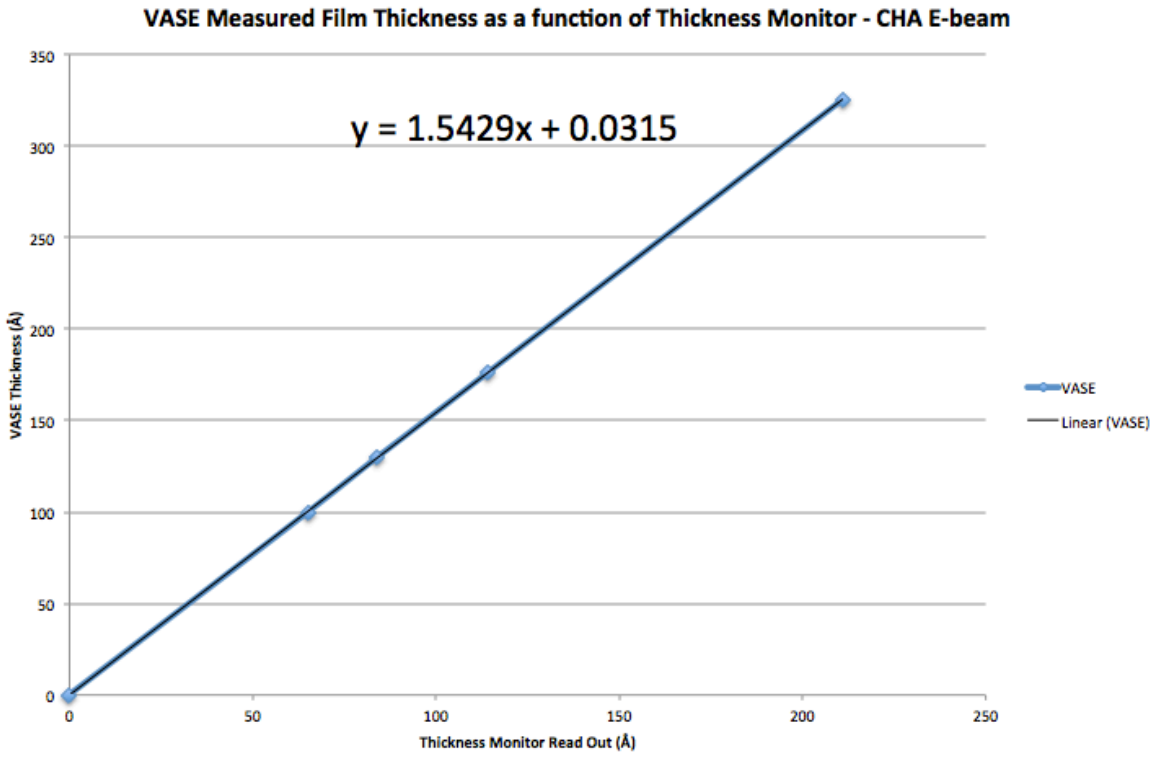


Figure 8. TANOS C-V Structure - Barrier Oxide

- Films are very uniform
- Film thickness monitors report 114Å and 211Å and Woollam VASE reports 160Å and 325Å, respectively.
- Characterization using Woollam VASE, reports reasonable responses for n and k, but point to composition or surface roughness issues, seemingly confirmed by XRR on 3/6.
- XRR exhibits low oscillation, pointing to similar thickness values but with high surface roughness.
- Alumina Deposited on C-V Wafers, ~110Å

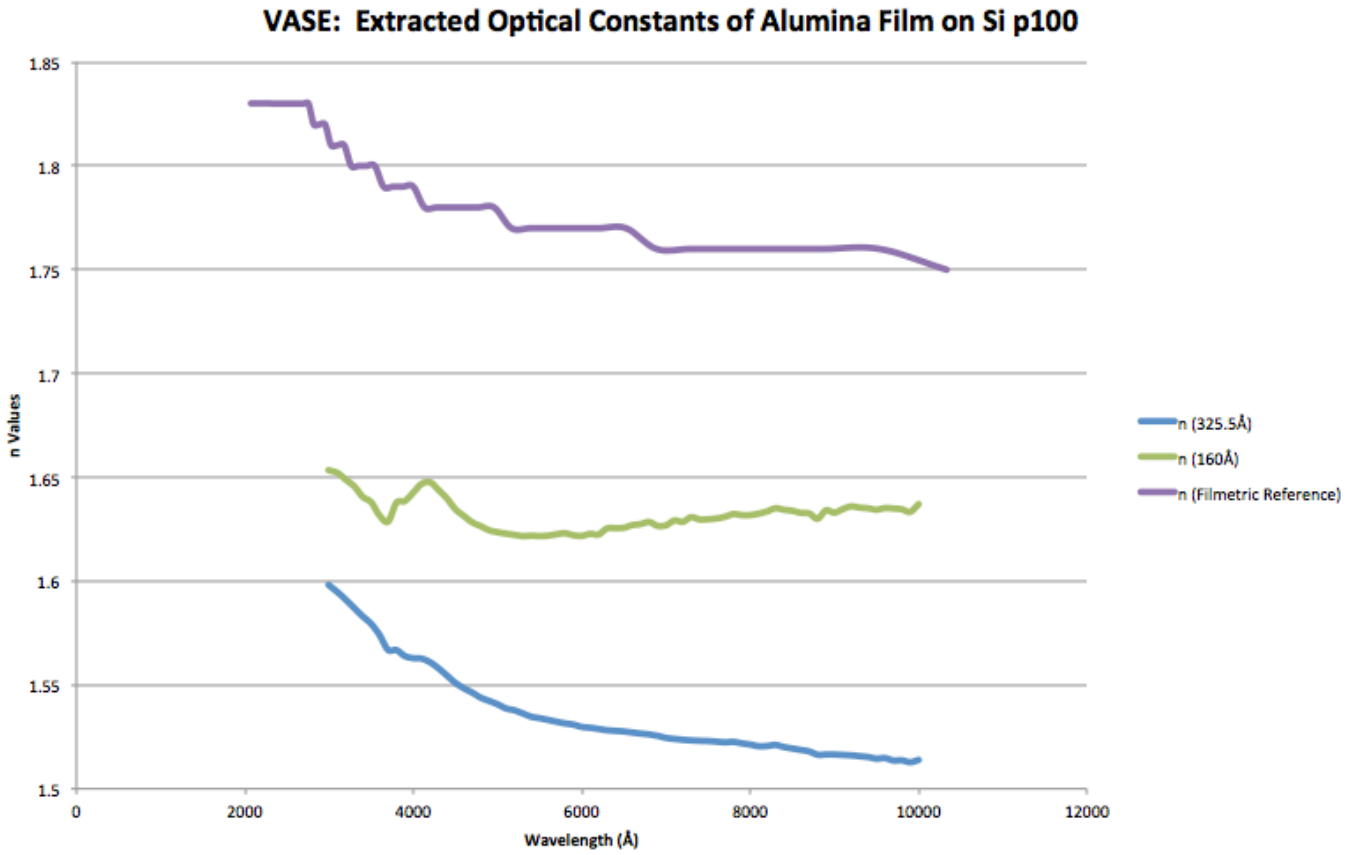
Film Optimization:

Alumina (Al_2O_3): CHA E-beam Scaling Factor



Film Optimization:

- Alumina (Al_2O_3)



Film Optimization:

Tantalum Nitride: CVC 601 (4” Target) & Drytech Quad

- Successfully deposited test film with characteristics which seem to describe a relatively stoichiometric and pure film. Auger and further Spectroscopic analysis will be performed to verify.

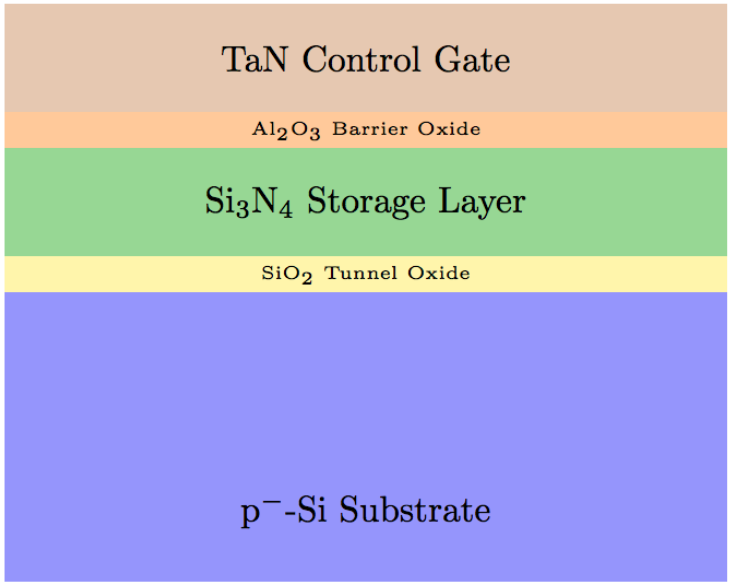
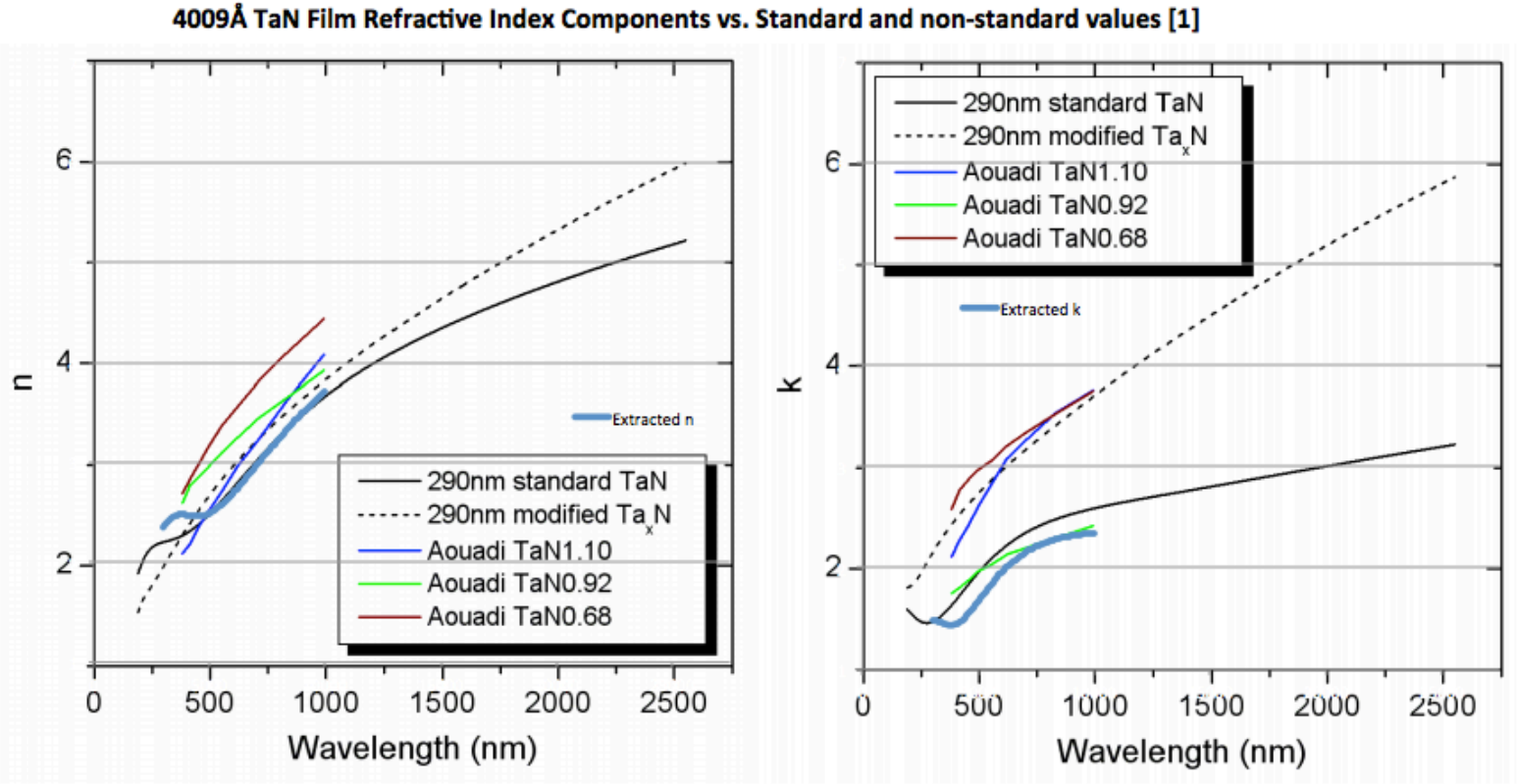


Figure 9. TANOS C-V Structure - Control Gate

- Sputter on the C-V wafers were relatively uniform (in center) and yield ~2500A thickness with similar optical properties to test films.

Film Optimization:

- TaN Optical Properties Extracted from VASE

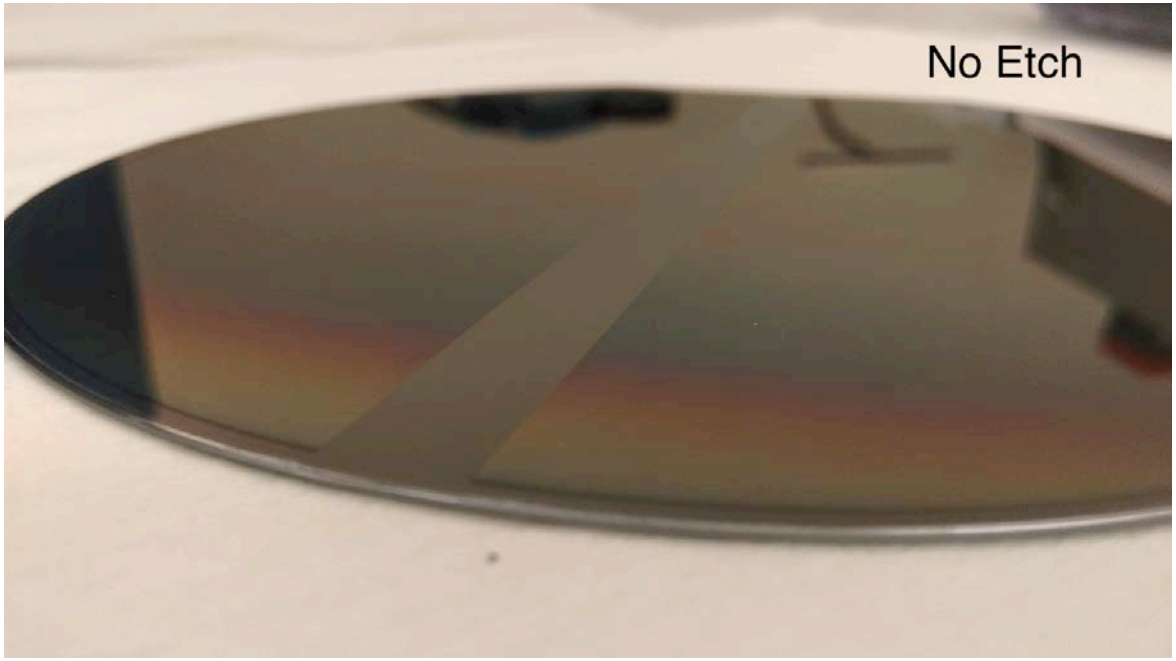


[1]T. Waechtler, B. Gruska, S. Zimmerman, S. Schulz and T. Gessner, 'Optical Properties of Sputtered Tantalum Nitride Films Determined by Spectroscopic Ellipsometry', Qucosa, 2015. [Online]. Available: http://www.qucosa.de/fileadmin/data/qucosa/documents/5145/data/ellips.pdf. [Accessed: 25- Feb- 2015].

Film Optimization:

Tantalum Nitride: CVC 601 & Drytech Quad

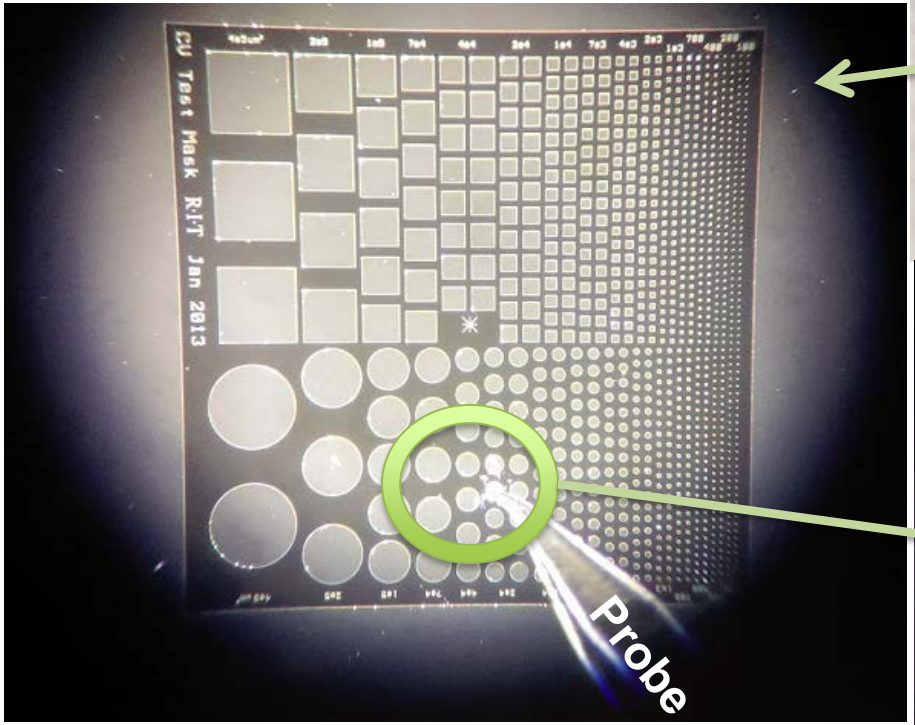
- Etching performed in the Drytech Quad, using existing Tantalum etch as a basis; etch rates were significantly slower than for pure Ta (~277Å/min).

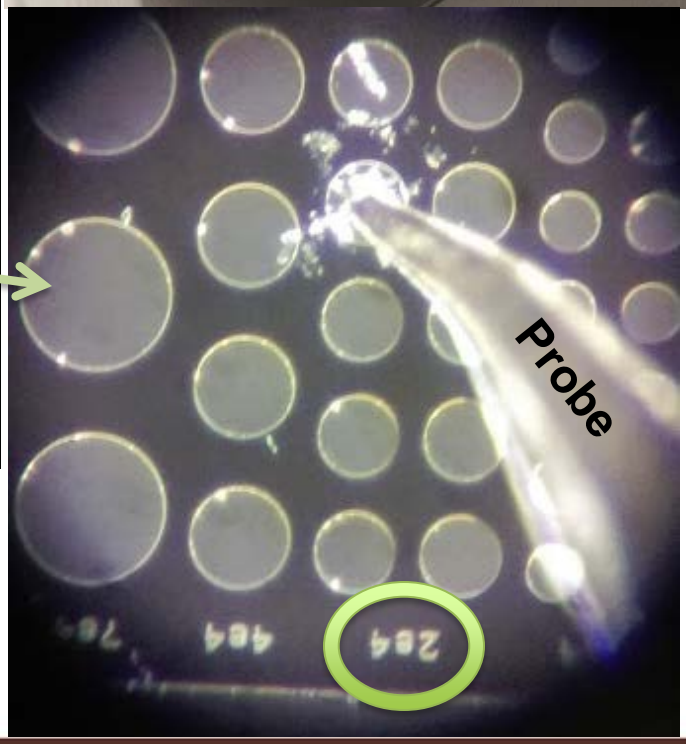


Capacitors

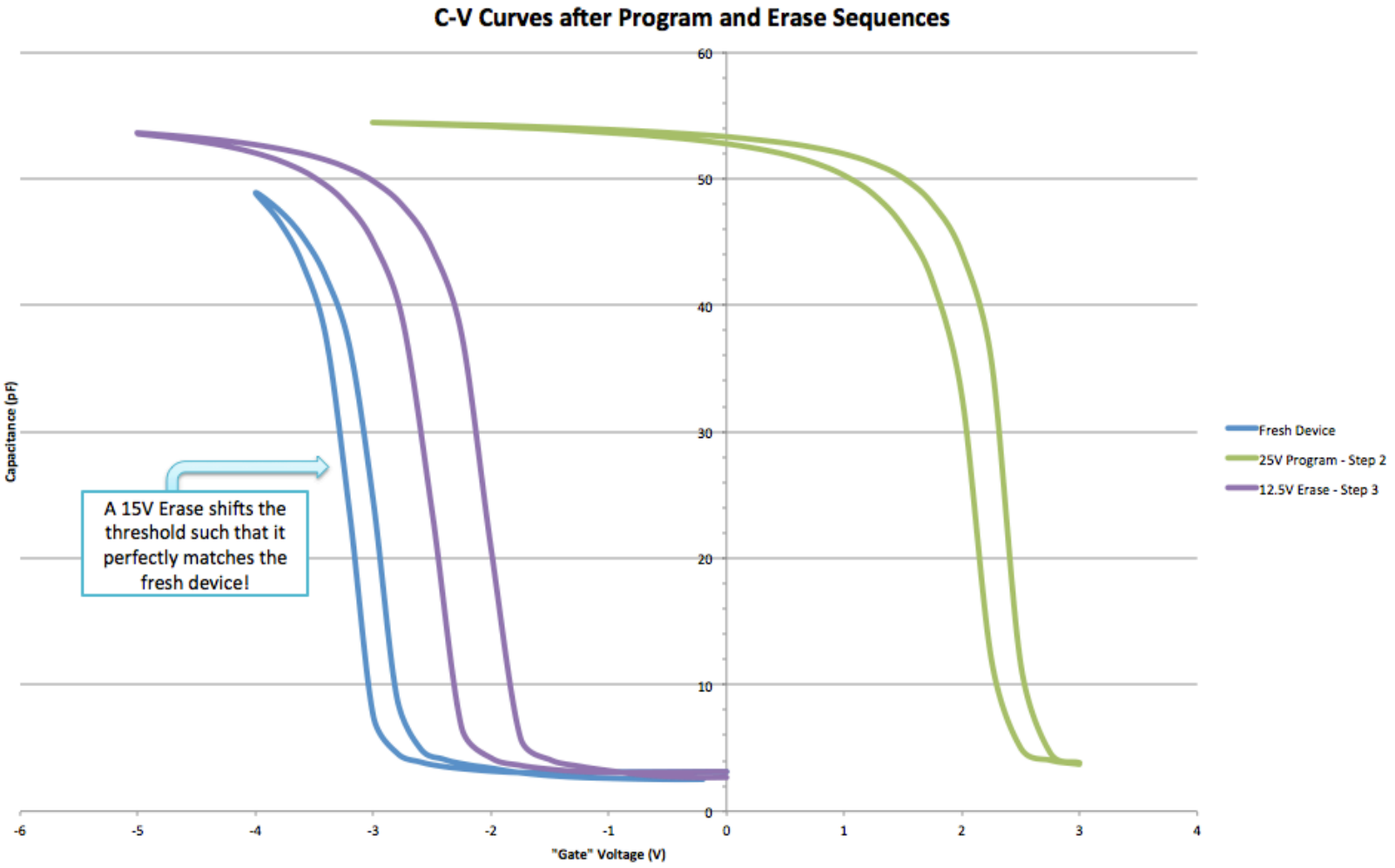
- Following process flow listed on slide 7:
  - Well dope followed by well-drive anneal, RCA clean
  - 3 Levels of Oxide grown (38Å, 52Å, 68Å, 1 wafer each)
  - Nitride deposited (~75Å All) with Device wafers
  - Alumina (~110Å All) deposited with device wafers
  - TaN (2500Å All) deposited as per Film Optimization
  - Aluminum (~5000Å All) deposited with CHA Flash Evaporator.
  - GCA C-V Mask patterned, Aluminum wet etched, and TaN etched with Drytech Quad.
  - Wet photoresist strip (PRS2000) performed, rather than O_2 plasma ash, to avoid formation of Ta_2O_5 after etch.

Capacitors





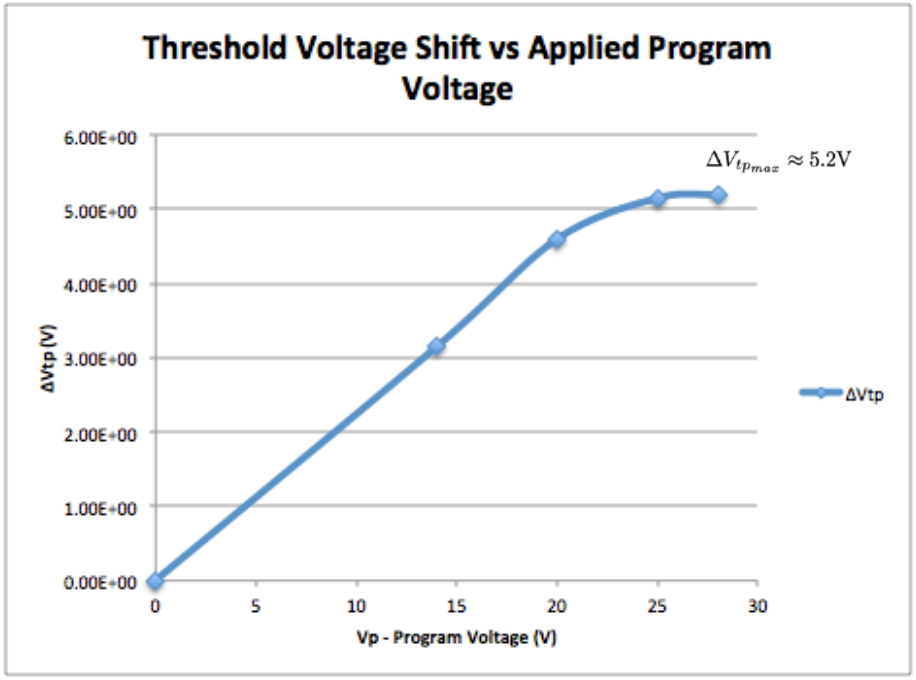
Capacitors

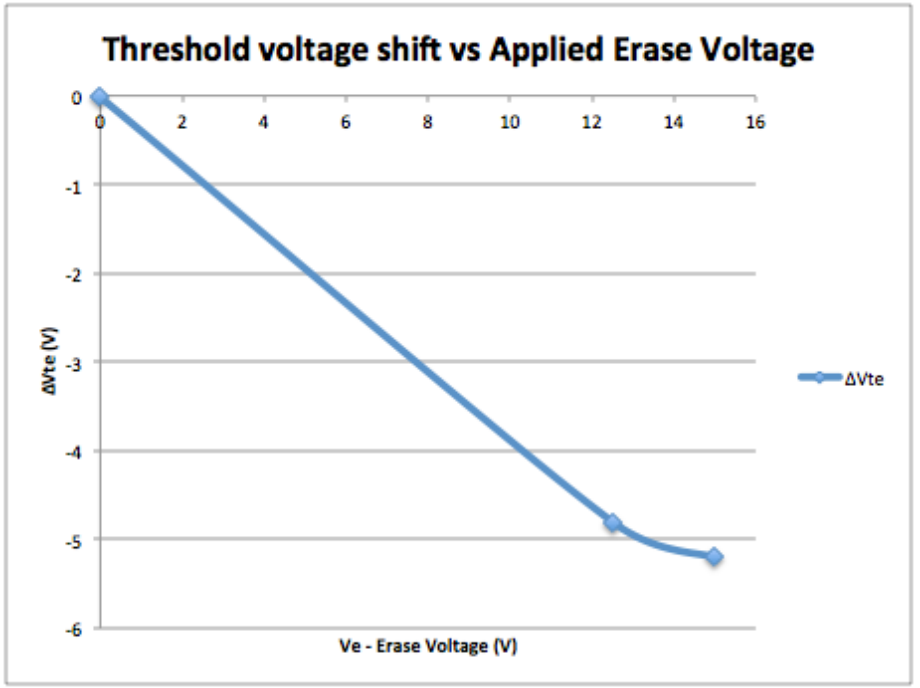

C-V Curves after Program and Erase Sequences
Capacitance (pF)
"Gate" Voltage (V)
60
50
40
30
20
10
0
-6
-5
-4
-3
-2
-1
0
1
2
3
4
A 15V Erase shifts the threshold such that it perfectly matches the fresh device!
Fresh Device
25V Program - Step 2
12.5V Erase - Step 3

Capacitors

$\Delta V_{tp} = V_{tp} - V_{t0}$ where, V_{tp} is the threshold voltage after program and V_{t0} is the threshold voltage of a fresh device.

$\Delta V_{te} = V_{te} - V_{tp_{max}}$ where, V_{te} is the threshold voltage after erase and $V_{tp_{max}}$ is the maximum possible programmed threshold voltage.





Further Work

Device Wafer Completion

- Once the device wafers have completed the process flow outlined in slide 7, they should prove fully functional
- Threshold voltage adjustment by hot carrier injection should be achievable, based on the good results seen with C-V wafers
- Theoretical scaling limits can then likely be extracted from these results.

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Questions?