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Characterization of Grid Contacts for n-Si Emitter Solar Cells

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CHARACTERIZATION OF GRID CONTACTS FOR n-Si EMITTER SOLAR CELLS

By

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Lastly, I would like to dedicate this work to my family.

ABSTRACT

Solar energy is abundant and is distributed all over the earth. While all renewable energy resources are important, solar energy has the potential to meet high levels of energy demand [1]. Silicon occupies 90% of the PV market and single crystalline silicon solar cells account for half of that share. Higher efficiencies along with abundance and reduction in silicon prices makes it the technology of choice for terrestrial applications.

With the mature technology available from crystalline silicon processing there is still room for significant research to improve the efficiencies. Further improved efficiencies and/or reduced cell costs are needed to reduce the overall cost. The motivation for this c-Si solar cell project was to continue development and optimize, a fabrication process for a baseline cell having a quick turnaround time which can be used as a venue for evaluating future process improvements. As a part of this process the contact materials for n-type doped silicon were investigated along with characterizing the process equipment. The experimental results indicated a Titanium/Aluminum stack had the lowest contact resistance and yielded the best fill factor. Efficiencies for the baseline cells were increased to 12.7%.

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CHAPTER 1: INTRODUCTION

Global energy needs are increasing every year. The current average global energy consumption is approximately 15 TW/year (Terawatts per year) [1]. These high energy demands are mostly met using fossil fuels such as oil, natural gas and coal, in both developed and developing countries. With the combustion of fossil fuels, the associated release of CO_2 has altered the natural atmospheric balance and triggered great debate over its potential impact on global temperature and weather. Continued reliance on fossil fuels possess two great challenges; the aforementioned long term impact on climate is compounded by increased consumption of non-renewable energy sources. Figure 1 illustrates the declining reserves of fossil fuels and the challenge of finding a sustainable replacement in next 30 years.

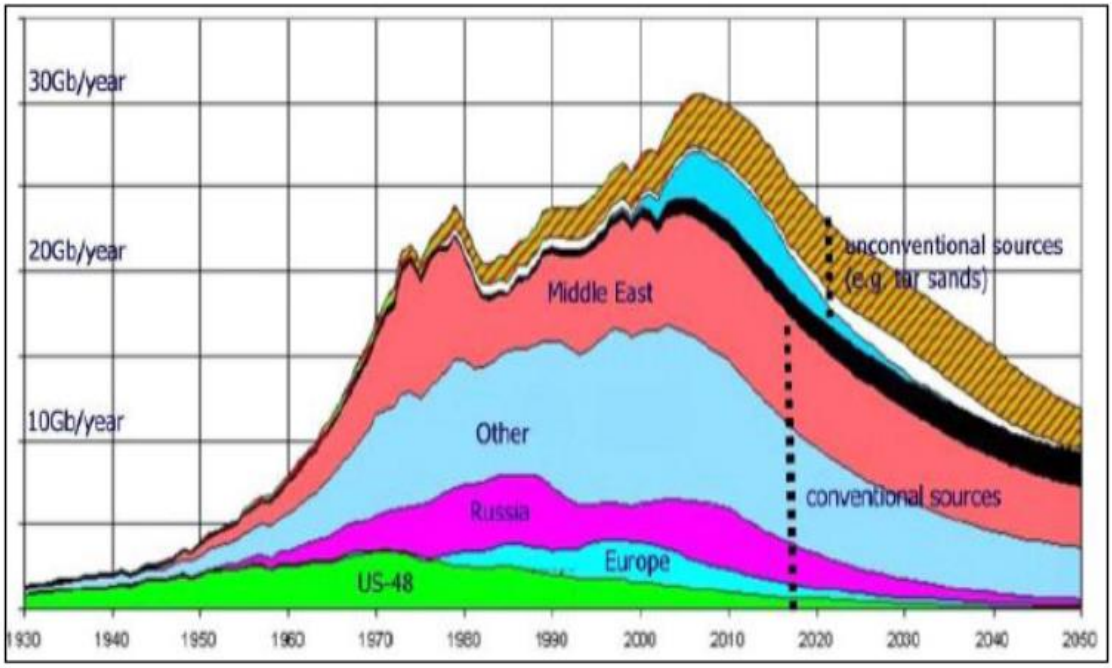


Figure 1: Declining reserves of natural resources available globally [2]

Therefore, alternative sources of renewable energy have to be developed. One such alternative source of energy is solar energy. Solar energy is abundant and is distributed all over the earth. While all the renewable energy resources are important, solar energy has the potential to meet high levels of energy demand [1]. Covering 0.16% of earth's land with 10% efficient solar cells would provide 20 TW of energy and this exceeds the current annual global energy consumption [3].

Solar insolation is the amount of incident solar radiation on the earth's surface and is about 1000W/m^2 on a clear day at sea level with sun overhead. Human Development Index (HDI) is a measure of the quality of life in a country, and takes into account factors such as per capita income, education and life expectancy [4]. Figure 2 clearly shows that countries with lower HDI have higher solar insolation. This clearly shows that solar energy presents developing countries a most viable solution for current and future energy needs.

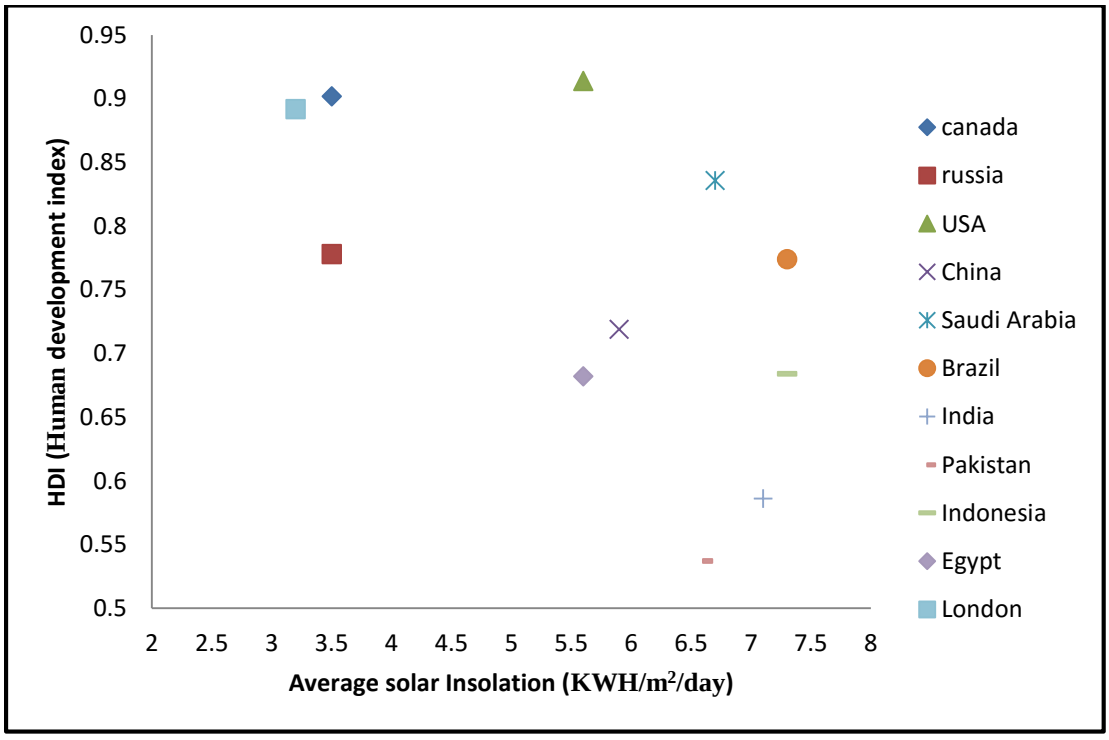


Figure 2: Human Development Index vs. solar insolation for different countries [4].

Photovoltaic systems are environmentally friendly, do not require fuel and can be used in applications that require milliwatts to megawatts of power [5]. Prices of solar electricity are already below $1/W for crystalline silicon solar cells and these costs are continuing to decline. The cost of the electricity produced by conventional sources has an average US price of 9.5¢/KWh. This value tends to increase as the demand increases. It will also increase in the event of carbon taxation. The crossover of these two price trends is commonly known as grid parity and is expected sometime in near future as shown in Figure 3. This grid parity is already met in southern California where marginal cost of electricity and solar insolation are high. The grid parity is an extrapolation of the learning curve that the ITRS road map of PV industry has been following [1].

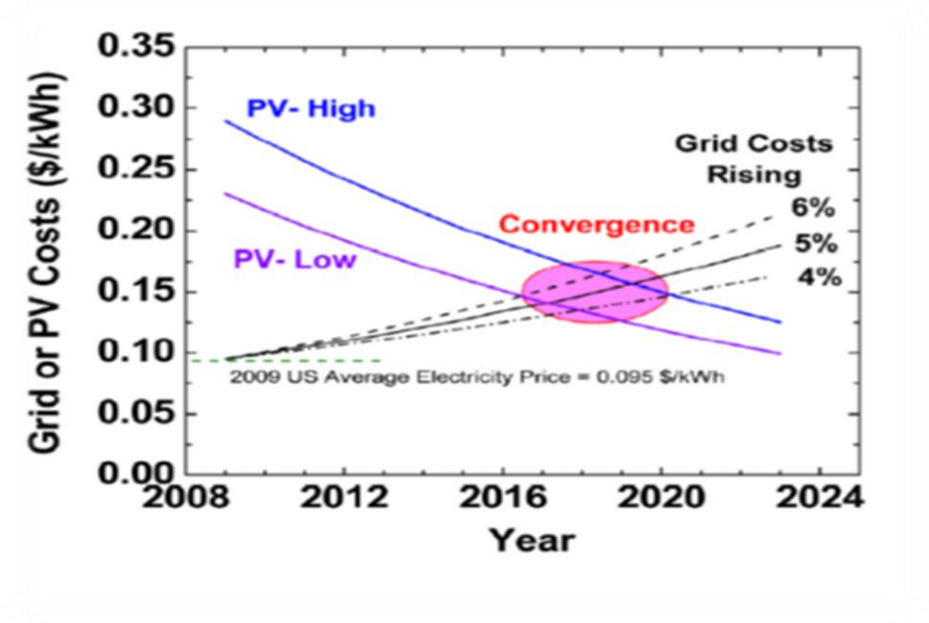


Figure 3: Grid cost vs. PV cost from 2008 to 2024 [1]

First generation PV cells refer to single crystalline silicon solar cells and gallium arsenide cells. Single crystalline silicon solar cells have maximum efficiencies of about 25% and GaAs

cells have maximum efficiencies of about 26% [6]. Silicon cells dominate the market and are most commonly used in all the terrestrial applications (such as roof tops). This mature technology adapts its processing from the IC industry. First generation cells have good stability, and good performance. The silicon raw material is abundant in nature, however, the energy required for production is high.

Second generation cells refer to amorphous silicon(a-Si), Cadmium Telluride (CdTe), Copper Indium Gallium DiSelenide (CIGS) and Copper Indium Selenide (CIS) which have a conversion efficiency of 13-22% [6]. The production costs are low compared to first generation cells but the efficiencies are also lower. Concerns with second generation cells are that the raw materials used for these cells are rare earth elements; and materials such as cadmium are toxic. Amorphous silicon has the potential for large scale production but the efficiency of the devices reduces with long time exposure to light, known as Staebler-Wronski effect [7]. With second generation cells, when an application has a fixed power requirement, more cells of lower efficiency are needed, which negates some of the cost savings. Recent decline in crystalline silicon prices has relegated these technologies to the back burner. One classic example would be the collapse of billion-dollar company Solyndra, which was a manufacturer of CIGS thin film solar cells [8].

Third generation cells refer to novel solar cell technologies using organic materials such as polymers, also referred to as Organic PhotoVoltaics (OPV) and Concentrating PhotoVoltaics (CPV). This generation cells also include multi-junction solar cells (each junction tuned to absorb different wavelength of light). Production costs of concentrating and multi-junction cells are very high. Organic cells have several advantages such as their flexibility, material availability and the potential to be inexpensive. The polymer cells can also be manufactured with Roll to

Roll (R2R) technology which is comparable to newspaper printing. However, these cells have low efficiencies and lifetime compared to those mentioned above, so while there is a future potential and research interest in polymer solar cells, there are significant hurdles to overcome. Recently, the Fraunhofer Institute for Solar Energy Systems ISE, Soitec, CE-Leti and the Helmholtz Center Berlin collectively announced a solar cell structure with 44.7% efficiency under concentration of 297 suns [9]. This shows tremendous potential for third generation technologies, but enormous cost reductions will be required if this technology is ever to be used for terrestrial applications.

With the reduction in silicon prices, first generation solar cells are currently priced equal to second generation, but their higher efficiency makes it the technology of choice. Figure 4 attempts to illustrate this shift in first generation costs and explains the renewed interest in silicon based technology.

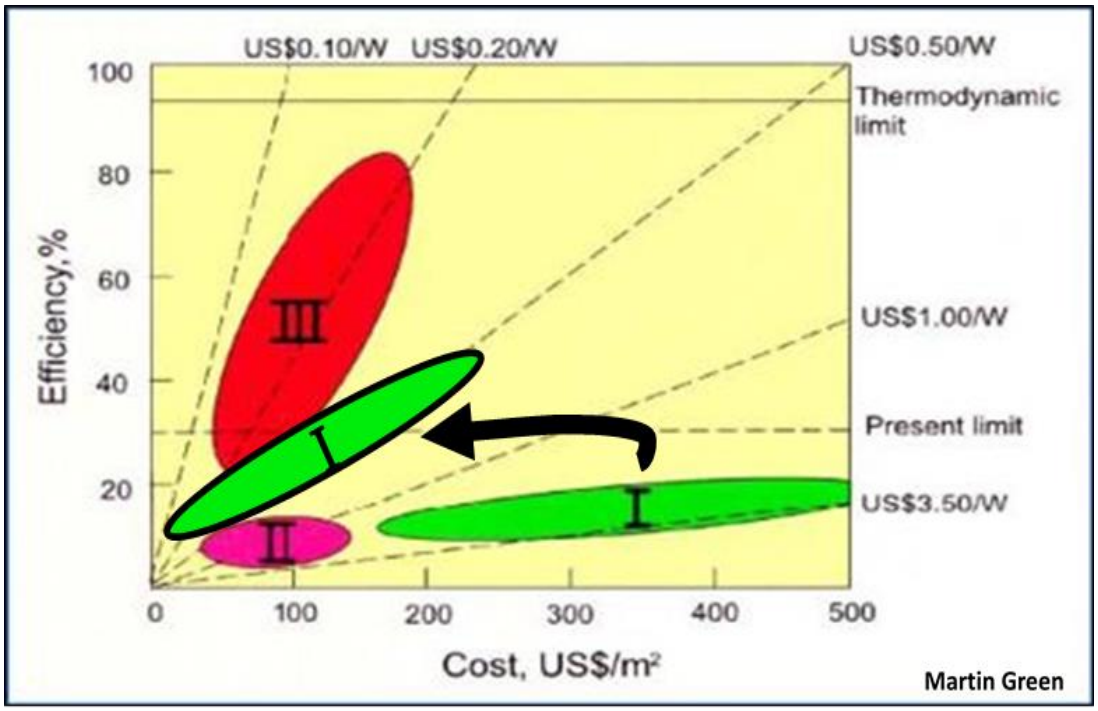


Figure 4: Cost vs. efficiency of solar cells [10]

Prices of residential and nonresidential fixed roof top PV systems have decreased consistently over the past years. Price of residential fixed PV as per SEIA report in Q2 2015 is $3.50 for installation and nonresidential fixed PV price is $2.13 for installation as shown in Figure 5 [11]. PV installation costs include prices of PV module, labor, supply chain, margin, inverter and legal fees. The United States solar industry has surpassed 20 gigawatts of total operational solar PV capacity during second quarter of 2015. The US installed 1.393 GW of solar power in Q2 2015 marking the seventh consecutive quarter to add more than 1 GW of PV installations. The residential market has seen an installation increase 70 percent in one year [11].

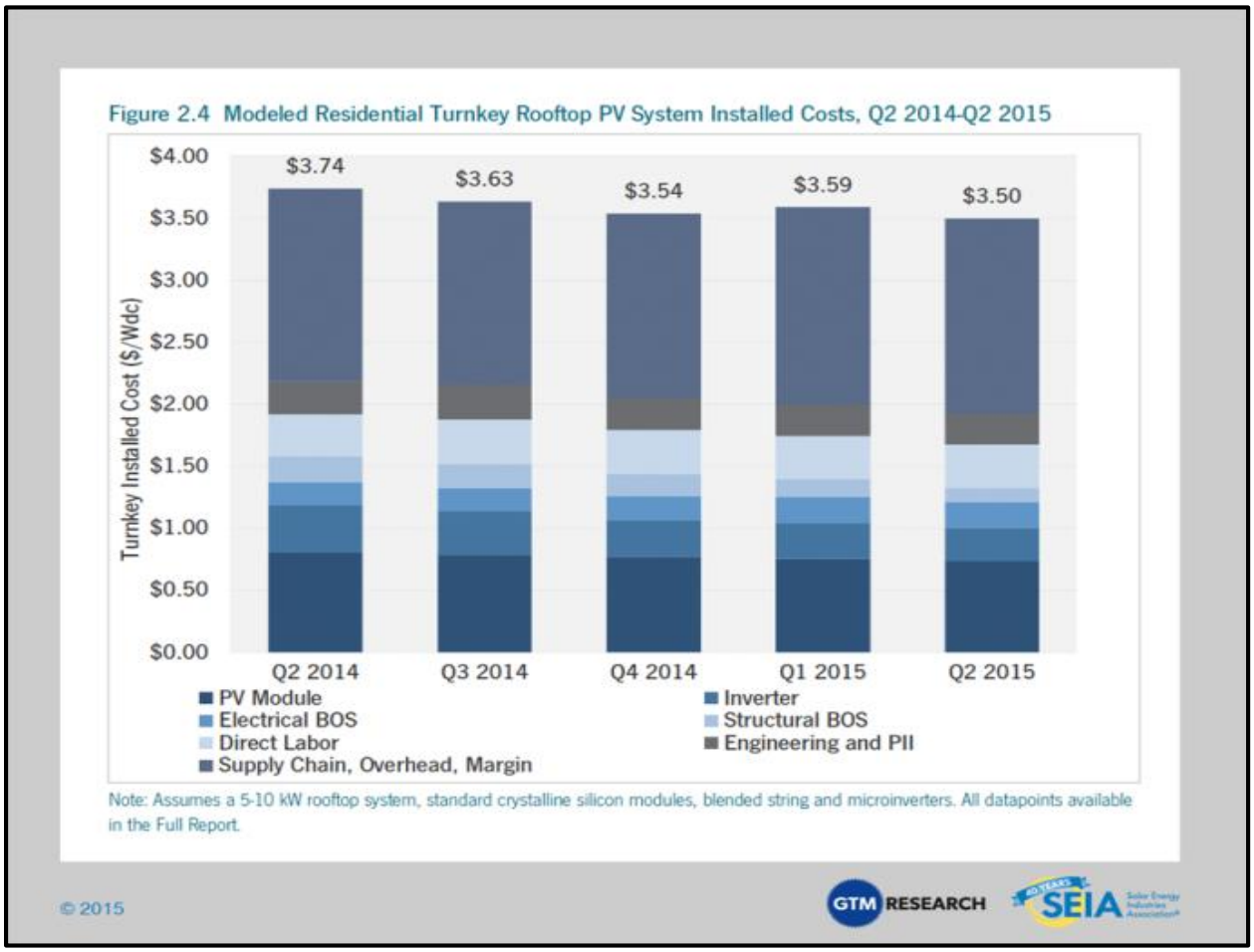


Figure 5: SEIA graphs showing residential PV cost over a year [11].

As stated as early as 1980, when considering the materials required for solar cells based on abundancy, silicon was the best. Even today it remains true and silicon occupies 90% of the PV market share as shown in Figure 6. Global PV module energy production in 2014 is estimated to be between 45 and 55GW and 90% of the share was from crystalline silicon (c-Si). The other 10 % is from thin film PV and this remains unchanged [12].

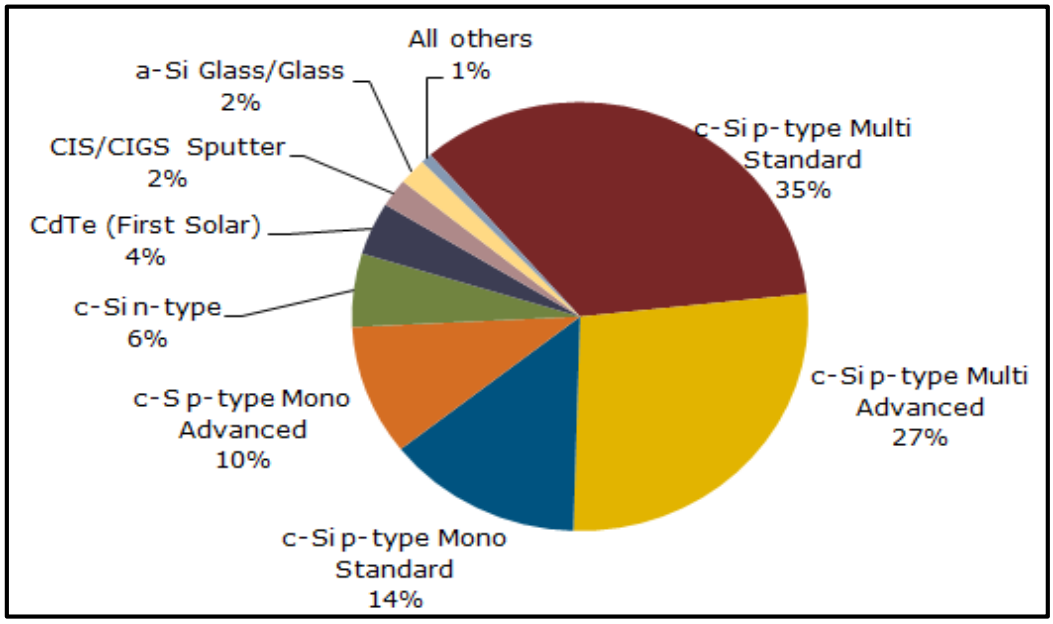


Figure 6: PV module production by Technology [12]

One of the golden standards for single crystalline silicon solar cells are Passivated Emitter Rear Locally diffused (PERL) solar cells. These cells have achieved 25% efficiency [10] but the fabrication process is complex and it involves lithographically defined contact and texturing, rear locally diffused contacts and titanium-palladium-silver metal is used for front contacts. The PERL cell structure is shown in Figure 7.

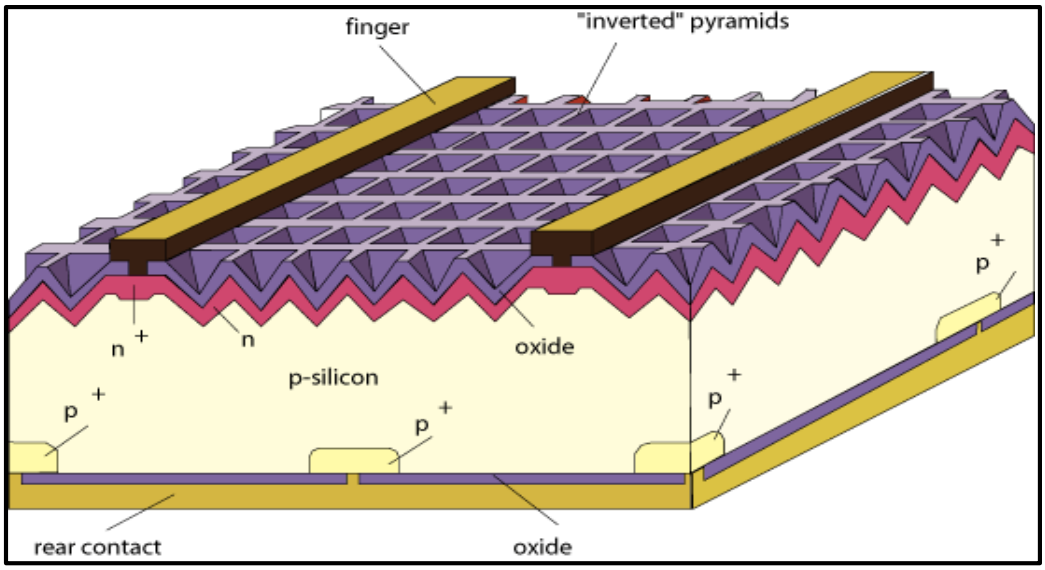


Figure 7: PERL cell structure [10]

An a-Si/c-Si heterojunction solar cell, known as Heterojunction with Intrinsic Thin-layer (HIT) solar cell, has been developed. These cells report to benefit from low temperature processing and shallow junctions [13] with a-Si layers chemically deposited on c-Si. HIT cells are reported to have efficiencies up to 25.6% [14] but these cells require more complex fabrication processes.

Crystal Solar and IMEC have demonstrated 22.5 % highest efficiency to date homojunction silicon solar cells on epitaxial grown wafers. Epitaxially grown wafers eliminate costs due to ingoting, wire saw and kerf loss. Also these wafers benefit high quality in-situ p-n junctions which result in high V_{oc}. High efficiency PERT solar cell process was adopted which includes selective front field using laser doping, advanced emitter passivation using Al_2O_3 and Ni/Cu contacts [15].

Apart from various manufacturing techniques available, there are challenges in PV manufacturing.

(a) Silicon feedstock: replacing Siemens process with Fluidized Bed process (FBR) yields solar grade silicon (99.9999% pure) compared to electronic grade (99.9999999% pure). This process consumes less electricity when compared to the Simens process and hence is expected to reduce the price of production. Use of FBR is predicted to rise from 10% in 2014 to 17% in 2020 [16]. However, there are questions if this technology can practically reach industrial demand of electronic grade and the FBR process needs complicated controls as dynamics change with size and the equipment cannot be easily scaled to industry level [17].

(b) Kerfless wafers: In the wire saw technology that produces thin wafers, almost 50% of the silicon material is lost as kerf or sawdust [1]. Kerfless wafers can be produced using Edge refined Film Fed Growth (EFG), string ribbon silicon and casting technologies. Neither of these technologies has cost efficiency and production close to that of the ingot based processing [17]. Use of diamond wire saw has also gained importance which enables higher cutting speeds and reduced silicon consumption [18]. 1366 Technologies uses one-step direct wafer process to manufacture kerfless silicon wafers [19]. While increasing the number of wafers from a fixed volume of silicon, 1366's wafers are on par with poly-crystalline substrates in terms of efficiencies.

(c) Ultra-thin Silicon: The entire photons incident on the cells are usually absorbed in first 300um [2]. For this reason, ultra-thin wafers are preferred, but challenges such as low cost substrate, wafer handling and surface passivation still remain.

(d) Others: Improving additional process techniques such as front side texturing, integration of back side reflectors, lowering the level of shadowing, engineered emitter design, appropriate ARC thickness and passivation techniques all have potential in improving efficiencies.

From this review it should be apparent that silicon is the most abundantly available material and the solar cells manufactured from silicon offer the best option in the present day to achieve reasonable efficiencies at desirable costs for terrestrial applications. Inspite of the mature technology available from c-Si processing there is still room for significant research to improve the efficiencies. Further improved efficiencies and/or reduced cell costs are needed to reduce the overall cost. The motivation for this c-Si solar cell project was to continue development and optimize, a fabrication process for a baseline cell having a quick turnaround time which can be used as a venue for evaluating future process improvements. This is called the "turn-key" process. The device physics of the cell and fabrication details are given in Chapter 2 and 3, respectively.

CHAPTER 2: DEVICE PHYSICS AND CHARACTERIZATION OF SOLAR CELLS

In this chapter, the basic equations of p-n junction solar cells, solar cell structure and solar cell performance parameters will be discussed.

2.1 Basic equations of p-n junction model

In a p-n junction, electrons and holes contribute to total current by drift and diffusion. Drift is due to the electric field in the depletion region and diffusion is due to any concentration gradients. The electron and hole currents can be expressed as,

$$\overrightarrow{J_n} = q\mu_n n\vec{E} + qD_n.\nabla \mathrm{n} \tag{1}$$

$$\overrightarrow{J_p} = q\mu_p p\vec{E} - qD_p.\nabla \mathrm{p} \tag{2}$$

where $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ represent current densities, D_n and D_p are the diffusion constants of electrons and holes, respectively, and μ_n and μ_p are electron and hole mobilities, respectively.

In the presence of external illumination, minority carriers (electrons in p-type material and holes in n-type material) are generated. Generation and recombination rates are related to divergence of current density and are given by,

$$\nabla \cdot \overrightarrow{J_n} = q(R_n - G) \tag{3}$$

$$\nabla \cdot \overrightarrow{J_p} = -q\left(R_p - G\right) \tag{4}$$

where R_n and R_p represent electron and hole recombination rates, and G represents the optical generation rate due to external illumination

Low level injection is a state of small disturbance from equilibrium where the majority carrier concentration remains unaffected but the minority carrier concentration is significantly affected. With low level injection and under steady state condition the above equations can be rewritten as follows,

$$\nabla \cdot \overrightarrow{J_n} = q\mu_n \frac{d(n\overrightarrow{E})}{dx} + qD_n \frac{d^2\Delta n}{dx^2} = q(R_n - G) \tag{5}$$

$$\nabla \cdot \overrightarrow{J_p} = q\mu_p \frac{d(p\overrightarrow{E})}{dx} - qD_p \frac{d^2\Delta p}{dx^2} = -q(R_p - G) \tag{6}$$

where $\Delta n = n - n_o$ and $\Delta p = p - p_o$ represent excess minority carrier concentration in p-side and n-side, respectively, and n_o and p_o are the equilibrium carrier concentrations controlled by doping. This state of low level injection can be achieved by external illumination and the generated carriers, when collected, contribute to the photo generated current.

2.1.1 p-n junction under equilibrium

Most single crystalline silicon solar cells are simple p-n junctions. When isolated n-type and p-type semiconductors are brought together electrons and holes flow from high concentration to low concentration regions. During this process of charge diffusion, electrons leave a positive immobile dopant charge and holes leave a negative immobile dopant charge behind. These charges are distributed in the crystal lattice and create an electric field or built in potential which increases until it prevents any further diffusion of the carriers. Diffusion current and drift current are balanced when a p-n junction is in equilibrium. In the quasi neutral region that lies beyond the space charge region, electrons and holes compensate donor and acceptor charges and hence the net charge density is zero. The majority carriers in the quasi neutral region are the dominant carriers and are controlled by dopant levels as shown here.

$$n_{no}=N_D \text{ and } p_{po}=N_A$$

The built in potential of the diode is given by,

$$V_{bi} = \frac{kT}{q}\ln(\frac{N_A N_D}{n_i^2}) \tag{7}$$

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = \frac{kT}{q}\ln\left(\frac{n_{no}p_{po}}{n_{po}p_{po}}\right) = \frac{kT}{q}\ln(\frac{n_{no}}{n_{po}}) \tag{8}$$

Solving for n_{no},

$$n_{no} = n_{po}\ \exp(\frac{q\ V_{bi}}{kT}) \tag{9}$$

Therefore, the electron density on n-side at the edge of space charge region is related to electron density on p-side by the term $\exp(\frac{q\ V_{bi}}{kT})$. Similarly, the hole density on p-side at the edge of space charge region is related to hole density on n-side by the term $\exp(\frac{q\ V_{bi}}{kT})$.

2.1.2 p-n junction at non equilibrium

The p-n junction under non equilibrium occurs in the presence of an external applied voltage (V_a). Due to applied voltage minority carrier concentrations and hence carrier concentration at the edge of depletion region change.

$$n_n = n_p\ \exp\frac{q(V_{bi}-V_a)}{kT} \tag{10}$$

$$p_p = p_n\ \exp\frac{q(V_{bi}-V_a)}{kT} \tag{11}$$

where $n_n, n_{p,} p_p$ and p_n are electron concentration on n-side and p-side, hole concentration on p-side and n-side under applied voltage V_a.

Assuming low level injection condition where majority carrier concentration is unaffected,

$$n_n = n_{no} \text{ and } p_{p=}p_{po}$$

Solving equation 9 and 10 gives,

$$n_{no} = n_p \exp\frac{q(V_{bi} - V_a)}{kT} = n_{po} \exp\frac{q(V_{bi})}{kT} \rightarrow n_p = n_{po} exp\frac{q(V_a)}{kT} \quad (12)$$

$$p_{po} = p_n \exp\frac{q(V_{bi} - V_a)}{kT} = p_{no} \exp\frac{q(V_{bi})}{kT} \rightarrow p_n = p_{no} exp\frac{q(V_a)}{kT} \quad (13)$$

Diffusion current densities on the n-side and p-side due to excess minority carriers are given by,

$$J_p = -qD_p\frac{dp_n}{dx} = \frac{qD_p p_{no}}{L_p}[\exp(\frac{qV_a}{kT}) - 1] \quad (14)$$

$$J_n = -qD_n\frac{dn_p}{dx} = \frac{qD_n n_{po}}{L_n}[\exp(\frac{qV_a}{kT}) - 1] \quad (15)$$

Total diffusion current as shown in Figure 8 is due to minority carriers in the p-n junction is the summation of individual diffusion currents and is given by,

$$J_{np} = q\left(\frac{D_n n_{po}}{L_n} + \frac{D_p p_{no}}{L_p}\right)[\exp(\frac{qV_a}{kT}) - 1] = qn_i^2\left(\frac{D_n}{L_n N_D} + \frac{D_p}{L_p N_A}\right)[\exp(\frac{qV_a}{kT}) - 1] \quad (16)$$

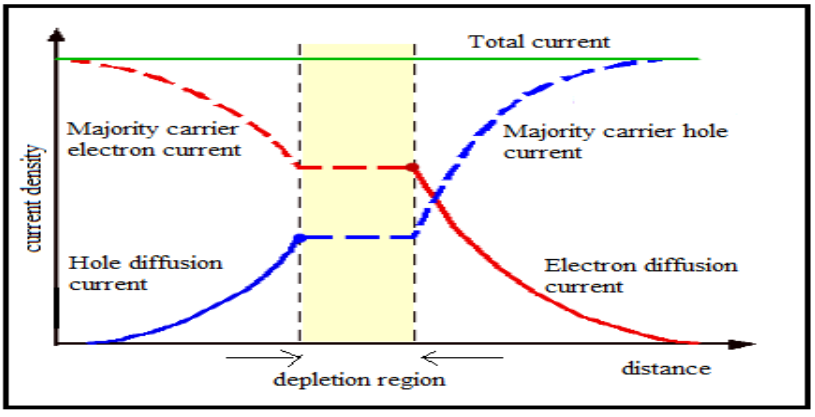


Figure 8: Neutral and depletion region carrier diffusion profiles [20]

For a p-n diode with cross sectional area A, the above equation can be rewritten in more representative format as,

$$I = I_{01}[\exp(\frac{qV_a}{nkT}) - 1] \tag{17}$$

where n is the ideality factor (usually n=1) and I_{01} is the saturation or leakage current,

$$I_{01} = Aqn_i^2(\frac{D_n}{L_n N_D} + \frac{D_p}{L_p N_A}) \tag{18}$$

2.1.3 p-n junction under illumination

In the presence of light, electron-hole pairs are generated in the semiconductor material provided the energy of incident photons is greater than the bandgap of the material. In solar cells the electron hole pairs created are not uniform throughout the device as the shorter wavelength (higher energy photons) of incident light are absorbed at the surface and longer wavelengths (lower energy photons) are absorbed deeper in the cell.

Generated minority carriers when collected, contribute to the photon generated current I_{ph}. Impurities present in the semiconductor create energy levels within the bandgap, known as traps, as they capture carriers. These trap sites act as recombination sites.

Shockley-Read-Hall model gives a complete analysis of recombination by taking into account all the probabilities of an electron presence at the trap energy position. In the space charge region of width W, any generation / recombination in this region is gives rise to an additional current density component and is given by,

$$J_{R/G} = \frac{qn_iW}{2\,\tau_{dep}}[\exp(\frac{q\,V_a}{2kT}) - 1] \tag{19}$$

where, τ_{dep} is the average minority carrier lifetime in depletion region. Hence the current in depletion region is equal to

$$I_{R/G} = \frac{qn_i WA}{2\,\tau_{dep}}\left[\exp\left(\frac{q\,V_a}{2kT}\right) - 1\right] \tag{20}$$

The above equation can be written in more representative format as,

$$I_{R/G} = I_{02}\left[\exp\left(\frac{q\,V_a}{2kT}\right) - 1\right] \tag{21}$$

where I_{02} is the leakage current due to generation and recombination.

The linear diode I-V plot does not reveal the various current components, but a ln (I) vs V plot of the data under forward bias does. Diode I-V curves are usually represented by two distinct regions with two ideality factors (n=1 at higher voltages and n=2 at lower voltages). This is known as two-diode model and the extraction of n values from I-V curve is shown in Figure 9. Total current in quasi neutral region and depletion region is given by,

$$I_{dark} = I_{01}\exp\left(\frac{q\,V_a}{nkT} - 1\right) + I_{02}\exp\left(\frac{q\,V_a}{2kT} - 1\right) \tag{22}$$

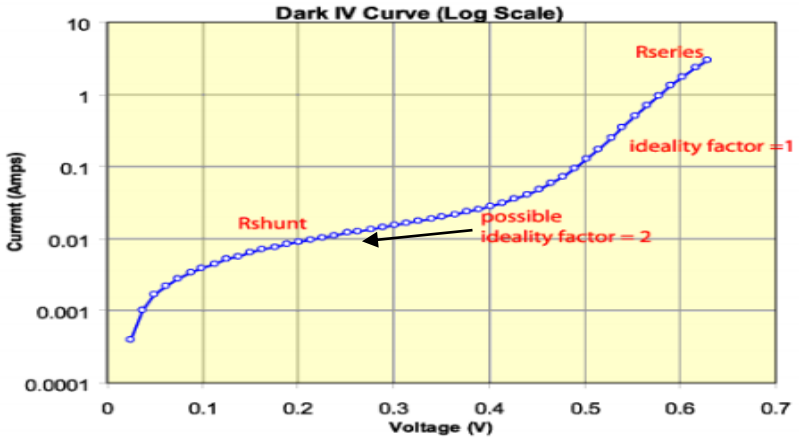


Figure 9: Total current as a sum of depletion region current and quasi-neutral region current [2]

Total current under illumination is given by,

$$I = I_{01} \exp\left(\frac{q\,V_a}{nkT} - 1\right) + I_{02} \exp\left(\frac{q\,V_a}{2kT} - 1\right) - I_{ph} \tag{23}$$

Equation 23 shows the photo generated current I_{ph} as a simple constant addition to the drift or leakage currents of the diode. This additional current manifests itself in the I-V plot as a negative shift in the current axis as seen in the Figure 10. The amount of the offset depends upon many factors, an overview of which is given in the next section.

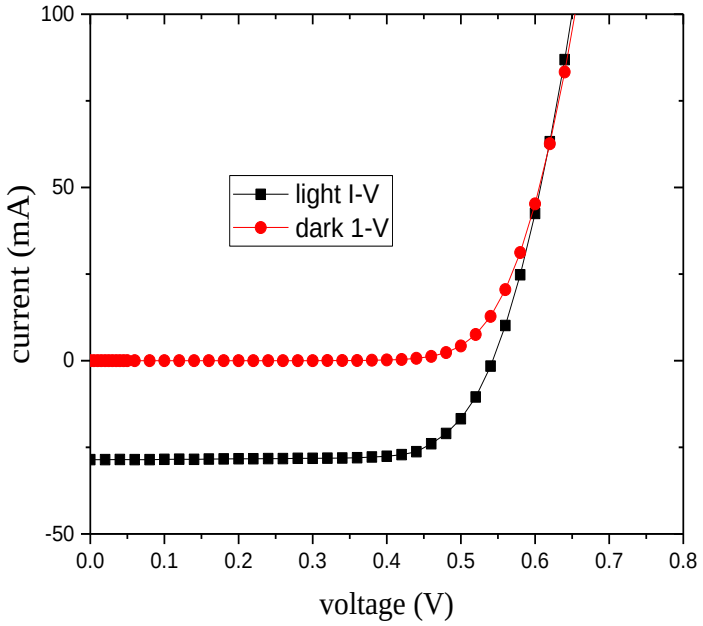


Figure 10: Shift of I-V from dark to illuminated in the presence of light

As a summary, carrier profiles of n-p junction under equilibrium, forward bias and under illumination is shown in Figure 11.

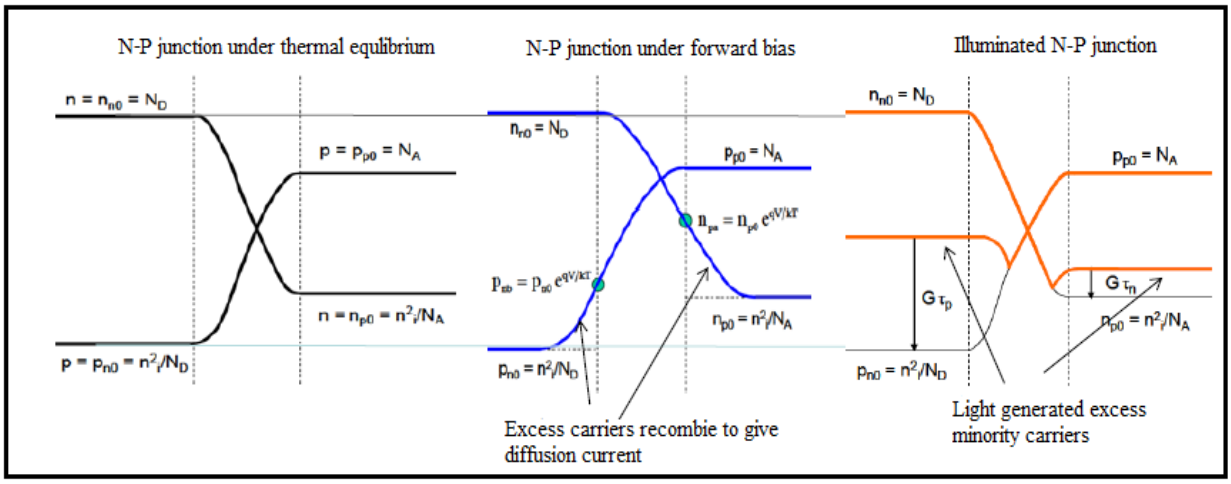


Figure 11: Carrier profiles under equilibrium, forward bias and illumination [2]

2.2 Incident spectrum, Generation and recombination

The spectrum outside Earth's atmosphere is Air Mass 0 and is labelled as AM0 radiation. This spectrum is used as an incident spectrum to measure output parameters of solar cells for extra-terrestrial applications. The spectrum incident on the earth surface is known as AM1.5 radiation. Figure 12 (a) depicts incident spectrum as a function of wavelength [20]. More details are given in Section 2.2.1

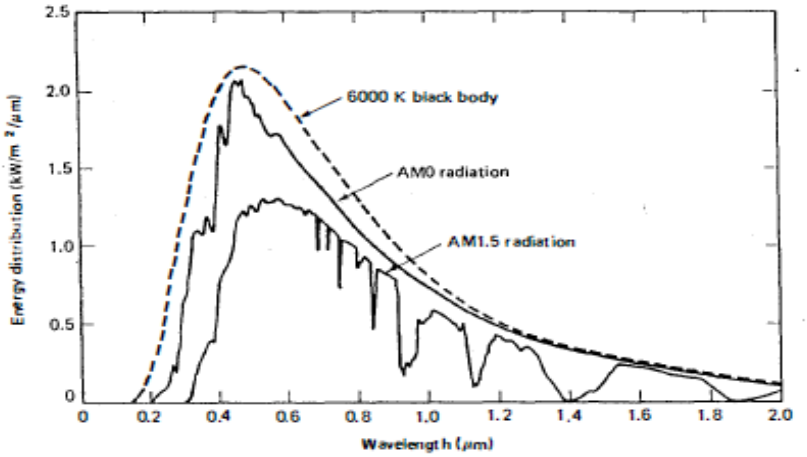
The generation (G) of the carriers depends upon absorption of photons at different depths the material,

$$G = \alpha N_o e^{-\alpha x} \tag{24}$$

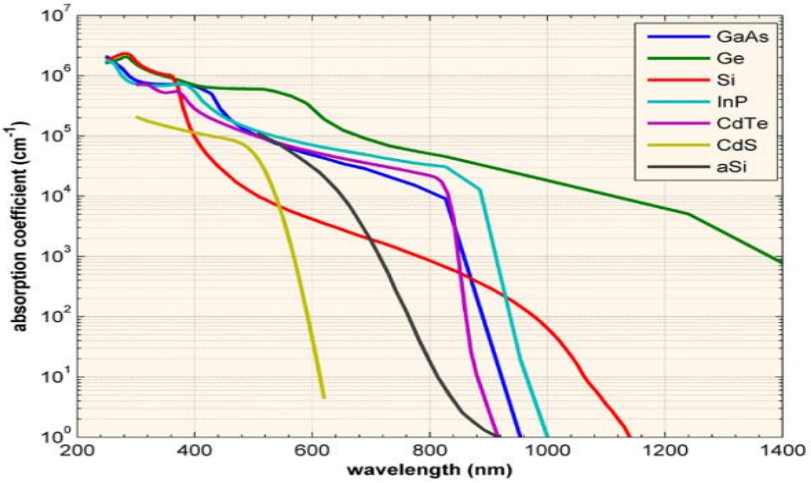
where N_o is the photon flux at the surface, α is the absorption coefficient, and x is the distance into the material. The absorption coefficient for different semiconductor materials is shown in Figure 12. Carrier generation at specific wavelength is given by,

$$G(\lambda, x) = F(\lambda, x)\alpha(\lambda) = F_o(\lambda)(1 - R(\lambda))\, e^{-\alpha(\lambda)x}\alpha(\lambda) \tag{25}$$

where $F_o(\lambda)$ is the incident photon flux of wavelength λ, $R(\lambda)$ is the reflection coefficient, and $\alpha(\lambda)$ is the absorption coefficient for wavelength λ. All these factors influence the photogenerated current.



(a)



(b)

Figure 12: (a) Spectral radiation of the sunlight showing AM0, AM1.5 and black body radiation (b) Absorption coefficients of different semiconductor materials [20]

2.2.1 Air mass and photon flux

Air mass is the path length taken by light in the atmosphere normalized to the shortest possible path length and it quantifies the amount of sunlight lost as it passes through the atmosphere. Solar irradiance in outer space is known as air mass zero (AM0) with an intensity of about 1.35kW/m^2, and it is used to predict solar cell performance in outer space. AM0 is reduced by about 28% as it reaches earth. This is due to atmospheric effects such as scattering, absorption, latitude and longitude, season of the year and the local variations such as pollution, clouds and water vapor. The standard average solar spectrum at earth's surface is known as AM1.5 and has an intensity of about 1kW/m^2 at sea level with sun overhead on a clear day.

2.2.2 Optical losses

Incident solar light may not be completely absorbed by the solar cells and hence the photogenerated current is reduced. This phenomenon is known as optical loss and results from reflected light or light that is not absorbed by the solar cells. For most common silicon solar cells the entire visible spectrum has enough energy to create electron-hole pairs [5] but bare silicon reflects about 30% of the light in the visible spectrum.

2.2.3 Anti-reflective coatings (ARC)

Anti-reflective coatings help in lowering the optical losses. An anti-reflective layer is a dielectric material of chosen thickness so that the light reflected from the film-substrate interface destructively interferes with the reflected light from the air-film interface. Ideally, no light is reflected from the material. In reality, the ARC has to be designed so as to minimize reflections

for the entire visible spectrum as the refractive index of most materials varies with the wavelength.

The thickness of the dielectric material is chosen such that the wavelength in the dielectric material is one quarter the wavelength of the incident light [20]. For a dielectric material of refractive index n_d and wavelength of incident light λ the thickness t calculated for minimum reflection is:

$$t = \frac{\lambda}{4n_d} \tag{26}$$

Reflection can be further minimized if the refractive index of the dielectric material is the geometric mean of the refractive indices of the surrounding materials such as air, glass and semiconductor. If the refractive index of the surrounding material is n_o, and the refractive index of the semiconductor is n_2, then appropriate refractive index of the dielectric material can be calculated as,

$$n_1 = \sqrt{n_0 n_2} \tag{27}$$

2.2.4 Surface Passivation

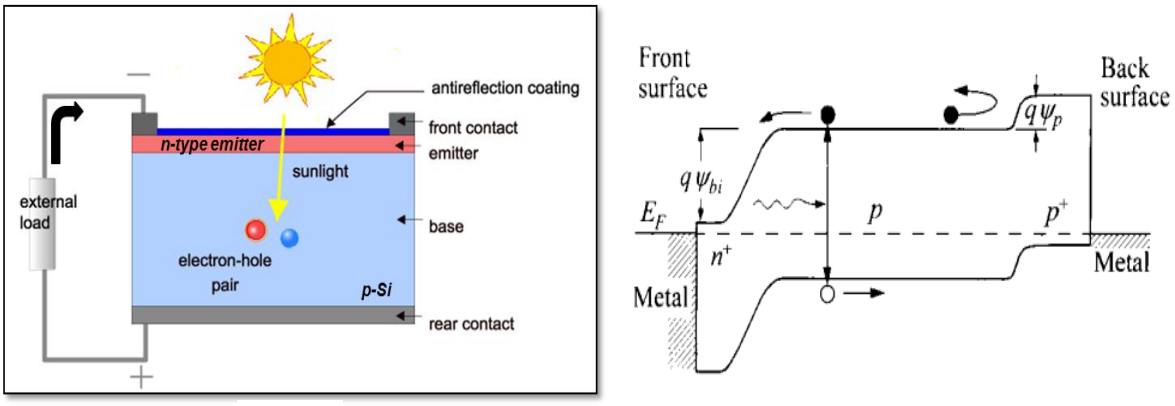
Anti-reflective coatings passivate the surface and reduce the dangling bonds which act as recombination sites. Surface recombination velocity (cm/sec) is a parameter used to quantify recombination as the carriers move along the surface. Well passivated surfaces improve the surface quality and reduce the surface recombination velocity. This enhances the collection of the photogenerated carriers that arrive at the surface [10].

2.2.5 Back Surface Field

Rear surface recombination should be reduced in order to collect the carriers generated deep in the bulk of the cell. In the back surface field device, dopant species which are the same as the substrate doping are introduced at the rear surface. Band bending due to the high and low doped regions inhibits loss of minority carriers by reflecting them towards the depletion region where they can be swept away by the electric field. Back surface field increases short circuit current and open circuit voltage, but requires additional processing.

2.2.6 Solar cell structure

Figure 13 (a) shows the cross section of a solar cell with a semiconductor substrate, p-type silicon in this case. The substrate acts as the base and is the main volume in which generation occurs. A p-n junction is formed utilizing doping techniques such as diffusion or ion implantation. This region is called emitter, its doping levels are usually greater than the substrate, and this usually extends 1μm into the substrate. Additional doping can increase the carrier concentrations at the front and back of the cell creating the front and back surface field which aid in carrier collection. The front surface field acts to increase cell performance in the same manner as the BSF as described above. Energy band diagram of solar cell is shown in Figure 13 (b) indicating front and back surface fields. The metal grid present at the top and the back contact serve to exchange carriers with the external circuit, delivering power to the load as shown in Figure 13 (a).



(a) **(b)**

Figure 13: (a) Cross section of solar cell (b) Energy band diagram of solar cell [10]

2.3 Solar cell parameters

Different parameters used to characterize the illuminated solar cells are short circuit current (I_{sc}), open circuit voltage (V_{oc}), fill factor (FF), Quantum Efficiency (QE) and efficiency (η) are shown in Figure 14.

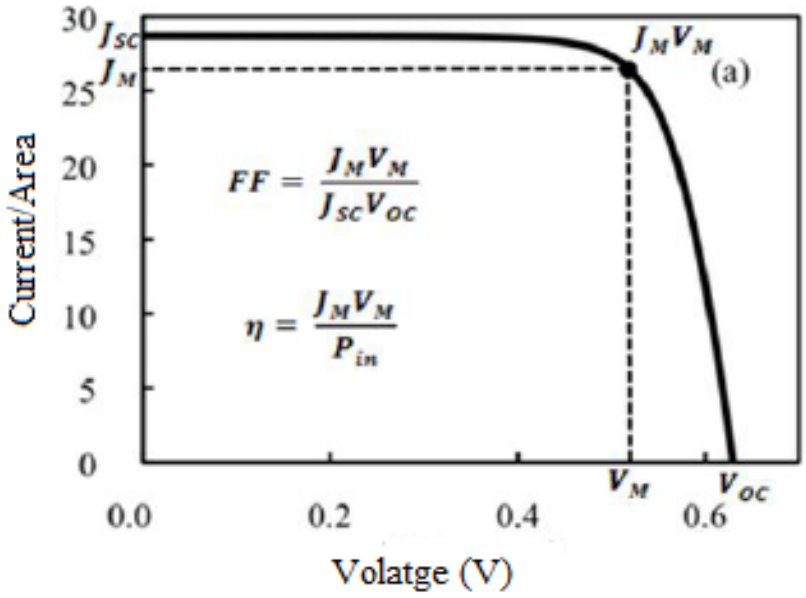


Figure 14: Solar cell I-V curve with output parameters [2]

2.3.1 Short circuit current (I_{sc})

Short circuit current I_{sc}, is the current produced in the solar cell when the applied voltage is zero. Short circuit current depends on several parameters such as area of the cell, number of incident photons, absorption and reflection, and collection probability. Ideally short circuit current is reported as current density to eliminate the effect of area. Assuming ideal conditions in which the surface is perfectly passivated, carrier generation is uniform and short circuit current density is given by,

$$J_{sc} = qG(L_n + L_p) \tag{28}$$

where L_n and L_p are diffusion lengths. Maximum achievable J_{sc} under AM 1.5 is about 46mA/cm^2 for silicon solar cells [20].

2.3.2 Open circuit Voltage (V_{oc})

Open circuit voltage is the voltage at which current from the cell is zero. Neglecting the generation and recombination currents in Equation 23, one may write V_{oc} as

$$V_{oc} = \frac{nKT}{q} ln\left(\frac{I_{ph}}{I_0} + 1\right) \approx \frac{nKT}{q} ln\left(\frac{I_{ph}}{I_0}\right) \tag{29}$$

This shows that V_{oc} depends on light generated current relative to the saturation current in the diode. Saturation current depends on doping, mobility and lifetime of the carriers. Hence, V_{oc} is affected by the quality of the diode and any increase in the n value and I_0 are usually not good. Maximum achievable V_{oc} under AM 1.5 conditions is reported to be 730mV [20].

2.3.3 Fill factor (FF)

Short circuit current and open circuit voltage are the maximum achievable current and voltage from the solar cell but the power at each of these points is zero. Fill factor, abbreviated as

FF, is used to determine the maximum power from the solar cell. Fill factor is given by the ratio of maximum power from solar cell to product of $I_{sc}$and V_{oc}. It is also measure of "squareness" of solar cell output. Figure 14 shows an I-V curve of solar cell along with other output parameters.

$$FF = \frac{V_{MP} I_{MP}}{V_{oc} I_{sc}} \tag{32}$$

A commonly used expression to determine fill factor empirically is:

$$FF = \frac{v_{oc} - \ln\ (v_{oc} + 0.72)}{v_{oc} + 1} \tag{30}$$

where is v_{oc} defined as normalized V_{oc} and is given by:

$$v_{oc} = \frac{q}{nkT} V_{oc} \tag{31}$$

The higher the open circuit voltage (ideal n value), the larger is the FF and Maximum achievable FF in laboratory is 0.85 [20]. Fill factor is also significantly affected by parasitic resistances.

2.3.4 Quantum Efficiency

Quantum Efficiency (QE) is the ratio of number of carriers collected to the number of incident photons of given energy on solar cell. An external quantum efficiency plot is shown in Figure 15, which includes the effect of optical losses such as reflection and transmission. An internal quantum efficiency does not include any of the factors mentioned. Both plots are used to gain insight into cell performance at various depths into the wafer. For example, lower response in the red wavelength region is indicative of carrier loss in the bulk or due to poor contact on the back side.

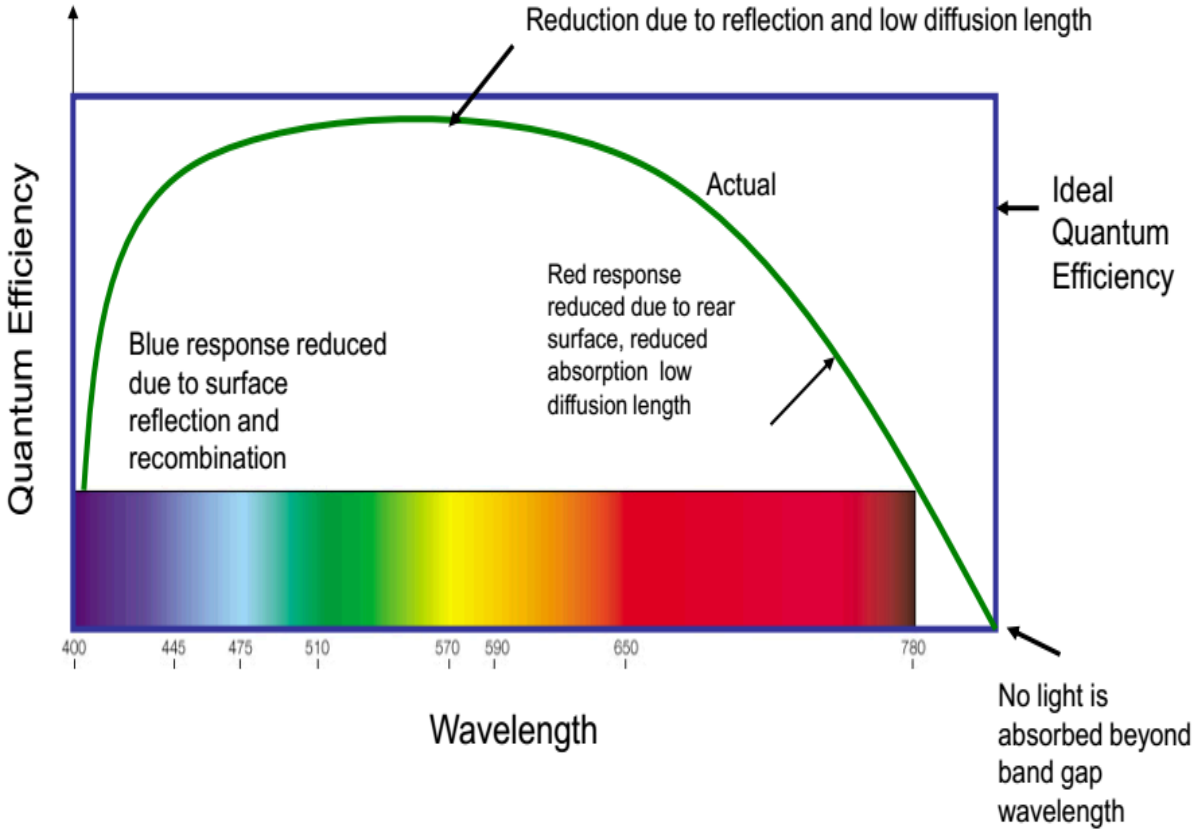


Figure 15: Quantum Efficiency curve for different wavelengths [2].

2.3.5 Efficiency

Efficiency is defined as ratio of output power to the input power (energy of incident light). Solar cell efficiency also depends on the temperature of the cell and intensity of the incident sunlight. Therefore, the conditions under which efficiency is measured should be controlled. Terrestrial solar cells are measured at 25^{o}C and under AM1.5 conditions. Solar cells for space applications are measured under AM0 at 25^{o}C.

Maximum output power and efficiency of the solar cell are given by,

$$P_{max} = V_{oc} I_{sc} FF \tag{32}$$

$$\eta = \frac{V_{oc} I_{sc} FF}{P_{in}} \tag{33}$$

P_{in} is the input power and is taken as 1kW/m^2 or 100mW/cm^2 for AM1.5 illumination.

2.4 Resistive effects

Parasitic resistances reduce efficiency of the solar cells in addition to reflection and recombination losses. Both series and parallel resistances reduce the fill factor. Hence a low series resistance and high shunt resistance are necessary. Shunt resistance creates an alternative path for the current in the circuit instead of current flow to the load. Series resistance arises from several components in the solar cell. Components that contribute to series resistance in solar cell are metal-semiconductor-contact on the back surface, semiconductor material base, emitter between the grid fingers, metal-semiconductor-contact of the grid finger, grid fingers and the collection bus. To reduce the overall series resistance, emitter doping, junction depth, spacing between the fingers and area of the fingers must be optimized.

The two diode model of p-n junction with photo current along with series and shunt resistance is shown in Figure 16. In general shunt resistance will shift the current away from the load, while series resistance creates a voltage drop lowering the output voltage of the cell. The effect of shunt and series resistance on fill factor and I-V response are illustrated in Figure 17. The effect of series and shunt resistance on fill factor is given by,

$$FF_s = FF_o(1 - 1.1R_s) + \frac{R_s^2}{5.4} \tag{34}$$

$$FF_{SH} = FF_s(1 - \frac{V_{oc} + 0.7}{V_{oc}} \frac{FF_s}{R_{SH}}) \tag{35}$$

where FF_o is the fill factor without any resistive effects and FF_s is the fill factor in the presence of series resistance, FF_{SH} is fill factor in the presence of shunt resistance [20].

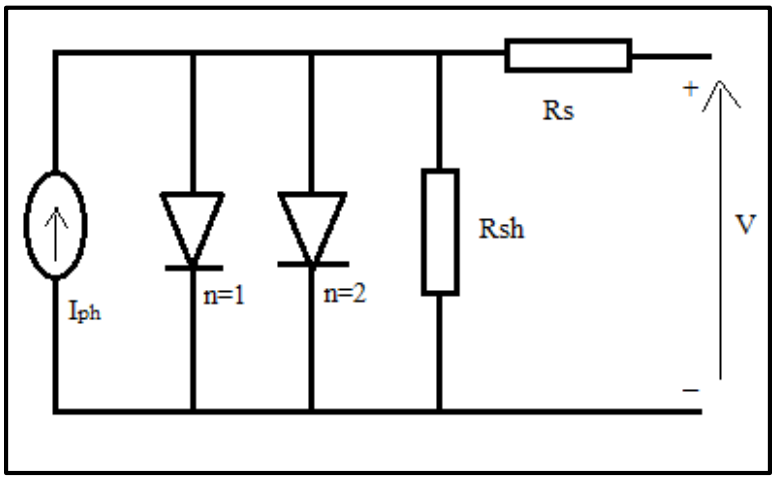


Figure 16: Two diode model of solar cell with series and shunt resistances.

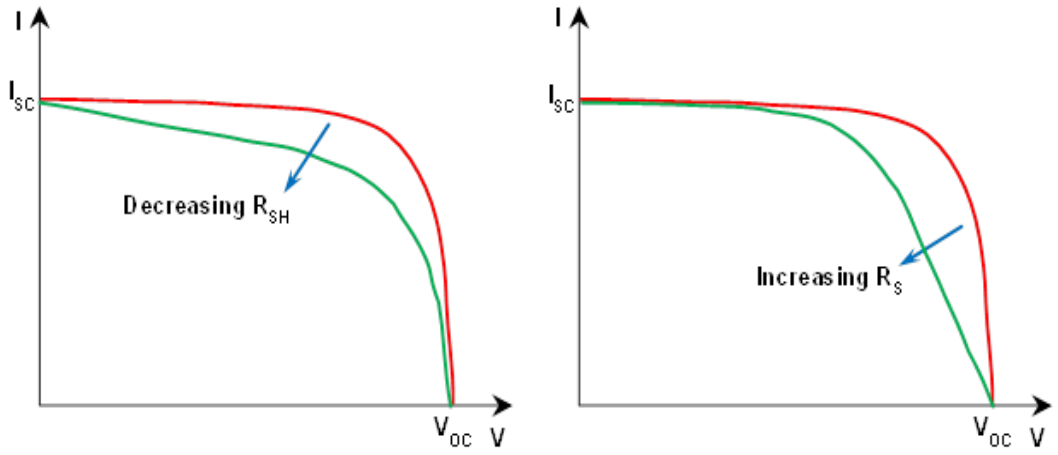


Figure 17: Effect of shunt and series resistance on Fill Factor [21]

2.4.1 Metal-Semiconductor Contacts

A metal-semiconductor contact is said to be ohmic if the charges from the semiconductor flow freely through the contact with minimal resistance. During metal deposition, as-deposited

metals may be ohmic or rectifying depending on the work function of the metal and doping levels and type of the semiconductor. Annealing metal-semiconductor contacts may change the type of the contact.

2.4.2 Transmission Line Measurement (TLM)

Of all the components that contribute to series resistance, metal semiconductor contact resistance is one of the most important and a figure of merit for ohmic contacts is specific contact resistance (ρ_c). Contact between metal and semiconductor can be explained as a resistive network. Measured total resistance at the metal semiconductor contact can be given as the sum of resistance due to metal (R_m), resistance due to contact (R_C) and resistance of the semiconductor (R_{semi}) [22].

$$R_T = 2R_m + R_{semi} + 2R_C \tag{36}$$

$$R_{semi} = R_S \frac{L}{W} \tag{37}$$

Compared to semiconductor resistance, metal resistance is usually neglected hence total resistance is given as,

$$R_T = R_S \frac{L}{W} + 2R_C \tag{38}$$

The above results suggest that when resistors of the same type of semiconductor are made with different lengths (L), total resistance can be measured as a function of distance and plotted as shown in Figure 18.

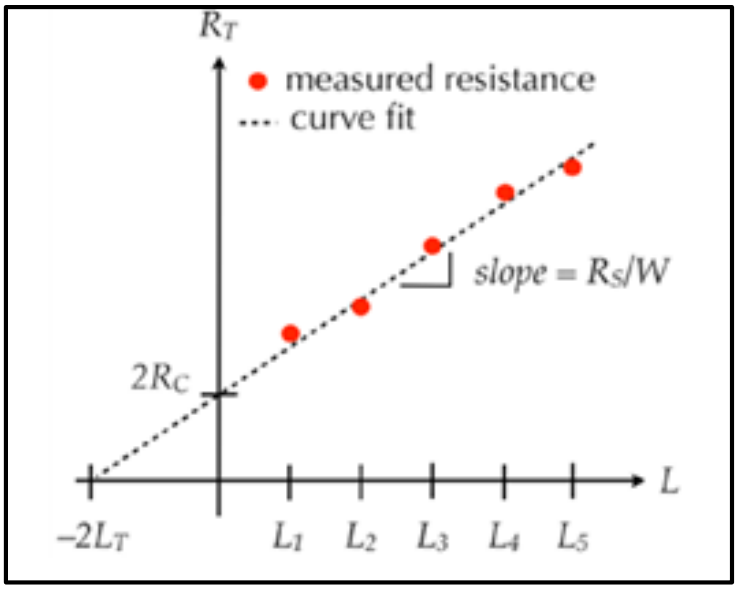


Figure 18: TLM plot to measure contact resistance [2].

Looking at the Equation 38, the slope of the line in the plot would be $\frac{R_S}{W}$ where, R_S is the sheet resistance. The Y-intercept is $2R_c$, where R_c is the contact resistance. The X-intercept is -$2L_T$, where L_T is the transfer length. Transfer length is the average distance an electron or hole travels before it flows up to the contact.

$$R_T = 0 = \frac{R_S(-2L_T)}{W} + 2R_C$$

Solving for L_T,

$$L_T = \sqrt{\frac{\rho_c}{R_S}} \tag{42}$$

where ρ_c=R_cW. Hence lowering ρ_c lowers R_c and series resistance. A TLM structure used to determine ρ_c is shown in Figure 19. A well-defined region, with doping equal to the emitter is

contacted by metal squares at varying distances. This structure is fabricated on the wafer as it goes through a series of fabrication steps.

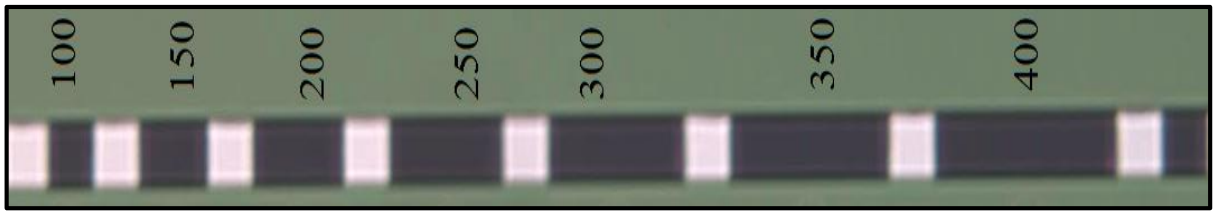


Figure 19: TLM structure on wafer (distance between metal squares in microns).

Fabrication procedure for solar cells in this project will be discussed in Chapter 3, and characterization techniques mentioned in this chapter will be used to evaluate the performance of the solar cells. The results will be discussed in Chapter 4.

CHAPTER 3: EXPERIMENTS

A turnkey solar cell process was developed at RIT to yield cells with modest efficiencies in a quick turnaround time with minimal processing steps [10]. The initial goal of this project was to optimize the process to improve cell efficiency, but that goal changed to study and investigate the contact materials for n-type doped silicon due to high metal contact resistance issues that arose. In this chapter, the general process for cell fabrication will be described followed by a description of the experiments performed.

3.1 Turnkey solar cell fabrication process flow

Device grade wafers are initially cleaned using the RCA (Radio Corporation of America) process in which mixtures of hydrogen peroxide with ammonium hydroxide or hydrochloric acid are used to remove any organic and metallic contaminants, respectively. A field oxide of thickness 350nm is grown in steam ambient at 1000^0C for 58 minutes. Oxide thickness was chosen based on simulations to mask the emitter implant in the field regions. The first lithography step was performed to define the emitter regions. Wafers are initially primed with HMDS (HexaMethylDiSilazane) to promote photoresist adhesion to the oxide layer. Wafers are then baked at 140^0C for 1 minute. HPR 504 Photoresist is spin coated at 3000RPM and a soft bake is performed at 100^0C for 1 minute. Contact alignment is used to expose the level 1 mask with the emitter design. The exposure time is calculated based on the photoresist dose and intensity of the light. Post exposure bake is done to remove any standing wave effects and edge roughness before developing the wafers in CD-26 or TMAH (TetraMethylAmmonium Hydroxide) which removes photoresist in exposed areas.

Oxide in the exposed emitter windows is thinned down in plasma etch with a mixture of gasses including CHF_3. Dry etch is employed to protect oxide on the back side of the wafer. Remaining oxide on the emitters is measured using a reflectance tool and a timed BOE etch is performed using 5.2:1 BOE (HF) solution to reach the bare silicon. Final masking oxide on the front and back sides are typically 350nm and 250nm, respectively. Emitter islands are implanted with Phosphorous (P^{31}) atoms at a dose of $2 \times 10^{15} cm^{-2}$ at 55KeV energy as shown in Figure 20. Dopant dose and energy were chosen to yield desired junction depth and sheet resistance following the thermal cycles.

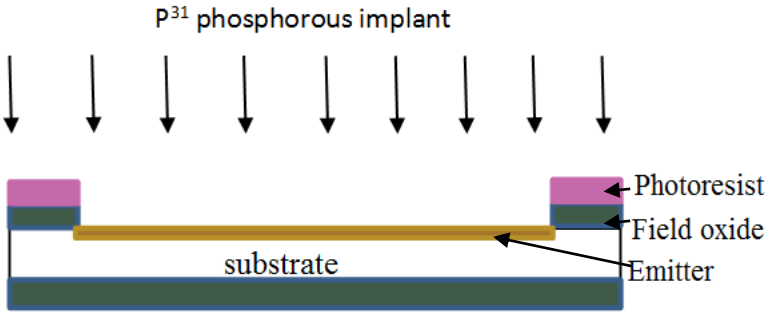


Figure 20: Phosphorous (P^{31}) implant during process flow

Photoresist is plasma stripped followed by an RCA clean to remove any contaminants. The implant dopants are then annealed and Anti-Reflective Coating (ARC) is grown in a single thermal step. This process of integrated anneal is done at 900^0C in the presence of nitrogen for 60 minutes to anneal any implant damage followed by steam for 12 minutes to grow the ARC layer. Finally, nitrogen flows for 120 minutes to drive the dopants into the substrate and define junction depth. The ARC thickness is measured with reflectance tool.

Second level lithography is performed by coating the wafers with HMDS, followed by a bake at 140^0C for 1 minute. Lift-off resist AZ-1518 is coated and soft bake is done at 100^0C for 1

minute. Contact exposure is done using level 2 mask; alignment marks on the wafer from the first level lithography are used to align to the second level mask. Exposure time is calculated based on intensity of the light from exposure tool and dose of the photoresist. Second level lithography defines grid lines and fingers for metal deposition. Post exposure bake is done at 100^0C for 1 minute. Exposed areas are developed in CD-26 TMAH developer and post development bake is done at 100^0C for 1 minute. The anti-reflective layer below exposed areas is etched in timed BOE and the wafers are spin rinse dried (SRD). This allows direct contact of the metal with silicon. The wafer after second level lithography is shown in Figure 21.

Figure 21: Wafer after second level lithography

For Aluminum metal contacts 99%Al/1% Si is used to prevent spiking at the metal semiconductor contact and to enhance ohmic contact formation. During Aluminum evaporation metal pellets are placed in tungsten baskets and the evaporator is pumped down to a base pressure below 5×10^{-5} Torr to avoid any contamination and achieve a desired mean free path length. Metal pellets are then evaporated from tungsten baskets by resistive heating achieved by passing high current through it. Approximately 1µm of aluminum is deposited on wafers by this evaporation process.

Wafers are removed from the evaporator and metal coated resist is removed by the lift-off process utilizing acetone in an ultrasonic wet bench. Following lift-off, the wafers are cleaned in

an IPA solution and spin rinse dried. For rear side metal deposition, the front of the wafer is protected from any contamination by coating with positive photoresist. Oxide on the back side of the wafer is removed in the BOE solution. Wafers are spin rinse dried and aluminum is evaporated on the back side, in a similar fashion as mentioned above, to deposit about 0.6 µm of metal. The protective resist is then stripped from the front surface and the wafers are sintered in H_2/N_2 forming gas ambient at 475^0C for 15 minutes. Final cross section of the wafer is shown in Figure 22.

Figure 22: Final cross section of completed wafer

3.2 Experiments for process optimization

Experiments performed to optimize the process are discussed in this section.

3.2.1 Substrate quality

Device grade wafers of resistivity 5-15 ohm-cm were chosen for the runs 1 through 4, and 1-5 ohm-cm wafers were used for a 5^{th} run. Wafers with low resistivity are preferred as the high substrate doping will yield larger V_{oc}, but very high doping of the substrate also increases recombination mechanisms. Therefore, different substrate dopings were chosen to monitor any affect in V_{oc}. A sample labelling scheme was adopted using R1, R2 for the runs and W1, W2 for each wafer in the run. Therefore, R4W3 would be third wafer in run 4.

3.2.2 Emitter optimization

Emitter dose and implant energy were carefully engineered using Athena simulation software to obtain desired junction depth and sheet resistance as the higher energy blue and green light is absorbed near the front surface which generates many minority carriers. With process flow mentioned in Section 3.1 different implant doses were chosen to optimize the junction depth to 1µm and sheet resistance to 100Ω/□ when coupled with anneal recipe as shown in Table 1 [20].

Table 1: Implant dose and energy engineering setup

P^{31} Implant		
Wafer	**Dose(cm^{-2})**	**Energy(KeV)**
R2W1	6×10^{14}	65
R4W1	2×10^{15}	55

The initial dose of 6×10^{14} cm^{-2} was chosen from prior turnkey process results and due to metal semiconductor contact issues, which will be discussed in Section 3.2.6, was later increased to $2 \times 10^{15} cm^{-2}$. Higher dose 2×10^{15} cm^{-2} along with lower implantation energy of 55KeV was chosen to achieve junction depth less than one micron and increase surface concentration to improve metal contact to n-type doped silicon.

3.2.3 Integrated anneal

During the integrated anneal, implanted dopants are annealed, the ARC layer is grown and the dopants are driven in. A four hour integrated thermal anneal process is done in the presence of nitrogen, along with steam or dry oxygen, as mentioned in Section 3.1. Two anneal temperatures were investigated to optimize the junction depth and ARC growth as shown in Table 2. Integrated anneal with oxygen was done in the presence of chlorine to passivate positive

oxide charges at the silicon, silicon-dioxide interface which could lead to surface inversion under the field oxide. During anneal, phosphorous dopants tend to outgas hence an oxide layer is grown before nitrogen anneal to reduce this out-diffusion. This is achieved by oxygen flown during initial ramp up from 800^0C to 900^0C for 15 minutes. Experiments with chlorine as part of the process were not possible in the tube with steam ambient. Implant recipes along with furnace anneal recipes were modeled to monitor junction depth, ARC thickness and surface concentration using Athena software. A typical simulation is shown in Figure 23.

Table 2: Furnace recipe engineering setup

Wafer	Ambient	Oxygen flow during ramp up	Temperature
R2W1	Steam	No	950^0C
R2W4	Dry Oxygen +TLC	No	950^0C
R4W1	Steam	Yes	900^0C

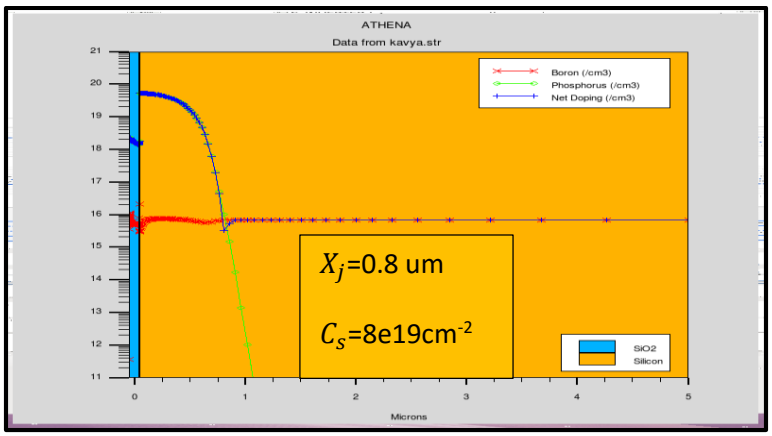


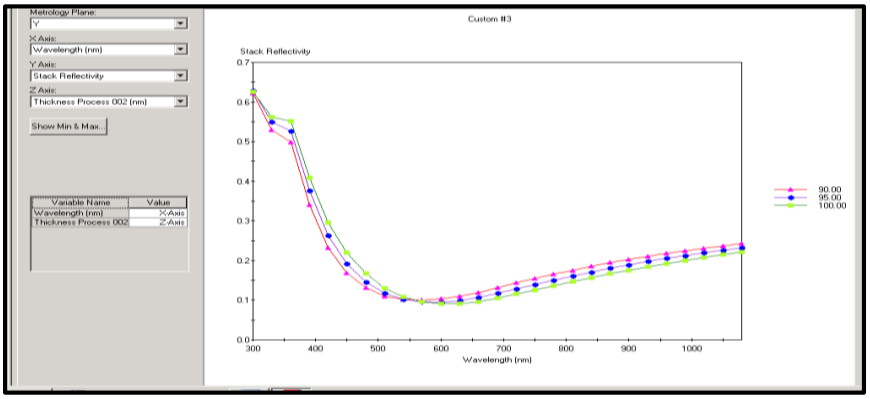
Figure 23: Athena simulation to model implanted dopants

3.2.4 Single layer ARC and Double Layer ARC (DLARC)

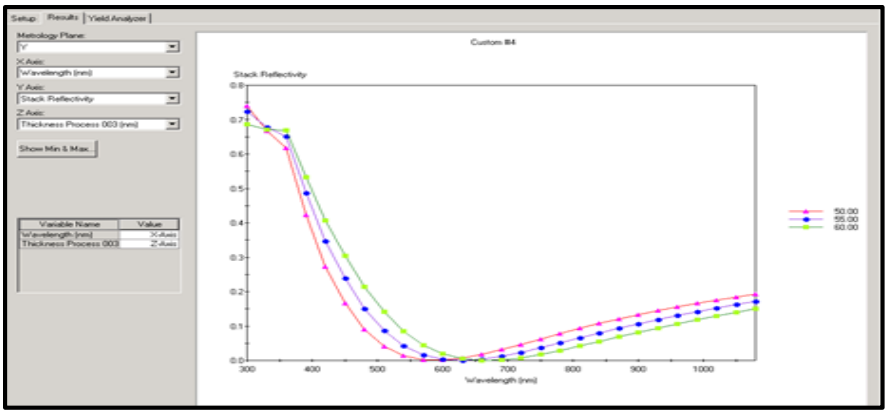
A single layer oxide anti-reflective coating was used to minimize surface reflections. Reflectance simulations using prolith showed a 95nm oxide thickness has the least reflectance at

550nm wavelength, where the incident energy is highest in visible spectrum. Figure 24 (a) is a Prolith output showing how reflectance changes with ARC thickness.

Double Layer ARC can be tailored using oxide and nitride layers to achieve less reflection. Thin oxide layer can be grown during integrated anneal and a nitride layer can be deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) to form a film stack. A stack consisting of 20nm oxide and 55nm nitride was simulated to achieve lowest reflectance using Prolith software as shown in Figure 24(b).



(a)



(b)

Figure 24: (a) ARC and (b) DLARC simulations for least reflectance via prolith

3.2.5 PC1D

PC1D is one of the commercial tools available to model solar cells. It is user friendly and can be used to evaluate device performance [20]. It is available for public use from University of New South Wales. Parameters such as doping densities, quantum efficiency, I-V curves, carrier generation and recombination can be evaluated. Figure 25 shows PC1D simulation for Run4 wafers with phosphorous implanted. PC1D input parameters used to for this simulation are listed in the Appendix.

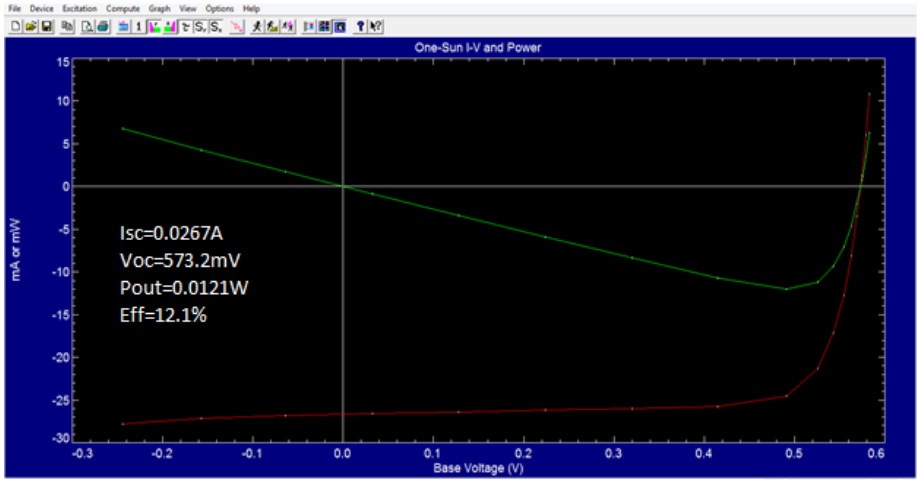


Figure 25: PC1D simulation showing I-V characteristics of a modeled cell

PC1D simulation had a predicted efficiency of 12.1%, but the achieved efficiency was 11.5%. This may be due to different front surface recombination velocities and bulk recombination in the actual device as compared to the values estimated in the model.

3.2.6 Spin-On dopants (SOD)

Spin-on dopants were used for the first run as the implanter was down for maintenance. Filmtronics P509 phosphorous spin-on dopant was coated using a manual spin coater at a spin of

3000 RPM for 30 seconds, followed by hot plate cure at 200^0C for 10 minutes. Pre-deposit was carried out at 850^0C for 30 minutes. Annealing is done in the presence of nitrogen along with oxygen (10:1 ratio). Oxygen flow during anneal was suggested in Filmtronics manual [23]. Dopants were also annealed in only nitrogen ambient to monitor any difference in the absence of oxygen. Oxide thickness was measured before and after pre-deposit to observe any changes in thickness. A plasma etch is performed on the front side to thin down the dopant film, followed by timed BOE etch down to bare silicon. This was done to maintain oxide coating on the back side of the wafer.

RCA clean was done to remove any contaminants. Dopants were then driven-in along with Anti-reflective layer growth in furnace for 4 hours. Ambients used during drive-in are explained in Section 3.2.3. Anti-reflective layer thickness was measured and Level 2 lithography was performed as mentioned in the Section 3.1.

3.2.7 Metallization

During Runs 2 and 3, a metal semiconductor contact issue arose. To address this issue, which will be discussed in detail further, aluminum was deposited on glass slides using two different methods, pellet and flash wire-feed evaporation. A significant difference in resistivity was observed between the two glass slides. Diodes were fabricated on test wafers to investigate this issue further. Aluminum was also deposited with a sputter tool (sputter target), to give additional results. This experiment was intended to observe resistivity differences between the same metal from different tools.

Three test wafers were RCA cleaned, 300nm oxide was deposited on the back side of the wafers in Plasma Enhanced Chemical Vapor Deposition (PECVD) tool. Oxide on the back of the

wafers protects the wafers from other existing dopants in the furnace during anneal after implant. Wafers were then blanket implanted with Phosphorous dopants (P^{31}) of dose $6 \times 10^{14} cm^{-2}$. An integrated anneal was performed to activate the dopants, drive them into the substrate and ARC layer was grown in steam ambient. Positive photoresist was coated on the front surface and the deposited oxide on the back side was completely etched off in a BOE solution. Aluminum of thickness 0.6μm was sputtered on the back of three wafers. Photoresist on the front side was removed using Acetone and IPA followed by spin rinse dry. Wafers were then sintered with same sinter recipe as mentioned in the Section 3.1, which rendered ohmic back contacts on all implanted wafers.

Wafers were then coated with photoresist on the backside and baked for a minute followed by 5.2:1 HF dip to remove oxide on the front surface. Different metals as shown in Table 3 were then deposited on the front surfaces using a shadow mask as shown in Figure 25 to make contacts for the diodes. These diodes could now be tested before and after sintering to investigate the front-side contact. Test runs are indicated as T1 or T2 to differentiate these experiments from solar cell runs.

Table 3: Aluminum deposition and sinter summary

Wafer	Aluminum Deposition method	Sinter
T1W1	Bell jar evaporator	Yes
T1W2	Flash evaporator	Yes
T1W3	Sputter	Yes

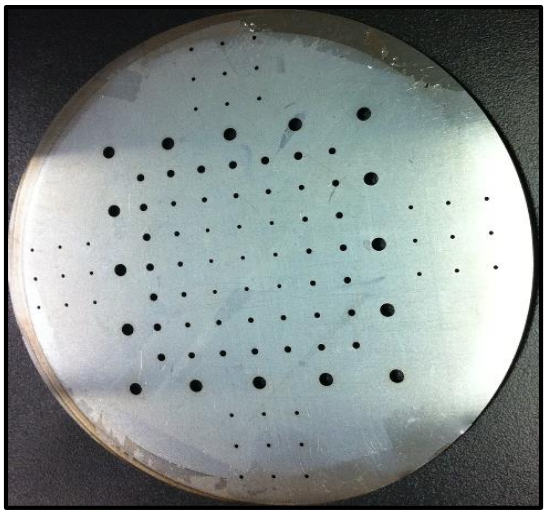


Figure 26: Shadow mask used for metal contacts.

The test results showed a significant difference in resistivity with the same initial metal deposited by two evaporation techniques.

Table 4: Metallization with different metals on test wafers

Wafer	Metal sputtered	Sinter
T2W1	Titanium/ Aluminum	No
T2W2	Aluminum	Yes

Commercial cells often use a titanium/palladium/silver (Ti/Pd/Ag) grid contact, so it was decided to complicate the PVD process by adding Ti deposition to see if there is a benefit. Experiments were done with Titanium/Aluminum (Ti/Al) and aluminum sputtered metal in a multi-target sputter tool, as shown in Table 4. During the experiments care was taken to maintain uniform metal thickness in order to compare output parameters. During Ti/Al sputter process, the aluminum target is pre-sputtered first at 1500W for 5minutes followed by titanium target pre-sputter at 700W for 5 minutes; titanium metal was then sputtered for 5 minutes at 700W to

obtain a thickness of 0.25µm and aluminum is sputtered for 20 minutes at 1500W to obtain a thickness 0.6µm. Ti/Al metal is reported to form a better contact with highly doped n-type silicon without sinter process [24], hence one wafer of Ti/Al was left without sinter. Results obtained from these test runs were used in Run 4 and the experimental setup is shown in Table 5.

Table 5: Metallization engineering setup

Wafer	Metal deposited	Deposition process	Sinter
R4W1	Titanium/Aluminum	Sputter	No
R4W2	Titanium/ Aluminum	Sputter	Yes
R4W3	Aluminum	Thermal Evaporator	Yes
R4W4	Aluminum	Flash Evaporator	Yes

3.2.8 Substrate dopant type

Traditionally p-type wafers were used for solar cells but n-type substrates have been under research, as n-type substrates are reported to be less sensitive to impurities that are usually present in silicon feedstock and are less susceptible to light induced degradation [25]. Also experiments suggest that n-type wafers with high diffusion length can be achieved from Czochralski process. Therefore, experiments were done on both p-type and n-type wafers as a first attempt utilizing turn-key process to fabricate n-type cells.

3.2.9 Back Surface Field (BSF)

A back surface field increases carrier collection at the rear of the cells. With the back surface implanted, metal semiconductor contact resistance also decreases. During Run 5, four device grade wafers were implanted on the back side with the same dopant as the substrate as shown in Table 6. BSF implant was done prior to RCA clean and the implanted dopants were

annealed during field oxide growth and the process was continued as mentioned in Section 3.1. Aluminum was deposited on the backside of the wafers as mentioned in Section 3.2.7. Metal deposited on the front was varied to monitor cells with less contact resistance.

Table 6: Back Surface Field engineering setup

Wafer	Substrate type	BSF	Metal grid	Sinter
Emitter (P^{31}, $2 \times 10^{15}cm^{-2}$ @55 keV); 900^0C Anneal				
R5W1	P type	B^{11} $1 \times 10^{16}cm^{-2}$ @50 KeV	Titanium/Aluminum	No
R5W3	P type	B^{11} $1 \times 10^{16}cm^{-2}$ @50 KeV	Aluminum evaporation	Yes
Emitter (B^{11}, $2 \times 10^{15}cm^{-2}$ @75 KeV); 900^0C Anneal				
R5W2	N type	P^{31}, $2 \times 10^{15}cm^{-2}$ @55 keV	Titanium/Aluminum	No
R5W4	N type	P^{31}, $2 \times 10^{15}cm^{-2}$ @55 keV	Aluminum evaporation	Yes

3.2.10 Layout design

Figure 27 shows a completed wafer. Cells with different area and shading were chosen for comparison purposes. Cells 1L and 1R were designed to have an area of $1.5625cm^2$ and have the same shading to compare uniformity of the process. Cells 2a, 2b have same area of $2.25cm^2$, same number of fingers but different shading. Cells 2a and 1 have same shading. Cells 3a, 3b have same area, $4cm^2$, but different number of fingers and different shading. Cells 3b and 4 have shading close to a commercial cell. Cells 4 and 5 are bigger with an area of $6.25cm^2$ and $9cm^2$. All the cell dimensions, number of fingers on each cell and shading are tabulated in Table 7

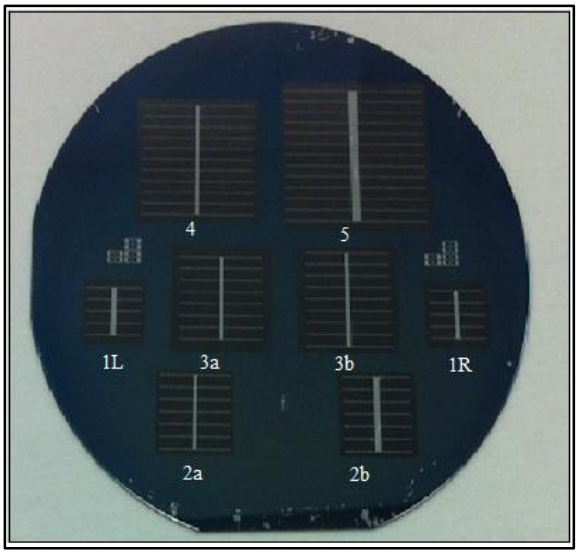


Figure 27: Final completed wafer

Table 7: Cell dimensions and shading

Cell	Dimension	Number of Fingers	Shadow
1	12.5x12.5	5	8.18 %
2a	15x15	7	8.18%
2b	15x15	7	9.94%
3a	20x20	8	6.11%
3b	20x20	9	6.92%
4	25x25	11	6.88%
5	30x30	13	9.05%

3.3 Characterization

3.3.1 I-V and Quantum Efficiency measurement

Fabricated solar cells were tested for I-V characteristics, Quantum Efficiency, Reflectance and contact resistivity to quantify the performance. Cells were tested under AM1.5G radiation using a solar simulator for I-V characteristics. I-V characteristics on one of the cells

was measured at College of Nano Science and Engineering (CNSE), Rochester, to confirm performance and quantify calibration of solar simulator at RIT. Figure 28 shows the equipment for I-V test. During I-V measurements wafers were grounded on a chuck and two probes were in contact with busbar to provide top contact. Using programmed software J_{sc}, V_{oc} , FF and efficiency were obtained.

For External Quantum efficiency measurement, the wafers were grounded on a chuck and a single metal probe contact on the busbar serves as top contact as shown in Figure 29. Light scanned at wavelengths starting from 300nm to 1100nm in intervals of 20 nm, and is allowed shine between the fingers of the cells and external quantum efficiency curves were obtained.

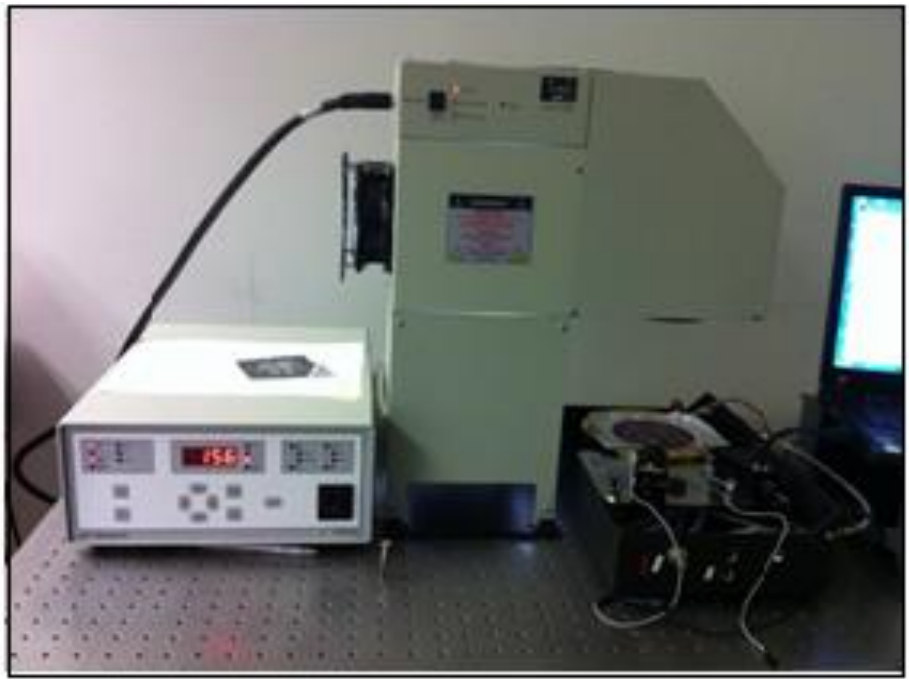


Figure 28: I-V measurement setup at RIT

Figure 29: Quantum Efficiency measurement setup at RIT

3.3.2 Transmission Line Measurement (TLM)

Transmission Line Measurement (TLM) technique, as mentioned in Chapter 2 was used to measure contact resistance. For a TLM measurement the back side of the wafer is grounded with the help of a vacuum chuck and two probes are used for the front metal contact. Use of four probes during the measurement eliminates any resistance from the measuring probes. I-V data was recorded separately at 250µm, 300µm, 350µm and 400µm distances of TLM structure as discussed in Chapter 2.4.2. Average resistance values are calculated for each of the measured distance based on the current and voltage values. Resistance values were plotted against distance to obtain contact resistance.

Chapter 4 will discuss the results from these experiments.

CHAPTER 4: RESULTS AND DISCUSSION

The results of different experiments mentioned in Chapter 3 are reported and discussed in this chapter.

4.1 Spin-on dopants and TLC

Experiment 1 was performed with Filmtronics P509 Spin-on Dopant. Furnace recipes were varied for different wafers to monitor output parameters as a function of ambient conditions during pre-deposition and drive-in as shown in Table 8. All the wafers were pre-deposited at 850^0C and were driven-in at 900^0C. Ambient changes were associated with residual charge levels in the oxide films.

Table 8: Furnace setup for wafers with spin-on dopants

Wafer	Pre-deposit ambient	Drive in ambient
R1W1	Only N_2	Dry O_2
R1W2	Only N_2	Dry O_2+TLC
R1W3	N_2+O_2	Dry O_2
R1W4	N_2+O_2	Dry O_2+TLC

TLC is a furnace clean recipe which contains chlorine and is used to grow higher quality oxides with less trapped and mobile oxide charges. R1W2 with only nitrogen during pre-deposit and oxygen along with TLC during drive-in, had better V_{oc} (0.53V), J_{sc} (27mA/cm^2) and fill-factor (76%) compared to other wafers. Wafers that received 10:1 nitrogen: oxygen during pre-deposit, although recommended by Filmtronics, had poorer performance metrics.

If the substrate is a lightly doped p-type wafer, the surface underneath the field oxide is vulnerable to inversion from charges in the masking oxide. This would result in low shunt

resistance and high leakage current which degrades V_{oc}, J_{sc} and FF. When testing the PV cell, electrons from this inverted region may enter the depletion region around the cell, increasing the diode leakage current in the dark and lowering the photogenerated current through recombination. Negative charge from chlorine during drive-in may act to balance the positive charges in the oxide preventing inversion. Hence wafers driven-in with a chlorine ambient would have better output characteristics. This was observed for R1W2.

Figure 30 compares I-V curves in the presence and absence of TLC during drive-in. A significant increase in efficiency from 7.5% to 9.7% was observed in the presence of chlorine comparing wafer 1 and 2.

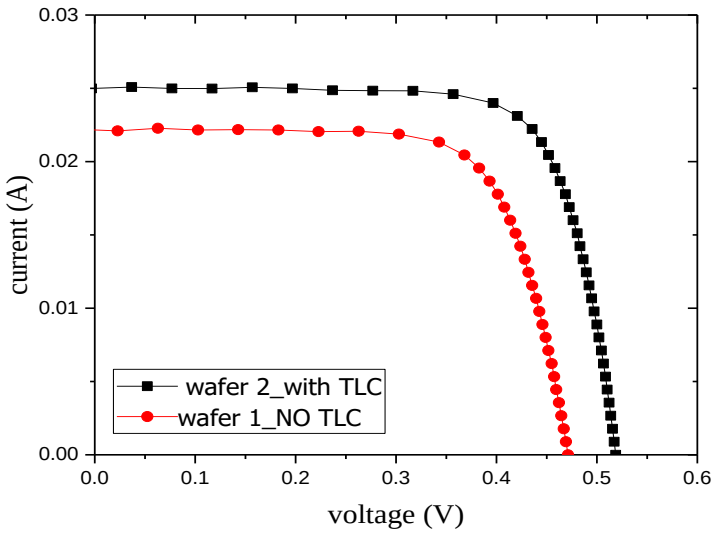


Figure 30: I-V curve comparison for the presence/absence of chlorine

This result indicates that the p-type wafer without TLC may have surface inversion due to oxide charges. The decrease in V_{oc} and J_{sc} indicates lower shunt resistance for wafer 1. Wafer 3 and wafer 4 had significantly lower fill factors and efficiencies, indicating that oxygen flow during

pre-deposit is not a good idea. Measured ARC thickness was 70nm as opposed to the target of 95nm. This results in 24% of incident light lost as reflection, so better efficiencies were possible.

Overall, Spin-on Dopants have good potential for PV fabrication, as they form emitters with high surface concentration. However, care is required to engineer the desired junction depth and sheet resistance during an integrated anneal.

During this experiment, after the wafers were pre-deposited, granulated patterns were observed in the oxide through optical microscopy as shown in the Figure 31. The reason for patterns may be due to film thickness decrease from 800nm to 270nm after pre-deposit, owing to change in density. A reaction in the film with the cleanroom ambient over time was observed which affected the thickness uniformity across the wafer. For these reasons ion-implantation was investigated as an alternative to spin-on dopant.

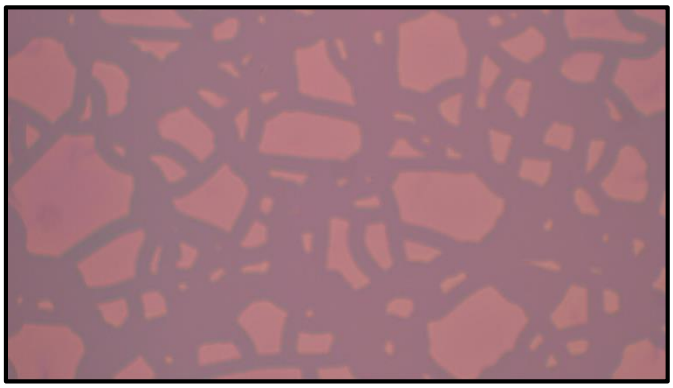


Figure 31: Granulated film observed on field oxide after Spin-on Dopant pre-deposit

4.2 Run 2 and 3 results with ion implantation

During Run 2, dopants were introduced into the substrate by ion implantation. An implant dose of 6×10^{14}cm^{-2} (P^{31}) was chosen from simulation to match the junction depth. A flash evaporator which uses wire feed of 99% Al/1% Si was used for metal deposition. When tested these wafers had good V_{OC} and J_{SC}values of about 0.45mV and 21mA/cm^2, respectively,

but the fill factors were about 65 % which indicated high series resistance. Series resistance of about 18-20 ohms was extracted from the solar simulator and high contact resistivities of about 8×10^{-2} ohm-cm^2 were calculated using the TLM structure on the wafer. Ideal contact resistivity of aluminum with silicon substrate is in the range of 1×10^{-5} ohm-cm^2 to 1×10^{-7} ohm-cm^2 [26]. Investigation into potential processing issues showed that the wafers did not have forming gas during the sinter which went undetected as the furnace alarm was inactive. This could have oxidized the Al surface which would increase contact resistance. The wafers were sintered again, but there was no improvement.

Experiment 3 was a repeat of Experiment 2. During this experiment the furnace ambient during ARC growth was varied to monitor the affects on output parameters. Table 9 summarizes these ambients. R3W4 had an initial ARC thickness from steam ambient which was low, hence this oxide was thinned down to 10-15nm in plasma assisted dry etch. A Plasma Enhanced Chemical Vapor Deposition (PECVD) nitride of thickness 50-60nm was deposited to form DLARC.

Table 9: Furnace engineering setup for Run 3

Wafer	Ambient during ARC growth
R3W1	Dry O_2
R3W2	Dry O_2+TLC
R3W3	Dry O_2+TLC
R3W4	Steam + PECVD nitride
R3W5	Steam

All these wafers had very low efficiencies along with very high contact and series resistance. Under electrical testing apparatus, the metal appeared “darker” than normal. Optical microscopy revealed significant surface features as shown in Figure 32. This raised concerns regarding the Al films from the flash evaporator.

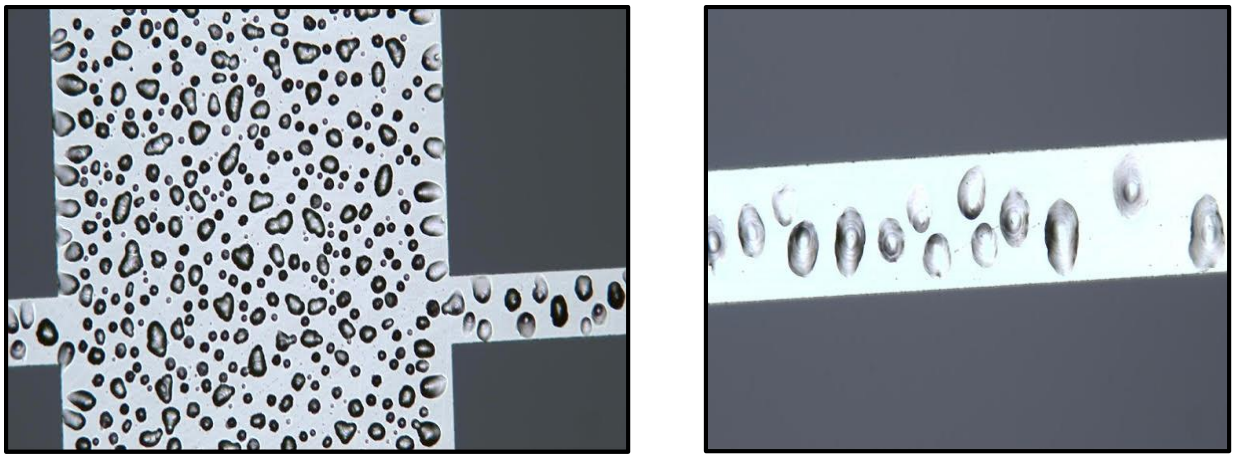


Figure 32: Defects oberved on the matal busbar and finger

4.3 Test runs to investigate metallization issues

To investigate the high contact resistance issues observed in Run 2 and Run 3, 99%Al/ 1% Si was deposited on two glass slides. One slide was coated using a Bell-jar evaporator and, the other one in a flash evaporator. The resistivities of the two films, as listed in the Table 10, showed a substantial difference. The resistivities were computed using sheet resistance data from a CDE resmap tool and film thickness from Tencor P2 profilometer.

Table 10: Glass wafer setup to monitor resistivities

Glass slide	Deposition technique	Resistivity
Glass slide 1	Bell jar evaporator	3×10^{-6} ohm-cm
Glass slide 2	Flash evaporator	6.9×10^{-6} ohm-cm

As it was observed that although the same initial metal was used for deposition, the resistivity of the film from the Flash evaporator was more than two times higher. This raises a possibility of contaminants from the ambient being a factor. This experiment was further continued to fabricate diodes to study film performance as metal contacts.

Three test wafers were used to fabricate diodes to monitor resistivities as mentioned in Section 3.2.7. The Al-Si was deposited on the front surface of the wafers using the Bell-jar evaporator on T1W1 and the Flash evaporator on T1W2. A CVC 601 sputter tool with a 99%Al/ 1%Si target was also used for deposition on T1W3. Glass slides were used during deposition along with the wafers to monitor deposited metal thickness and resistivity as shown in Table 11.

Table 11: Thickness and resistivity results for various Al-Si films

Wafer	Deposition technique	Thickness of metal deposited	Resistivity
T1W1	Bell jar evaporator	0.51µm	3×10^{-6}ohm-cm
T1W2	Flash evaporator	0.53 µm	6.9×10^{-6}ohm-cm
T1W3	Sputter	0.58 µm	8.5×10^{-6}ohm-cm

Resistivity of the film deposited in the Flash evaporator was more than two times higher when compared to the film deposited in the Bell-jar evaporator and seen previously. Resistivity of the sputtered film was even higher when compared to the Flash evaporated film. Wafers were then cut in half, and one half of each wafer was sintered to observe any change in resistivity of the metal after sinter.

Sintered and un-sintered wafers were then tested for I-V characteristics using 4145A semiconductor parameter analyzer. The voltage required to achieve 30mA of current for different test diodes is shown in Figure 34. Only the sputtered film shows a reduction in voltage upon

sinter as seen in Figure 33 and Figure 34. This is normally expected due to native oxides present during deposition. The increase in voltage for evaporated films indicates additional reactions that may be hindering the performance. Since the flash-evaporated film has the highest voltage to pass 30mA, it may be assumed this contact has the most resistance.

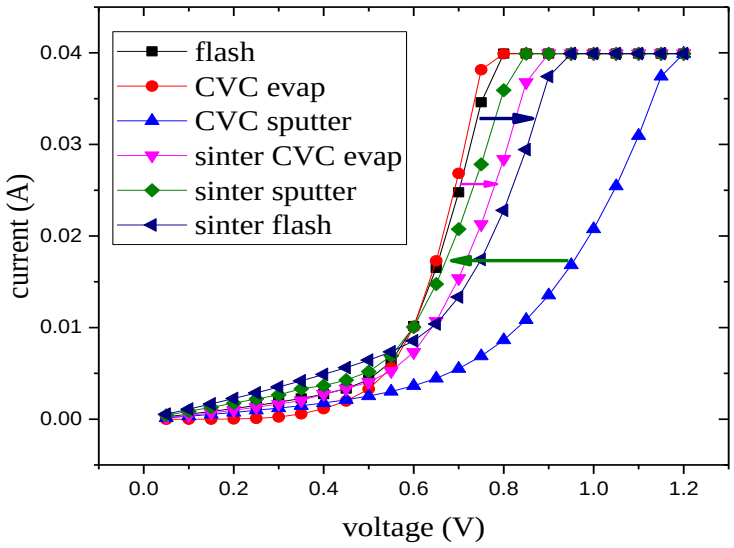


Figure 33: I-V comparison for sintered and un-sintered wafers where the arrows show the shift in voltage resulted from sinter

Titanium/Aluminum (Ti/Al) metal was chosen as it forms low resistive contacts with n-type semiconductors [24]. Two wafers were prepared in the same procedure as the previous test wafers. Ti/Al and Aluminum were sputtered on two wafers in the same procedure as mentioned in Section 3.2.6. Wafers were then split in half and one half of each wafer was sintered to monitor the affect of sinter process. Wafers were tested using 4145A parameter analyzer.

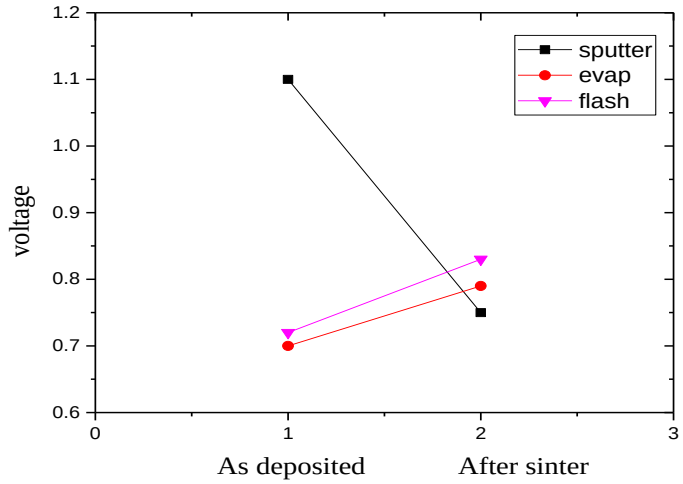


Figure 34: Voltage shift required to achieve 30mA of current for different samples

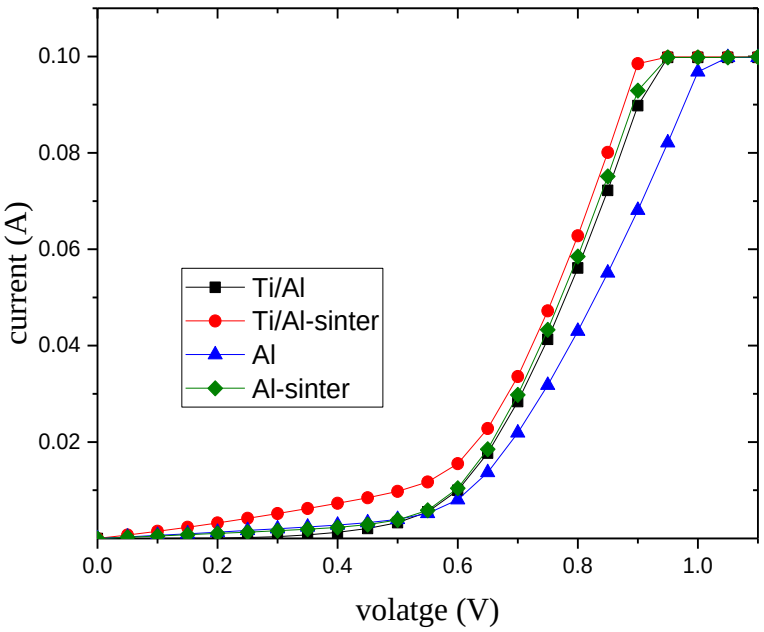


Figure 35: Ti/Al vs. Al contacts before and after sinter

Figure 35 compares the I-V curves of the diodes with Ti/Al and Al metal before and after sinter. The as-deposited Al curve has a lower slope, indicative of parasitic resistance. Sintering increased the slope without changing the turn-on voltage. The Ti/Al contact essentially matched the sintered Al curve for the sputtered film. Sintering of the Ti/Al contact shifted the entire curve showing no change in slope, but more leakage. For this reason, any Ti/Al contacts would not be sintered, for good cell performance.

4.4 Run 4 adopting resulting from test runs

During Run 4, implant dose was changed to 2×10^{15} cm^{-2} to increase surface dopant concentration; furnace temperature was reduced to 900^0C to reduce the junction depth to 0.7μm, and Ti/Al and Aluminum were deposited and sintered as mentioned in Chapter 3 and the results of this run are summarized in Table 12.

Comparison between efficiencies and contact resistivities from Run 4 wafers is shown in Figure 36. The Ti/Al contact to the n-type emitter was best when left un-sintered (W1) and performance degraded when sintered (W2). Ti/Al had contact resistivity of 2.5×10^{-5} ohm-cm^2; ideally Ti/Al contact with Si would have contact resistivity in the range of 5×10^{-6} ohm-cm^2 to 3×10^{-5} ohm-cm^2 [27]. This indicates that un-sintered Ti/Al is a better metal of choice for n-type emitter. Also fill factors achieved during Run 4 were in the range of 70-75% indicating low series resistance. A sample TLM measurement for R4W1 is shown in Figure 37 and parameters described in Chapter 2.4.2 are extracted from the plot.

Table 12: Run 4 results summary

R4W1(Ti/Al)	Area(cm^2)	Jsc(mA/cm^2)	Voc(V)	FF(%)	Eff(%)	n1	n2	Contact resistivity
1R	0.5625	28.29	0.548	74.15	11.49	1.5	2.7	2.5×10^{-5} ohmcm²
2b	2.25	26.49	0.552	75.00	10.96	1.3	2.7	2.5×10^{-5} ohmcm²
3b	4	23.15	0.518	73.20	8.78	1.4	2.4	2.5×10^{-5} ohmcm²
R4W2(Ti/Al sinter)	**Area(cm^2)**	**Jsc(mA/cm^2)**	**Voc(V)**	**FF(%)**	**Eff(%)**	**n1**	**n2**	**Contact resistivity**
1R	0.5625	27.23	0.535	63.49	9.24	2.8	3.1	8.5×10^{-5} ohmcm²
2b	2.25	26.21	0.534	64.78	9.07	1.4	2.8	8.5×10^{-5} ohmcm²
3b	4	24.25	0.513	53.80	6.69	1.9	2.8	8.5×10^{-5} ohmcm²
R4W3(Al sputtered)	**Area(cm^2)**	**Jsc(mA/cm^2)**	**Voc(V)**	**FF(%)**	**Eff(%)**	**n1**	**n2**	**Contact resistivity**
1R	0.5625	28.01	0.545	74.06	11.31	1.4	2.6	3.2×10^{-5} ohmcm²
2b	2.25	27.46	0.543	72.59	10.83	1.7	2.9	3.2×10^{-5} ohmcm²
3b	4	24.65	0.520	68.73	8.79	1.6	2.8	3.2×10^{-5} ohmcm²
R4W4(Al evap)	**Area(cm^2)**	**Jsc(mA/cm^2)**	**Voc(V)**	**FF(%)**	**Eff(%)**	**n1**	**n2**	**Contact resistivity**
1R	0.5625	26.18	0.536	74.77	10.50	1.5	2.5	4.5×10^{-5} ohmcm²
2b	2.25	25.80	0.538	74.52	10.34	1.5	2.8	4.5×10^{-5} ohmcm²
3b	4	24.85	0.517	68.86	8.85	1.6	2.7	4.5×10^{-5} ohmcm²

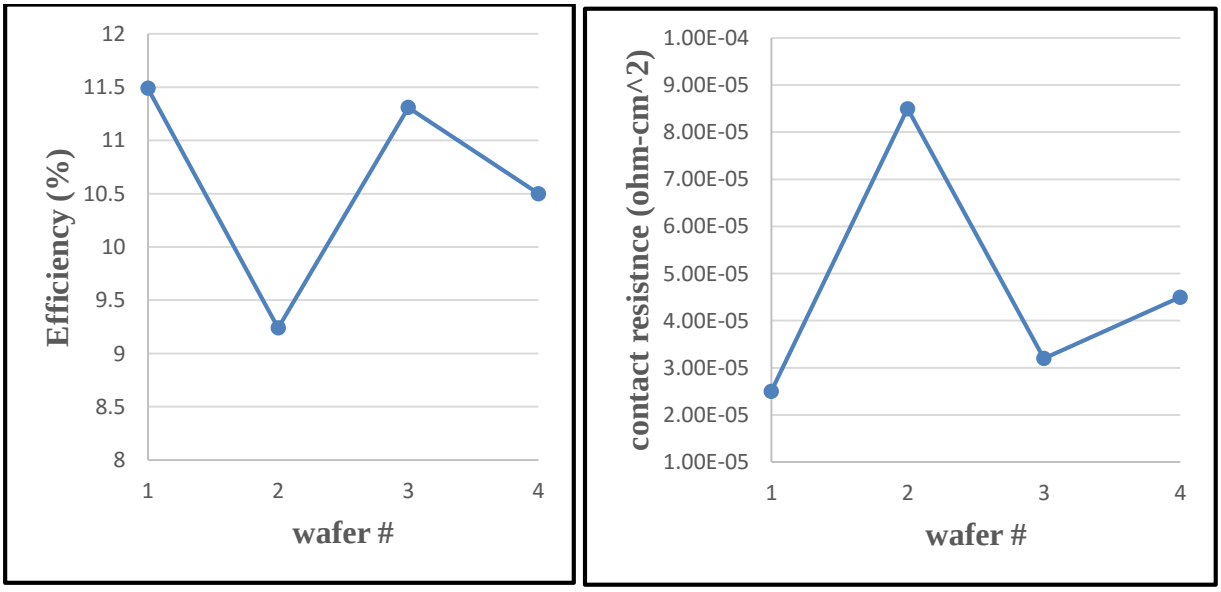


Figure 36: Comparison of Run 4 efficiencies and contact resistances

d (um)	R
200	93.6
250	117
300	140
350	160
400	182

W=Z (um)	100
L (um)	100
Intercept-y	6.64
Slope	0.43960
pm (Ohm/sq)	0
Rc(ohm)	3.32
Intercept-x	-15.10
LT (um)	7.55
Rsh (ohm/sq)	43.96
rho_c (ohm-cm2)	2.5E-05
pc1 (ohm-cm2)	2.5E-05
LT' (um)	7.55
pc2 (ohm-cm2)	2.51E-05

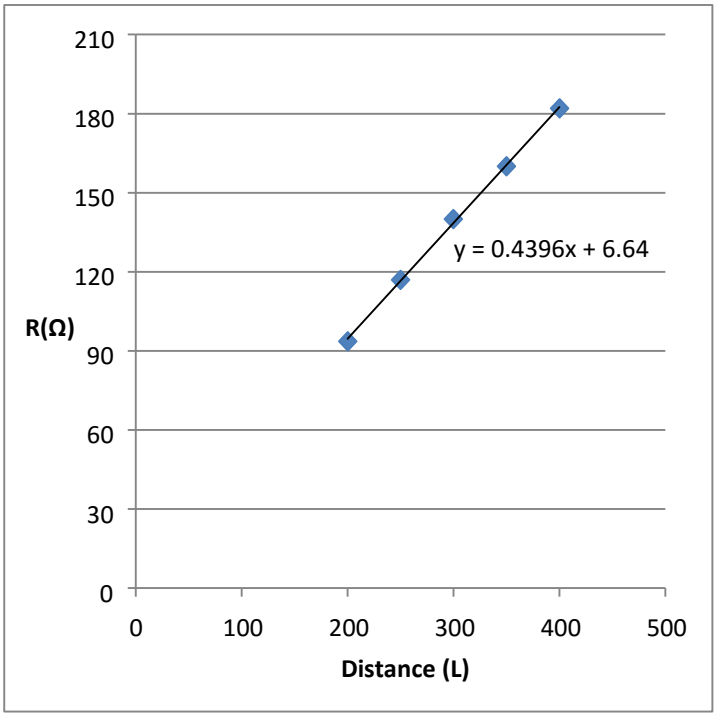


Figure 37: TLM measurement on R4W1

External Quantum efficiency comparison plot for R4W1 and W2 is shown in Figure 38 also indicate that the wafer with un-sintered Ti/Al metal is ideal for carrier collection. An interesting trend is observed as all the wafers have the same EQE for wavelengths less than 550nm and vary largely with increasing wavelength. With same wafer processing, but different metallization schemes, a difference in EQE indicate changes are occurring in the bulk carriers explaining this observation will require additional studies.

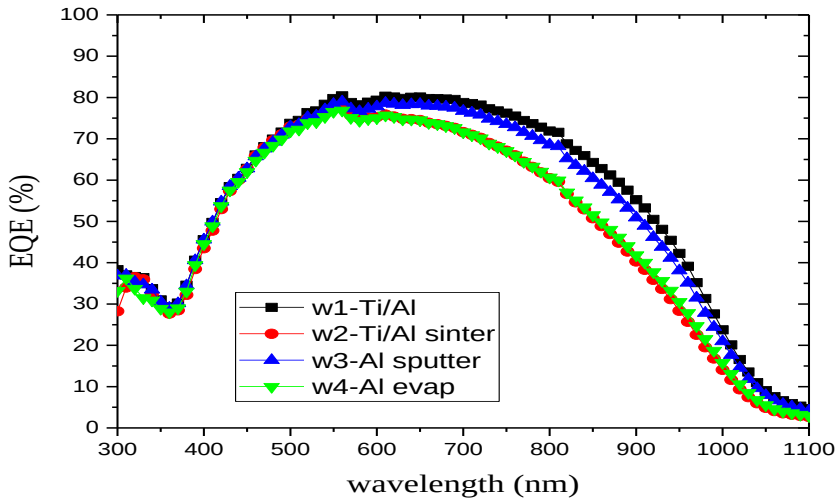


Figure 38: External Quantum Efficiency comparison plot

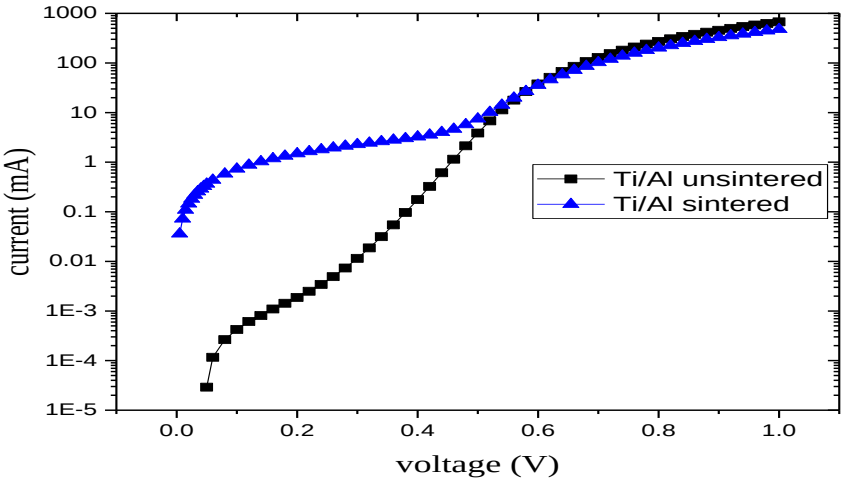


Figure 39: Dark I-V curve of Ti/Al contacted cells ohmic effect after sinter

A comparison of the Ti/Al contact using ln(I)-V curve plot, as shown in Figure 39, clearly shows the deleterious effects sintering had on the Ti/Al contact quality as there is a dramatic increase in leakage current due to recombination. This may signify a shunt issue as well as increased recombination.

4.4.1 J_{01} and J_{02} extraction

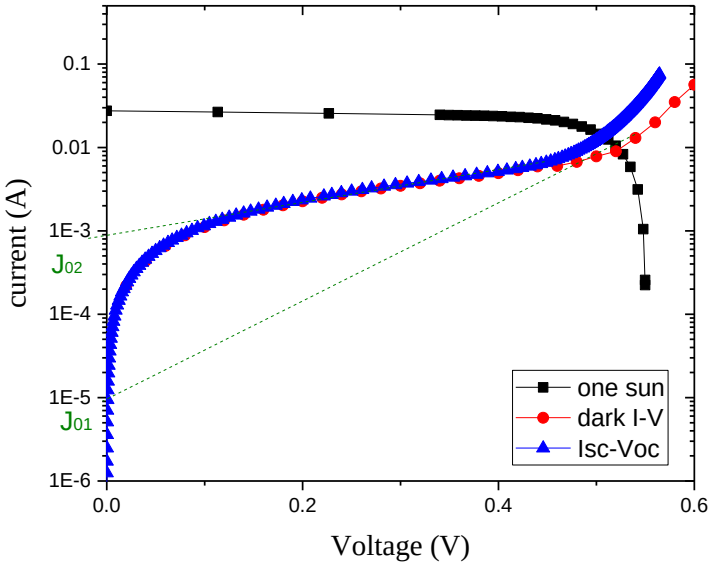


Figure 40: Overlay of one sun I-V, dark I-V and Jsc-Voc

To extract series and shunt resistance values along with J_{01} and J_{02} a one-sun I-V, dark I-V and J_{sc}-V_{oc} are plotted together as shown in Figure 40. To trace J_{sc}-V_{oc} curve, illumination is varied on the cell (R4W2-1R) and the J_{sc} and V_{oc} are measured at each illumination level. Series resistance is absent in J_{sc}-V_{oc} curve as the series resistance has no effect on V_{oc} as no current is drawn, and it has no effect on J_{sc} as long as the series resistance is less than 10 ohm-cm^2 since the I-V curve is flat around J_{sc} [20]. Series resistance is calculated as a difference in voltage between J_{sc}-V_{oc} plot and dark I-V plot divided by the current at maximum power point of one sun measurement. Shunt resistance is the slope of I-V curve in the reverse bias.

Extracted series resistance was about 2 ohms and shunt resistance was about 100 ohms. Ideal series and shunt resistances would be in the range of milliohms and kilo-ohms,

respectively. Extrapolated J_{01} and J_{02} values were 1×10^{-5}A/cm^{-2} and 1×10^{-3}A/cm^{-2}, respectively. Ideally J_{01} and J_{02} values are in the range of fA/cm^{-2} and nA/cm^{-2}. Also the ideality factors were not exactly 1 and 2, this might be due to high shunt resistance domination on the overall performance. Ideality factor n1 is greater than 1, when there is a high leakage current due to high J_{02} or low shunt [28]. In this case this is due to lower shunt. J_{sc}-V_{oc} and dark I-V plot overlap for R4W1 indicating very low series resistance.

4.4.2 Isolated cells from the wafer to test surface inversion

As mentioned earlier all the p-type wafers may have surface inversion under the field regions due to oxide charges. Hence cells 2a, 2b of Wafers 1 and 4 from Run 4 were isolated by cleaving the wafer using a diamond scribe and I-V data was measured and tabulated as shown in Table 13.

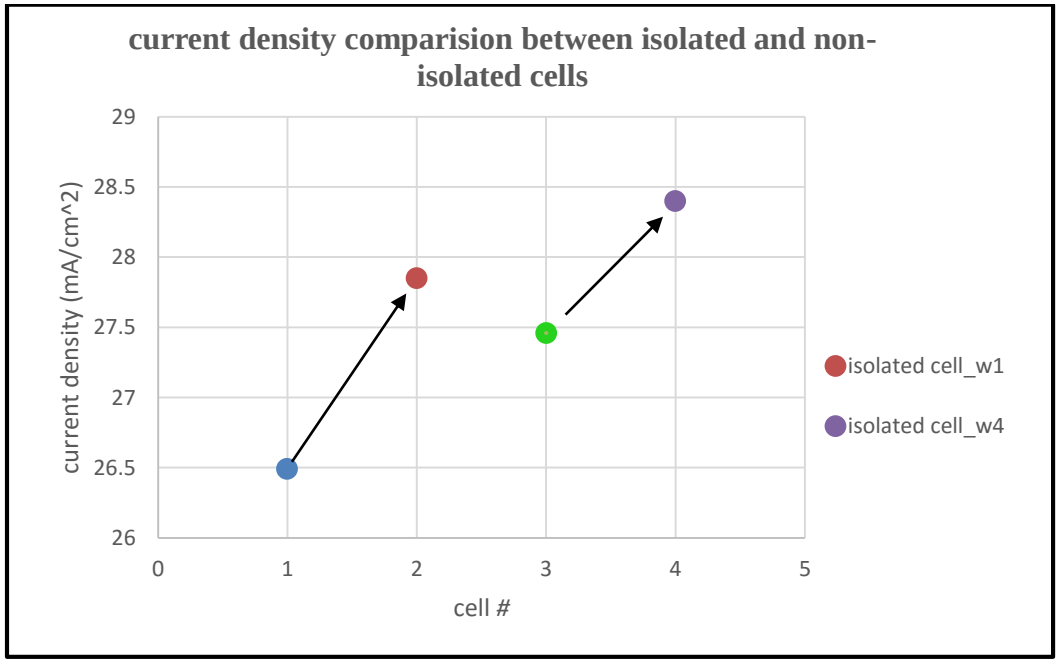


Figure 41: Comparison of current densities for isolated and non-isolated cells

Table 13: Output parameters of isolated cells during Run 4

R4W1(Ti/Al) (un-sintered)	Area(cm^2)	Jsc(mA/cm^2)	Voc(V)	FF(%)	Eff(%)
2b	2.25	26.49	0.552	75.00	10.96
2b-1 (isolated)	2.25	27.85	0.550	74.8	11.46
2a	2.25	25.6	0.550	74.5	10.48
2a-1(isolated)	2.25	26.9	0.539	74.3	10.77
R4W1(Al evaporated)	**Area(cm^2)**	**Jsc(mA/cm^2)**	**Voc(V)**	**FF(%)**	**Eff(%)**
2b	2.25	27.46	0.543	72.59	10.83
2b-1(isolated)	2.25	28.4	0.542	72.35	11.14
2a	2.25	26.67	0.540	71.6	10.31
2a-1(isolated)	2.25	27.71	0.536	71.4	10.6

An increase in the current density of about 1.5mA/cm^2 was observed as shown in Figure 41 for the isolated cells and this supports the hypothesis that the wafer surface under field region may be inverted.

4.5 Secondary Ion Mass Spectroscopy (SIMS)

The difference in performance of Al/Si films led to concern regarding film purity or possibility of contaminants in the film. SIMS is a metrology technique used to analyze composition of the surfaces, interfaces, and thin films by sputtering the material with a focused ion beam. These ions strike the surface and the secondary ions ejected from the sample are collected. The ions are analyzed in a vacuum chamber with a mass spectrometer. This measurement requires ultrahigh vacuum (around 10^{-10} to 10^{-12} torr) [29]. The mass spectrometer can separate the ions, which are focused onto an electron multiplier. An impact of single ion creates a cascade of electrons and the resulting pulse is recorded. Pulse size correlates to ion mass and count rate correlates with concentration in the film. Figure 42 is a schematic of the SIMS technique.

The incident ions are usually selected to be Cs^+, O_2^-, O_2^+ or Ar^+ based on the collision chemistry that can best produce secondary ions [29]. Time of Flight (ToF) mass spectrometer has high mass resolution and high sensitivity (ppm/ppb range) and hence trace elements can be detected and quantified. ToF-SIMS can detect as many as 10 to 50% of the emitted ions while other mass spectrometers can detect only 0.001% of the emitted ions. In ToF-SIMS depth profiling analysis, two ion beams are used. First ion beam is used for sputtering a crater, while the second beam is used for analysis. The rate of material removal is very slow, so that only a fraction of surface layer may be removed in an hour. Hence ToF-SIMS can be considered a nondestructive technique to analyze very thin films on wafer surfaces.

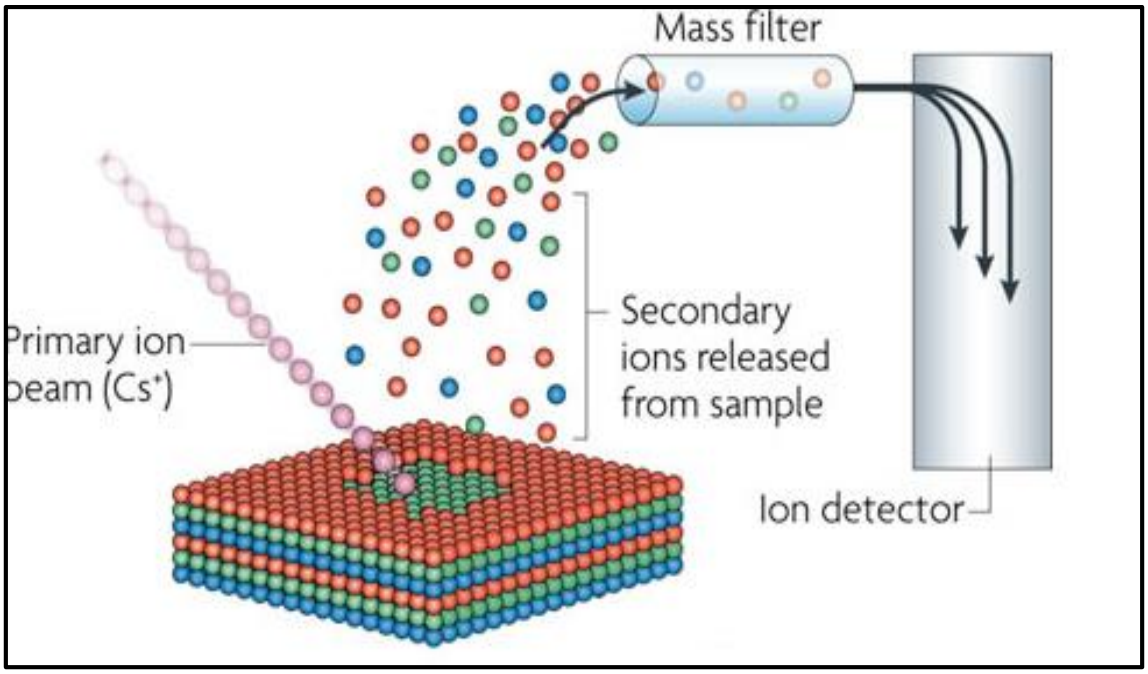


Figure 42: SIMS analysis of a sample [30]

4.5.1 SIMS analysis

ToF-SIMS was used to study the chemical composition of deposited 99%Al/ 1% Si metal films. ToF SIMS was used to analyze three films, one each from the flash and resistive heating

evaporators using the same wire source, and a sputtered film. Samples were cleaved and half of them were annealed to investigate any changes from thermal activation.

While no major sources of film contamination appeared in the spectra, there was an interesting trend in the relative concentration of Si. Since the films are normally 99% Al/ 1% Si, comparison of major Si and Al peaks in the spectrum is difficult. However, Al readily forms a molecular fragment AlH^+, which has a mass of 26.98+1.008=27.99amu while Si^+ is 28.0855amu. Because, the AlH^+ fragment has small probability of formation, the result was two peaks of relative intensity side-by-side, resolvable in the ToF-SIMS spectra.

Figure 43 shows SIMS spectra for various samples. Using the area under each curve as the total counts, a ratio of Al/Si signal strength was computed. Table 14 summarizes the peak ratios. In all as-deposited films the amount of AlH^+/Si is larger than 1, with only the resistively heated evaporated film with the ratio near 1. After sinter, all ratios decreased below 1, except for the flash evaporated film. Based on this data, we conclude the flash-evaporated film is Si deficient and sintering leads to a film dramatically different from the other two.

Table 14: Ratio of Al/Si present in the films

Deposition method	As deposited	After sinter
Sputter	2.9	0.16
Evaporator	1.2	0.8
Flash	2.5	1.7

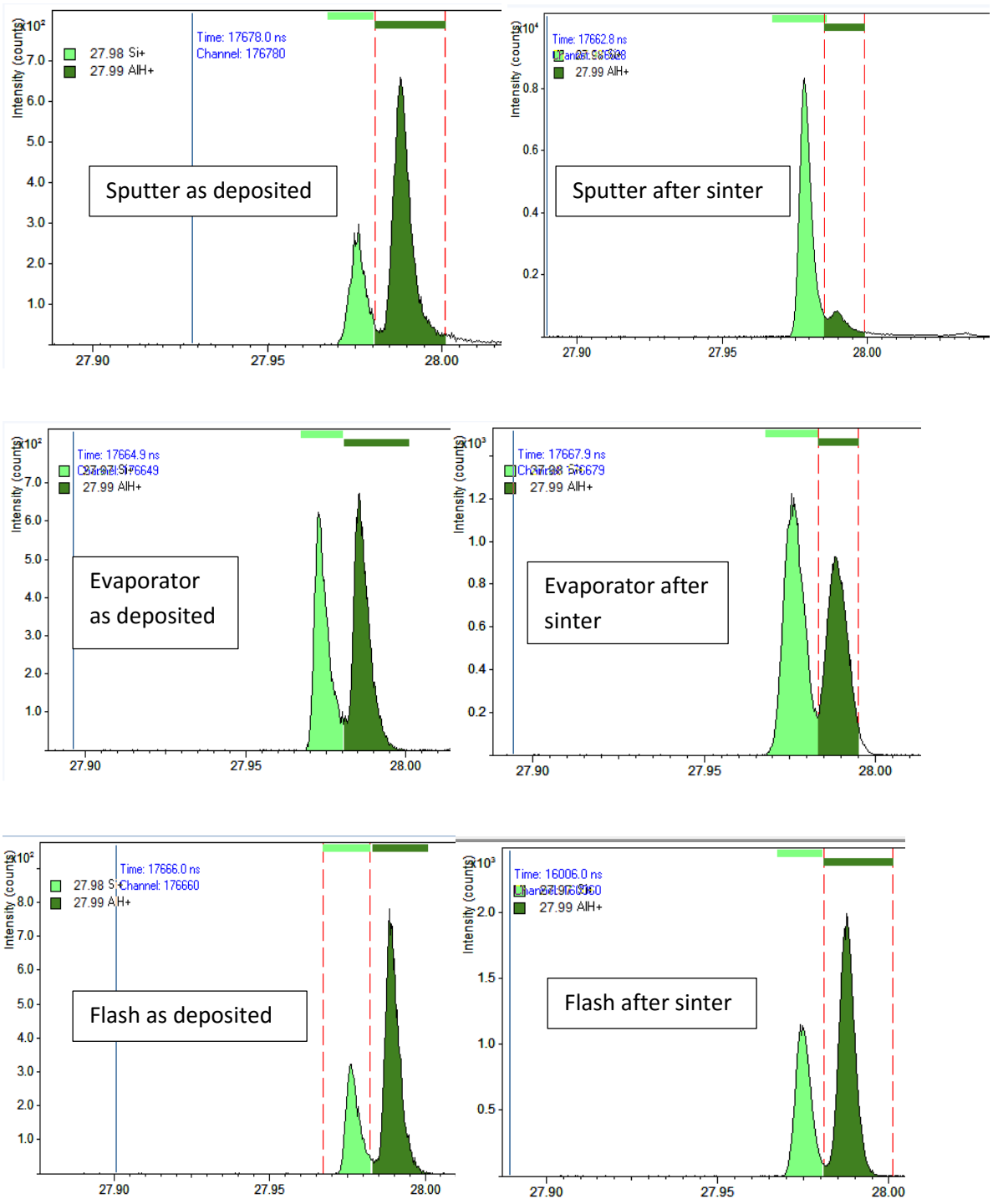


Figure 43: SIMS data for Al deposited using Sputter, Bell-jar and Flash evaporator

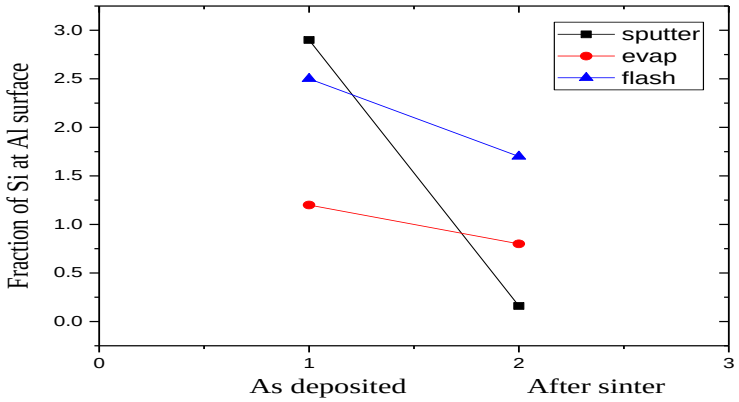


Figure 44: Fraction of silicon present in the film after deposition and after sinter

Figure 44 is plot of the peak ratios discussed above. All three films show a relatively stronger Si to Al signal. Flash evaporator film indicates that silicon concentration was the least of the three. This result, coupled with the abnormally high contact resistivity and poor performance of the solar cells, raised concerns regarding film composition. The purpose of 1% Si is to stabilize the Al/Si contact, prevent intermixing and avoid junction spiking. These results suggest that flash evaporated films may be react with the silicon wafer and subsequently damaging cell integrity. An investigation into vapor pressure data showed that at deposition pressure of 1×10^{-6} Torr the vapor pressure of Aluminum is reached at 800^0C, but silicon requires 1200^0C. This is a significant temperature range. Further testing on the flash tool would be needed to determine actual deposition temperature to confirm this hypothesis.

4.6 Run 5 with additional BSF

During Run 5, two p-type substrates with starting resistivity of 1-5 ohm-cm and two were used. All these wafers received BSF implant as the process parameters were mentioned in Table 6. The results from this run from p-type substrates are summarized in Table 15.

Table 15: Summary of results from Run 5

R5W1(Ti/Al)	Area(cm^2)	Jsc(mA/cm^2)	Voc(V)	FF(%)	Eff(%)	n1	n2	Contact resistivity
1R	0.5625	29.31	580.39	74.62	12.68	1.1	2.1	4.7×10^{-5} ohmcm^2
2b	2.25	28.52	580.45	73.33	12.14	1.2	2.2	4.7×10^{-5} ohmcm^2
3b	4	29.15	585.13	61.28	10.45	1.3	2.5	4.7×10^{-5} ohmcm^2
R5W3(Al evap)	**Area(cm^2)**	**Jsc(mA/cm^2)**	**Voc(V)**	**FF(%)**	**Eff(%)**	**n1**	**n2**	**Contact resistivity**
1R	0.5625	27.94	580.64	76.80	12.46	1.6	2.1	7.7×10^{-5} ohmcm^2
2b	2.25	28.26	585.42	76.3	12.64	1.4	2.4	7.7×10^{-5} ohmcm^2
3b	4	28.63	582.65	71.19	11.86.	1.5	2.3	7.7×10^{-5} ohmcm^2

Figure 45 shows I-V data comparison for Run 4 and Run 5 which are p-type substrates but different resistivities. In addition, Run 5 had BSF. A significant increase in V_{oc} of about 40mV was observed for Run 5 wafers although current densities remained almost the same.

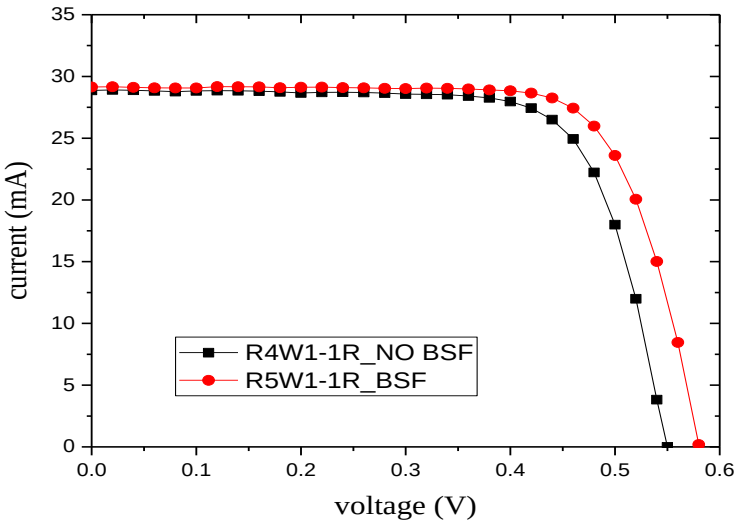


Figure 45: Comparison of I-V plot from Run 4 and Run 5 with and without BSF

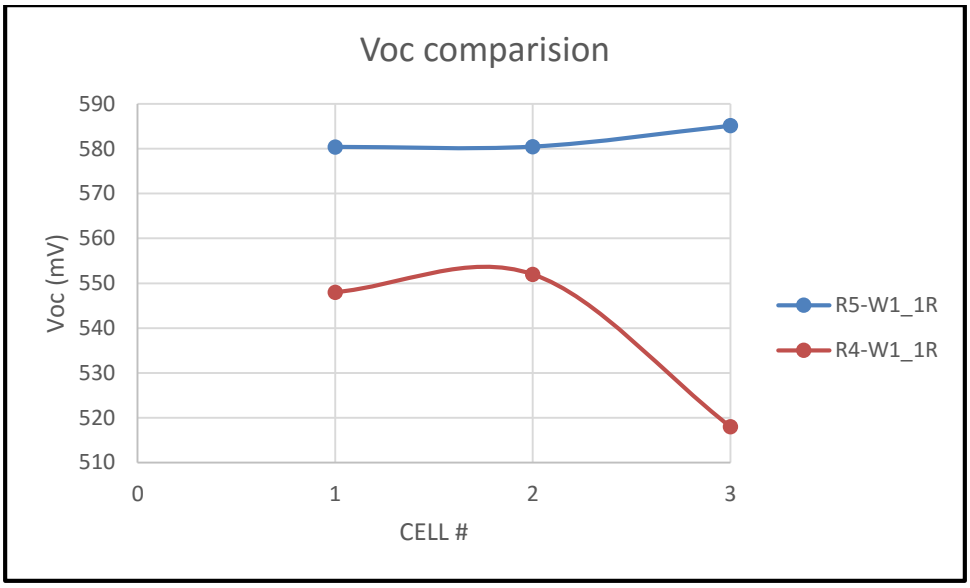


Figure 46: V_{oc}comparison of cells from Run 4 and Run 5 with and without BSF

Figure 46 shows comparison of cells on wafers from Run 4 and Run 5 and a clear trend of increase in V_{oc} was observed in the presence of BSF. The combination of new implant dose and energy, the Ti/Al contact, and the BSF yielded a cell efficiency of 12.7% from Run 5, which was best to date for the turnkey process.

CHAPTER 5: CONCLUSION

This project started with an initial goal to improve turn-key process designed to provide rapid evaluation of novel materials and processes for PV cells. Issues encountered during the processing altered the focus to characterizing process equipment. At the conclusion of this work, single crystal silicon solar cells were fabricated with an efficiency of 12.7%

During Run 1 Spin-On Dopants were used, along with TLC during ARC growth. A significant increase in efficiency from 7.5% to 9.7% was observed in the presence of chlorine. This suggests that the emitter islands may be connected due to surface inversion resulting from field oxide charges. In the presence of chlorine these changes may be neglected. Further runs with chlorine were not pursued due to supply issues with chlorine ambient.

Runs 2 and Run 3 results were precluded due to high contact resistances. ToF-SIMS analysis, along with TLM was performed. Changes in Al/Si ratio at the metal surface leads to a hypothesis that 1% Si may not be present in Al film deposited with flash evaporator, hence silicon from the substrate could be migrating to the metal film creating voids in silicon substrate, resulting in junction spiking and increased and contact resistance.

During Run 4 Ti/Al metal was used along with sputtered and evaporated Al. Implant dose was increased from $6 \times 10^{14}\text{cm}^{-2}$ to $2 \times 10^{15}\text{cm}^{-2}$ to increase surface dopant concentration. Efficiencies of the range 8.5-11.5% were obtained. A Ti/Al un-sintered contact was found to be best for contacting n-type emitter. During Run 5, Run 4 parameters along with BSF was used and modest efficiencies of range 10.5-12.7% were obtained.

CHAPTER 6: FUTURE WORK

Successful experiments were made to obtain solar cells with modest working efficiencies along with characterization of metal contacts. However, there is room for further improvements. Suggestions for process improvement are presented while bearing in mind the desire to keep process less complex.

6.1 Mask design

A new mask design is suggested for further characterization of solar cells. The current design has tight alignment tolerance in the TLM structures, and deposited metal was often off by about 3µm. Hence, increased tolerance would make the TLM structures better. TLM can be further investigated by optimizing the geometry of TLM structures while having multiple of them across the wafer. Also small diodes should be added to the mask to monitor output parameters in case cell results were not good. This would eliminate the need of repeating the fabrication process to investigate issues.

6.2 Anti-reflective coating

Silicon dioxide ARC was optimized for this process and experiments were done with oxide-nitride stack. Optimized oxide nitride stack as mentioned can have better light trapping properties as oxide layer passivates the surface and nitride layer minimizes the reflection losses. Experiments with stack of materials that have refractive index close to 2 should be done to further reduce the reflection from the surface.

6.3 Spin-On dopants

Spin-on dopants used during Run 1 were not optimized for the process flow but spin on dopants have potential to form emitters with high surface concentration. They have the capability to achieve doping, ARC and surface passivation in a single step with an optimized process [31]. Further experiments to study surface concentration along with contact resistivity can improve efficiencies. Repeatability and uniformity issues must be addressed.

6.4 Chlorine during drive-in

Results from Run 1 indicated promising results with TLC during drive-in as negative charge from chlorine may act to balance the positive charges in the oxide preventing surface inversion under field oxide. Chlorine was not used during other runs due to supply issues in the cleanroom. Hence presence of TLC during drive-in is suggested.

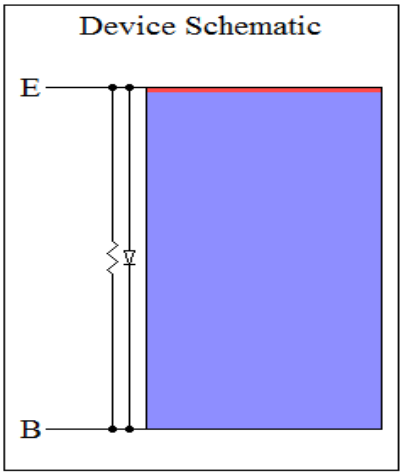
APPENDIX

PC1D input file

File Device Excitation Compute Graph View Options Help

DEVICE
Device area: 1×10^{0} cm^{2}
No surface texturing
No surface charge
Exterior Front Reflectance: 2×10^{1}%
Exterior Rear Reflectance: 6.6×10^{1}%
No internal optical reflectance
Emitter contact enabled
Base contact enabled
Internal conductor: 2×10^{-3} S
Internal diode: 1×10^{-5} A

REGION 1
Thickness: 5.25×10^{2} µm
Material from si.mat
Carrier mobilities from internal model
Dielectric constant: 1.19×10^{1}
Band gap: 1.124×10^{0} eV
Intrinsic conc. at 300 K: 1×10^{10} cm^{-3}
Refractive index from si.inr
Absorption coeff. from si300.abs
Free carrier absorption enabled
P-type background doping: 1.969×10^{15} cm^{-3}
1st front diff.: N-type, 1×10^{19} cm^{-3} peak
No 2nd front diffusion
No rear diffusion
Bulk recombination: $\tau_n = \tau_p = 1\times10^{12}$ µs
Front-surface recom.: S model, $S_n = S_p = 1\times10^{6}$ cm/s
Rear-surface recom.: S model, $S_n = S_p = 1\times10^{10}$ cm/s



REFERENCES

[1] Colin A. Wolden et al, “Photovoltaic Manufacturing: Present Status, Future Prospects and Research Needs”, Journal and Technology A: Vacuum, Surfaces and Films, Vol. 29, No. 3, 030801, 05.2011

[2] Dr. Kurinec “MCEE.620.01/02- Photovoltaic Science and Engineering, R.I.T, MicroE Program”, Spring 2015.

[3] Mikolasek Miroslav et al, “Current status and progress in the new generation’s silicon based solar cells” 2009, ISSN 1338-0087.

[4] Source of HDI data
https://en.wikipedia.org/wiki/List_of_countries_by_Human_Development_Index

[5] Ji Youn Lee “Rapid Thermal Processing of Silicon Solar Cells-Passivation and Diffusion”, J. Korean Phys. Soc. 44,1581

[6] https://commons.wikimedia.org/wiki/File:PVeff(rev140627).jpg

[7] Kim solesvik oppedal, “A study of the staebler-wronski effect and amorphous silicon solar cells” (2013). Thesis. Technische Universiteit Delft

[8] https://en.wikipedia.org/wiki/Solyndra

[9] Solid state technology, The Fraunhofer institute for Solar Energy Systems ISE “World record solar cell with 44.7% efficiency”

[10] Bohra, Mihir H., "Process Development for Single-Crystal Silicon Solar Cells" (2014). Thesis. Rochester Institute of Technology.

[11] SEIA- Solar market insight report Q2 2015

[12] http://cleantechnica.com/2013/10/29/multicrystalline-silicon-modules-dominate-solar-pv-industry-2014/

[13] Makoto Tanaka et al “Development of new a-Si/c-Si Heterojunction solar cells: ACJ-HIT (Artificially constructed Junction- Heterojunction with Intrinsic Thin-layer)”, Japanese Journal of Applied Physics, Volume 31, Issue 11R, pp. 3518 (1992)

[14] http://news.panasonic.com/press/news/official.data/data.dir/2014/04/en140410-4/en140410-4.html

[15] Solid state technology "Imec and Crystal solar demonstrate 22.5% nPERT Si solar cells on kerfless epitaxial wafers" 2016

[16] http://www.pv-magazine.com/news/details/beitrag/sunedison-begins-production-of-electronic-grade-polysilicon-using-fluidized-bed-reactor-technology_100016659/#axzz3TSIHgplE

[17] IHS Technology "Fluidized Bed Reactor Technology Stakes Its Claim in Solar Polysilicon Manufacturing", 7 May 2014

[18] International Technology Roadmap for Photovoltaics (ITPRV) sixth edition, results 2014.

[19] http://1366tech.com/

[20] http://pveducation.org/

[21] https://wiki.analog.com/university/courses/alm1k/alm-lab-pv

[22] N. Stavitski, M. van Dal, R. Wolters, A. Kovalgin, and J. Schmitz, "Specific contact resistance measurements of metal-semiconductor junctions," IEEE International Conference on Microelectronic Test Structures, pp. 13–17, March 2006.

[23] Filmtronics Semiconductor material, "Spin-On Diffusants" material

[24] Brown et al., "Ohmic contacts to Si-implanted and un-implanted n-type GaN", Mat. Res. Soc. Proc. Vol. 395, 1996 Material Research Society, pp. 855-860

[25] O. Nakatsuka, T. Takei, Y. Koide, M. Murakami, "Low resistance TiAl ohmic contacts with multi-layered structure for p-type 4H-SiC", Materials Transactions 43 1684 1688, 2002.

[26] http://web.stanford.edu/class/ee311/NOTES/Ohmic_Contacts.pdf

[27] Wright, P. J., W. M. Loh, and K. C. Saraswat, "Low-resistance sub micrometer contacts to silicon", Electron devices, IEEE Transactions, vol. 35, no. 8, pp. 1328-1333, 1988

[28] S. Bowden and A. Rohatgi “Rapid accurate determination of series resistance and fill factor losses in industrial silicon solar cells”, Georgia Institute of Technology, USA

[29] https://www.iontof.com/download/IONTOF_TOF-SIMS_5_Brochure.pdf

[30] Anthony G. O'Donnell, Iain M. Young, Steven P. Rushton, Mark D. Shirley & John W. Crawford “ Visualization, modelling and prediction in soil microbiology” , Nature Reviews Microbiology **5**, 689-699 (September 2007).

[31] Silicon PV devices based on a single step for doping, anti-reflection and surface passivation by Vikram K. Iyengar et al. *2010*