DESIGN, LAYOUT AND REALIZATION OF AN ALL NOR ENHANCEMENT TYPE PMOS SERIAL ADDER

By

Steven M. Macaluso
5th Year Microelectronics Student
Rochester Institute of Technology

ABSTRACT

A four bit serial adder was designed with PMOS NOR gates from a truth table that models binary serial addition. Three storage registers were also included in the design, two-four bit shift registers for the incoming digits and one-five bit register for the sum. A simple five gate latch was used for the bits of these registers. The circuit was layed out using ICE (Integrated Circuit Editor), a software program designed to facilitate circuit layout for mask making at R.I.T.

INTRODUCTION

Most computers can perform arithmetic operations. Addition is one such of these operations. Addition can be performed in parallel or serially. Independent of the technology chosen; PMOS, NMOS, BIPOLAR, etc., the truth table describing binary serial addition is shown below in Table 1. The numbers X and Y represent the two single bits that are to be added. The carry-in bit is Ci and the binary sum of X, Y and Ci is S. The carry-out bit that may result from this addition is Co.

X	Y	Ci	S	Co
1	1	1	1	1
1	1	0	0	1
1	0	1	0	1
1	0	0	1	0
0	1	1	0	1
0	1	0	1	0
0	0	1	1	0
0	0	0	0	0

Table 1. Truth table for a full adder.

A schematic of a circuit to perform binary, serial addition might look something like the one depicted in Figure 1. The rectangle labelled ADDER is a black box that performs tha actual addition. Realization of this adder will be discussed later. The X an Y regi-

sters are shift registers that feed their bits into the adder two bits at a time, one from the X register and one from the Y register. The S register is the sum register that stores the sum of the X and Y registers.

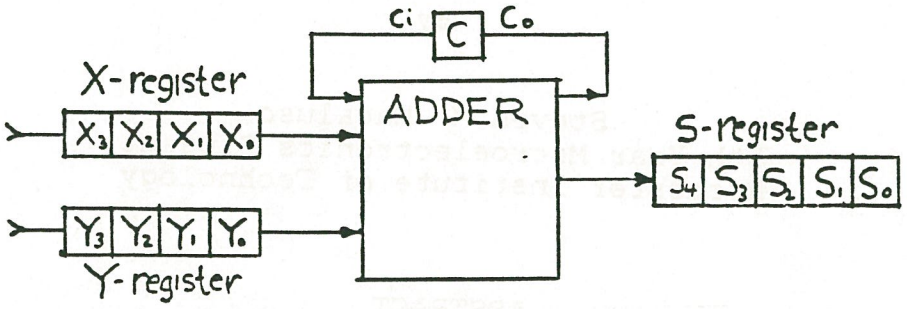

Figure 1. Architectural structure for a four bit serial adder.

The truth table in Table 1 can represented in equation form by using Boolean algebra. Equations 1 and 2 represent the sum and the carry-out functions respectively.

$$S = XYCi + X\bar{Y}\bar{C}i + \bar{X}Y\bar{C}i + \bar{X}\bar{Y}Ci. \quad (1)$$

$$Co = XYCi + XY\bar{C}i + X\bar{Y}Ci + \bar{X}YCi. \quad (2)$$

These equations are written in what is known as disjunctive normal form. To arrive at these equations pick the desired column to be reprsented and count the number of 1's in it. For every 1 in that column write down the products of the variables and then add them together. So for the S column which has four 1's in it XYCi is written four times and added: XYCi + XYCi + XYCi + XYCi. To complete th process a bar should be placed over those variables that have zero values in the rows which have 1's in the column of concern. So for the S column the result is as in Equation 1.

Simplification of these equations is necessary to reduce the number of gates needed to perform the desired logic function. Karnaugh maps (K-maps) and Boolean algebra are the tools generally used. Simplification of the sum and carry-out equations is briefly described below. [1]

$$S = XYCi + X\bar{Y}\bar{C}i + \bar{X}Y\bar{C}i + \bar{X}\bar{Y}Ci$$
$$\quad 111 \quad\quad 100 \quad\quad 010 \quad\quad 001$$
$$\quad m7 \quad\quad m4 \quad\quad m2 \quad\quad m1$$

Ci \ XY	00	01	11	10
0	0	2 1	6	4 1
1	1 1	3	7 1	5

As can be seen from the K-map above, there are no adjacent boxes but Boolean algebra can be used to rearrange Equation 1 to the form of Equation 3. This form is helpful because the last part of the equation is related to the denial of Equation 4, the representation of the carry function.

$$S = (X+Y+Ci)(XYCi+\overline{YCi+XCi+XY}). \quad (3)$$

$$Co = \underset{111}{XYCi} + \underset{110}{XY\overline{Ci}} + \underset{101}{X\overline{Y}Ci} + \underset{011}{\overline{X}YCi}$$
$$m7 \quad m6 \quad m5 \quad m3$$

Ci \ XY	00	01	11	10
0	0	2	6 1	4
1	1	3 1	7 1	5 1

Adjacent Boxes lead to simplification. Therefore,

$$Co = YCi+XCi+XY. \quad (4)$$

For more information about how to use and fill in K-maps see Reference 1.

Now that the equations for the sum and carry-out are simplified, they can be translated into their corresponding logic gates. To do this Boolean multiplication and addition are changed to the AND-ing and OR-ing functions respectively. Figure 2 shows the realization of the Equations 3 and 4, the add and carry-out functions using only NOR gates.

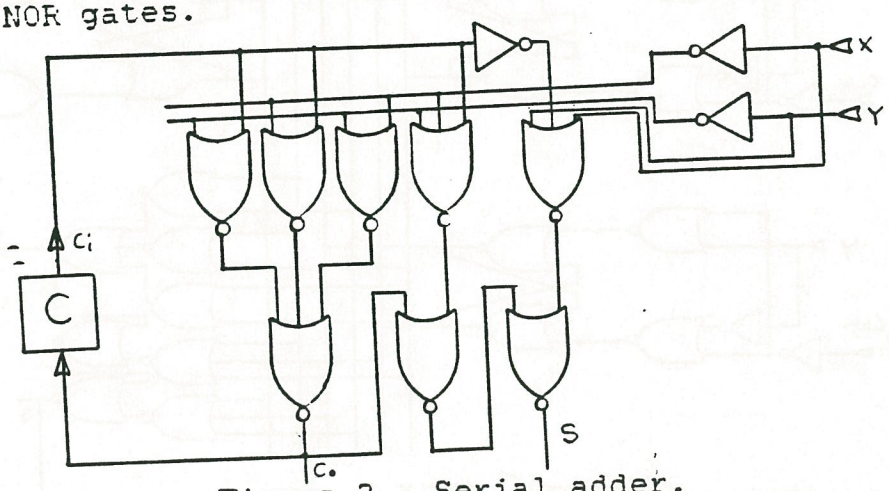

Figure 2. Serial adder.

Note that only NOR gates were used. The reason that this is so is due to something known as the "body effect." The body effect refers to the changes in the transistors characteristics when a bias voltage is applied between substrate (body) and source. When the source and substrate of a MOS device are at different potentials the depletion region between the channel and substrate widens and contains more charge; consequently, the gate electric field necessary to form a channel is increased. Thus the apparent threshold of the transistor is increased. If, as in MOS NAND gates, their are transistors in series this body effect can grossly alter the transistors operating point. For certain bias conditions it is possible that the serial transistors are both operating in the saturation region. This being the case the final output voltage will be Vgg less the threshold drops across each serial transistor, each of which is enhanced by th body effect phenomenon. It is possible that the output voltage will not be suffcient to

meet the specified minimum value.[4] So where ever there is an AND gate, a negated input NOR gate will replace it. Gates performing an OR function will be replaced by NOR gates followed by an inverter.

Now that the full adder has been designed, a unit storage cell must be chosen. An all NOR simple latch flip-flop was chosen. Figure 3 is an example of this type of flip-flop.

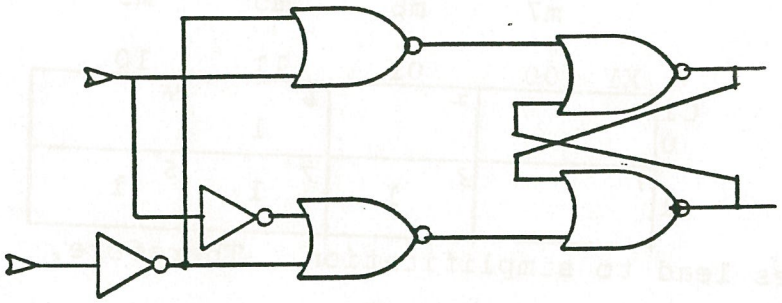

Figure 3. All NOR simple flip-flop.

Figure 4 shows the gate representation of Figure 1. The clock pulse timing lines have been included.

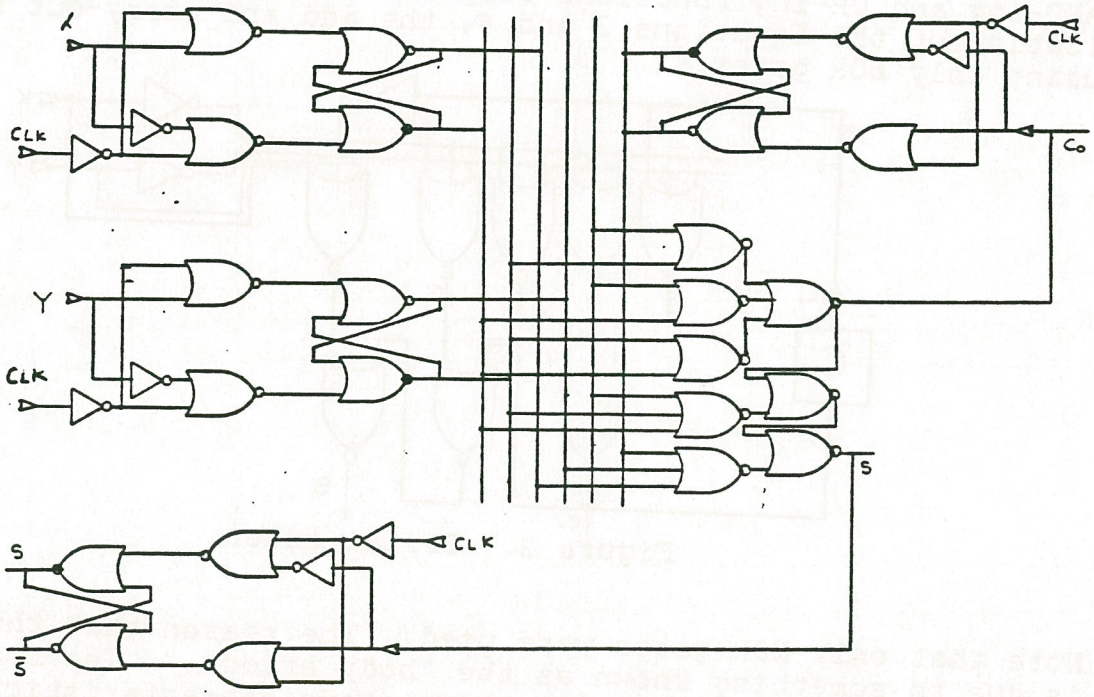

Figure 4. Full adder with storage cells for one-bit numbers.

The simplest of all gates is the inverter. With MOSFET inverters it turns out that load resistors are required with resistances of many tens of thousands of ohms, conventional diffused resistors fabricated in integrated circuits occupy large areas on the silicon chip which are roughly proportional to the resistance. That is why almost invariably that a MOSFET "load" is used instead of a diffused resistor. Figure 5 shows a basic MOSFET inverter.

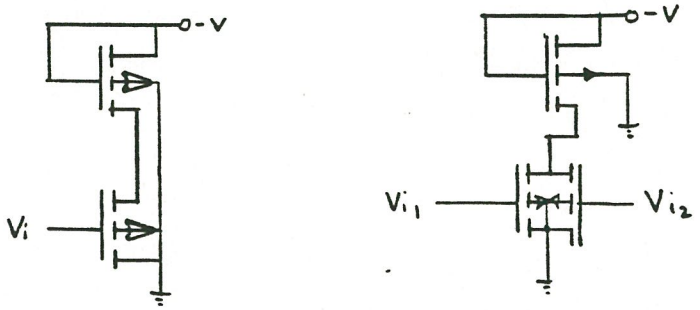

Figure 5. The basic PMOSFET inverter and nor gates.

One imporant parameter that has a profound effect on the characteristics of the inverter is the z-factor. The z-factor is defined as (W/L)d/(W/L)1 where (W/L)d and (W/L)1 are the width to length ratio of the channel in the driver and load respectively [2]. Figure 6 shows the input-output characteristics of figure 5 for various values of z.

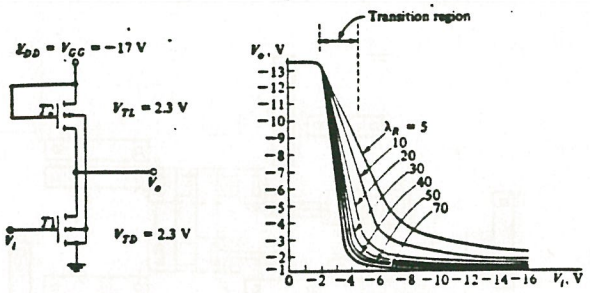

Figure 6. Various output-input curves for different values of z

Note that in order to effect reasonably sharp response of output to input it is necessary that z be large; i.e., relative to the driver the load channel should be narrow and long. In the case of R.I.T. the minimum PMOS line geometry that is used is 10 microns. So for (W/L)d/(W/L)1 the minimum geometry was used for the width of the driver and the length of the load. The length of the driver and the width of theload were chosen to be three times the minimum geomtry to give a maximum value of z and a use a minimum amount of area. Thus the z factor worked out to be (3/1)/(1/3)=9=z.

The above disscussion can be expanded to include PMOS NOR gates by putting a second driver in parallel with the first.

RESULTS

Once all the preliminary work was done the a partial circuit was layed out with ICE. The layout shown on the following page is the actual adder without the storage cells (shift registers.) The ICE files are now ready to be converted into Mann files which in turn will be used to make the necessary masks to process the adder, the final product. The ICE layout is shown in Figure 7.

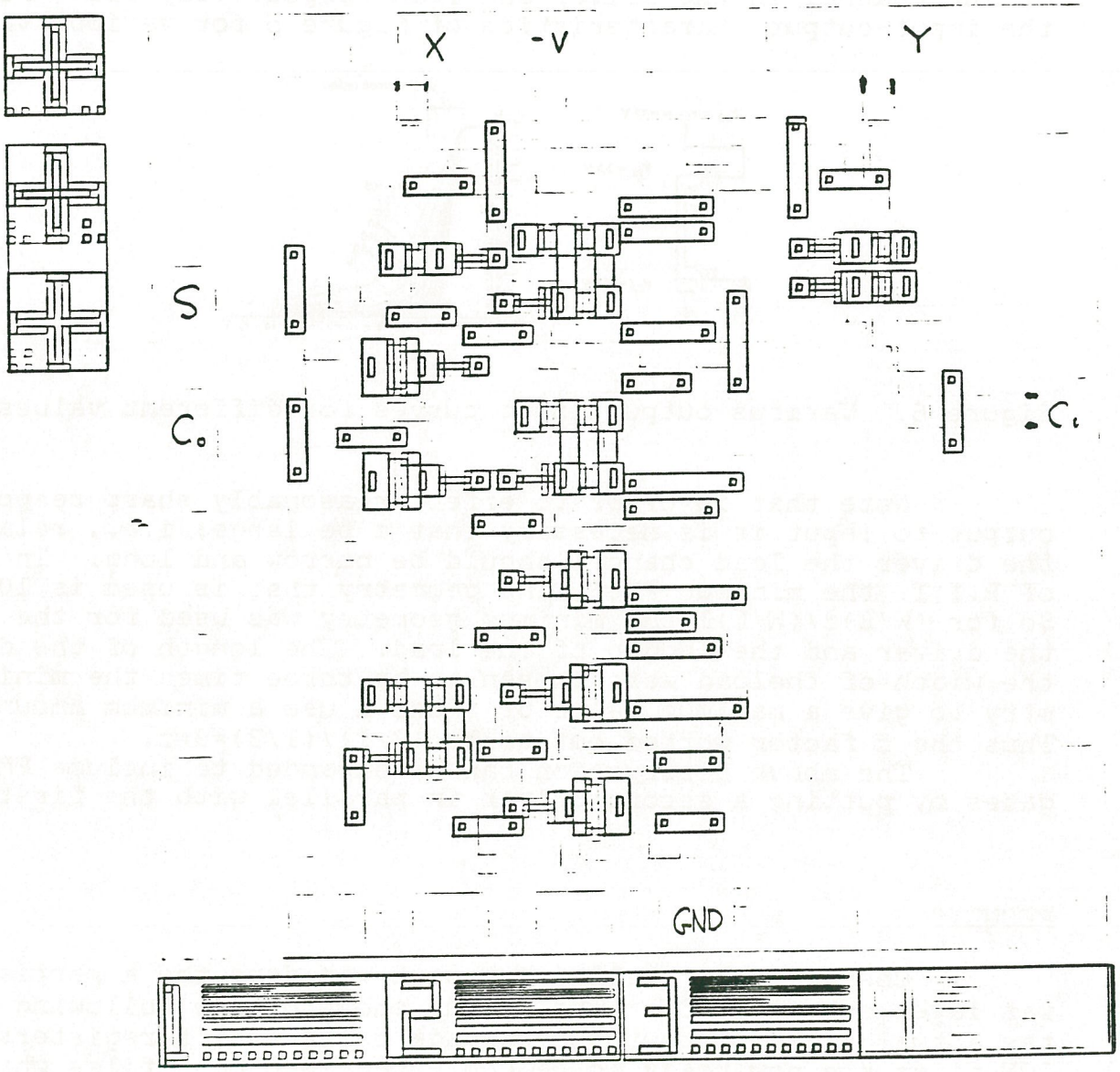

Figure 7. ICI layout of serial adder.

SUMMARY

The origional intent of this paper was to design, layout, fabricate and test a four bit serial PMOS adder. Due to time restraints only the first two steps were accomplished. Even so the necessary masks for the adder can be generated from the ice files. The project was done in such a way as to allow for incoming students create the masks for the adder without the storage cells and still be able to test the function of the adder using ordinary DC volatges.

ACKNOWLEDGEMENTS

Rob Pearson for his help with geomerties, Michael Jackson for his continual overall help.

REFERENCES

[1] Herbert, T. and Schilling, D. Digital Integrated Electronics, McGraw-Hill, N.Y., 1977, pp. 100-120.

[2] Pearson, R. "PMOS Digital Structures." 1986, pp. 77-92.

[3] Carr, W.N. and Mize, J.P. "MOS/LSI Design and Applications," McGraw-Hill; Chap.4, 1972

[4] Engineering staff of American Micro-systems, Inc. MOS Integrated Circuits, Van Nostrand Reinhold Co., 1972, pp. 90-93, 246-247.