

DESIGN AND FABRICATION OF A SIXTEEN BIT PMOS STATIC RAM

by

Douglas J. Lange

5th Year Microelectronic Student

Rochester Institute of Technology

DESIGN AND FABRICATION OF A SIXTEEN BIT PMOS STATIC RAM

by

Douglas J. Lange

5th Year Microelectronics Student

Rochester Institute of Technology

ABSTRACT

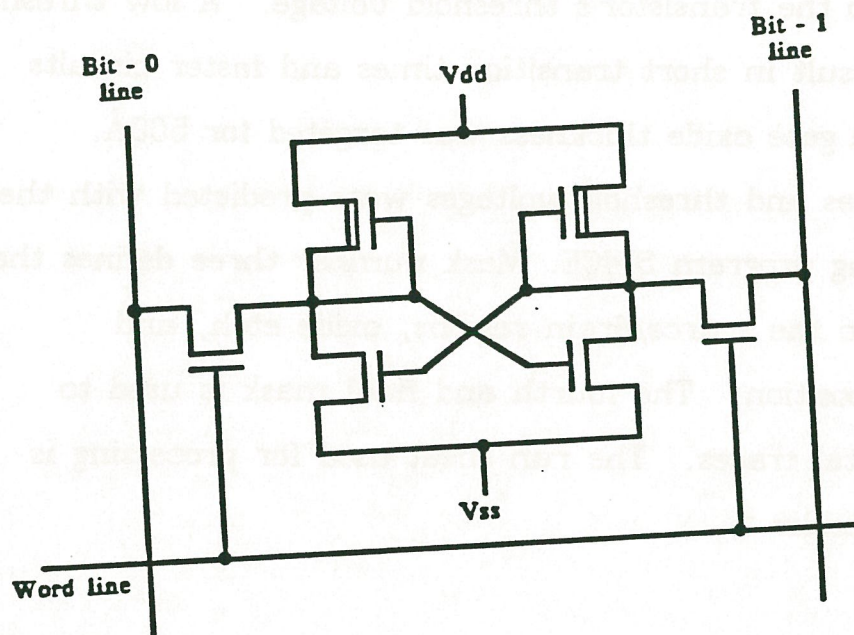
This project is focused on fabricating a self containing 16 bit PMOS static RAM using $10\mu\text{m}$ minimum geometries. The basic structure was designed previously but changes had to be made to the CIF files which contained the circuit layout. Diffusion runs were added to allow for connections between inputs /outputs and pads. Alignment marks were also added. MANN files were generated, from which reticles, and finally, the masks were made. The process used to fabricate the SRAM was modelled on SUPREM. SPICE was used to determine the threshold voltage and read/write time. The circuit was then fabricated and tested.

INTRODUCTION

One of the most important VLSI products is the memory chip. Memory circuits form an essential part of any digital system. Among memory chips, the random access memory (RAM) has the highest component density per chip. The more favorable characteristics of RAMs are storage capacity, cost per bit, physical size, power consumption, reliability, access time, and cycle time. Static memories have a higher cost per bit than dynamic memories, but are favored for small memory systems because they require a minimum of controls¹. An array of storage cells, each holding 1 bit of data, are used to store digital data in a semiconductor memory. The storage cells are

flip-flops, which consist of two cross-coupled inverters.

Figure 1. STATIC MOS RAM CELL¹



In a RAM device, information can be put into and taken out of a memory, and any of its address locations can be accessed in any desired sequence with similar access time to each location. This is known as *read/write* memory. A RAM consist of memory cells, an address decoder, a memory register, and a read-write control. Storage cells in a RAM can be fabricated with either bipolar or MOS devices. MOS technology uses fewer masking cycles with higher component density and will therefore be employed.

For a PMOS process the number of photolithographic masking cycles is four. The first mask is used to define the source/drain regions, and boron is diffused into lightly doped (100) n-type

silicon wafers (7-12ohm-cm). If the doping is too light problems may arise due to source-drain punch through. The second masking cycle is used to remove the field oxide from the channel, and a thin high density oxide layer is grown to serve as the dielectric isolating the gate. The thickness of the gate oxide is proportional to the transistor's threshold voltage. A low threshold voltage will result in short transition times and faster circuits. Therefore, the gate oxide thickness was targeted for 500Å. Transition times and threshold voltages were predicted with the device modeling program SPICE. Mask number three defines the contact cuts to the source/drain regions, oxide etch, and aluminum deposition. The fourth and final mask is used to define the metal traces. The run sheet used for processing is shown in Appendix 1.

EXPERIMENT

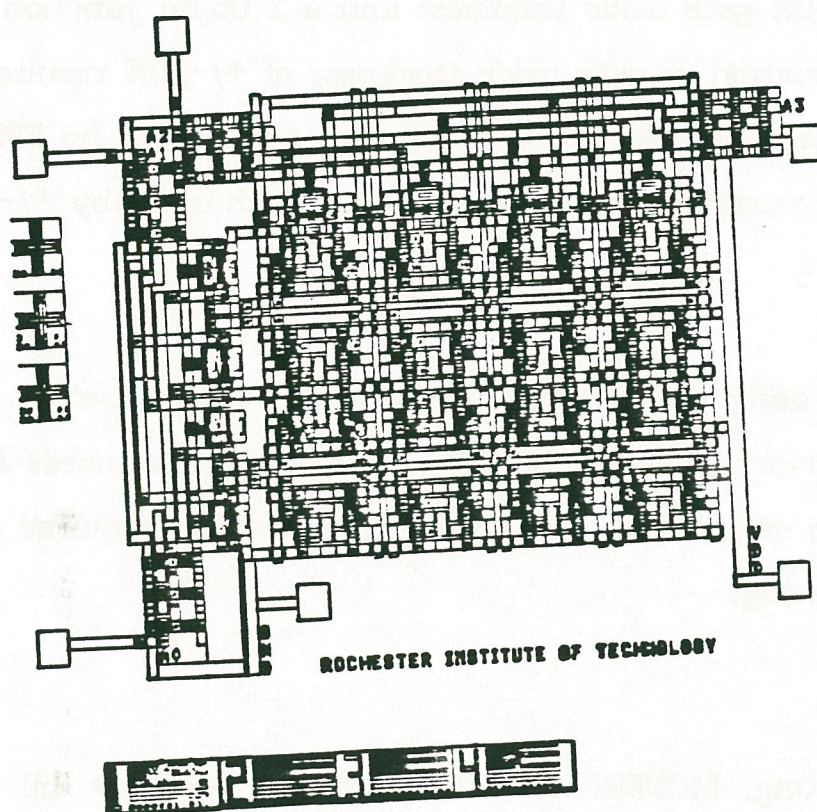
The basic computer layout of the sixteen bit static RAM design was started by John Schaller² using an RIT produced program called ICE (Integrated Circuit Editor). This was the starting point of this project. After examining the layout design for errors, alignment keys and input/output pad drivers are added to allow for testing on an automatic probe station, (see figure 2). The ICE file was then used to produce a MANN file which contains the information required to expose the reticles with the MANN pattern generator. The reticles were used to create the masks needed for fabrication.

The times and temperatures of the boron predeposit and drive-in steps were computed using a process simulation program called SUPREM, (see appendix 2). SUPREM simulates the

one-dimensional changes occurring in a device structure along a perpendicular to the surface of the silicon wafer. The information provided by the program consists of the various layers of materials in the structure, the distribution of impurities within those layers, and the sheet resistivity of the diffused regions. The fabrication process followed the modeling of the structure with SPICE and SUPREM.

RESULTS & DISCUSSION

Figure 2. STATIC RAM DESIGN LAYOUT



Some of the problems encountered stem from the lack of a second level metal process. Because of the original design, the only way to route the inputs and outputs to pads was to run diffusion lines under the metal that isolated them. Diffusion runners represent a high resistive path and the result is slower device

operation. The present design should be changed in that respect. The processing was not fully completed because of an error in the oxide mask. The alignment key was not visible because box defining an antiregion was covering it. An attempt was made to align the mask with unfavorable results. However, some useful processing information was obtained. Using the groove & stain technique the source and drain junction depths were found to be approximately $2.3\mu\text{m}$ after all the temperature steps. This was close to the predicted value of $2.05\mu\text{m}$ calculated by SUPREM. The oxide growths were also compared to SUPREM obtained values. SPICE was run under conditions of variability in processing, (see Appendix 3). The threshold voltage was 2.66 volts for a 500\AA gate oxide thickness and a $2.05\mu\text{m}$ junction depth. A variation in gate oxide thickness of $\pm 20\%$ results in a threshold voltage between 2.3v and 3.0v as predicted by SPICE. For the same variation, the transition time changed by $\pm 1\text{ns}$.

CONCLUSION

A SRAM was designed, the mask set created, and initial fabrication performed. Results show that the layout needs some changes. The oxide mask is faulty and a new one required for further processing.

REFERENCE

1. Dewitt G. Ong, MODERN MOS TECHNOLOGY, McGraw Hill
2. John W. Schaller, DESIGN AND ANALYSIS OF A SIXTEEN BIT PMOS STATIC RAM
3. ICE users manual
4. Saburo Muroga, VLSI SYSTEM DESIGN, Wiley & Sons, Inc.