DESIGN OF AN ADVANCED CMOS PROCESS TEST CHIP

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ABSTRACT

An advanced ten level five micron CMOS test chip was designed. Design rules were established and layout was completed with Integrated Circuit Editor.

INTRODUCTION

Complimentary Metal Gate Oxide Technology incorporates n-channel and p-channel field effect devices on the same wafer. CMOS devices consume less power, have better noise immunity, and higher packing densities than other integrated circuit technologies(2).

Presently, an advanced CMOS process is in development at RIT. This project consists of creating the preliminary design rules and designing the test masks for this CMOS process. The process uses 10 masking levels to fabricate five micron, self-aligned, poly-gate CMOS devices on N-type wafers and features bimetal interconnect.

The design was created with the aid of an Integrated Circuit Editor (ICE) software package presently available at RIT. This required the creation of a control program (CMOS.ICE) and alignment targets to allow for the 10 mask level 5um process.

The actual design includes discrete MOSFETs with variety of transistor length to width ratios. In each case, CMOS gates are designed with the length to width ratio of the PMOSFETs three times greater than that of the complementary NMOSFETs. This matches current drive capability as electrons are three times more mobile than holes.

The number of masks is reduced to ten by using self aligned gates. This practice also reduces device geometries and parasitics. PMOSFETs are built in an n-type well while NMOSFETs are built directly into a p-type substrate. Oxide and n-plus guard rings surround the PMOSFET, isolating it from devices and reducing the gain of the lateral NPN parasitic transistor. This reduces the potential for

latchup. Consequently, PMOSFETs are much larger than their complementary NMOSFETs.

A thick field oxide is grown in all non-active regions of the chip. A boron implant under the field oxide increases the threshold of parasitic devices which may form under metal or poly interconnects.

NMOS and PMOS threshold are matched at 1.5 volts. Supply voltages are +5 volts and ground. Parametric structures are also included to evaluate the bimetal processes.

The ten photomasks are used to:

1] define n-well regions
2] define field regions
3] protect n-well regions
4] define poly gates and interconnect
5] expose n+ regions
6] define contacts
7] define metal1 pattern
8] define vias
9] define metal2 pattern
10] clear bonding pads

DESIGN RULES

The 10 masks designed will be made with RIT's present silver halide mask technology. The silver grain size limits the minimum critical dimension to five microns. When chrome mask technology is developed at RIT, the minimum critical dimensions may be reduced.

The design also allows for a five micron alignment tolerance at all mask levels. This design rule was liberally made so students who are not experts with the exposure system can align the masks quickly and still fabricate working devices. Although this reduces packing density, the tradeoff was practical for a university environment. Alignment targets are defined by the first mask (define n-well regions). All subsequent mask levels are aligned to this first mask.

This design will be used to test a process which has not yet been run at RIT. Estimates of the final junction depths are

necessary to establish preliminary design rules. Targets for these parameters were based on Reference (1). Although all impurities are implanted, both vertical and lateral diffusion of impurities occur during subsequent high temperature processes (drive in, oxide growth, anneal). SUPREM was then used to predict final junction depths. It was assumed that the final vertical junction depth is equal to the final lateral junction depth.

RESULTS/DISCUSSION

Table 1 summarizes the junction depths calculated by SUPREM

Table 1: SUPREM junction depths

	Junction depth
N-well	8.00 um
N+ source/drain and guard ring	1.12 um
P+ source/drain	0.88 um

The gate length is patterned at 5 microns, the minimum critical dimension. The source/drain diffusions encroach approximately 1 micron in from each side of the gate, so the effective length of each gate is approximately 3 microns.

Three different gate widths for the NMOSETs are designed. The gate lengths are 10, 15, and 50 um. The PMOSFET gate widths are each three time their NMOSFET counterparts. The gate lengths are 30, 75, and 150 um. Comparisons between gate widths should be made after fabrication.

Contact length is also designed at the minimum critical dimension, 5 microns. Contacts are surrounded by 5 um of metal on each side to allow for alignment tolerance. The width of each contact is maximized for individual devices. This practice reduces contact resistance but does not increase device size.

The inner field oxide ring and the n-plus guard ring surrounding the PMOSFETs are both 10 micron wide. This is a preliminary design rule which should be enough to prevent latchup and should be investigated upon fabrication.

Table 2 : Design Rule Summary

minimum critical dimension	5 um
alignment tolerance	5 um
patterned gate length	5 um
effective NMOSFET gate length	2.76 um
effective PMOSFET gate length	3.24 um
minimum contact size	5 um × 5 um
minimum via size	10 um × 10 um
minimum poly width	5 um
minimum metal 1 width	10 um
minimum metal 2 width	10 um

CONCLUSIONS

An advanced CMOS process design rule set and test chip have been designed. The ICE process file is called CMOS.ICE. The final 10 mask design file is called CMOSCHIP.CIF. These files, along with the alignment targets, parametric structures, and individual devices have been submitted to Mike Jackson.

ACKNOWLEDGEMENTS

John Hock designed the process and drew the cross-sections. Many thanks to Mike Jackson and Lynn Fuller for all their time and constructive input throughout this project.

REFERENCES

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(2) Chen, John Y., CMOS - The Emerging VLSI Technology, IEEE Circuits and Device Magazine, 1986

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Structures on the test chip include:

1] 5um alignment targets for all mask levels

2] metal1 - poly contact chain array :
85 (10um x 10um) connected by 30um metal 1
and poly segments.
* pads 11 - 12 [resistance]

3] metal2 - metal1 via chain array :
85 (10um x 10um) connected by 30um metal 2
and metal1 segments.
* pads 10 - 11 [resistance]

4] discrete NMOSFET : w/l = 10/5um (2:1)
* pad 1 [drain]
* pad 2 [gate]
* pad 3 [source]

5] discrete NMOSFET : w/l = 25/5um (5:1)
* pad 4 [drain]
* pad 5 [gate]
* pad 6 [source]

6] discrete NMOSFET : w/l = 50/5um (10:1)
* pad 7 [drain]
* pad 8 [gate]
* pad 9 [source]

7] discrete PMOSFET : w/l = 30/5um (6:1)
* pad 13 [drain]
* pad 14 [gate]
* pad 15 [source]

8] discrete PMOSFET : w/l = 75/5um (15:1)
* pad 16 [drain]
* pad 17 [gate]
* pad 18 [source]

9] discrete PMOSFET : w/l = 150/5um (30:1)
* pad 19 [drain]
* pad 20 [gate]
* pad 21 [source]

10] CMOS inverter gate : NMOSFET (2:1) PMOSFET (6:1)
* pad 25 [output]
* pad 26 [input]
* pad 27 [ground]
* pad 28 [+5 volts]

11] CMOS inverter gate : NMOSFET (5:1) PMOSFET (15:1)
* pad 29 [output]
* pad 30 [input]
* pad 31 [ground]
* pad 32 [+5 volts]

12] CMOS inverter gate : NMOSFET (10:1) PMOSFET (30:1)
* pad 33 [output]
* pad 34 [input]
* pad 35 [ground]
* pad 36 [+5 volts]

13] CMOS inverter ring oscillator :
15 inverters; NMOSFETs (5:1) PMOSFETs (15:1)
* pad 46 [+5 volts]
* pad 47 [ground]
* pad 48 [output]