DESIGN AND MODELING OF AN ADVANCED CMOS PROCESS

By

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ABSTRACT

An advanced ten level five micron CMOS process was designed. The process was modelled using SUPREM II software to calculate doping profiles, junction depths, and threshold voltages.

INTRODUCTION

Some of advantages of CMOS over other integrated circuit technologies include lower power consumption, better noise immunity, and higher packing density(1). A ten level polysilicon self aligned gate CMOS process using an n-well was designed. Self aligned gates reduce the cost of processing and increase device performance by reducing the number of masking steps and allowing smaller transistor geometries while reducing parasitics. The use of an n-well allows for optimization of the NMOS performance(2) since the NMOS device is built directly in the uniformly doped substrate. As a result, the CMOS devices will be compatible with current NMOS technology. Similarly, the threshold voltage of the PMOS device can be tailored to specification by selecting the doping for the n-well.

For a process using silver halide masks, it is possible to produce a ten level five micron advanced poly-gate CMOS process. The advantages of developing such a process include the ability to build more complex circuits, and perhaps fabricate circuits currently being built in industry. The use of silver halide masks instead of chrome limits the minimum critical dimension to five microns due to the silver grain size, but is much more economical and practical for a university environment.

To layout the general process, a series of cross-sectional drawings of the device must be made. Figure 1 is an illustration of the final device cross-section (see Appendix 1 for detailed description).

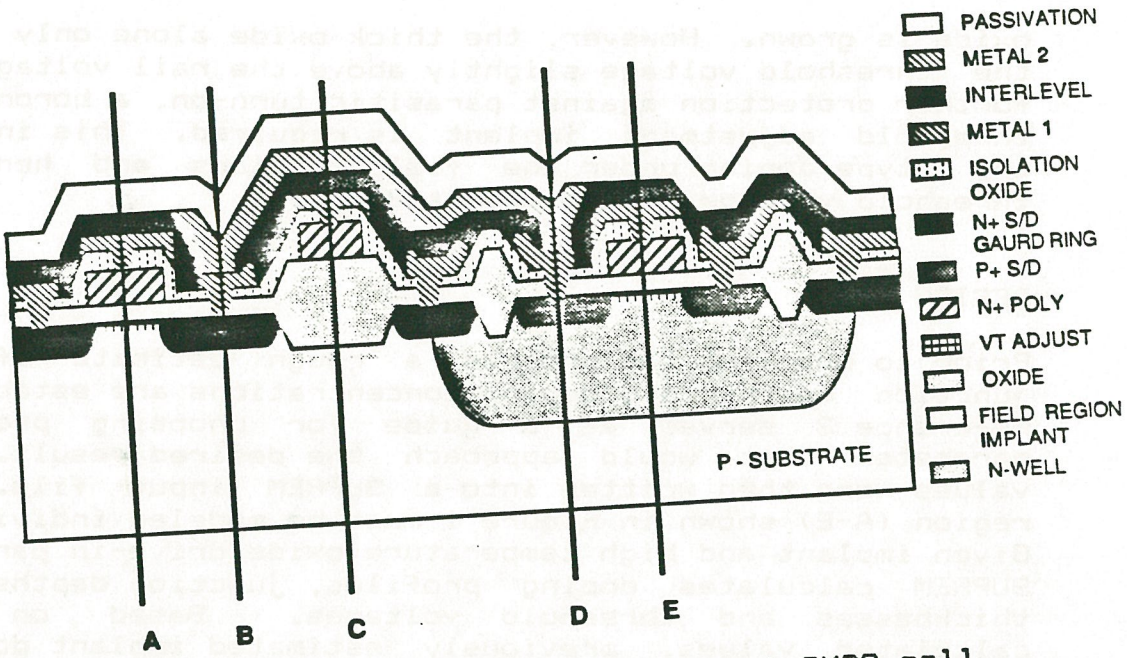

FIGURE 1: Cross-section of typical CMOS cell

Letters (A-E) indicate cross-sectional profiles analyzed using SUPREM software.

The basic requirements of the process were 1) matched NMOS and PMOS threshold voltages, 2) heavily doped, shallow junction source-drains, and 3) high threshold voltage in the field region.

To obtain minimum power consumption and maximum noise immunity threshold voltages of the P and N channel FET must be matched. The first step towards matching the threshold voltages is insuring the n-well is lightly doped. A low phosphorous dose and long drive-in is required. However, the junction depth should not exceed eight microns since the lateral diffusion will affect packing density. For fine tuning, a boron threshold adjust implant is included. Adding p-type impurities to both N and P channels raises both threshold voltages, thus allowing their magnitudes to converge.

Due to the nature of the self-aligned process, the N+ source-drain receives both a P+ and N+ implant. As a result, it becomes difficult to obtain the necessary heavily doped source-drains. A balance must be obtained such that the P+ implant is heavy enough to make a good source-drain, but not so heavy that it cannot be counter doped by the N+ implant. The high temperature anneal and drive-in are done at the same time to maintain the shallow junction depths.

To prevent the possibility of forming a parasitic channel under a metal or poly run in the field region, a thick field

oxide is grown. However, the thick oxide alone only raises the threshold voltage slightly above the rail voltage. For further protection against parasitic turn-on, a boron field threshold adjustment implant is required. This increases the p-type doping under the field regions and hence the threshold voltage of the unwanted device.

DESIGN

Prior to modeling the process a rough estimate of final junction depths, and doping concentrations are established. Reference 3 served as a guide for choosing processing parameter that would approach the desired result. These values were then written into a SUPREM input file. Each region (A-E) shown in Figure 1 must be modeled individually. Given implant and high temperature oxide/drive-in parameters SUPREM calculates doping profiles, junction depths, oxide thicknesses and threshold voltages. Based on these calculated values, previously estimated implant doses and voltages, and oxide/drive-in/anneal times and temperatures are adjusted. The above process is repeated until threshold voltages are matched at approximately 1.5 volts, source-drain surface concentrations approximately 1E19 atoms/cm3 with a junction depth of about 1 micron, and threshold voltages in the field region of approximately 30 volts. The flowchart in Figure 2 illustrates this iterative process.

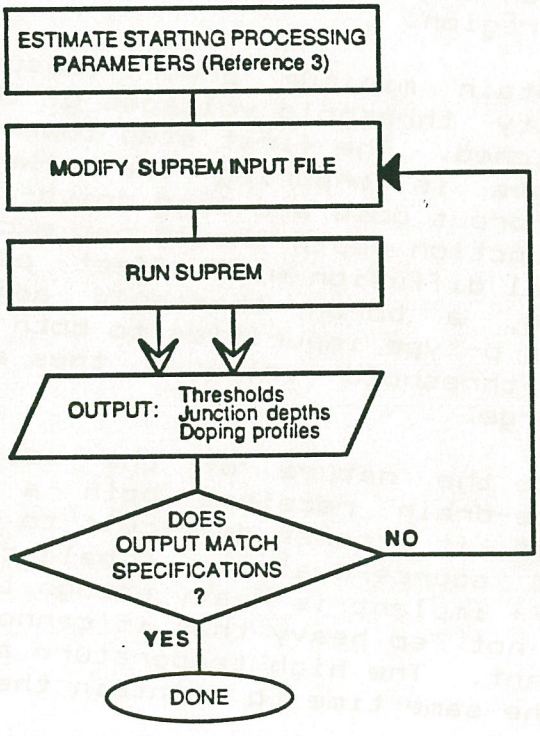

FIGURE 2: Flowchart illustrating modelling process

RESULTS/DISCUSSION

Table 1 summarizes the actual device specifications as calculated by SUPREM (see Appendix 2 for the detailed simulations).

REGION (FROM FIG. 1)	SURFACE CONCENTRATION (ATOMS/CM^3)	TYPE	JUNCTION DEPTH (MICRON)	THRESHOLD VOLTAGE (VOLTS)
N+ S/D (B)	9.30E18	N	1.12	--
P+ S/D (D)	7.30E18	P	.88	--
FIELD (C)	3.67E16	P	--	33.22
NMOS GATE (A)	2.79E16	P	--	1.48
PMOS GATE (E)	1.39E15	N	--	-1.46
N-WELL	1.39E15	N	8.00	--

+ GATE OXIDE = 800A
+ FIELD OXIDE = 12000A

TABLE 1: Summary of device specifications

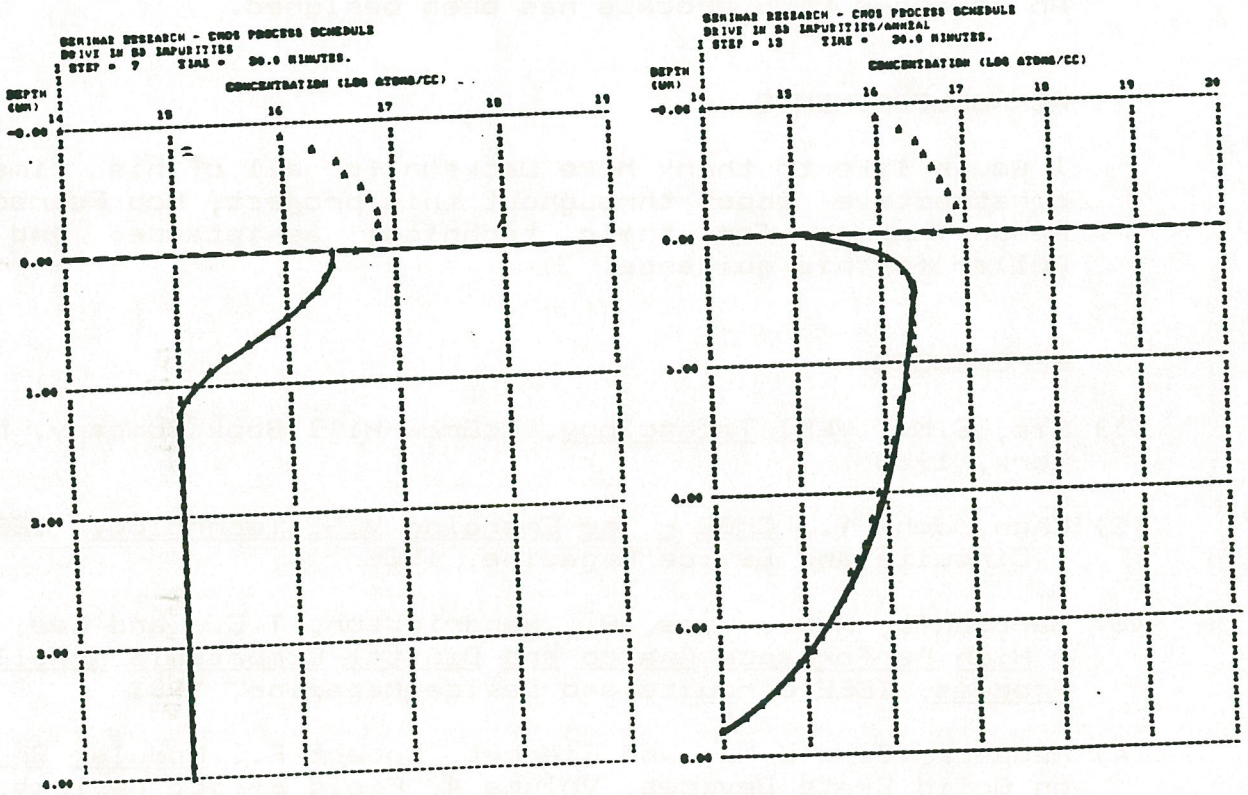

FIGURE 3: SUPREM doping profile plots

Left - NMOS device (p-type material under gate)
Right - PMOS device (n-type material under gate)

Gate oxide thickness and the doping profile under the gate are the critical parameters in determining threshold voltage. Figure 3 shows the doping profile under the gate of both devices as calculated by SUPREM.

Before this process can be used in the RIT's new factory environment, it must be written in a production format. The resulting process sheets contain step-by-step instructions to be followed by the processing operators (see Appendix 3). Unfortunately, since information on the operation of the implanter an CVD system are not yet available, the process sheets only include the raw information (i.e. dose and energy for implants, and film thicknesses for CVD).

Prior to processing, one should be aware that many of the SUPREM calculations used to model this process are based on internal default values that may not equal the actual values obtained in lab. These include impurity diffusivities, oxide growth rate, implant impurity distributions, and segregation coefficients. As a result, implant doses and energies may need to be altered to obtain the precise doping profiles specified in this process.

CONCLUSIONS

An advanced CMOS process has been designed.

ACKNOWLEDGEMENTS

I would like to thank Mike Jackson for all of his time and constructive input throughout this project, Rob Pearson and Renan Turkman for their technical assistance, and Lynn Fuller for his guidance.

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