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Development of Nanowire Structures on 2D and 3D Substrates for Pool Boiling Heat Transfer Enhancement

By

Zhonghua Yao

A DISSERTATION

Submitted in partial fulfillment of the requirements
For the degree of Doctor of Philosophy
in
Microsystems Engineering
at the
Rochester Institute of Technology
April 2013

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Development of Nanowire Structures on 2D and 3D Substrates for Pool Boiling Heat Transfer Enhancement

By

Zhonghua Yao

Submitted by Zhonghua Yao in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microsystems Engineering and accepted on behalf of the Rochester Institute of Technology by the dissertation committee.

We, the undersigned members of the Faculty of the Rochester Institute of Technology, certify that we have advised and/or supervised the candidate on the work described in this dissertation. We further certify that we have reviewed the dissertation manuscript and approve it in partial fulfillment of the requirements of the degree of Doctor of Philosophy in Microsystems Engineering.

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Dr. Sean Rommel ________________________________

Dr. Yen-wen Lu ________________________________

MICROSYSTEMS ENGINEERING PROGRAM

ROCHESTER INSTITUTE OF TECHNOLOGY

April 2013

ABSTRACT

Kate Gleason College of Engineering
Rochester Institute of Technology

Degree Doctor of Philosophy **Program** Microsystems Engineering

Name of Candidate Zhonghua Yao

Title Development of Nanowire Structures on 2D and 3D Substrates for Pool Boiling Heat Transfer Enhancement

Boiling is a common mechanism for liquid-vapor phase transition and is widely exploited in power generation, refrigeration and many other systems. The efficacy of boiling heat transfer is characterized by two parameters: (a) heat transfer coefficient (HTC) or the thermal conductance; (b) the critical heat flux (CHF). Increasing the CHF and the HTC has significant impacts on system-level energy efficiency, safety and cost. As the surface modification at nano-scale has proven to be an effective approach to improve pool boiling heat transfer, the enhancement due to combination of nanomaterials with micro-scale structures on boiling heat transfer is an area of current interest. In this study, metallic- and semiconductor- material based nanowire structures were fabricated and studied for boiling enhancement. A new technique is developed to directly grow Cu nanowire (CuNW) on Si substrate with electro-chemical deposition, and to produce height-controlled hydrophilic nanowired surfaces. Using a two-step electroless etching process, silicon nanowire (SiNW) have been selectively fabricated on top, bottom, and sidewall surfaces of silicon microchannels. An array of the SiNW coated microchannels functioned as a heat sink and was investigated for its pool boiling performance with water. This microchannel heat sink yielded superior boiling performance compared to a sample substrate with only microchannels and a plain substrate with nanowires. The enhancement was associated with the area covered by SiNWs. The sidewalls with SiNWs greatly affected bubble dynamics, resulting in a significant performance enhancement. The maximum heat flux of the microchannel with SiNW on all surfaces was improved by 150% over the microchannel-only heat sink and by more than 400% over a plain silicon substrate. These results provide a viable solution to meet the demands for dissipating a

high heat transfer rate in a compact space, with additional insight gained into the boiling mechanism for the microchannel heat sinks with nanostructures.

Abstract Approval: Committee Chair ____________________________________

Program Director ____________________________________

Dean KGCOE ____________________________________

ACKNOWLEDGEMENT

First and foremost I want to thank my advisor Dr. Satish G. Kandlikar. It has been an honor to be his Ph.D. student. I appreciate all his contributions of time, ideas and funding to make my Ph.D. experience productive and stimulating. Dr. Kandlikar has gained a distinction in the field of thermal analysis and the enthusiasm he has for his research is contagious and motivational for me. He is an excellent example as a successful teacher and professor.

I would also want to thank Dr. Yen-wen Lu, who leads me to the field of MEMS. He has taught me, both consciously and unconsciously, how good research is done. I conducted several projects under his guidance, and I very much appreciated his enthusiasm, patience and knowledge on the experimental research.

The members of the Thermal Analysis, Microfludics and Fuel Cell Lab have contributed immensely to my personal and professional time at RIT. The group has been a source of friendships as well as good advice and collaboration. I am especially grateful for the lab member Dwight Cook who helped me build the boiling test fixture and debug the data acquisition system. I really appreciated his work on obtaining the thermal contact resistance of the testing fixture and amazing machine shop ability to craft various parts for the experimental setup. I would like to acknowledge other lab members Jeet Mehta, who shared his knowledge in Solidworks with me and Mike Daino, who trained me on the Confocal Laser microscopy. Other past and present group members that I have had the pleasure to work with are graduate students Ankit Kalani, Matthew Garofalo, Preethi

Gopalan, Mustafa Koz, and Rupak Banerjee, postdocs Guangsheng Zhang, Ting-Yu Lin and Zijie Lu, and numerous summer and co-op students who have worked in the lab.

In regards to the NW fabrication and Imaging, I thank Sean O'Brien and Thomas Grimsley for the clean room equipment training and certification. I would also like to thank Dr. Preble, Dr. Rommel and Brain Mcintyre, for training me on the FESEM-FIB and EDX X-ray Spectrometer at RIT and University of Rochester.

The studies on NW fabrication on orthogonal surfaces of microchannel would not have been possible without the Si chips from the group of Dr. Yen-Wen Lu at the National Taiwan University. I have appreciated their collaboration and the impressive fabrication skills of P.C. Kao who help made the Si microchannels for SiNW synthesis.

For this dissertation I would like to thank my committee members: Sean Rommel, Karl Hirschman and Jiandi Wan for their time, insightful questions and helpful comments.

I gratefully acknowledge the funding sources that made my Ph.D. work possible. I was funded by the National Science Foundation (EPDT Grant # 0802100) and the Microsystem Engineering Department at RIT. The project is also supported by Taiwan National Science Council (NSC98-2218-E002-023-MY3).

Lastly, I would like to thank my family for all their love and encouragement. I am ever grateful to my parents who supported me in all my pursuits. And most of all for my loving, supportive and patient wife Dan Zhang, who encouraged me and supported me during my Ph.D. life at RIT, I can not image how my life would be without you.

Zhonghua Yao

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Nomenclature

<u>English</u>

A	Heater area
a_i	Measured parameter for uncertainty analysis
B	A constant used in Nusselt number in the convection model
C_b	A constant used in Rohsenow's model
C_k	A constant used in Kutateladze model, for flat surface, C_k=0.131
C_p	Specific heat
C_{pl}	Specific heat of liquid
C_{sf}	A constant used in Rohsenow's model
D_d	Critical bubble diameter
f	Bubble departure frequency
g	Gravitational acceleration
h	Thermal conductance
H	Depth of the microchannel
K	Empirical constant in the hydrodynamic theory of the CHF model
k	Thermal conductivity
k_l	Liquid thermal conductivity
k_{Cu}	Thermal conductivity of copper
k_{Si}	Thermal conductivity of silicon
L	Length of single microchannel on the chip
L_1	Width of microchannel arrays on the chip
L_b	Bubble length scale used in Rohsenow's model

L_{Cu}	Thickness of copper layer
L_{Si}	Thickness of silicon substrate
N_a	Bubble nucleation site density
P_l	Liquid pressure
P_v	Vapor pressure
P_{rl}	Prandtl number of liquid
q''	Heat flux
r	Constant used in Rohsenow's model, for water, $r = 0.33$
$R_{t,c}$	Contact resistance between heater and testing chip
R_{eb}	Reynold's number of a vapor bubble
R_{ev}	Reynold's number of vapor flow
s	Constant used in Rohsenow's model, for water, $s = 1$
T	Temperature
$T_1 \sim T_3$	Temperature measured at thermocouple 1~3
T_s	Boiling surface temperature
T_{sat}	Boiling liquid saturation temperature
T_w	Wall superheat
U	Uncertainty
U_b	Bubble velocity used in Rohsenow's model
V	Voltage
W_f	Width of microchannel fin
W_{ch}	Width of microchannel

Greek

α	Thermal diffusivity
δ	Film thickness
θ	Contact angle
μ	Dynamic viscosity
μ_l	Dynamic viscosity of liquid
μ_v	Dynamic viscosity of vapor
ρ	Density
ρ_l	Liquid density
ρ_v	Vapor density
σ	Surface tension

Subscripts

l	Liquid
v	Vapor or gas
sat	Saturation condition
w	Wall

CHAPTER 1

INTRODUCTION

From nuclear reactors with 1000 Mega-Watt (MW) output to 5 Milli-Watt (mW) single microchip, phase change heat transfer is the dominant component of thermal transport at all length scales. It is reported that the thermal energy generated by phase change heat transfer plays a primary role in the world's total energy: More than 90% of world's total power is produced by heat engines [1]. Boiling, a process of convection heat transfer with phase change, is considered as one of the most efficient heat dissipation methods and is utilized in various energy conversion and heat exchange systems and in cooling of high energy density electronic components. Enhancing boiling heat transfer would improve the efficiency of thermal energy transport and conversion; thereby increases the overall energy efficiency. Numerous efforts have been dedicated in the boiling enhancement research over the last several decades [2]. In many cases, the targets of utilizing enhancement techniques of boiling heat transfer are to minimize the surface temperature of heated objects at given heat loads, and to maximize the dissipation of heat energy at given operating temperature.

The need for advanced thermal management systems based on boiling heat transfer is driven by the fast development of very-large-scale integration (VLSI) industry and the associated increase in chip power density. High performance equipment can generate heat flux up to several hundred or even a thousand W/cm^2 levels, while for most integrated circuit and logic chips, a relatively constant component temperature below

85 ℃ has to been maintained. Nevertheless, due to the complexity of today's chip designs, there are local hot-spots which might have local heat flux of 300 W/cm^2 [3] formed on a chip. This requires more advanced cooling solutions in order to keep the chip and its local hot spots cool, and these challenges will be exacerbated by 3D integration, which seems imminent. The commonly used air cooling's ability to address temperature concerns is limited by low heat transfer coefficient (HTC), and boiling therefore provides a valuable alternative, as can be seen in Table 1.1[4] , as follows.

Table 1.1: Standard heat transfer coefficient ranges for convective heat transfer method [4]

Cooling method	**Heat transfer coefficient (W/m^{2}K)**
Natural convection with gas	2-25
Forced convection with gas	25-250
Natural convection with liquid	50-1000
Forced convection with liquid	100-20,000
Boiling (convection with phase change)	2500-100,000

1.1 Boiling mechanism

Boiling is a phase change process in which vapor bubbles are formed either on a heated surface and/or in a superheated liquid layer adjacent to the heated surface. It can be further classified into pool boiling and forced flow boiling. Pool boiling refers to boiling under natural convection conditions, whereas in forced flow boiling, liquid flow

over the heater surface is imposed by external forces. The noticeably high HTC observed in the boiling process is due to the addition of the latent heat of vaporization associated with the phase change from liquid to vapor. The heat transfer during the boiling process is highly advantageous in systems that generate large amount of heat over a relatively small area. In this work, the major interests are focusing on pool boiling and pool boiling enhancement methods.

1.2 Pool boiling

Pool boiling typically requires a surface submerged in an extensive pool under stagnant condition with heat transfer driven by the buoyancy force. The first systematic study of boiling behavior was carried out by Nukiyama who explored the boiling phenomena on a horizontal chrome wire, demonstrating the different regimes of pool boiling performance using boiling curve [5], which depicts the dependence of the wall heat flux q on the wall superheat on a surface submerged in a pool of saturated liquid. The wall superheat, ΔT, is defined as the difference between the wall temperature and the saturation temperature of the liquid at the system pressure.

A plot of heat flux versus wall superheat is shown in Fig1.1 [6] for a liquid at saturation condition. At very low superheat levels, no bubble nucleation is observed and heat is transferred from the surface to the liquid by natural convection. At a certain value of the wall superheat (point A), vapor bubbles appear on the heater surface. This is the onset of nucleate boiling. The bubbles form on cavities on the surface that contain pre-existing gas/vapor nuclei. As more heat is supplied to the liquid, more cavities become

active, and the bubble frequency at each cavity generally increases. As the spacing between isolated bubbles becomes close and there is a rapid increase in bubble frequency, bubbles from adjacent cavities merge together and eventually form vapor mushrooms or vapor columns. This results in a dramatic increase in the slope of the boiling curve. In partial nucleate boiling, corresponding to the curve a-b, discrete bubbles are released from randomly located active sites on the heater surface.

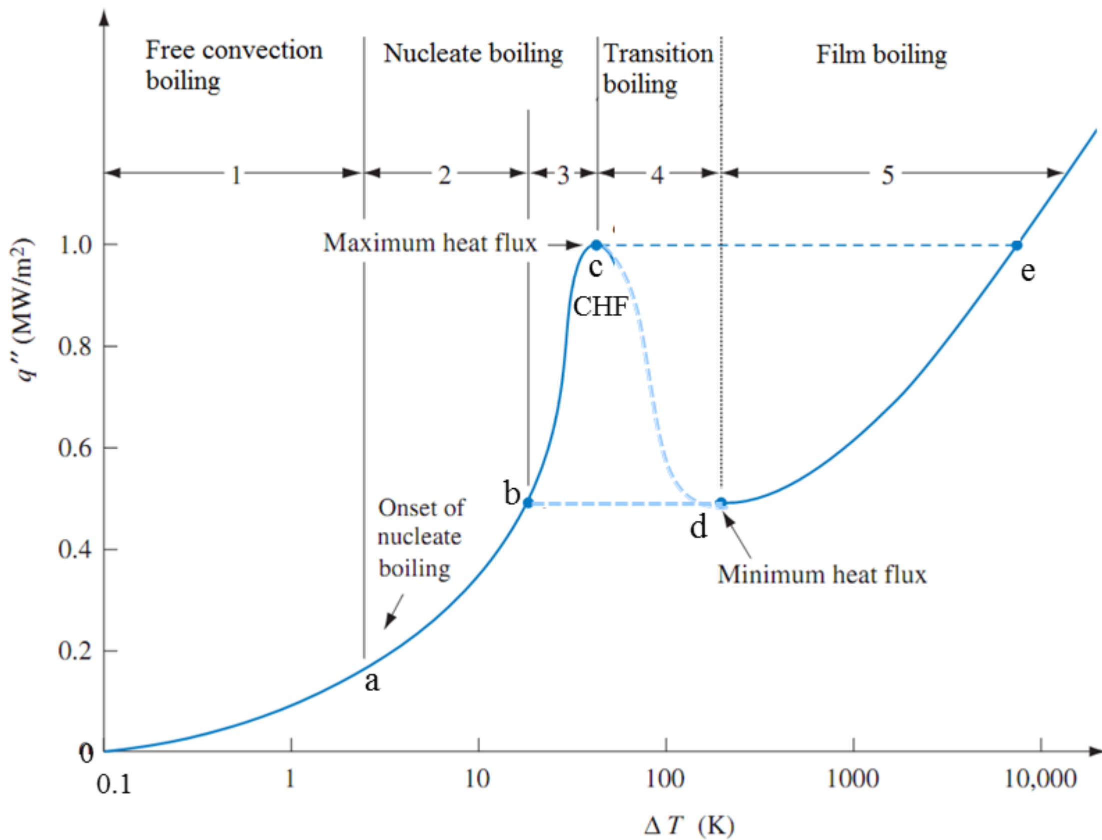


Figure 1.1 Typical boiling curve, showing qualitatively the dependence of the wall heat flux on the wall superheat [6]

With increasing surface superheat in the region of vapor slugs and columns, vapor accumulates near the surface at some sites interfering with the inflow of the liquid toward the surface, which eventually leads to dry out on some parts of the surface. Due to the fact that the heat transfer coefficient with vapor is significantly lower than that with the

liquid, the overall heat flux from the surface decreases (curve c-d). The maximum peak heat flux during pool boiling (point c) is referred as the critical heat flux (CHF). The CHF sets the upper limit of fully developed nucleate boiling. If the wall superheat is increased beyond the critical heat flux condition, overall heat flux continues to be reduced. This regime is referred to as the transition boiling regime. In this regime, dry portions on the surface are unstable, showing significant fluctuations which result from the irregularity of surface rewetting. If the transition boiling is continued with increasing heat, the regime enters the film boiling regime (curve d-e). Stable vapor film is formed in this regime and it insulates the heat transfer between heat transfer surface and the liquid. On a horizontal surface, the vapor release pattern is governed by Taylor instability of the vapor-liquid interface. With a reduction of heat flux in film boiling, a condition is reached when a stable vapor film on the heater can no longer be sustained. In the case of a heat flux controlled heater, an increase in heat flux beyond CHF results in a sudden rise in temperature and the operating point shifts to E in the film boiling region on the pool boiling curve. It is desirable to limit the operation to safe heat fluxes, generally about 70-80 percent below the CHF to avoid catastrophic failure of the boiling surface.

1.2.1 Nucleate boiling

The onset of nucleate boiling on a heater submerged in a pool of liquid is characterized by the appearance of vapor bubbles at discrete locations on the heater surface. These bubbles form on surface imperfections, such as cavities and scratches. The gas/vapor trapped in these imperfections serves as nuclei for the bubbles. After inception, the bubbles generate and depart from the surface. A certain time elapses before a new bubble is formed in the same manner. The nucleate boiling region can be divided into two

regions: partial nucleate boiling regime and fully developed nucleate boiling regime, as shown in Fig 1.1. On a nucleate boiling surface, the overall heat dissipation is divided into four modes of heat transfer: latent, micro-convection, natural convection and Marangoni flow [7]. Latent heat transfer takes place when liquid vaporizes and leaves the heated surface. Micro-convection results from sensible heat energy removed by entrainment of the superheated liquid in the departing bubble's wake. Natural convection is the sensible energy transport removed on inactive areas of the heated surface. Marangoni flow is caused by the surface tension gradient while the bubble is still attached to the surface. Latent and micro-convection heat transfer are the dominant mode of heat transfer mechanisms in the fully developed and saturated nucleate boiling.

Rohsenow [8] proposed a model correlating the heat flux to the wall superheat during nucleate boiling for both the partial nucleate boiling regimen and fully developed nucleate boiling regime. It is on the basis that the bubble nucleation is attributed to the liquid agitation induced by bubble growth and bubble departure. The single phase heat transfer correlation is created by using the liquid Reynolds number and Nusselt number in the vicinity of a bubble.

$$Nu_b = \frac{hL_b}{kl} = ARe_b^n Pr_l^m \qquad [1.1]$$

$$Re_b = \frac{\rho_v U_b L_b}{\mu_l} \qquad [1.2]$$

Bubble departure diameter is correlated in order to identify L_b, appropriate bubble length scale,

$$L_b = C_b \theta \left[\frac{2\sigma}{g(\rho_l - \rho_v)}\right]^{\frac{1}{2}} \qquad [1.3]$$

$$U_b = \frac{q''}{\rho_v h_{lv}} \qquad [1.4]$$

C_b is a constant that is specific to the system. U_b is determined from an energy balance eq. [1.4]. Re_b is defined as a ratio of vapor inertia to liquid viscous force. Heat transfer coefficient (h) is defined based on $T_{sat}(P_l)$ since experiments indicated that the effect of subcooling generally decreased rapidly with an increasing heat flux [1.5].

$$h = \frac{q''}{T_w - T_{sat}(P_l)} \qquad [1.5]$$

With the substitution of above equations, the following Rohsenow's correlation is obtained.

$$\frac{q''}{\mu_l h_{lv}}\left[\frac{\sigma}{g(\rho_l - \rho_v)}\right]^{\frac{1}{2}} = \left(\frac{1}{C_{sf}}\right) Pr_l^{-\frac{s}{r}}\left[\frac{c_{pl}(T_w - T_{sat})}{h_{lv}}\right] \qquad [1.6]$$

The constants r and s equal to 0.33 and 1.0 for water respectively. The values of C_{sf} and n for depend on the heater material and surface combination. In case the constant C_{sf} is not available for a given fluid-surface combination, a value of 0.013 is recommended as an initial guess. Liaw and Dhir [9] established a clear dependence of the constant C_{sf} and the contact angle during pool boiling of water on copper surfaces. By varying the surface condition, they obtained different contact angles and showed that the contact angle and C_{sf} decreased as the surface was made smoother.

1.2.2 Critical Heat Flux (CHF) in pool boiling

The CHF point represents the maximum heat dissipation rate that can endure in the nucleate boiling region. It sets an upper limit for safe operation of the maximum power generation of given boiling systems. Models to describe the occurrence of CHF are divided into three groups [6] and the points of view differ on the initiation of CHF condition, as the CHF is caused when either evaporation or vapor-escape is restricted. The model that the vapor-escape limit yields CHF was proposed by Zuber [10] and then developed by Sun and Lienhard [11] and Lienhard and Dhir [12]. It is called *vapor escape path instability model*. The other model comes from the limit of evaporation, in which the large scale dry patch is assumed to suppress the evaporation. Katto and Yokoya [13] first proposed such model and it is called *macrolayer dry-out model*. Haramura and Katto [14] later proposed the mechanism of how the supply of liquid to the surface is restricted. On the other hand, Dhir and Liaw [9] considered that the triple (three phase) contact line around nucleation sites plays an important role in liquid evaporation, proposing a model in which the triple contact line is shortened by merging vapor stems on the surface. It is called *vapor stem merging model*.

The *vapor escape path instability model* is a widely-accepted CHF mechanism due to its agreement with experimental data. In 1959, Zuber [10] developed a hydrodynamic prediction of the CHF basing on the theory originally proposed by Kutateladze [15] in 1948, on a horizontal flat plate. According to the prediction, the primary factors affecting CHF consists of liquid property, densities of vapor and liquid, heat of vaporization and surface tension. The correlation is given as:

$$q''_{\max} = 0.131 \rho_v h_{lv} \left| \frac{\sigma(\rho_l - \rho_v) g}{\rho_v^2} \right|^{1/4} \quad [1.7]$$

Lienhard and Dhir later proposed another correlation on the basis of Zuber's CHF prediction, applying Helmholtz instability [12]. The premise of this correlation is that when large vapor column becomes unstable due to the Helmholtz instability which is caused by perturbed interface, CHF occurs. The instability results in distorting the vapor column and blocking liquid to prevent effectively rewetting the surface. The correlation proposed by Lienhard and Dhir is shown below,

$$q''_{\max} = 0.419 \rho_v h_{lv} \left| \frac{\sigma(\rho_l - \rho_v) g}{\rho_v^2} \right|^{1/4} \quad [1.8]$$

It is noticed that the prediction of CHF is extremely difficult due to its challenge of evaluating certain parameters such as bubble departure diameter, cavity density and bubble frequency. Although those models can agree well with some of experimental results [16], they can not well explain the experimentally observed surface property dependence of CHF, for example, surface wettability, surface capillarity, nucleation site density on the heating surface, etc. In the past decades, researches were struggling to find exact mechanism of CHF. General observation based on experiments are that pool hydrodynamics [16] and surface properties [9, 17] can both affect the value of CHF. Therefore, one purpose of this work is to enhance the CHF and identify the mechanism of CHF on nanostructured surface.

1.2.3 Enhancement of pool boiling

The preceding introduction to the boiling curve and CHF is just a glimpse of the underlying complexity inherent in boiling heat transfer. There are a number of controlling factors that can have marked effects on the boiling heat transfer performance. Some of these factors are related to system control parameters like pressure and liquid subcooling. Others pertain to surface related characteristics like surface roughness, orientation, geometry, size and wettability. Even surface thermal properties can have an effect on boiling heat transfer. Pioro [2] provided a comprehensive review of some of the common effects of surface parameters on boiling heat transfer enhancement. Due to the inherent complexity of boiling process, in this work, the major boiling enhancement techniques are simplified into two types: passive and active. The active methods involve externally powered equipment to accomplish the heat dissipation such as surface vibration and electrohydrodynamic enhancement. This method is less attractive than the passive technique because of its more complicated design. On the other hand, passive methods, not requiring any external power input, have been intensively investigated by Dewan et al [18]. Various surface enhancement techniques as a passive method have been exploited to maximize boiling heat transfer by augmenting the nucleate boiling heat transfer coefficient and extending the CHF. One of the earliest methods used to produce an enhanced boiling surface was to roughen a plain surface with abrasive. Kurihara and Myers [19] reported that the roughened surfaces provide more active nucleation sites therefore promote nucleate boiling. In general, the passive techniques employed in pool boiling heat transfer enhancement can be classified into three categories: (1) To generate reentry boiling cavities for higher nucleation site density while decreasing the wall

superheat; (2) to increase the total area of thin liquid film under the boiling bubbles and inside the cavities for promoting the latent heat; (3) to increase the forced convection heat transfer between the heating surface and the working fluid for increasing the accumulated superheat in liquid.

The surface morphology has significant impacts on nucleate boiling heat transfer and its effect on CHF has been extensively investigated from the early stages of boiling research. Berenson [20] conducted boiling tests with n-pentane, showing that the roughest surface gives the highest CHF, and that the mirror finished surface gives about 20% lower CHF than that for the roughest surface. Polezhaev and Kovalev [21] suggested that the enhancement was due to decreased vapor jet spacing while Tehver [22] proposed that the enhancement was due to increased macrolayer evaporation time.

Griffith and Wallis [23] first found that the geometry of the cavity containing trapped vapor/gases would directly affect the bubble nucleation process and a variety of surface treatment methods have been employed to modify the morphology of the boiling surface to yield high heat dissipation thereafter [24-26]. Recent developments include increasing the surface area with micro pin-fins [27], applying wicking structure to promote the liquid supply by capillary pumping [28], and depositing nano-particles or coating with nanomaterials [29-35]. Among these development, surface modification by incorporating nanomaterials and nanostructures has appeared as a promising technique for a more effective boiling heat transfer surface.

1.3 Nanostructure for pool boiling enhancement

Surface modification by nanostructures for pool boiling enhancement has attracted great attentions recently due to some unique properties they possessed. The nanostructure modified surface generally has higher wettability, which causes an increased CHF through the enhanced liquid spreading over the heated area. In addition, the modified surface contains more microscale cavities, which serve as the starting sites for nucleation of liquid for bubble formation. Those properties induced by nanostructure are discussed in details as following.

1.3.1 Surface wettability

Nanostructure coated surfaces can remarkably enhance boiling heat transfer by either promoting wetting or inhibiting substance, as reported by Phan et al [36]. In their work, various nanocoating materials were applied to control the wetting characteristics of the surface and the effect of surface wettability induced by nanostructure was investigated. Their study also took an in-depth look at the effect of surface wettability on bubble growth and nucleation. Using various nanocoating materials and deposition method, the test surfaces had a measured static contact angle range from 22˚ to 112˚. For the hydrophobic surfaces they observed low incipient superheats with minimal bubble departure. Hydrophobic surface also displayed early onset of film boiling due to bubble coalescence from the high density of non-departed bubbles. For the hydrophilic surface, the bubble departure diameter increased and the bubble departure frequency decreased, as the wettability increased. According to the study, the best heat transfer occurred under the

highly wetting conditions and a dynamic contact angle approach is adopted in order to explain some of the anomalous behavior observed.

Titanium dioxide (TiO_2) particle is another type of nanostructure widely studied for boiling enhancement due to its super-hydrophilicity. Such nanoparticle deposition can significantly improve the wettability of heating surface leading to an increase in CHF [32]. Nano-particle deposition is commonly achieved by boiling a nanofluid with the desired particle species on the heating surface as a pretreatment. Deposition of the nanoparticles occurs as a result of microlayer dry-out in the ebullition process. The leftover nanoparticles are therefore adsorbed onto the surface.

1.3.2 Surface area and cavity

The surface feature modified by nanostructures could increase the overall heat transfer area and provide numerous surface cavities. The micro/nano-scale surface cavities would function as active bubble nucleation sites during nucleate boiling process and are desirable for boiling enhancement. Ujereh et al [34] investigated the use of carbon nanotube arrays (CNT) for heat transfer enhancement in nucleate pool boiling. CNT were tested on two different substrates with various array densities. Pool boiling curves compared with bare silicon and copper surfaces show significant improvements in incipience temperature, heat transfer coefficient and CHF. The study shows that for silicon substrate there is a monotonic increase in nucleate boiling and CHF with increasing CNT coverage. In addition, by increasing CNT coverage, a consistent decrease in incipience temperature is observed. The authors report similar results for the copper

substrates and propose that the remarkable boiling enhancement is due to more active heat transfer area and micro/nano-scale cavities created by CNT.

Chen et al. [32] investigated pool boiling on a heating surface coated with TiO_2 nanotube arrays. Pool boiling experiments with water on a bare Titanium surface and one coated with TiO_2 nanotubes were conducted to observe the effect of the surface nanostructures. The surface with TiO_2 nanotubes showed better nucleation and heat transfer performance. Small bubble sizes and a higher departure frequency were observed from the nanotube coated surface during nucleate boiling, which is attributed to the increased number of available bubble nucleation sites and increased intrinsic area, as reported by this study.

Honda et al. [27] studied pool boiling heat transfer of FC-72 on silicon chip with micro pin-fins and micro/nanostructures. In addition, different degrees of subcooling as well as degassed and dissolved gas solutions were used. The authors report that both the micro pin-fin surface and the surface with micro/nanostructure improved the overall heat transfer and CHF compared to the smooth surface. Additionally, the micro pin-fin surface with micro/nanostructure showed the greatest improvement in boiling heat transfer. It is reported that all the surfaces with micro/nanostructure showed the same increasing trend of heat transfer with increase in subcooling as well as an increase in heat transfer in the low heat flux region with the presence of dissolved gas. This finding shows that augmenting the surface feature on the micro/nano-scale would drastically alter the heat transfer performance of the heating surface.

1.3.3 Summary of nanostructure on pool boiling enhancement

Table 1.2 gives a summary of recent studies that are related to the enhancement of boiling heat transfer by use of nanomaterials and nanostructures. Wu [31] reported a coating of hydrophilic titanium oxide (TiO_2) nanoparticles on the heater surface that increased CHF by 50.4% in pool boiling with FC-72. The enhancement is attributed to the increased hydrophilicity of the nano-porous layer. Chen et al. [32] studied the boiling performance of a super-hydrophilic TiO_2 nanotube array covered surface. It reduced the wall superheats by half during boiling at a given heat flux compared to the bare Ti surface. It is concluded that the nanotube array introduced large number of active nucleation sites that promoted bubble generation. Carbon nanotube (CNT) is also studied for pool boiling application [37]. The CNT coated surface is highly effective in improving both CHF and heat transfer coefficient (HTC) in the low heat flux region due to increased surface cavity density and enhanced roughness. Significant enhancements in both CHF and HTC have also been obtained from surfaces coated with Cu nanorods and nanowire (NW) arrays [38-42]; the reported CHF (220 W/cm^2) for CuNW surface is one of the highest for pool boiling heat transfer with water [38].

The NWs enhance surface wettability, which helps in increasing CHF and delaying the dry-out condition [43]. Due to the pin fin effect, NW structures greatly increase the active heat transfer area. In addition, the NW height was found to directly affect the heat transfer [42]. By incorporating the hydrophilic NW structure in conjunction with hydrophobic surfaces, the pool boiling performance can be further enhanced [44].

Table 1.2: Summary of pool boiling enhancement with nanostructures

Researchers	**Heater/ Working fluid**	**Nanostructure**	**Surface characterization**	**Results**	**Mechanism / Comments**
Vemuri et al. [30]	Flat plate heater /FC-72	Aluminum oxide particle thin layer	Pore diameter = 50 ~250 nm	Incipient superheat reduced by 30%	Porous structure and enhanced surface wettability
Wu et al. [31]	Cu block / FC-72 and water	Titanium oxide nanoparticle coating	Layer thickness = 1μm	CHF increased by 50.4% for water	Enhanced surface wettability
Ujereh et al. [34]	Plane heater / FC-72	CNT coated on Si and Cu surface	CNT height = 40 μm	CHF and HTC enhanced on CNT surface	Increased surface cavity
Launay et al. [33]	Cu heater / PF5060 and water	CNT coated on plain Si and 3D Si micro-structure	CNT height = 40 ~ 100 μm	Moderate enhancement at low heat flux region	Roughness enhancement
Ahn et al. [37]	Cu heater / H_2O	MWCNT forest	CNT height = 25 μm	CHF improved by 28%	Surface roughness enhancement
Li et al. [39]	Cu heater / H_2O	Cu nanorod array	Nanorod height = 450 nm	High heat flux coupling with low incipience	Enhanced wettability and coupling effects of micro / nanostructure
Chen et al. [38]	Si chip heater / H_2O	Cu / Si nanowire (CuNW, SiNW)	CuNW, SiNW height = 50 μm	CHF and HTC enhanced by 100%	Capillary effect, enhanced wettability and active nucleation sites
Im et al. [40]	Cu heater / FC-72	Cu Nanowire (CuNW)	CuNW height = 2, 4, 6, 8 μm	200% CHF enhancement on 2 μm NW	Enhanced micro-scale cavities and surface roughness

These studies have shown that most of the surface nanostructures were effective in decreasing the wall superheat at boiling incipience, and enhancing the nucleate boiling heat transfer and critical heat flux. The factors leading to enhanced boiling surfaces, however is not fully understood, therefore, it is of great interest to investigate the enhancement mechanism behind those phenomena.

1.4 Objective and outline

The ultimate objective of this work is to identify nanostructures that enhance the pool boiling enhancement at 2D and 3D substrates and investigate the mechanism behind the micro-scale heat transfer phenomenon. To realize this goal, metallic and semiconductor nanowire structures were studied, fabricated and tested on different substrates for boiling enhancement. The effects of nanowire property and substrate geometry were further investigated. Nanowire structure were chosen for constructing nanostructured surface due to their excellent properties of being scalable, cost-effective and able to produce uniform geometrical features at a large scale. Nanowires can be defined as structures that have a thickness or diameter constrained to tens of nanometers or less and an unconstrained length. Nanowire structures possess properties which could be utilized to promote boiling performance. First, it has been observed that a surface coated with nanowires can be superhydrophilic, which helps in increasing CHF and delaying the dry-out condition. Second, nanowire arrays contain many orders of magnitude more cavities and pores compared to other microfabricated or micromachined surfaces, thereby effectively increasing the nucleation site density. Furthermore, due to the pin fin effect, the effective heat transfer area of nanowires is much higher than that of micro-fabricated surfaces. Finally, nanowire arrays may act as an efficient wicking structure, which provide significant capillary force to hold the liquid.

The nanowire coated substrate has been shown to efficiently remove large amount of heat. A recent pool boiling heat transfer study with SiNW-coated silicon substrates suggests a 100% enhancement in both CHF and HTC, compared to the same test with the plain surfaces [39]. The NW structure is promising in the field of thermal management

and energy conversion of high heat flux; however, the current fabrication methods are only able to develop the NWs on 2D substrate, which significantly limits the NW application. Because of this, the fabrication technique of NW structure on 3D substrate is another focus in this work. Basically, a new synthesis technique is first developed to control the height of NW structures grown on flat surfaces, and then it is utilized to fabricate SiNW structure on the whole surface of Si microchannel, including top, bottom and sidewall areas. Utilizing the 3D structures with NW structure to study their pool boiling behavior can provide a new insight into enhancing boiling transfer more effectively and the technique to incorporate NW and 3D structure can be directly applied for semiconductor cooling, thermal management and high-heat-flux energy conversion at micro/nano-scales.

The structure of this work is as follows: In chapter 2, a new technique for direct growth of Cu nanowire on flat substrate is introduced, and the parameters used for controlling NW height and the merits of this technique are discussed. In chapter 3, the synthesis of SiNW on 2D substrate and 3D microchannel is presented and an in-depth investigation of the fabrication process of SiNW on the whole surface area of microchannel is conducted. The pool boiling setup and testing methodology are discussed in chapter 4. The boiling test results of various NW structures on different substrate are presented in chapter 5. In addition, in chapter 5, the effect of NW height on CHF and HTC will be discussed in details, and the bubble dynamics and surface wettability change on microchannel heat sink due to NW structure are analyzed accordingly. In chapter 6, conclusions based on the observed experimental results are summarized and the

mechanisms responsible for the heat transfer enhancement are discussed. Finally, the recommendations for future work are presented in chapter 7.

CHAPTER 2

DIRECT GROWTH OF COPPER NANOWIRE (CuNW) ON 2D SUBSTRATES

Cu has superior thermal conductivity and it is one of the most common-used metals in semiconductor industry. Therefore, Cu-based nanowire is chosen as one of the nanowire candidates for pool boiling enhancement tests. In this chapter, a new fabrication process developed for direct growing of vertically aligned CuNW on flat substrates was presented and the fabrication merit comparing to conventional method was discussed.

2.1 CuNW fabrication by electro-chemical deposition through AAO template

2.1.1 Template synthesis of nanowires

Nanostructured materials have been widely applied in many fields, including optics, semiconductors and microelectromechanical systems (MEMS). Metallic nanowires (NW) have attracted considerable attention owing to their interesting electronic and physical properties [45-48]. Many fabrication methods, such as vapor-liquid-solid (VLS) growth [49], thermal decomposition [50] and surfactant-assisted hydrothermal process [51] have been developed to create metallic NW arrays. Among them, the fabrication method with the assistance of porous membrane as a template is considered to be a convenient and versatile approach for NW preparation [52]. The

templates can be porous polycarbonate membranes, nanochannel glasses and anodic aluminum oxide (AAO) membranes [53]. For the template-assisted synthesis method, the template materials must meet certain criteria. First, the template materials must be compatible with the processing conditions. For example, the template used in electrochemical deposition has to be an electrical insulator, and be chemically stable during the synthesis. Secondly, the internal pores of the template need to be wet or immersed by the deposition solution or materials. In addition, as a bottom up approach, the template-based deposition has to start from the bottom of the template and proceed towards to the other side. Therefore, the closure of one side of the template is necessary.

In this study, the anodic aluminum oxide (AAO) membrane was chosen as the template material for CuNW synthesis because it possesses desirable characteristics, including tunable pore size, uniform structure and high thermal stability. By electro-deposition through the AAO membrane template, a variety of metallic [54], semiconductor [55, 56], and conductive polymer NW arrays [57] can be created.

In addition, using AAO as the template for NW synthesis offers many advantages over other fabrication method: (1) The process can be conducted under room temperature, no high vacuum or expensive instrumentation is needed; (2) the morphology of the deposited material is determined by the template pore size, thus the dimension of as-fabricated nanowire is tunable by the pore geometry; (3) two or more components can be deposited through the template sequentially to form multi-segmented materials or hetero-junctions.

However, as the template has to be in direct contact with the substrate, this synthesis method so far can only be used on flat surface for NW fabrication.

2.1.2 AAO template for CuNW synthesis

AAO is a self-ordered nanoporous template that consists of a hexagonal array of cells with uniform and parallel straight cylindrical nanopores perpendicular to the template surface [58]. AAO templates can be obtained easily by a two-step electro-chemical anodization process of aluminum foil [59]. The diameter of the pore, the pore density and the thickness of the AAO template can be controlled by changing their anodization conditions, such as voltage, types of electrolyte acids, temperature of the electrolyte solution, etc. Fig 2.1(a) and (b) show the surface morphology of a typical AAO template, which possesses an average pore size of 200 nm with 50 nm pore spacing and overall thickness of 60 μm. The highly ordered pore arrays are desirable for growing nanowire structure more uniformly.

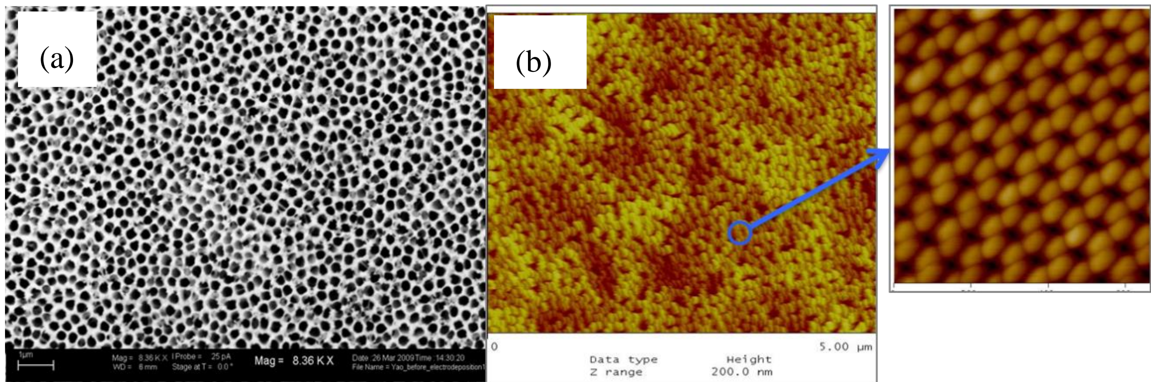


Figure 2.1 Surface morphology of AAO template: (a) top view in SEM image, (b) top view in AFM image

Although the electro-deposition assisted by the utilization of the AAO membrane template is considered to be the most straightforward and versatile technique for nanowire fabrication, the NW fabrication using AAO membrane usually requires a bonding layer for NW growth. In particular, a conductive thin film layer has to be deposited on one side of the AAO membrane before the electrochemical deposition. In

addition, an extra epoxy layer is also needed to bond the thin film layer on the AAO membrane to the substrate, which introduces additional interfacial layer and becomes troublesome in practical applications. While this epoxy layer is inevitable in creating the NW arrays using the AAO templates, the additional thermal resistance is introduced. The thermal resistance of a typical epoxy adhesive containing boron nitride fillers is in the range of 0.7~1.6 ℃/W [60]. As the epoxy layer becomes thicker, its thermal resistance proportionately increases. The resistance furthermore increases as the temperature rises. The epoxy adhesive also traps air bubbles and forms voids, creating a non-uniform surface due to the high viscosity of the epoxy during its application. As a result, the epoxy layer becomes a major problem in the NW fabrication using the AAO template. In addition, when applying the epoxy on a large area, the difference in coefficient of thermal expansion (CTE) between the epoxy layer and NW array has to be taken into account as it causes mismatch due to thermal stress at the interface and compromises mechanical reliability of the assembly.

2.2 Direct grow of CuNW through AAO template

To address issues that occur on the conventional method for CuNW synthesis, a new fabrication method is developed to directly deposit metallic NW array on a plain substrate using the AAO template without any epoxy bonding layer. The mechanical reliability and flexibility of the NW arrays are therefore greatly enhanced. The interfacial thermal resistance between the NW array and the substrate are eliminated, making the samples with the NW array capable of sustaining high temperatures for pool boiling application. With this method, the NWs can be fabricated onto various substrates; thus

the selections of the substrate materials are flexible and the potential applications of the NW arrays are greatly broadened. For example, semiconducting substrates used for growing piezoelectric NWs are not preferred in many applications which require flexible power source, such as implantable bio-sensor. Using polymeric or plastic substrate instead of brittle metallic substrate for piezoelectric NW deposition in energy harvesting is advantageous [61].

2.2.1 Preparation of Substrate Materials

To examine the effect of substrate materials on the NW structures, three different substrates were employed for the CuNW deposition:

(i) A (111) polished 4” silicon wafer was coated with a 500 nm thick silver (Ag) layer by E-beam evaporation.

(ii) The 25×25 mm glass substrate was cut from a 75×25 mm glass slide coated with 80 nm gold (Au) layer (BioGold®, Thermo Scientific).

(iii) The $20\times20\times3$ mm copper substrate was customized by computer numerical control (CNC) machine tools and mechanically polished.

All three types of the substrates (i.e. Ag-silicon, Au-glass and Cu) were cleaned by Acetone, Isopropanol, DI water rinse, and dried at room temperature before used for the NW deposition. The substrates were also examined by atomic force microscopy (AFM, Veeco Dimension 3000) for the surface roughness measurement, as shown in Table 2.2.

2.2.2 Fabrication procedure

In this study, AAO membranes with a thickness of 60 μm and pore sizes of 200 nm (Anodisc, Whatman) were used as the templates for NW synthesis. The pore size of the commercial AAO membrane can be as small as 20 nm. In order to study the application of metallic NW structure on pool boiling enhancement, Cu was chosen as the NW material due to its high thermal conductivity and mechanical reliability. For CuNW directly grown on the Si substrate, a thin conductive film is still needed (e.g. Ag layer), and it is coated on the Si substrate instead of AAO membrane. The silver layer serves three purposes: (i) it provides the counter electrode for electro-chemical deposition, (ii) it acts as the seeding layer for CuNW synthesis and (iii) it reduces the surface roughness for better contact with the AAO template. For the Au-glass and Cu substrates, no conductive thin film is needed but the surfaces are polished for better surface contact. The AAO membrane was attached on the substrate before electro-chemical deposition (Fig 2.2(c)). A liquid film of DI water was first applied between the AAO and substrate. Because of the hydrophilicity of the AAO membrane, the surface tension induced by the liquid film provided enough adhesion forces to attach the AAO membrane onto the substrate. Platinum gauze was attached on top of the AAO membrane and served as counter electrode. The gauze was employed since it permitted high and stable diffusion flux of ions migrating through the AAO membrane, creating a uniform NW growth rate.

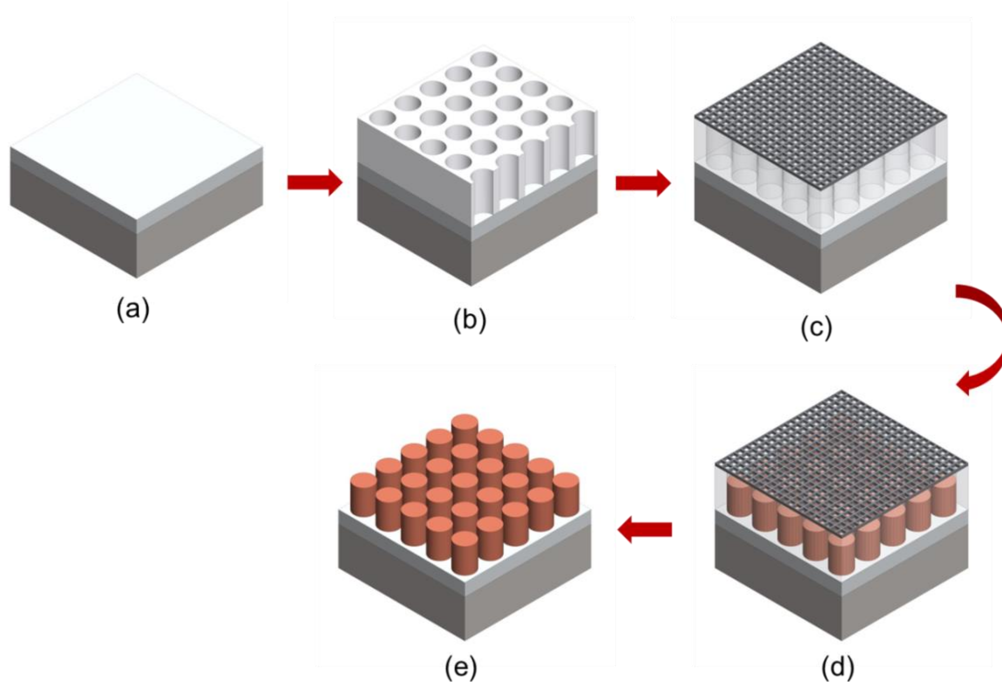


Figure 2.2 Schematic of metallic NW synthesis process: (a) substrate surface treatment (depositing additional thin film layer when needed), (b) AAO template attachment, (c) application of Pt gauze as the counter electrode (d) Electrochemical deposition of CuNW and (e) AAO template removal

In addition, the gauze allows the attraction forces to sandwich the AAO membrane between the working and counter electrodes (e.g. the Pt gauze and substrate). The electrochemical deposition was performed in a three-electrode potentiostat system (VersaSTAT, Princeton Applied Research). The substrate, Ag/AgCl electrode, and Pt gauze are used as the working electrode, reference electrode and counter electrode respectively, as shown in Fig 2.3(a).

The Pt gauze was employed since it permitted high and stable diffusion flux of ions migrating through the AAO membrane, creating a uniform NW growth rate. In addition, the gauze allows the attraction forces to sandwich the AAO membrane between working and counter electrodes (e.g. the Pt gauze and substrate). A clamping apparatus is used to hold the electrodes during the electrochemical deposition process. The CuNW

arrays were prepared in 0.1 M $CuSO_4$ aqueous electrolyte without any additives under potentiostat condition at room temperature.

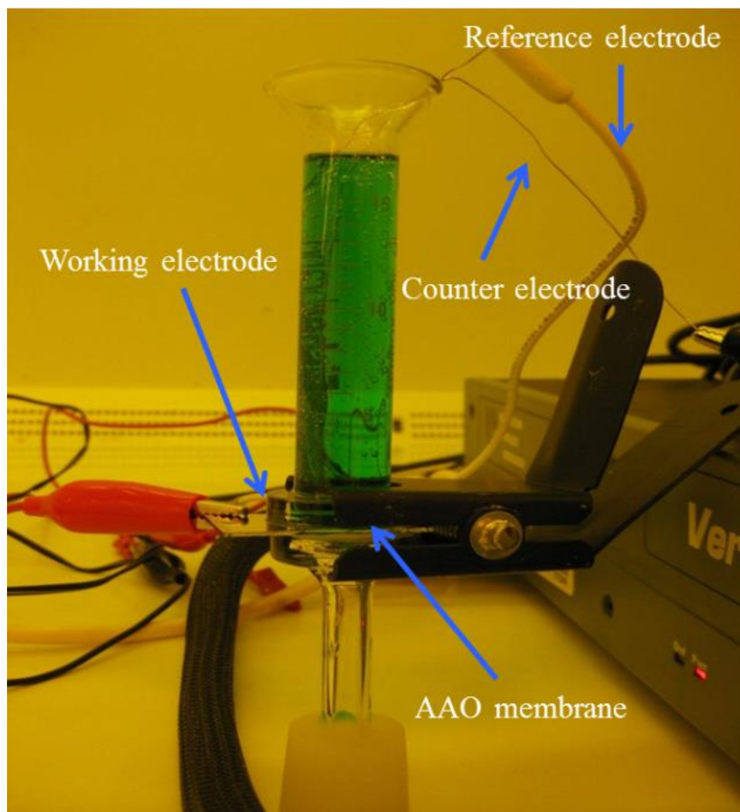


Figure 2.3 Electro-chemical deposition setup for CuNW synthesis

As the NW growth rate is a function of time and applied potential, the deposition time duration was controlled from 600 to 900 seconds and the potential was kept around 0.9 V, as shown in Table 2.1. At low potentials (<0.45 V), the electrochemical deposition may only result in poor coverage of recesses/vias and low NW growth rate. On the other hand, high potentials (>0.9 V), which presents excessive current, are not preferred as faster reduction of Cu ions on the tip of the nanowire would roughen surface, create particle cluster and nano-branches, or even obstruct the nanopores of the AAO template.

The high potential does not necessarily result in increased growth rate and is liable to the presence of hydrogen discharge once the limiting current density is reached [62].

After deposition, the as-prepared samples were immersed in NaOH solution and the AAO membrane was completely removed. The samples were then rinsed at least three times with deionized (DI) water and vacuum dried at room temperature. Free standing CuNW arrays were obtained on the substrate.

2.2.3 Control of CuNW height

For electroless chemical deposition of CuNW, it is found that the electrical potential and time duration are the major parameters used to control the height of CuNW. Four different kinds of CuNW samples, with the average NW height of 20 μm, 10 μm, 5 μm, and 2 μm were successfully fabricated on flat Si substrate, as shown in Fig.2.4 (a) ~ (d). The maximum NW height was found to be around 20 μm (Fig.2.4 (a)), which was fabricated under potential range between 0.9~1.2 V for 900 second electro-chemical deposition. Table 2.1 shows a complete list of deposition condition for CuNW synthesis on Si substrate.

Table 2.1: Deposition conditions for CuNW synthesis on 2D Si substrate

NW height	Potential	Duration
20 μm	0.9~1.2 V	900 sec
10 μm	0.6~0.75 V	900 sec
5 μm	0.45~0.5V	900 sec
2 μm	0.4 V	600 sec

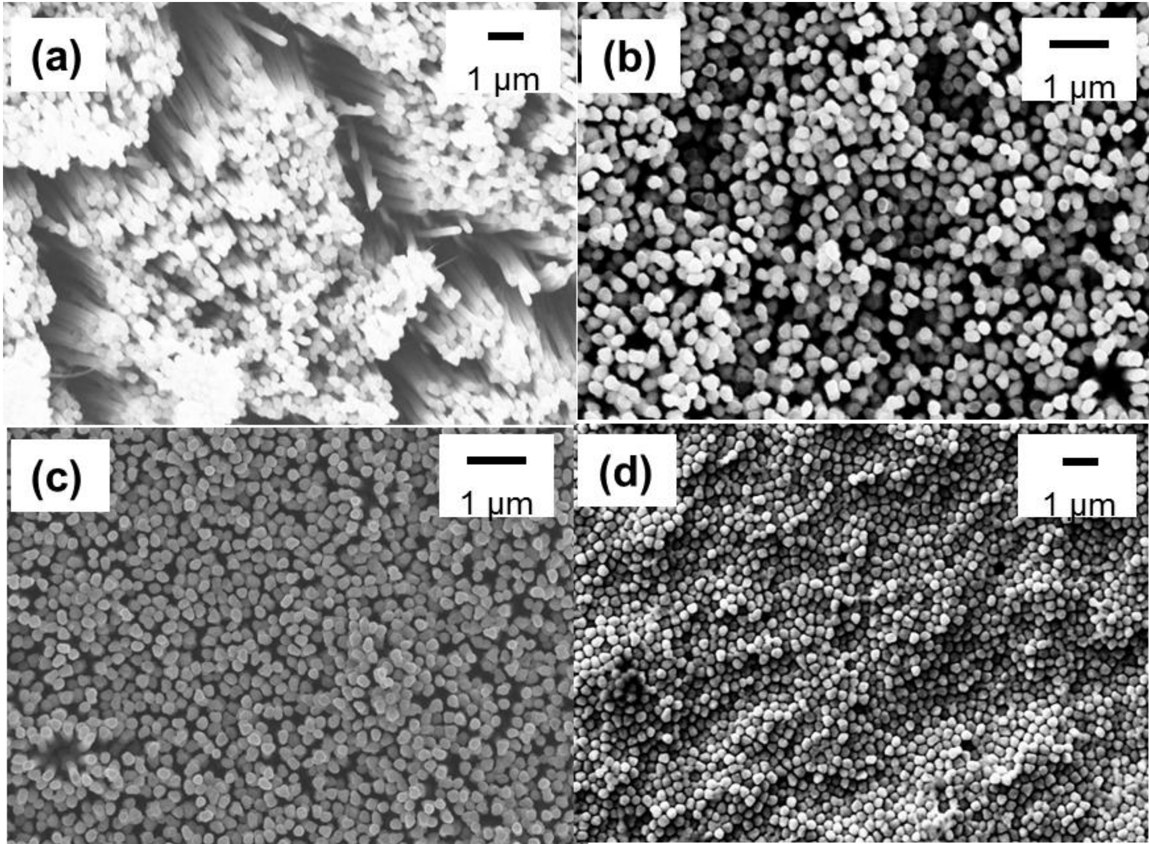


Figure 2.4 SEM images of CuNW on Si substrate with average heights of (a) 20 μm, (b) 10 μm, (c) 5 μm and (d) 2 μm

2.5 CuNW growth on different substrates

In recent years, extensive studies have been performed using various electrochemical methods and in situ SPM (scanning probe microscopy) techniques to realize the electrochemical deposition mechanism of metallic materials on foreign substrates [63]. It is believed that the kinetics and mechanism of electrochemical deposition and the involved phase formation phenomena can be affected by electronic properties and surface homogeneities of the substrate materials. The electrochemical deposition inside the pores of the AAO membranes therefore relies not only on the deposition potentials, but also on the surface condition of the substrates. Fig. 2.5 (a) and

(b) show the AAO template used in the experiment and the CuNW structures obtained, respectively. Although they have different heights, similar CuNW arrays are observed on different substrate materials. Since the NW structures are formed inside the pores of the AAO template, the NW are aligned vertically as the pores are. The as-deposited CuNW arrays on Ag-silicon, Au-glass and Cu substrates also have the same diameter of 200 nm as the pore size.

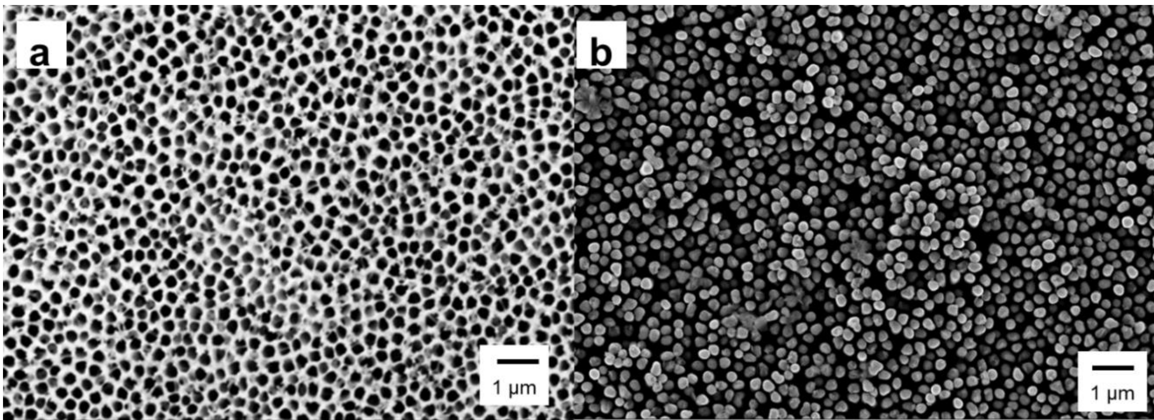


Figure 2.5 SEM images of (a) AAO template, (b) CuNW directly grown on Si substrate (similar CuNW structures were obtained on other substrates, including Au-glass and copper substrate)

In addition, it is found that the NW arrays have different growth rates on different substrates under the same deposition conditions, as summarized in Table 2.2. Although there are many parameters, including the geometry and material property of the electrodes, can affect the electrodeposition rates, the surface roughness of the substrates plays the most critical role [64]. The Ag-silicon has the smallest surface roughness of 5.2 nm and longest NW of 20~25 μm. The Au-glass has a larger surface roughness of 12 nm and shorter NW of 10~15 μm. Finally, the mechanically-polished Cu substrate has the largest surface roughness of 400 nm and shortest NW of 5~10 μm. The Ag-silicon surfaces with the smallest surface roughness provide better surface contact with the AAO template

than Au-glass and mechanically polished Cu substrate. As the rough topography usually has a higher requirement to ensure that the peaks of the roughened area are covered by an adequate coating material , copper ions (Cu^{2+}) take longer time to accumulate inside the pores for rough surfaces such as Cu substrates. Consequently, at a given synthesis condition, the NW growth rate varies and highly depends on the surface roughness of the substrate materials.

Table 2.2: Deposition conditions for CuNW synthesis on different substrates

Substrate	**Surface roughness of the substrate (in RMS)**	**Deposition condition (potentiostat)**	**Average NW height**
Ag-silicon (500 nm thick Ag on 450 μm thick silicon)	5.2 nm	0.9V for 900 sec	20~25 μm
Au-glass (80 nm thick Au on 1.1 mm thick glass)	12 nm	0.9V for 900 sec	10~ 15 μm
Cu (polished, 3 mm thick copper)	400 nm	0.9V for 900 sec	5~10 μm

2.3 Surface wettability of CuNW surface

In order to investigate the surface wettability of the samples, static contact angle (CA) measurements were conducted on the substrate with and without CuNWs. A brief introduction of surface wettability and contact angle were presented first for a better understanding of the wetting phenomenon.

2.3.1 Surface wettability and contact angle

The behavior of liquids in contact with a solid varies from one surface to another depending on the type of liquid. Acetone, for example, makes a thin film when its droplet is placed on aluminum surface. For contrast, a water droplet would hold itself as a discrete drop of water. Generally liquids with week affinities for solid will maintain beads shape while those with higher affinities for solids will tend to spread out and form a film. The affinity of liquids for solids is referred to as the wettability. The wettability of the liquid is quantified by contact angle θ, defined as the vapor interface and the solid surface, measured through the liquid at point O where all three points meet as illustrated in Fig.2.6. As θ decreases, liquid will spread more on the surface and as θ tends to form a thin liquid film on the surface.

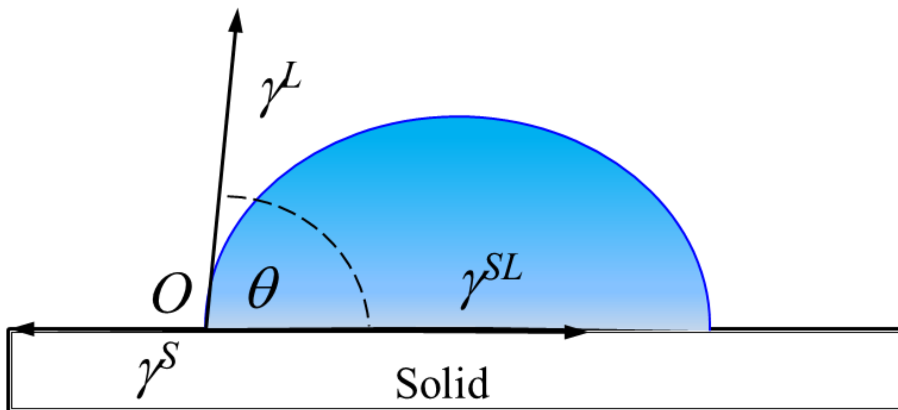


Figure 2.6 Interfacial regions associated with a liquid droplet on a solid surface

In this work, the contact angle measurement is performed by static sessile drop method to determine the liquid-solid contact angle. In this method, the contact angle is measured by Goniometer that utilizes an optical subsystem to capture the profile of a pure liquid on a solid surface. Basically, a drop of liquid is placed or allowed to fall from a

certain height onto the testing surface. When the liquid has become sessile, the drop will retain its surface tension and become ovate against the solid surface. The contact angle at which the oval of the drop contacts the surface determines the affinity between the two substances. That is, a flat drop (θ <90˚) indicates a high affinity, in which case the substrate is hydrophilic. A more rounded drop on top of the surface (θ > 90˚) indicates lower affinity and the substrate is called hydrophobic. It is noticed that, the static sessile drop method is sensitive to the ambient environment such as temperature, oxygen, chemicals. Surface active elements may exist in a large volume on the surface than in the bulk liquid. So for better accuracy, DI water should be used, and before testing surface cleaning is highly recommended.

2.3.2 Wettability of CuNW surface

Now back to the contact angle measurement of CuNW surfaces. The results suggest that all CuNW covered surfaces become hydrophilic regardless the substrate material. The contact angle of plain Cu substrate is about 80˚ while for CuNW coated substrate, it decreases to 28˚, as shown in Fig.3.4. The super-hydrophilicity induced by CuNW is favored in boiling heat transfer as it is expected to result in a higher CHF. The surface-hydrophilicity of the nanowire arrays can be explained with the Wenzel equation [65]:

$$\cos\theta = r\cos\theta' \qquad [2.1]$$

Where θ and θ' are contact angles on the roughened surface and completely smooth surface, respectively. r denotes the roughness factor. This equation indicates that the surface roughness enhances the hydrophilicity of hydrophilic surfaces and enhances the

hydrophobicity of hydrophobic ones because *r* is always larger than 1. The water contact angle of a flat Cu surface is less than 90˚ due to native oxides formed on the surface, so the nanowire covered surface become more hydrophilic due to the enhanced roughness.

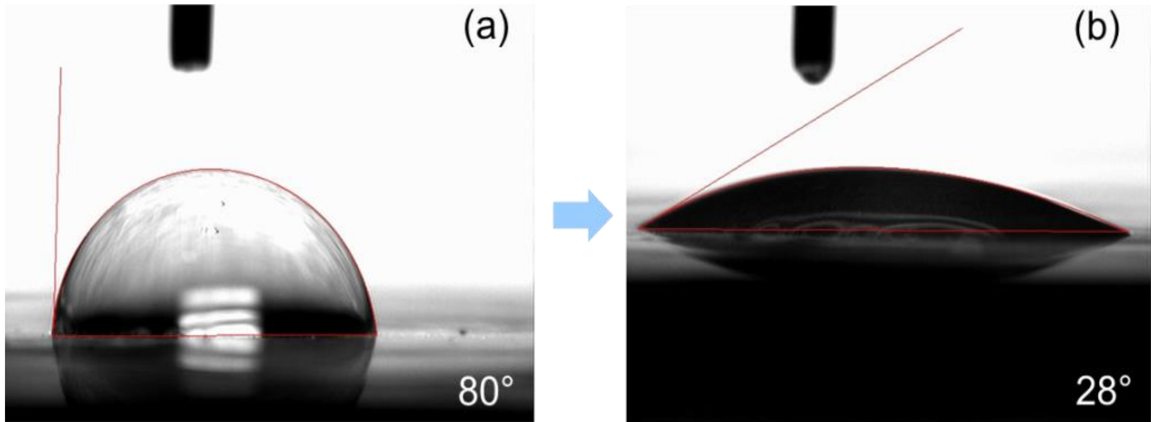


Figure 2.7 Contact angle of (a) plain Cu substrate ~80˚ and (b) CuNW coated substrate ~28˚

2.4 Merit of the technique

The NW fabrication technique presented in this work is a simple and controllable method for directly growing metallic nanowires (NW) on plain surfaces using porous AAO templates. It does not require sputtering layer at the backside of AAO template which is mandatory in the conventional method. No extra bonding layer is needed since it can directly grow NW on smooth surface through electro-plating, which release the fragile NW layer from the local stress induced by the CTE difference of interfacial materials. With this method, CuNW arrays are successfully fabricated on Ag-silicon, Au-glass and copper substrates, and this method can be further applied to a variety of substrates. The NW array without an intermediate epoxy layer proves to be beneficial in other applications where larger area coverage of nanowires is desired.

CHAPTER 3

SILICON NANOWIRE (SiNW) SYNTHESIS ON 2D AND 3D SILICON SUBSTRATES

To investigate the effect of material property at micro/nano scale on pool boiling, SiNW with similar dimension of CuNW were fabricated on 2D substrates and tested for boiling enhancement. The study on SiNW fabrication leaded to a further attempt on fabricating SiNW non-flat surface and a two-step etching method was developed to realize this goal. In this chapter, SiNW synthesis on 2D and 3D substrates was presented and the method used for fabricating uniform SiNW on Si microchannel surface was discussed in details.

3.1 An overview of SiNW synthesis

SiNWs have attracted great attention due to their unique properties and potential applications as building blocks for optoelectronic devices [66], biochemical sensors [67, 68], as well as for advanced electronic cooling methods [38]. Well-ordered and high aspect-ratio SiNW arrays with controllable density are desirable for many practical applications such as in Field-Effect Transistors (FET) [69-71]. Considerable efforts have been devoted to fabricating SiNW by different techniques which fall into two grand schemes: bottom-up and top-down. The most representative fabrication methods are summarized in the following.

3.1.1 VLS growth for SiNW fabrication

The vapor-liquid-solid (VLS) growth as a bottom-up approach was first introduced by Wanger and et al. [49] about 50 years ago in the study of 1D crystal growth mechanism. This method was majorly used to grow various whiskers on the μm or mm scales back in 1970s [72-74] and till 1990s it was utilized for the growth of 1D structures on nanosacle, i.e., nanowires and nanorods [75-77]. Fig.3.1[78] shows a schematic of the VLS mechanism for SiNW synthesis. In this mechanism, the gold nanoparticle catalyst forms liquid alloy droplets at a high temperature by adsorbing silane (SiH_4) vapor. The alloy is further supersaturated, i.e., it becomes a solution in which the actual concentration of the components is higher than the equilibrium concentration. It then drives the precipitation of the component at the liquid-solid interface to achieve minimum free energy of the alloy system. Accordingly, the 1D silicon growth begins, and it continues as long as the silane is supplied. Because the vapor (silane), liquid (gold nanoparticle catalyst alloy), and solid (SiNW structures) are involved in this process, it is therefore known as VLS mechanism. The diameter and position of the SiNW are confined by the size and position of the gold nanoparticle catalyst, as shown in Fig.3.1.

The mechanism works at a high temperature at which the metal catalyst forms a liquid alloy. Because of this, some chemical process that occur at high temperatures, such as Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE) and Laser Ablation (LA) can be applied in conjunction with the VLS mechanism. Occasionally, metal catalysts may work in a solid state in a vapor or liquid phase in a process, which are identified as VSS (Vapor-Solid-Solid) and LSS (Liquid-Solid-Solid) processes.

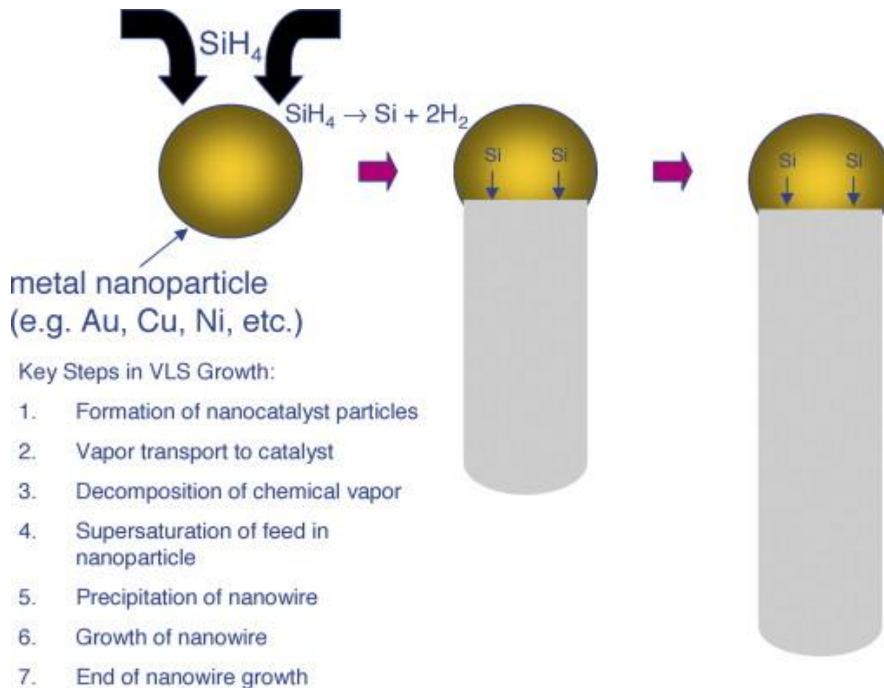


Figure 3.1 Schematic of VLS mechanisms for SiNW growth [78]

3.1.2 Oxide Assisted Growth

The Oxide Assisted Growth (OAG) is another bottom up approach for SiNW synthesis. The process assembles to the VLS growth but instead of metal catalyst, a vapor of Si_xO generated by laser ablating of Si and SiO_2 functions as the catalyst and the seeds for the growth of nanowires [79]. The diameter of the SiNWs grown by OAG method is determined by the ambient environment such as He, H_2 and Ar which control the cluster migration and phase transformation at the tip of the SiNW. The required growth temperature is reduced due to the metal-free environment.

3.1.3 Deep Reaction Ion Etching (DRIE) for SiNW fabrication

The DRIE is considered as a powerful top-down approach for Si nanostructure synthesis. A typical DRIE process involves the use of high-density plasma and comprises

a sequence of alternating steps of silicon etching and polymer deposition to protect the sidewall from further lateral etching. There are two main technologies for DRIE: Cryogenic process and Bosch process. In Cryogenic process, the wafer is chilled to –110 ℃ to reduce the etch rate on passivated sidewalls. It is one-step etching as etch gases and passivation gases are released at the same time. The Bosch process, in the contrast, alternates repeatedly between isotropic plasma etching and passivation layer deposition, and each phase lasts for several seconds. The passivation layer protects the entire substrate from further chemical attack and prevents further etching. An optimized DRIE Bosch process combined with bottom up method was introduced by Fu et al [80] to fabricate various silicon nanostructures including nanopillars, nanowires, and nanowalls. The nanodot mask is first patterned by e-beam lithography and followed by nanoparticle preparation. The Si etching then is performed using a mask of Au or Co nanoparticles. After DRIE etching, as-prepared Au or Co particles are used to grown SiNWs. With this method, NWs can be fabricated with height of 5~20 μm at various density.

3.1.4 Electrochemical etching for SiNW synthesis

Electrochemical etching technique is another top down approach widely used for Si nanostructure fabrication. It can be further divided into four routes depending on the nature of the process. Those routes are anodic etching, photoelectrochemical etching, lasser-assisted etching and electroless etching, all of which occur in acidic fluoride solutions [81]. The boundaries of those routes are not completely distinct and sometimes the etching process is a combination of them. Anodic etching involves the working electrode and a counter electrode to a power supply, therefore the voltage can be used to control the electrochemisty during the process. The photoelectrochemical etching and

laser-assisted etching are used primarily in n-type Si because free carriers need to be made available by illumination of the Si electrode. By irradiating a small spot on a Si wafer, free carriers are produced and band bending is used to separate holes from electrons. In n-type Si, holes are forced to the surface of the irradiated area and Si nanostructure forms there. In p-type Si, holes are forced to the un-irradiated area where Si nanostructure starts to form. For electroless etching process however, neither power supply nor photon source is needed for the electrochemical reaction. In addition, the electroless etching of Si to form Si nananostructure is a simple process that can be performed on the Si substrate with different geometry, therefore it is the major technique used for SiNW fabrication in this work. There are three types of electroless etching: stain etching, chemical vapor etching and metal-assisted etching.

3.1.4.1 Stain etching

Stain etching is the etching that results from a solution consisted of fluoride and an oxidant. Turner et al [82] were among the first to study stain etching and propose that there were anodic and cathodic sites on the Si surface with local cell currents flowing between them. The mechanism of stain etching assembles to anodic etching as the Si structures fabricated by the two etching methods are similar. The Si goes into solution at the anodic sites while the oxidant is reduced at the cathodic areas. During the etching process, any given area on the surface continually alternates between being cathodic and anodic. When one spot is anodic more than it is cathodic, an etch groove may form. Conversely, rods are formed on areas that are cathodic more than they are anodic. Repeatedly, Si nanostructures develop.

3.1.4.2 Chemical vapor etching

Unlike stain etching and metal-assisted etching which occur in a solution, chemical vapor etching of Si involve the vapor of fluoride and oxidant which is directly contact with Si [83]. During the etching process, the Si substrate is held above the solution consisted of concentrated HF and HNO_3. By controlling the temperature and the exposure time, a thin layer of porous Si nanostructure can be formed. Saadoun et al [84] reported that a combination of hydrogen termination and oxidation of the surface accounted for the porous Si formation. The formation would be suppressed when vapor condensation occurs and droplets start to form on the surface.

3.1.4.3 Metal-assisted etching

The first demonstration of metal-assisted chemical etching of Si was reported by Dimova-Malinovska et al. [85]. Porous Si was fabricated by etching an aluminum coated Si substrate in a solution composed of HF, HNO_3 and H_2O. This method was further developed by Bohn et al [86]. In their work, it is reported that a thin layer of noble metal sputtered on the surface of a Si substrate promoted the etching Si in a solution composed of HF and H_2O_2, resulting in straight pores or columnar structures. Various approaches were developed to fabricate Si nanostructure based on this method thereafter. During a metal-assisted etching process, a Si substrate coated by a thin film of noble metal is subjected to an etchant consisted of HF and an oxidant. Specifically, the etching rate of Si beneath the noble metal is much faster than that of Si without noble metal coverage. As a result, the noble metal etches down the Si substrate, formatting pores or additionally Si nanowires. Various possible cathode and anode reactions have been proposed to describe the metal-assisted etching. While the chemical reactions at the cathode side were well

identified, the etching mechanism at the anode side was not fully understood and three major models were proposed for the dissolution process of Si.

For the cathode side, two reductions occur at the metal [87]:

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \quad [3.1]$$

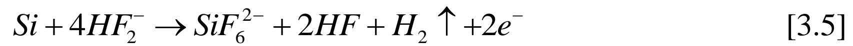
$$2H^+ \rightarrow H_2 \uparrow + 2h^+ \quad [3.2]$$

For the anode side, the first model attributes the Si etching to the direct dissolution of Si in tetravalent state [88, 89]:

$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+ \quad [3.3]$$

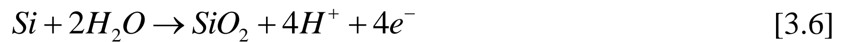
$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad [3.4]$$

The second model suggests a direct dissolution of Si in divalent state [90, 91]:



$$Si + 4HF_2^- \rightarrow SiF_6^{2-} + 2HF + H_2 \uparrow + 2e^- \quad [3.5]$$

The third model involves SiO_2 formation followed by oxide dissolution [92-95]:



$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \quad [3.6]$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad [3.7]$$

Whether SiO_2 is formed at the Si substrate surface before the dissolution of Si and whether H_2 is generated during the dissolution of Si are the major differences between the second and third model. In this work, the third model is used for explaining the mechanism as hydrogen is generated in a typical etching process.

3.2 SiNW synthesis on 2D Si substrate

The metal-assisted etching was chosen for SiNW synthesis in this study due to its advantages comparing to other fabrication methods. First of all, metal-assisted etching is a simple and low-cost method with the ability to control various etching parameters. In addition, although the metal-assisted etching is intrinsically anisotropic, the etching direction can be controlled t, enabling the fabrication of vertically aligned SiNW on (100) and non-(100) substrates. Unlike bottom-up approach such as VLS growth which can only grow SiNW with circular cross-sections at defined diameter, there is no obvious limitation on the size, diameter and aspect ratio of SiNWs fabricated by metal-assisted etching. The diameter of individual SiNW can be as small as 5 nm or as large as several μm, and the average height can be more than 50 μm. Therefore, metal-assisted etching is primarily utilized for SiNW synthesis on 2D substrate in this work.

3.2.1 Synthesis procedure

The fabrication of SiNW on 2D substrates was conducted on B-doped p-type (100) Si wafers in $AgNO_3$ and HF aqueous solution. The SiNW synthesis was based on a galvanostatic reaction between Ag^+ and Si^0. Due to the higher positive redox level of Ag/Ag^+, the deposited Ag^+ was reduced into Ag^0, and consequently, Si was oxidized into SiO_2, which was later dissolved by HF as shown in Equation [3.7].

The reactions selectively took place on the region where etching had already initiated. As a consequence of this selective growth of holes throughout the surface, the remaining structure became vertically aligned SiNW arrays. Fig.3.2 illustrated the sequence of the bulk silicon at the (100) surface gradually etched into an array of SiNW

along the <100> direction. The average height was about 20 μm, with a diameter of 50 nm, after 60 minute etching time. The surface cavity, formed in between bundled SiNWs, meanwhile increased as the etching time increased.

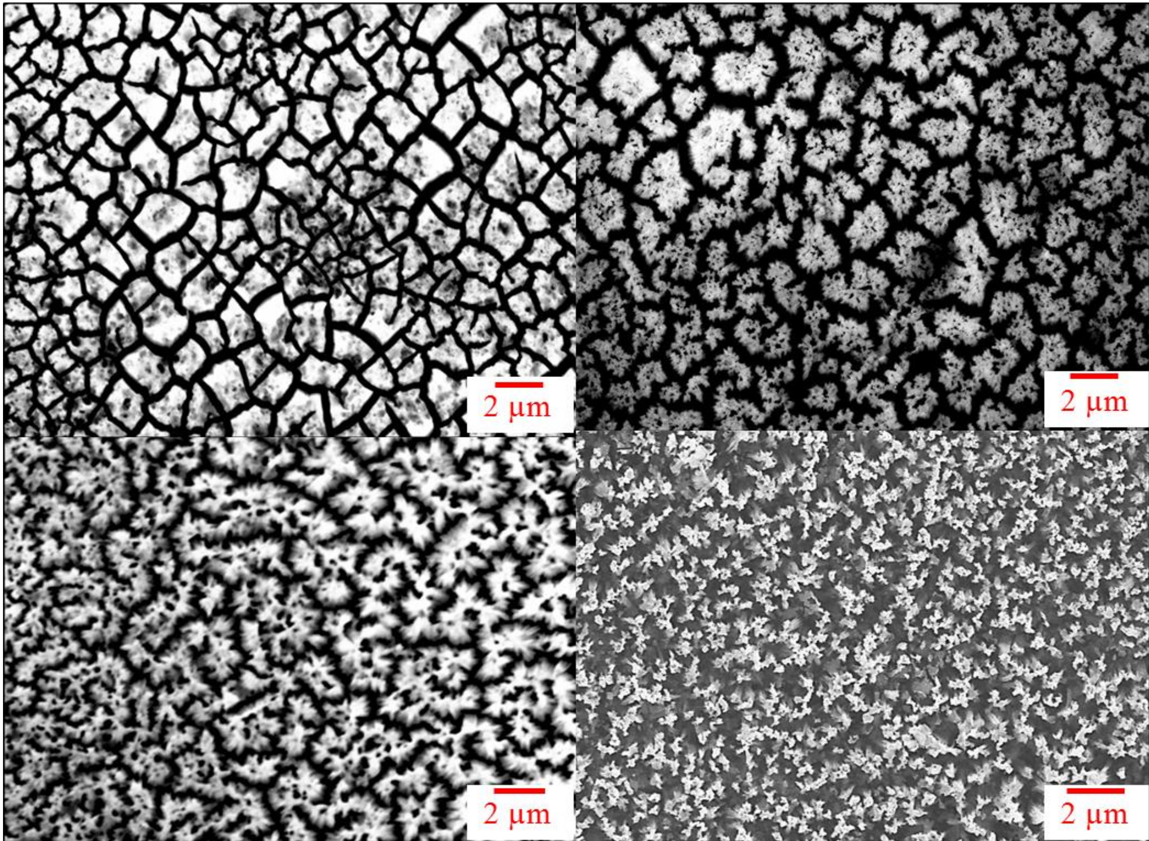


Figure 3.2 SEM images of the (100) surfaces in sequence during first step etching: (a) after 15 minute etching, (b) after 30 minute etching, (c) after 45 minute etching, and (d) after 60 minute etching.

3.2.2 Control of SiNW heights on Si substrate

By controlling the HF concentration and reaction temperature, SiNWs with heights of 35 and 20 μm were successfully fabricated on the Si substrates, as shown in Fig. 3.3(a) and (b). Table 3.1 showed the process conditions of temperature, HF concentration and time durations for the SiNW fabrication. The heights of Si nanowires increased approximately linearly with the etching time and temperature [42]. Because of

the bundling effect, the micro-scale cavities were observed; they increased in both number and size as the NW height increased.

Table 3.1: Etching conditions for SiNW synthesis

NW height	Solution	Duration and temperature
35 μm	10 M HF with 0.02 M $AgNO_3$	60 min at 50 ℃
20 μm	5 M HF with 0.02 M $AgNO_3$	60 min at 24 ℃

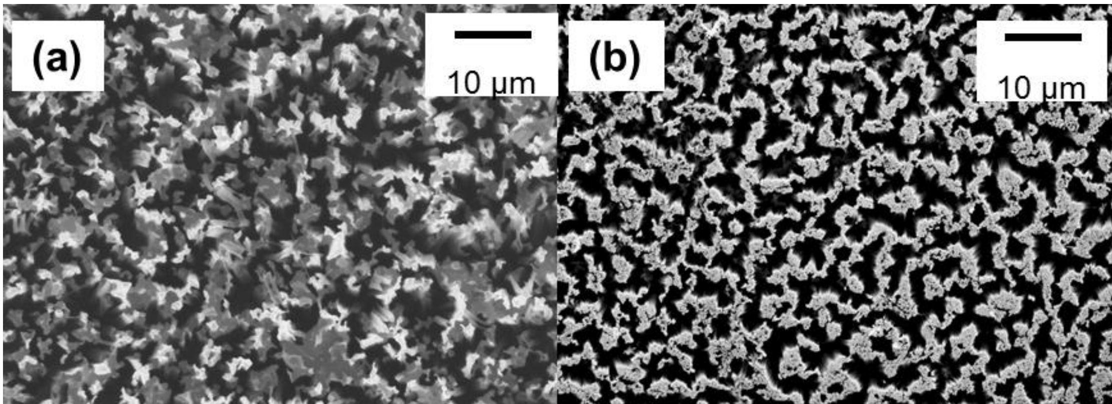


Figure 3.3 SEM images of SiNW with average heights of (a) 35 μm and (b) 20 μm

3.3 Surface wettability of SiNW coated flat surface

Similar to CuNW coated flat surface, the CA measurement results suggested that the SiNW surface is completely wetting, as shown in Fig. 3.4. As the contact angle of water on the plain Si surface is hydrophilic, the surfaces with nanowire structures become more hydrophilic. The hydrophilic surface is preferred in pool boiling as it can promote bubble nucleation and increase the CHF by preventing dry out. At the same time, the

availability of larger cavities with taller micro/ nanostructures allows the onset of nucleate boiling at lower wall superheats.

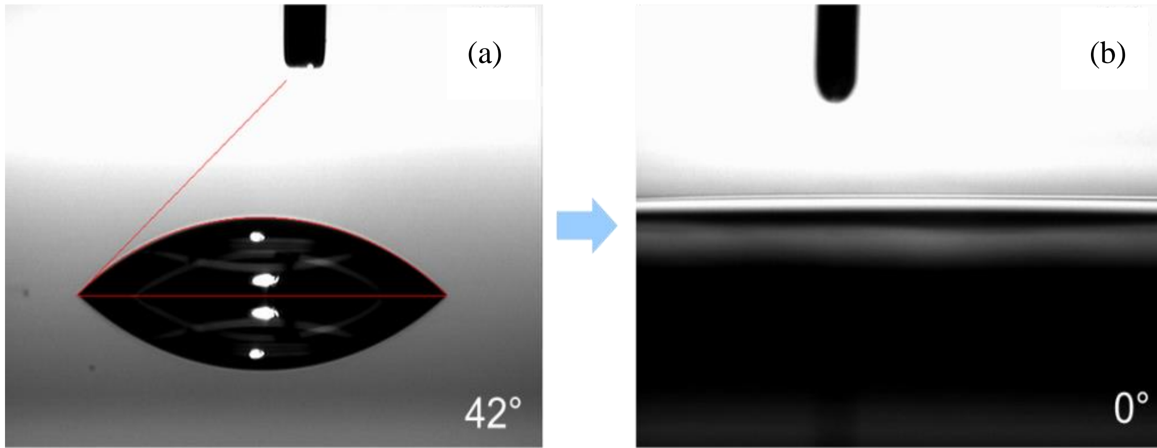


Figure 3.4 Contact angle measurements of (a) plain Si substrate and (b) SiNW surface

3.4 Comparison of SiNW and CuNW on 2D substrates

Due to the differences in their synthesis processes, the morphology of CuNW is slightly different from that of SiNW. CuNW arrays are more uniform in dimension as the array spacing and single pore diameter are constrained by the AAO template. However, the NW height varies along with the locations due to an unavoidable deposition rate variation, which could result from surface roughness, interfacial contact intimacy and so on. For SiNW structure, the dimension depends on the etchant concentration and reaction temperature. A higher $AgNO_3$ concentration and reaction temperature would result in more single NW arrays and less branch structures. In addition, as the etching is anisotropic along (100) orientation, no surface waviness is observed on the SiNW surface, the average height is more uniform than that of the CuNW.

3.5 SiNW fabrication on 3D Si substrates

3.5.1 Introduction to Microchannel

As continuous miniaturization of microelectronic components urgently demands an efficient cooling technique, utilizing microfabrication techniques to make microchannels as a heat sink for boiling heat transfer has proven to be an effective means of dissipating large amounts of heat from small surfaces [96, 97]. The microchannels provide a combination of small flow passage, large heat transfer area, and efficient boiling heat transfer. Such a combination can produce very high heat transfer coefficients with low space requirement. Although the technology to make microchannels at this scale is currently feasible, design considerations are intertwined and usually involve (i) geometric constraints (e.g. cross-section shape), (ii) surface properties of channel walls, and (iii) fabrication complexity. Heat sinks with simple rectangular, semi-circular, triangular, or trapezoidal channel shapes have been extensively studied [98-100].

The microchannel designs have been continuously evolving since the pioneering research on microchannel liquid cooling led by Tuckerman and Pease [96]. Kandlikar and Upadhye [101] investigated single-phase heat transfer in plain and offset strip fins and presented performance plots for optimizing heat transfer and pressure drop requirements. Li and Peterson [102] optimized microchannel spacing and channel dimensions by modifying the channel depth, channel width and fin width. The overall heat dissipation capacity of the microchannel was enhanced by more than 20% at a given condition. Gong et al [103] performed a parametric numerical study of heat transfer in microchannels with wavy walls and suggested a 55% improvement in heat transfer performance

compared to microchannels with straight walls. Kosar et al. [100] employed staggered pin fin geometries in rectangular microchannel heat sinks.

However, only a few studies have addressed the surface property of the microchannel interior walls, mainly due to the limitation of the microchannel fabrication [104] . While it is known that both topological and chemical properties of the surfaces play a critical role in determining the surface wettability, the recent advancement of hybrid micro/nano fabrications provide us a powerful tool to study and exploit many surface phenomena [105-108]. In particular, the nanoscale modification on surface topology has been increasingly of interest to improve heat transfer performance, due to (i) better durability, (ii) finer control over porosity and surface roughness, and (iii) thinner coating layers, which offer lower thermal resistance and thermal stresses [32-34, 37, 109]. Significantly higher pool-boiling heat fluxes have been found on nanostructure-coated substrates against bare substrates [37, 110].

With the individual advantages of using microchannel heat sinks and introducing NW on the surfaces, it is of great interest to combine the nanostructures onto the surfaces of microchannel heat sink for further enhancing the heat transfer performance. Dixit et al. [111] presented a multilayered water cooled microchannel heat sink where silicon (Si) nanopillars were grown on the bottom walls of the microchannels by utilizing the micro-masking effects in DRIE. The thermal performance of the heat sink was evaluated by developing a simple thermal resistance model and compared with a heat sink without the nanopillars. Their analysis showed 16% improvement in the nanopillar based microchannel heat sink. Li et al. [112] fabricated SiNW arrays on the bottom of Si microchannel and tested the flow boiling performance of the microchannel heat sink.

Earlier onset of nucleate boiling and delayed onset of flow oscillation, as well as enhanced HTC were observed, which suggested a significant performance enhancement. However, in these two experiments, only certain area (i.e. the bottom surface) of the microchannel was covered by the nanostructures, thus the mechanism and advantage of nanostructures on microchannel pool boiling was not fully utilized.

In the present study, a two-step etching process is developed to create uniform SiNW structures in rectangular silicon microchannel heat sinks, including the top, bottom and sidewall areas. The major motivation of this work is to understand the underlying mechanisms and influence of nanostructures on all surfaces of a microchannel chip during pool boiling.

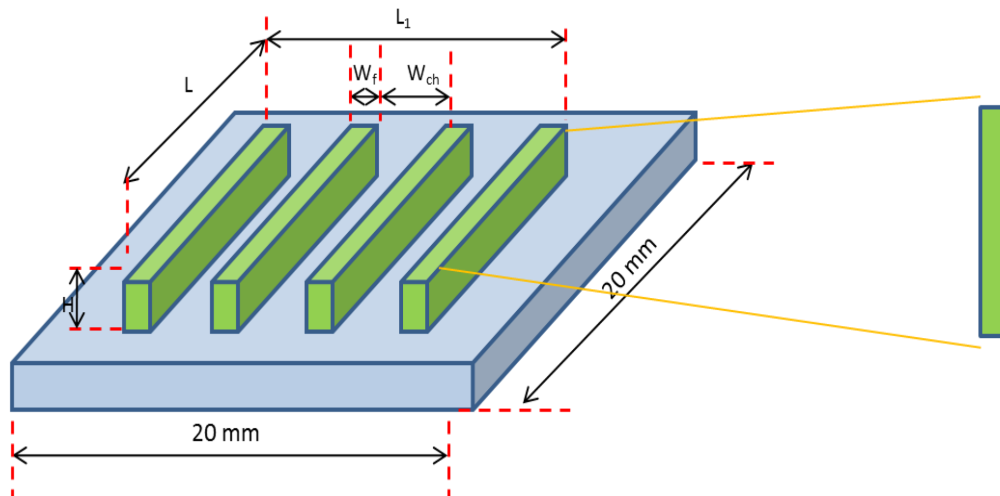


Figure 3.5 Dimension of the Microchannel design

In order to find the best combination of micro/nano structures, nine microchannel patterns with different widths of channel and fin were first fabricated and then coated with SiNW on the all surfaces exposed to pool boiling liquid. The boiling performances

of those microchannels with and without SiNW coating were compared. The channel configuration is shown in Fig. 3.5. The 10 × 10 mm^2 microchannel patterns were centered in the 20 × 20 mm^2 silicon chips. All microchannels possessed the same channel length (10 mm) and fin depth (100 μm). The fin pitches and channel width range from 100 to 300 μm on different microchannel surfaces, as listed in table 3.2. It is the first investigation to evaluate the pool boiling performance of water on the Si microchannels coated with SiNW structures on all surfaces, including the top, bottom and side walls.

Table 3.2: Summary of all sample dimensions

Sample #	**W_f (μm)**	**L(mm)**	**L_1 (mm)**	**# of W_f**	**W_{ch}(μm)**	**H(μm)**
Sample #1	100	10	9.9	50	100	100
Sample #2	100	10	10.0	34	200	100
Sample #3	100	10	9.7	25	300	100
Sample #4	200	10	10.1	34	100	100
Sample #5	200	10	9.8	25	200	100
Sample #6	200	10	9.7	20	300	100
Sample #7	300	10	9.9	25	100	100
Sample #8	300	10	9.8	20	200	100
Sample #9	300	10	9.9	17	300	100

3.6. Fabrication of SiNW on Si Microchannel surfaces

3.5.1 Si Microchannel Fabrication procedure

To create the silicon microchannel heat sinks, the process flow starts as shown in Fig.3.6(a), a (100) p-type silicon wafer (1-3 Ω-cm) was first cleaned with Piranha, containing H_2SO_4 (97%) and H_2O_2 (35%) at a 3:1 volume ratio, and HF solutions to remove organic residues and native oxide from substrates, then rinsed by deionized (DI) water. The wafer was dehydrated at 150 ℃. A 6-μm thick photoresist (SPR220, Megaposit) was spin-coated (WS-400BZ-6NPP, Laurell) on the silicon wafer then used as the masking material for the silicon etching process (Fig 3.6(a)-(b)) to define the microchannels.

After the wafer was soft baked, the wafer was photo lithographically patterned by using the mask aligner (EVG620, EV Group), developed in TMAH, and hard baked. The sample was anisotropically etched by using the inductively coupled plasma (ICP) machine (MESC Multiplex ICP, STS). The process consists of 13 second injection of 130 sccm SF_6 and 13 sccm O_2 in etching step and 7 second polymer deposition in C_4F_8 at 80 sccm in passivation step. The etching rate is about 5 μm/min. After the ICP process, the probe-type surface analyzer (ET4000A, Kosaka Laboratory Ltd) was employed to confirm the microchannel geometrical dimensions as designed. The wafer was then diced into 20×20 mm^2 chips by using the dicing saw (DS-150 II, Everprecision). The remaining photoresist was removed. Fifty 10 mm long parallel channels with 100 μm fin width and spacing were therefore created at the center of 20×20 mm^2 chips, as schematically shown in Fig. 3.7(a).

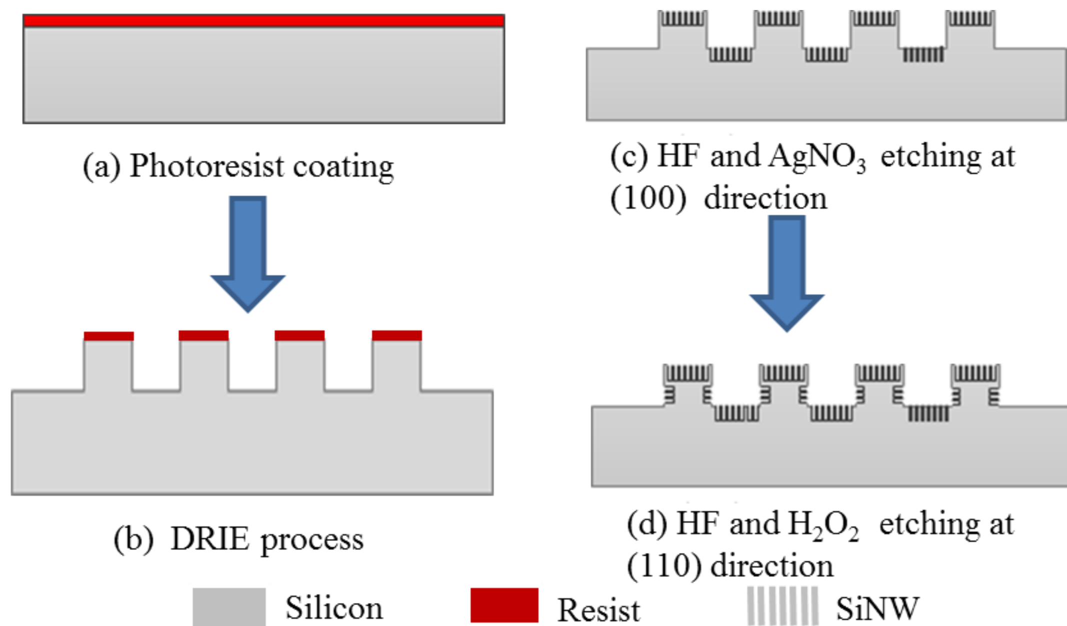


Figure 3.6 (a)-(b) Microchannel fabrication process flow and (c)-(d) SiNW synthesis

3.6.1 SiNW on (100) surfaces of microchannel

Different from a flat silicon surface with only one crystalline orientation, the silicon microchannels involve multiple crystalline directions. For example, the channel interior walls of a microchannel, made on a (100) silicon wafer, have the top and bottom surfaces in (100) direction while the sidewall surfaces in the (110) direction, as shown in Fig. 3.7(b). To create uniform SiNW on the all surface area of the microchannel, a two-step metal-assisted etching process targeted at two orthogonal crystalline directions have been developed as depicted in Fig. 3.6(c)-(d).

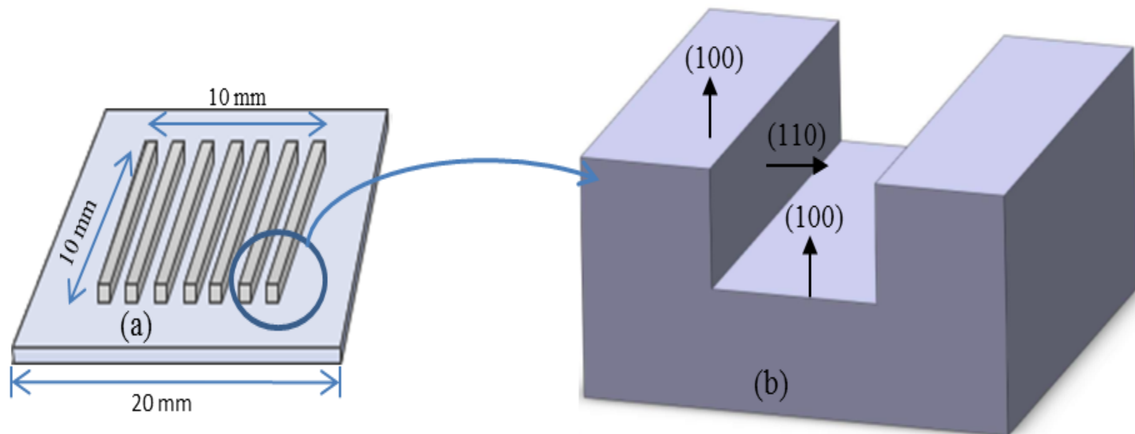


Figure 3.7 (a) Microchannel dimension, (b) internal channel size and silicon crystalline direction of the microchannel made on a p-type (100) wafer

To fabricate the SiNW in the microchannel interior surfaces, the first step is to initiate the SiNW formation on the (100) surfaces (Fig. 3.6(c)). The microchannel chips obtained from the previous step were cleaned by using Piranha solution then 5% HF solution to remove the organics and native oxide layer. Once cleaned, the chips were immediately immersed into the etching solution consisted of 4.8 M HF and 0.02 M $AgNO_3$ at room temperature for SiNW synthesis at the <100> direction.

These reactions selectively took place on the region where etching had already initiated. As a consequence of this selective growth of holes throughout the surface, the remaining structure became vertically aligned SiNW arrays. Figure 3 illustrated the sequence of the bulk silicon at the (100) surface gradually etched into an array of SiNW along the <100> direction. The average height was about 15 ~ 20 μm, with a diameter of 50 nm, after 60 minute etching time. The surface cavity, formed in between bundled SiNWs, meanwhile increased as the etching time increased.

At this stage, the formation of SiNW occurs on the top and bottom surfaces of the microchannels at the (100) planes because the charge transfer preferentially occurred at the interface between the silicon and deposited Ag nanoparticles. As evident in Fig. 3.10(a), the sidewall surfaces were barely affected because no Ag particles were deposited. In addition, since the oxidation and dissolution of silicon atoms on a substrate surface were required to break the back-bonds between the atoms on and underneath the surfaces, removing atoms from the surface proved difficult. As the number of back-bonds of a silicon atom on the surface was determined by the crystallographic orientation of the substrate, the etching rates were different on different surfaces. On the (100) surface, each atom has two back-bonds, while on the (110) or (111) surface, an atom has three back-bonds [113]. Due to the different bonding strength, the atom on the (100) surface was the most easily removed, with etching occurring preferentially along the <100> direction, thereby resulting the SiNW formation only on the top and bottom surfaces. The SiNW density and height was controlled by the HF concentration, reaction temperature and etching time [113].

3.6.2 SiNW fabrication on (110) surfaces of microchannel

Recent studies on microchannel heat sinks suggest that sidewall structures play considerable roles on laminar flow and heat transfer [114, 115]. To study the effect of sidewall SiNW structure on microchannel pool boiling heat transfer, method for SiNW fabrication on sidewall surface was developed and discussed in this chapter.

3.6.2.1 Etching direction on Si substrate

In early experiments [116-118] it was speculated that the metal-assisted etching is isotropic and the noble metal always catalyzes the etching along the vertical direction relative to the substrate surface. However, it was later revealed that slanting, aligned Si nanostructures can be fabricated by non-vertical etching on (111) and (110) substrates [119, 120]. The non-vertical etching was ascribed to the back-bond theory, which was used to explain the anisotropy in the (110) surface etching in the previous chapter. For the oxidation or dissolution of a Si atom of a substrate, it is necessary to break the back-bonds of the surface atom that connects to the underneath atoms. The stronger the back-bond strength, the more difficult to remove the surface atom. The number of back-bonds of a Si atom on the surface is determined by the crystallographic orientation of the substrate. Each atom on the (100) surface has two back-bonds, while the atom on the (110) or (111) surface has three back-bonds [121]. Due to the different back-bond strength, the Si atom on the (100) surface plane is the easiest to remove, and the etching occurs preferentially along the <100> directions. However, the etching direction preference could be altered by varying the concentration of oxidant in the etchant [122]. The back-bond theory implies that the anisotropy could be reduced or eliminated if the back-bond strength is weakened. A study of Si etching in alkaline solution revealed that the addition of oxidant into the alkaline etchant could reduce the anisotropy [123]. It was speculated that the dangling bonds of the surface Si atoms varied from –H in alkaline solution to –OH with the addition of oxidant, and the –OH surface bond effectively reduced the strength of the back bond, accordingly reduced the anisotropy, enabling a reduction of the hillock structures which are a characteristic of (100) Si substrates. These

results suggest an approach to alter the etching direction preference by addition of an oxidant.

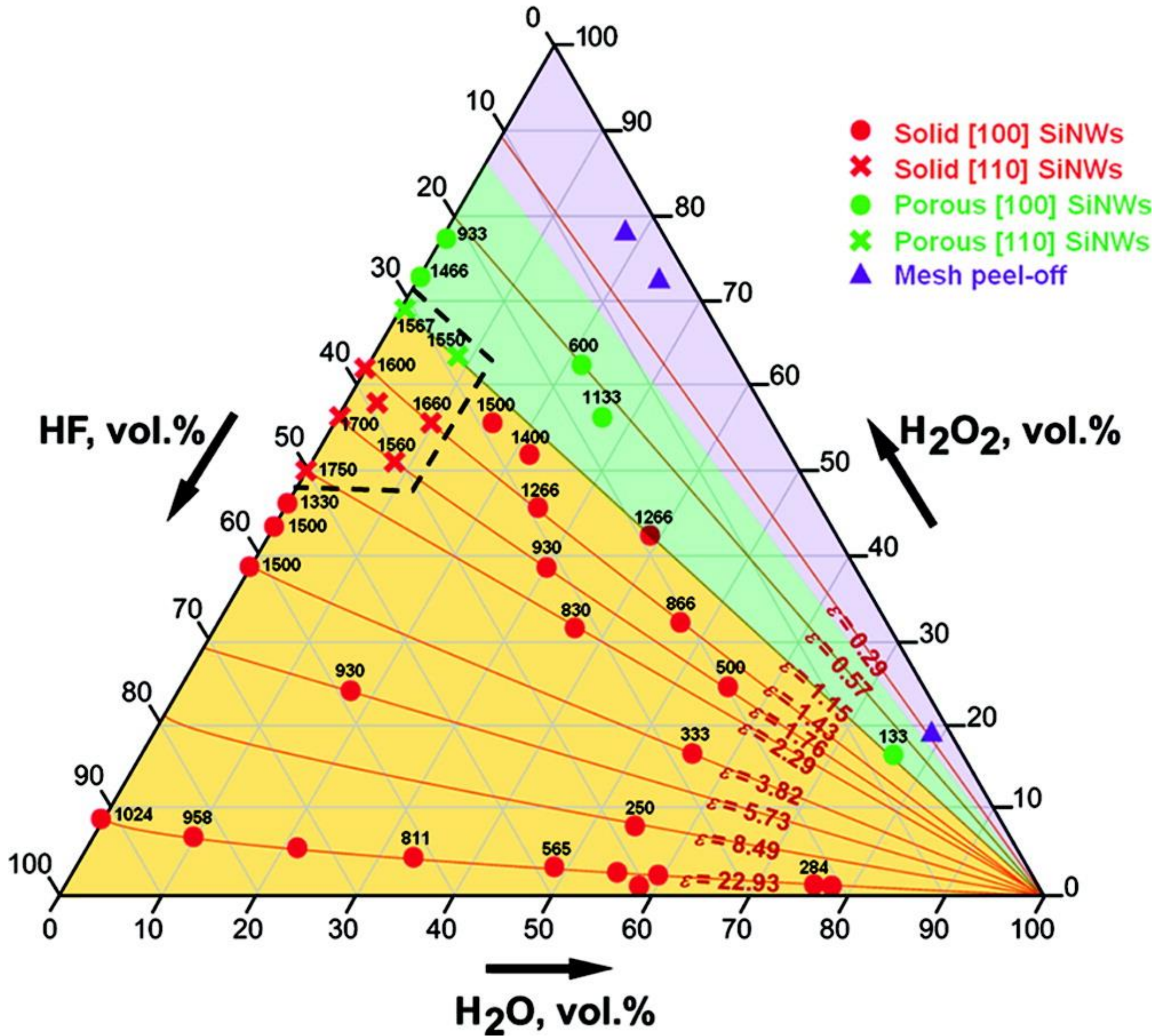


Figure 3.8 [122] The evolution of etching rate (nm/min), nanowire axial orientation, and morphology during metal-assisted etching of Si (100) wafers in ternary mixtures of 46 wt % HF, 35 wt % H_2O_2 and H_2O at room temperature. The numbers on symbols are the measured etch rates in nm/min. Circle and cross symbols denote experimentally determined axial orientations of SiNWs. Triangle symbols represent the peeling-off metal mesh from the Si surfaces. The background areas colored with pale yellow, green, and purple represent the projected etchant conditions, yielding solid nonporous SiNWs, porous SiNWs, and peeling off, respectively

Kim et al [122] developed a diagram (Fig. 3.9) to show the evolution of etching rate, etching direction, and morphology of SiNWs during metal-assisted etching of Si (100) wafers in ternary mixtures of HF, H_2O_2 and H_2O at room temperature. Each red

line in the present ternary diagram represents the solution composition of the same molar ratio of HF to H_2O_2. Although the diagram suggested that there is no obvious correlation between the etching direction and the concentration ratio of HF to H_2O_2, as the etching along slanted <110> directions occurs only within a narrow window of solution composition, it does show that etching direction is primarily controlled by the etching rate, that is, etching occurs along vertical <100> direction at low etching rate, while occurring along <110> directions at high etching rates.

3.6.2.2 Etching towards <110> direction on Si microchannel

Based on those studies, an additional etching step of microchannel was developed to fabricate uniform SiNW structure on the sidewall area without affecting the existed NWs on the top/bottom surface. Because etching of Si atoms is a net consequence of injection of a positive hole (h^+) into bulk silicon and removal of oxidized silicon by HF from underneath the Ag nanoparticles, the etching rate is governed by the interplay between the two processes.

Since the amount of holes (h^+) injected into silicon can be controlled by the H_2O_2 concentration and decomposition activity, the process of catalytic decomposition of H_2O_2 will determine the etching rate at different planes. Basically, at low H_2O_2 concentration, the hole (h^+) injection into silicon atoms will locally occur at the (100) plane, as the (100) plane has the fewest back-bonds to break, resulting in etching along the <100> direction. When the H_2O_2 concentration increases with the amount of generated holes (h^+) exceeding the threshold, silicon atoms will be rapidly removed in the crystal planes where there will be more silicon back-bonds to polarize (such as (110) and (111) planes). This will result in different SiNW etching behaviors – a faster etching rate in <110>

direction than <100> direction [122]. Therefore, a solution containing HF and H_2O_2 was prepared to form [110] SiNW. The silicon microchannel chips, which have [100] SiNW on the top and bottom surfaces, after the first etching step, were immersed in the etching solution for sufficient time.

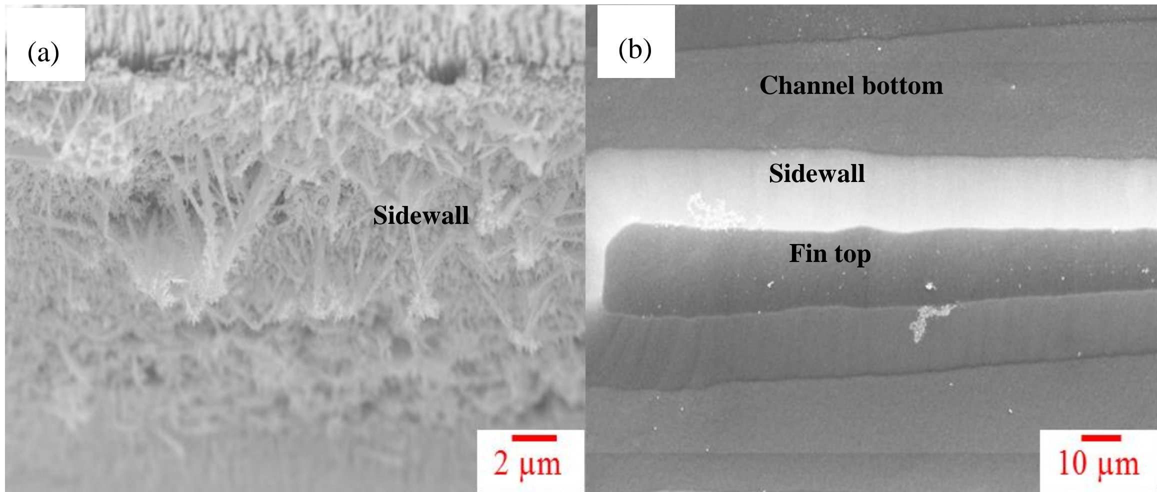


Figure 3.9 SEM images of (a) SiNWs starting to form on the microchannel sidewall after a 30-minute etching by H_2O_2:HF solution in a 1:5 molar ratio and (b) smooth fin surface after 60 minute etching by H_2O_2 :HF solution in a 2:1 molar ratio

To obtain uniform SiNW structures on the sidewall, different recipes, as listed in Table 3.3, were investigated. It is found that the sidewall morphology was greatly affected by the H_2O_2 concentration at a given concentration of HF. The SiNW structure, as shown in Fig.3.9, started to form at certain locations of the sidewalls when the molar ratio of H_2O_2 : HF is larger than 1:5. The ideal molar ratio for creating uniform sidewall SiNWs was between 1:5 to 2:1, because H_2O_2 at higher concentrations may completely etch off the SiNW structure, leaving smooth fin and channel surfaces, as shown in Figure 4(b). In this work, the solution was prepared at 4.8 M HF and 2.4 M H_2O_2; the etching duration was controlled within 30 minutes at room temperature. Longer etching duration was not preferable since it may result in significant reduction of the microchannel fin

width. The formation of NW at the sidewall is directly related to the etching time, as shown in Fig. 3.10.

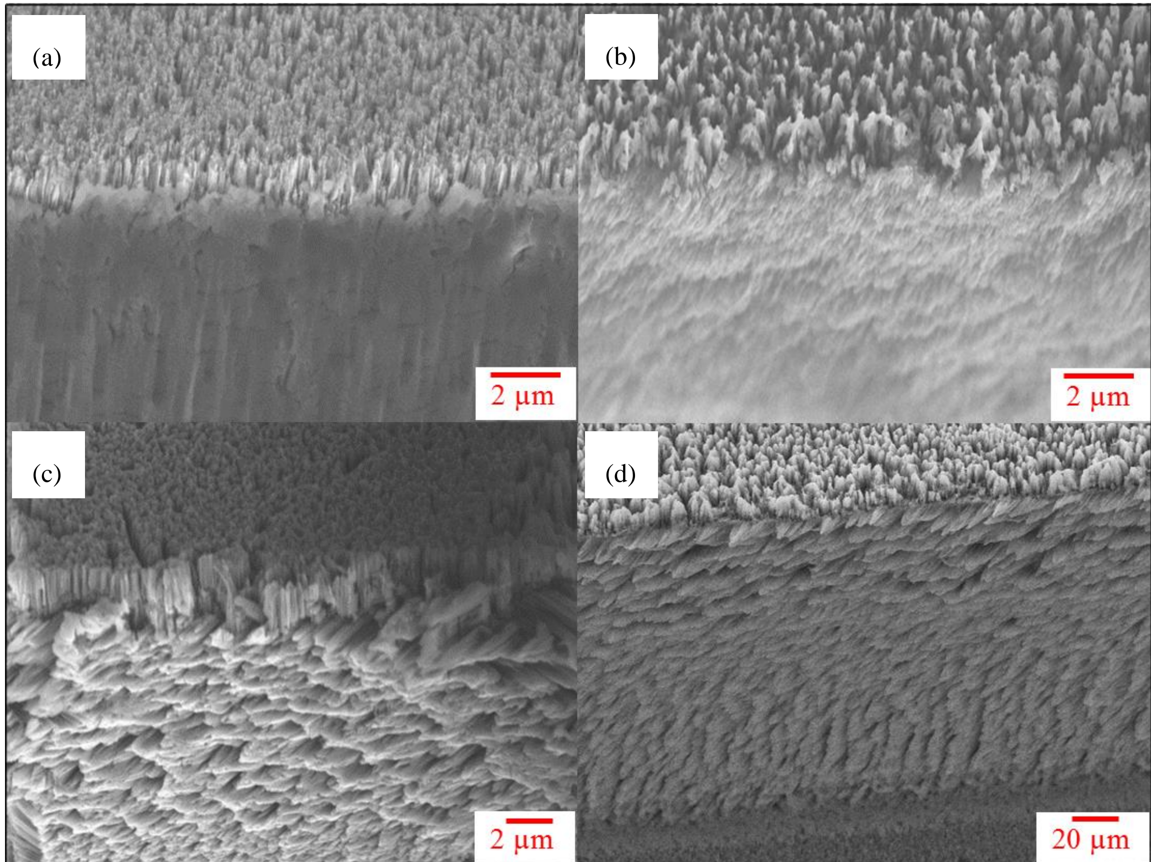


Figure 3.10 SEM images of the top (100) surface and sidewall (110) surfaces during the second SiNW etching step in sequence: (a) before etching, (b) after 15 minute etching, (c) after 30 minute etching, and (d) after entire etching

After this second etching step, the chips were cleaned with DI water then placed in dilute HNO_3 solution to dissolve the Ag catalyst. [110] SiNWs were then revealed in the microchannel sidewalls. The chips again were washed with HF again to remove the oxide layer then cleaned with DI water and dried.

The average height of the as-grown [110] SiNW was between 10~15 μm. The SiNWs were slightly inclined to the (110) surfaces and shorter than SiNWs grown on the (100) surfaces due to the shorter etching duration. After the two-step etching process,

uniform SiNWs were created on the entire surface area of the microchannels, including top, bottom and sidewall surfaces, as shown in Fig. 3.10(d).

Table 3.3: Effects of H_2O_2 concentration on sidewall morphology at 2nd step etching

Molar ratio of H_2O_2:HF	**Etching time and temperature**	**Sidewall structure**
1:5 (0.96 M H_2O_2 +4.8 M HF)	30 minutes of etching at room temperature (20 ℃)	Non-uniform nanowire structure formed at certain areas of the sidewall (Fig.6.4(a))
1:2 (2.4 M H_2O_2 + 4.8 M HF)	30 minutes of etching at room temperature (20 ℃)	Uniform nanowire structure formed on the entire sidewall surface (Fig.6.5(c))
2:1 (9.6 M H_2O_2 + 4.8 M HF)	60 minutes of etching at room temperature (20 ℃)	Entire surface etched off, no nanowire structure found at any location (Fig. 6.4(b))

The successful SiNW fabrication on the designated areas of the microchannel interior walls indicated that the metal-assisted electroless etching was capable of creating uniform SiNW on silicon-based three-dimensional geometry by applying different etching conditions for different crystalline directions. This two-step SiNW fabrication technique makes itself more advantageous than other approaches of creating nanostructures on geometrical confined surfaces because of its simplicity, controllability, and low-cost. In addition, when incorporated with microchannels, this SiNW fabrication can further expand onto the applications of nanostructure in advanced heat and mass transfer devices, not limited to the flat substrates.

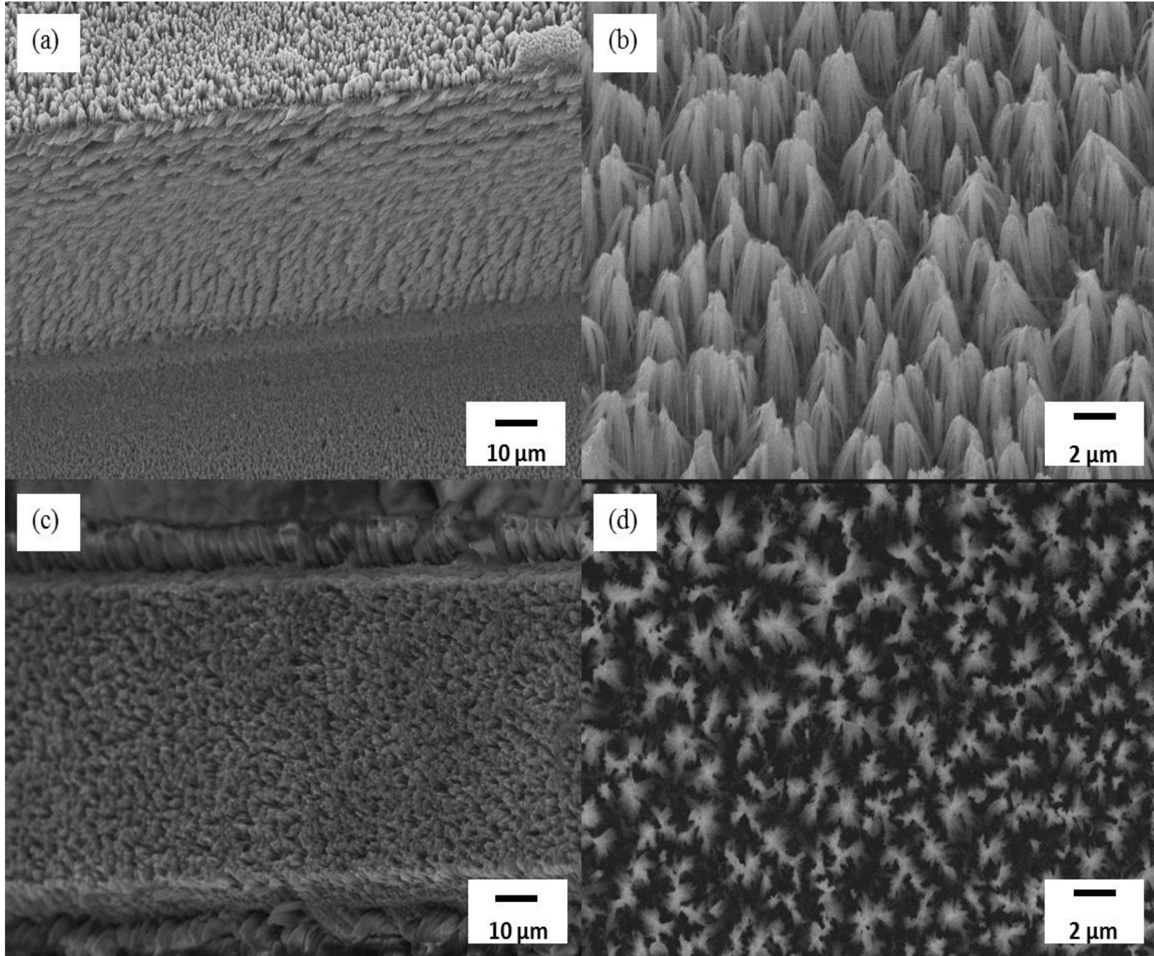


Figure 3.11 SEM images of the microchannel surface with SiNW: (a) sidewall area, (b) top area, (c) fin area, and (d) bottom area

Table 3.4: Recipe of SiNW synthesis process adapted in this study for boiling tests

Etching Process				
Formulation	**Temperature**	**Duration**	**Etching Rate**	**Targeted Surface**
1st step etching: 100 mL aqueous solution of 4.8 M HF and 0.02 M $AgNO_3$	Room temperature (21 ℃)	60 minutes	0.3 µm/min (approximately)	(100) surfaces: top and bottom areas of microchannel
2nd step etching: 100 mL aqueous solution of 4.8 M HF and 2.4 M H_2O_2	Room temperature (21 ℃)	30 minutes	0.5 µm/min (approximately)	(110) surfaces: sidewall area of microchannel

Finally, the two-step etching process adapted in this study for the following boiling test was listed in Table 3.4. The etching rates at different steps were calculated based upon the final SiNW height and the overall etching duration.

3.7 Surface wettability of Microchannel surfaces

By improving the surface hydrophilicity, SiNW improve surface wettability and enhance the CHF due to delayed dryout. The surface wettability of the micro/nano hierarchical structures was quantified by the static contact angle measurements of water droplets on the test surfaces.

Table 3.5: Contact angle (CA) measurement results

Sample No.	CA of microchannel without SiNW		CA of microchannel with SiNW (X-directions)
	X-direction	Y-direction	
1	137°	109°	0°
2	139°	124°	0°
3	156°	133°	0°
4	135°	113°	0°
5	142°	122°	0°
6	149°	131°	0°
7	134°	101°	0°
8	141°	120°	0°
9	150°	128°	0°

Table 3.5 presents the results of measurement of the contact angles for the microchannel samples. All samples were cleaned by Piranha solution and nitrogen dried prior to measurement. Due to the geometry of the microchannel, the contact angles were examined from both X direction (referring to Fig. 3.5, along the channel direction) and Y direction (referring to Fig. 3.5, across the channel direction) for microchannel-only samples (no SiNW). Depending on the channel width and fin width, the contact angles on the microchannel-only samples ranged from 134 ° ~ 156 ° in the X direction and 100 ° ~ 130 ° in the Y direction. For all SiNW samples, the micro/nano hierarchical structures

enhanced the surface wettability. The droplet spreads through and across the microchannels, showing a completely-wetting behavior. Fig. 3.12 shows the contact angle of the samples with different fin widths (left column), and a comparison with the same sample coated with the SiNW (right column).

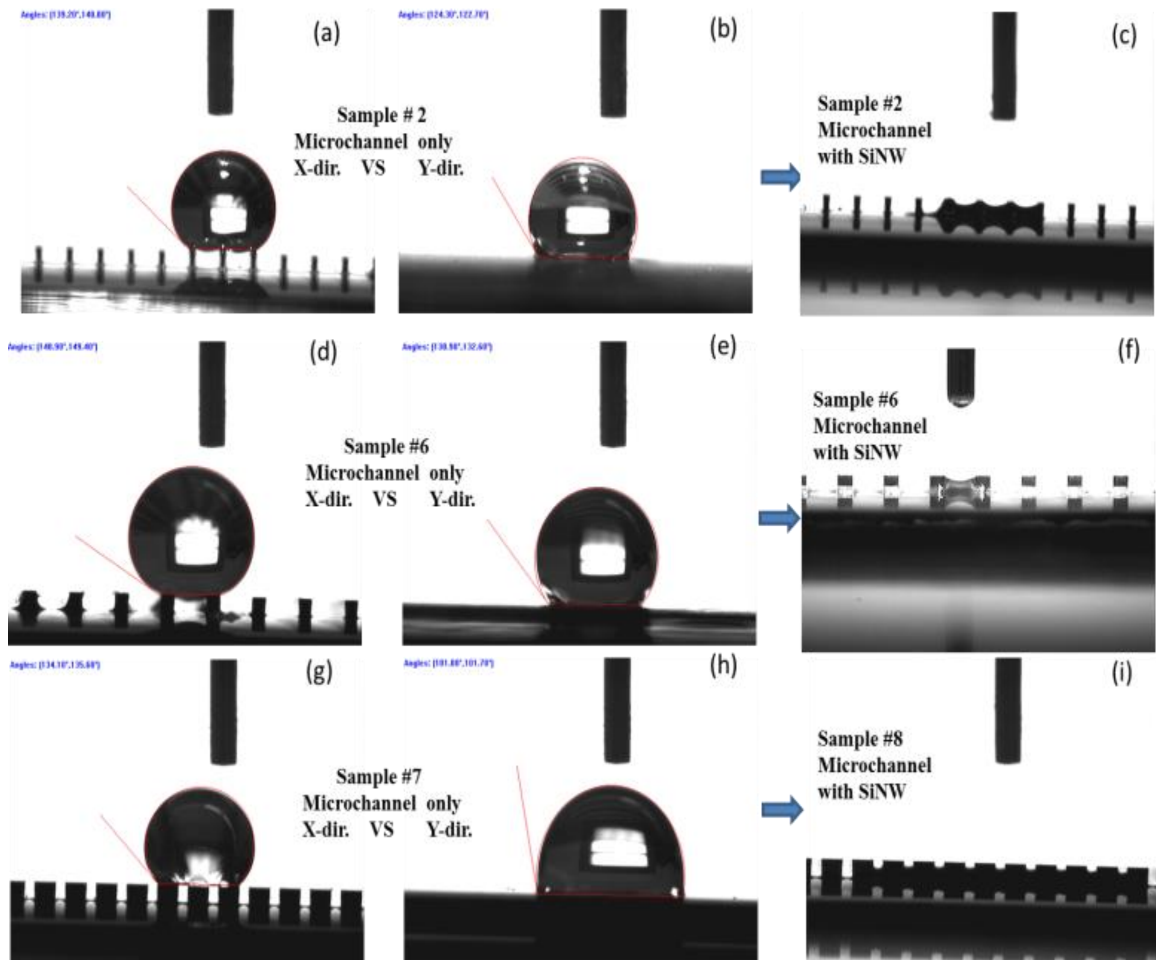


Figure 3.12 Contact angles of (a-b) sample #2 (100 μm fin width) at X and Y directions, (c) sample #2 with SiNW, (d-e) sample #6 (200 μm fin width) at X and Y direction, (f) sample #6 with SiNW, (g-h) sample #7 (300 μm fin width) at X and Y direction, and (i) sample #7 with SiNW

The surface hydrophilicity may attribute to the capillary wicking induced by the micro/nano hierarchical structures [40]. The capillary wicking supplied fresh liquid to

the dry region beneath the vapor bubbles during boiling, which delayed the irreversible growth of hot spots and CHF. As the whole surface area of SiNW sample is superhydrophilic, water can easily re-wet the bottom of the channel and fin areas after bubble departure, leaving neither local hot spot nor dryout area. In contrast, the bubbles that remained or grew on the microchannel only samples may result in local hot spots on the sidewall and top of the fin area during nucleate boiling stage.

CHAPTER 4

POOL BOILING SETUP AND TESTING METHODLOGY

An experimental setup was designed and built to allow testing of different plain and surface with NW structures. Detailed descriptions of the boiling setup, data acquisition system and testing calibration were presented in this chapter.

4.1 Boiling setup

To study the pool boiling performance of the NW coated substrates, an experimental setup shown in Fig. 4.1 was employed [36]. The test section consists of the testing samples, with a water reservoir above it and a copper block underneath. The copper block is heated by a cartridge heater, while the water reservoir has an auxiliary heater to maintain the working liquid at the saturation temperature.

To apply a heat flux, a 450 W capacity cartridge heater was inserted into the copper block served as the main heating element. The copper block was machined to have a 10 mm × 10 mm tip with 25 mm in height. Three K-type thermocouples were placed along the axis of the copper block to measure the temperature gradient at the top of the heater block with 8 mm spacing and the first one (T_1) was 3 mm below the copper block surface. At the top of the water reservoir, a 100 W auxiliary heater was used to maintain the water at the saturation temperature. The temperature of water was monitored by a K-type thermocouple (T_4). An NI-cDaq-9172 data acquisition system was used to record the temperatures during testing. A Labview virtual instrument (VI) was created to

display temperatures, determine when the system was at steady-state, and record the datea. (See Appendix A for the block diagram and the front panel of the Labview program.)

In order to study the bubble dynamics during the boiling process, a Keyence high speed digital camera (Fig. 4.1(j)) was used to take image of the boiling phenomena at an angle of 15 deg. The camera was inclined at this angle so that nucleation at the heated surface could be clearly viewed. The high speed color camera has frame rates capable of 24,000 frames per second. In order to keep resolution satisfactory, slower frame rates of 1000 fps were employed at resolution of 256 × 256.

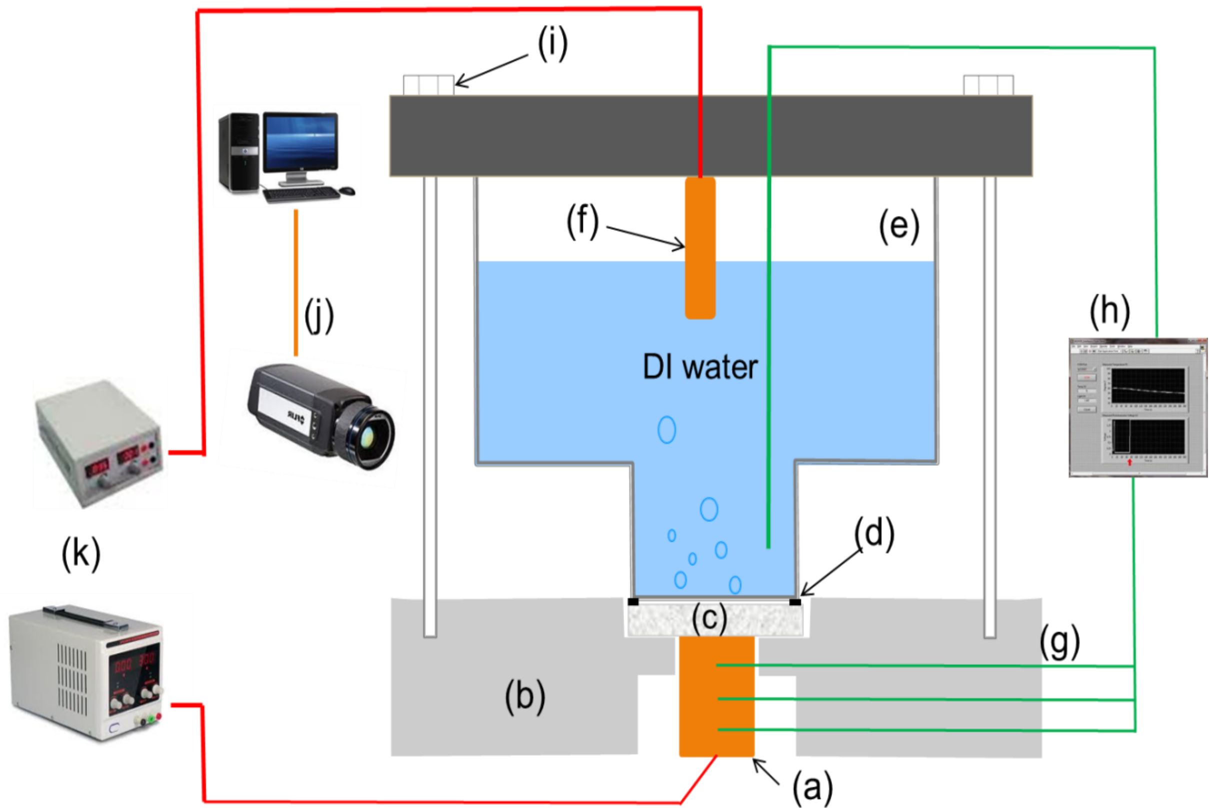


Figure 4.1 Schematic of boiling test fixture (a) Cartridge heater, (b) Ceramic block, (c) Testing chip, (d) Gasket, (e) Polycarbonate visualization tube, (f) Auxiliary heater, (g) K-type thermocouples, (h) Data acquisition system, (i) Compression screws, (j) High speed camera, and (k) Power supply

For the tests, a layer of conductive, polysynthetic silver thermal paste was used to decrease the contact resistance between the copper block and silicon chip. Screws with springs underneath the caps were placed on both sides of the chip, and were compressed, so the force applied between the chip and the copper block for each test was consistent. Contact resistance was quantified, as discussed in the following section.

During the tests, fresh distilled water was used as the boiling liquid. Water is chosen because of its well-known fluid properties and minimal handling risk. Sufficient time was given to remove dissolved air by vigorously boiling the water before commencing the test by using the 100W auxiliary heater, which was also used to maintain the water temperature in the reservoir at saturation condition. A venting hole was provided on top of the water tank to maintain the pressure and vent vapors. After water was kept in saturation temperature for 30 min, the main heater was started and the power was increased in small increments. Periodically, water is added to the pool to compensate the evaporated water vapor. Data collection continues after the water reaches steady-state again.

4.2 Data acquisition

To evaluate the boiling data, the heat flux was first calculated from the following equation:

$$q'' = -k_{cu} \frac{dT}{dx} \qquad [4.1]$$

The temperature gradient, *dT/dx*, was calculated using a three-point backward-difference Taylor series approximation as given below,

$$\frac{dT}{dx} = \frac{3T_1 - 4T_2 + T_3}{2\Delta x} \qquad [4.2]$$

where T_1, T_2 and T_3 are the temperatures measured by thermocouples located at distances Δx= 8 mm apart. The surface temperature of the microchannel, T_s, was obtained by calculating the heat flux through the copper block, as well as the reading from thermocouple T_1, from the following equation,

$$T_s = T_1 - q''(\frac{L_{Cu}}{k_{Cu}} + R''_{t,c} + \frac{L_{Si}}{k_{Si}}) \qquad [4.3]$$

where L and k represent material thickness and thermal conductivity, respectively. $R''_{t,c}$ represents the thermal contact resistance of the interface, which is found to be 5×10^{-6} $m^2 \cdot K/W$, with an uncertainty less than 4%, as reported in an earlier publication [36]. The wall superheat ΔT_{sat} is obtained by

$$\Delta T_{sat} = T_s - T_{sat} \qquad [4.4]$$

For boiling with water at atmosphere pressures, the saturation temperature T_{sat} = 100 ℃. Corrections were applied to the saturation temperature based on the local atmospheric pressure readings.

4.3 Sample preparation

As 3 different substrates were used in the boiling tests, the samples are prepared in different manners. For CuNW coated on copper substrate, the surface was polished to maintain low surface roughness prior to CuNW deposition. The copper chip was machined to be 20 mm $\times$ 20 mm with a thickness of 3 mm. Specifically, in order to keep

the heater transfer through the block one dimensional, preventing any two dimensional or fin effects from the highly conductive copper, a square channel 1 mm wide cut around the area of the heater was made on the copper substrate.

The flat Si substrate was also cut into 20mm $\times$ 20mm Si chips by wafer saw before SiNW synthesis. Prior to boiling test, the SiNW samples were immersed in HNO_3 (1:1 v/v) to remove the Ag catalyst followed by an Acetone clean to remove possible contamination. No other treatment is needed since the thickness is only 400 μm.

Similar process was also carried out on Si microchannel substrates before pool boiling tests. The HNO_3 immersion was also conducted after 2nd step etching.

4.4 Contact resistance

Thermal contact resistance was a factor in the test setup. Due to small asperities between the copper heating block and the silicon chip, a layer of thermal paste was applied to decrease the contact resistance. To ensure that the pressure between the surfaces was constant for each test run, compression screws with sprints were used to provide the same amount of force between the test chip and the heat block.

A test piece was fabricated out of copper in order to help measure the contact resistance of the setup as shown in Fig.4.2 (a). This block was machined to have the same outer dimensions as the rest of the test chips, but had a square channel 1-mm wide cut around the area of the heater. This was done in order to keep the heat transfer through the block one dimensional, reducing any two dimensional or fin effects from the highly conductive copper. A thermocouple hole was machined into the center of the chip to

measure the temperature in the chip, so that the contact resistance could be back calculated.

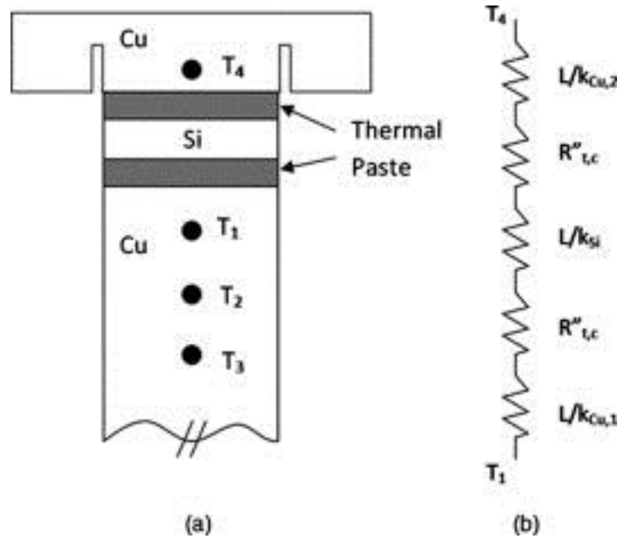


Figure 4.2 (a) Schematic of copper chip setup for contact resistance calculations and (b) equivalent thermal circuit for 1D heat conduction analysis [35]

Sandwiched between the copper chip and the copper block is a silicon chip of the same area as the heater. This layer helps to provide the same conditions for the contact as in actual testing: a copper-thermal paste-silicon combination. Inserting two layers of thermal paste (one on each side of the silicon) allows for a more accurate measurement of the contact resistance because it is averaged between the two sides. A schematic of the contact resistance test setup and the equivalent thermal circuit are shown in Fig. 4.2.

The contact resistance was found to be repeatedly 5×10^{-6} m^2K/w, with an uncertainty of less than 4%. Using this contact resistance, the surface temperature of a test chip can be calculated using the heat flux through the copper block, as well as the thermocouple T_1 from the following relation:

$$R''_{t,c} = \frac{1}{2}\left(\frac{T_1 - T_4}{q''} - \frac{L}{K}\bigg|_{Cu,1} - \frac{L}{K}\bigg|_{Si} - \frac{L}{K}\bigg|_{Cu,2} \right) \quad [4.5]$$

Tests were run, recording temperatures from thermocouples T_1 and T_4, while also recording the heat flux. The contact resistance was then calculated as follows:

$$T_s = T_1 - q''\left(\frac{L_{Cu}}{K_{Cu}} + R''_{t,c} + \frac{L_{Si}}{K_{Si}} \right) \quad [4.6]$$

4.5 Uncertainty analysis

The uncertainty analysis was conducted according to the method proposed by Kline and McClintock [124]. The major uncertainties originated from the following aspects: 1) thermocouple calibration accuracy and precision resolution; 2) thermal conductivity of materials being altered due to temperature changes and 3) actual size of the boiling area due to gasket cover, measurement of spacing between thermocouples, and thickness of materials. Multiple parameters can lead to propagation of uncertainty. The method used to find the error propagation is through partial sums in Equation [4.7], where p is the calculated parameter, a_i is a measured parameter, and U denotes the uncertainty of the subscripted parameter.

$$U_p = \pm\sqrt{\sum_{i=1}^{n}\left(\frac{\partial p}{\partial a_i} u_{a_i} \right)^2} \quad [4.7]$$

The uncertainties in multimeters to measure voltage and current are 0.8%. The uncertainty for the heat flux can be derived from Equation [4.1] and [4.2] by using the

partial sums described in Equation [4.7]. Dividing by the heat flux value yields the uncertainty as a percentage of the calculated value, which is shown as follows:

$$\frac{U_{q''}}{q''} = \pm\sqrt{\left(\frac{U_k}{h}\right)^2 + \left(\frac{3U_{T_1}\cdot k_{Si}}{\Delta x\cdot q''}\right)^2 + \left(\frac{4U_{T_2}\cdot k_{Si}}{\Delta x\cdot q''}\right)^2 + \left(\frac{U_{T_3}\cdot k_{Si}}{\Delta x\cdot q''}\right)^2 + \left(\frac{U_{\Delta x}}{\Delta x}\right)^2} \quad [4.8]$$

The uncertainty of surface temperature is obtained in the same manner using the partial sums from Equation [4.3]. Table 4.1 shows the uncertainty sources and values. At low heat fluxes the uncertainty value comprises 20% of the calculated value, while at the high heat fluxes it is only slightly more than 4%. This is considered to be acceptable because the sample performance is evaluated mainly at elevated heat fluxes.

Table 4.1: Uncertainty sources and values

Source	Uncertainty
T-type thermocouple reading	±0.25 K
Thermal conductivity of Cu	±2%
Thermal conductivity of Si	±3.7%
Surface temperature reading	±4.5%
Thermal contact resistance	±4%
heat flux	±2 kW/cm^2 at lowest heat flux, ±6 kW/cm^2 at highest heat flux

CHAPTER 5

POOL BOILING RESULTS

A serial of pool boiling tests on substrates with and without NW structures were conducted and the results were presented in this chapter in the manner of metallic NW → metallic NW and semiconductor NW with different height → semiconductor NW on 3D substrates. The first testing was carried out on flat copper surface coated with CuNW, the results were compared with flat copper surface. Followed is the testing of SiNW and CuNW grown on Si substrates. A comparison of SiNW and CuNW with different height was made based on the pool boiling performance. For boiling tests on 3D substrates, 9 Si microchannel heat sinks with different geometry were examined and compared with the same samples coated with SiNW. In addition, to study the effect of NW grown on the microchannel sidewall on pool boiling enhancement, samples with SiNW only on top/bottom and samples with SiNW on whole surface area were also compared in pool boiling performances.

5.1 Pool boiling test of CuNW on 2D copper substrates

The pool boiling was conducted on 20 mm $\times$ 20 mm copper chips using the setup described in Chapter 4. CuNW was deposited in the center of 10 mm $\times$ 10 mm area, by the electro-chemical deposition through AAO template method described in Chapter 2. The thickness of the copper substrate is 3 mm and the average height of CuNW is about 15 μm. The boiling characteristic of testing samples is depicted in Fig. 5.1. The heat flux is based on the projected base area. The wall temperature was calculated as the

temperature at the top surface of the test samples. The wall superheat was then obtained by subtracting water saturation temperature from the wall temperature. Boiling on plain Cu substrate served as the primary control for comparing boiling performance and the results were consistent with previous study [125]. Two CuNW samples were tested and compared with the performance of plain Cu substrate. It is clear from Fig.5.1 that higher heat flux can be dissipated through the substrates with the NW arrays compared to the plain substrate for a given wall superheat. For both samples with the NW arrays, the heat flux in most wall superheat region was at least twice as much as that of plain surface, and the maximum heat flux was 160 W/cm^2 at 11.2 K wall superheat.

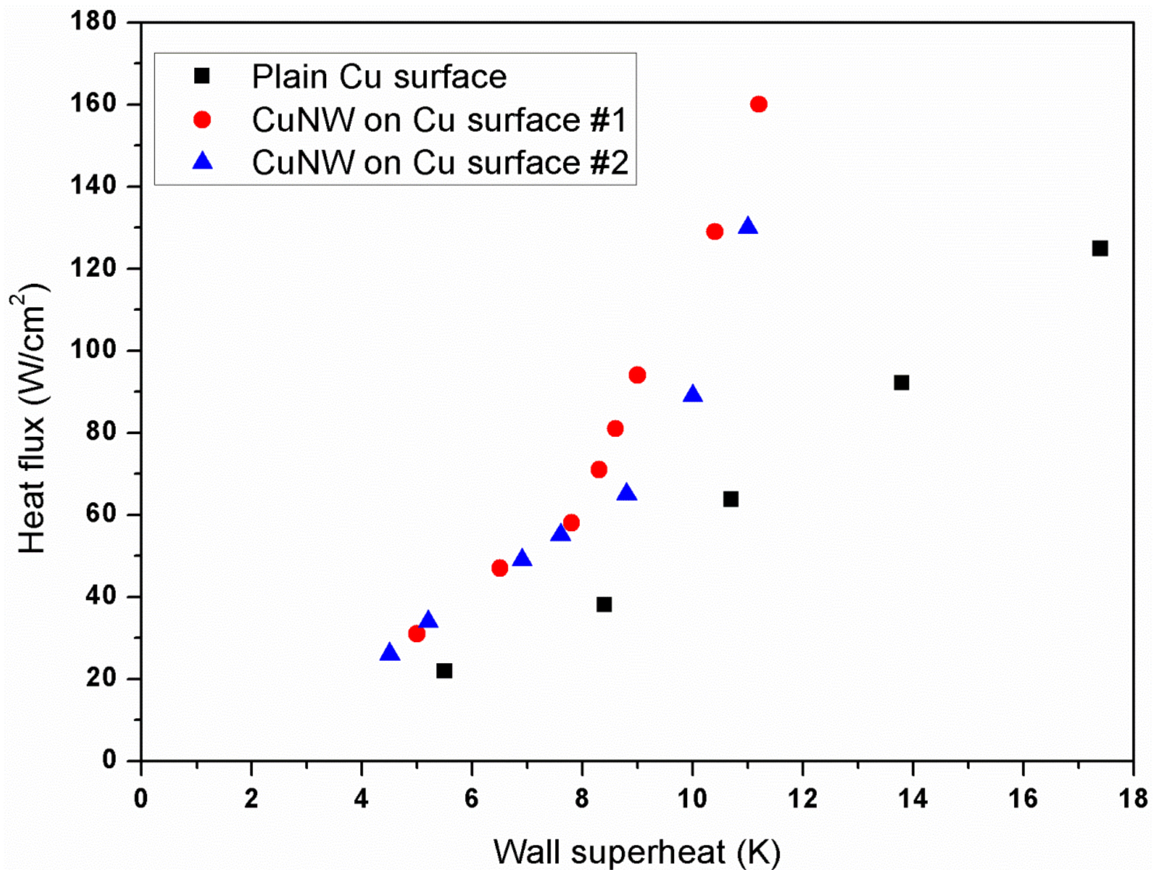


Figure 5.1 Boiling curve of plain Cu surface and Cu surface with CuNW

Similar results on Si substrate with CuNW at previous study [42] were also observed, but the maximum heat flux value was only 134 W/cm^2 at 23 K superheat, suggesting that by changing the substrate material, the pool boiling performance of NW structure can be further improved. The mechanism of such enhancement will be discussed in details in Chapter 6.

During the tests, no damage or peeling off was observed for NW sample after repeated boiling which confirm that the directly grown CuNW arrays possess high mechanical and thermal reliability. The testing results suggested that application of NW structures on the heater surface may greatly enhance pool boiling heat transfer.

Table 5.1: Comparison of recent studies on Cu nanostructure on pool boiling enhancement

Material Nanostructure	**Working fluid**	**Surface characterization**	**Boiling performance (W/cm^2 @ K)**	**References**
CuNW attached on Si substrate with an epoxy layer	water	200 nm in diameter, 50 µm in height	180~220 W/cm^2 at 30 K superheat	Chen et al 2009. [38]
Cu nanorods created on Cu substrate by oblique-angle deposition	water	50 nm in tip diameter, 450 nm in height	160 W/cm^2 at 15~20 K superheat	Li et al 2008. [39]
CuNW bonded on Si substrate with an epoxy layer	FC-72	200 nm in diameter, 300 nm in pitching, 1~8 µm in height	19.5 W/cm^2 at 38 K superheat for 2 µm NW arrays	Im et al 2010. [40]
CuNW directly deposited on Cu substrate using AAO templates	water	200 nm in diameter, 5~10 µm in height	164 W/cm^2 at 11 K superheat	This work

To the author's best knowledge, this is the first pool boiling study using bulk substrates with directly-grown nanowires without any interfacial layer. The heat flux for

CuNW on Cu substrate during the testing reaches 164 W/cm^2 at 11 K wall superheat, which is among the highest values for pool boiling heat transfer with water. A comparison of recent study on Cu nanostructure for pool boiling is summarized in Table 5.1. Our directly grown metallic NW has shown advantageous in pool boiling heat transfer.

5.2 Pool boiling test of SiNW and CuNW on 2D Si substrate

To better understand the effect of material properties and NW geometry on pool boiling, SiNW and CuNW with different heights were fabricated on flat Si substrate and compared in boiling performance.

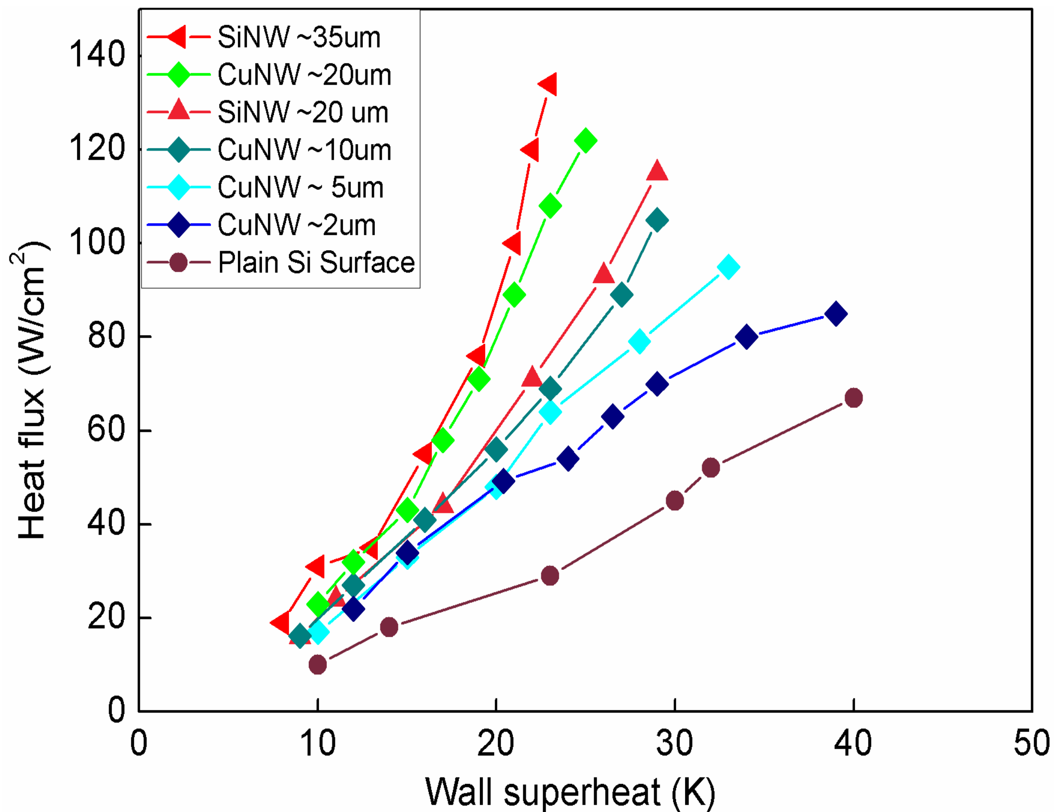


Figure 5.2 Boiling characterization of the samples with CuNW and SiNW at different heights

The boiling curves for the plain Si surface, the SiNW surface, and the CuNW surface were therefore obtained and depicted in Fig. 5.2. Boiling on the plain Si substrate served as the primary control for comparing boiling performance. The results were consistent with experimental results reported previously [36]. The NW surfaces are able to provide more active nucleation sites than the plain Si surface, making more bubbles generated at a given heat flux, as shown in Fig. 5.3. In addition, the incipient wall superheat on the NW surfaces was found to be lower than that on the plain Si surfaces. Particularly, the wall superheat at low heat fluxes decreased as the nanowire height increased. This result is in agreement with Hsu's model [126] which states, for the sizes considered in this study, the surface superheat decreases as the cavity size increases.

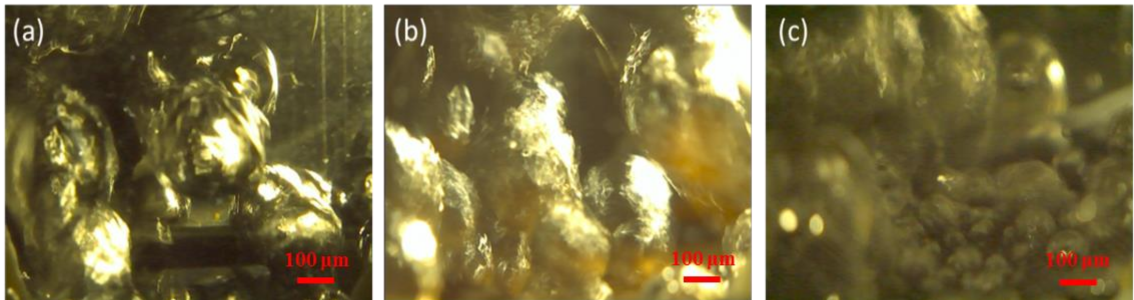


Figure 5.3 Bubble images of (a) plain Si surface, (b) CuNW surface and (c) SiNW surface at 40 W/cm^2 heat flux

The observed results suggested that boiling heat transfer was greatly enhanced by NW surfaces, and the enhancement was further improved by increasing the average NW heights for both Cu and Si NW samples. Table 5.2 summarizes the boiling performance of NW samples with different heights. The 35 μm SiNW sample reached a heat flux of 134 W/cm^2 at 23 K wall superheat, which is among one of the highest recorded for Si surfaces at this wall superheat. In addition, the CuNW grown on the Si substrate

without an intermediate epoxy layer proves to be beneficial in pool boiling application as the samples were repeatedly tested, no degradation in performance was observed.

Table 5.2: Pool boiling performance of the surfaces with CuNW and SiNW in different heights

	NW height	**Maximum heat flux (W/cm^2) / superheat (K)**
CuNW	20 μm	122 W/cm^2 / 24 K
CuNW	10 μm	105 W/cm^2 / 29 K
CuNW	5 μm	95 W/cm^2 / 33 K
CuNW	2 μm	85W/cm^2 / 39 K
SiNW	35 μm	134 W/cm^2 / 23 K
SiNW	20 μm	115 W/cm^2 / 25 K

It can also be seen that boiling characteristics of SiNW and CuNW appear similar to each other although the thermal conductivities of Cu and Si are quite different (400 W/m·K for Cu and 150 W/m·K for Si at 25 ℃ [127]). This is understandable as the boiling behavior is more dependent on the surface morphology than the material properties at micro/nano-scale. However, for a given height, the CuNW outperforms SiNW. The HTC of 20 μm CuNW is much higher than that of SiNW at a given wall superheat. The local heat transfer coefficient of CuNW and SiNW surfaces measured at 25 K superheat are shown and compared with the published data [38] in Fig. 5.4. The heat transfer coefficients of the NW surfaces increases proportionally as NW height increases for both CuNWs and SiNWs. By incorporating Chen's results [38] for SiNW and CuNW with a 50 μm height, the linear relationship between NW height and the HTC for water pool boiling performance can be further extended, as shown in Fig. 5.4. It is observed that the micro-scale cavities increase in number and size as the NW height increases, but it is still unclear if the cavities alone are responsible for the heat transfer enhancement.

The enhanced capillary forces due to higher NW structures could supply the liquid and prevent dry-out of the heater surface. However, there must be an optimal NW height beyond which the benefit brought from increasing height would become limited. Im et al [40] suggested that the 2 μm CuNW structure has the best boiling performance for FC-72,

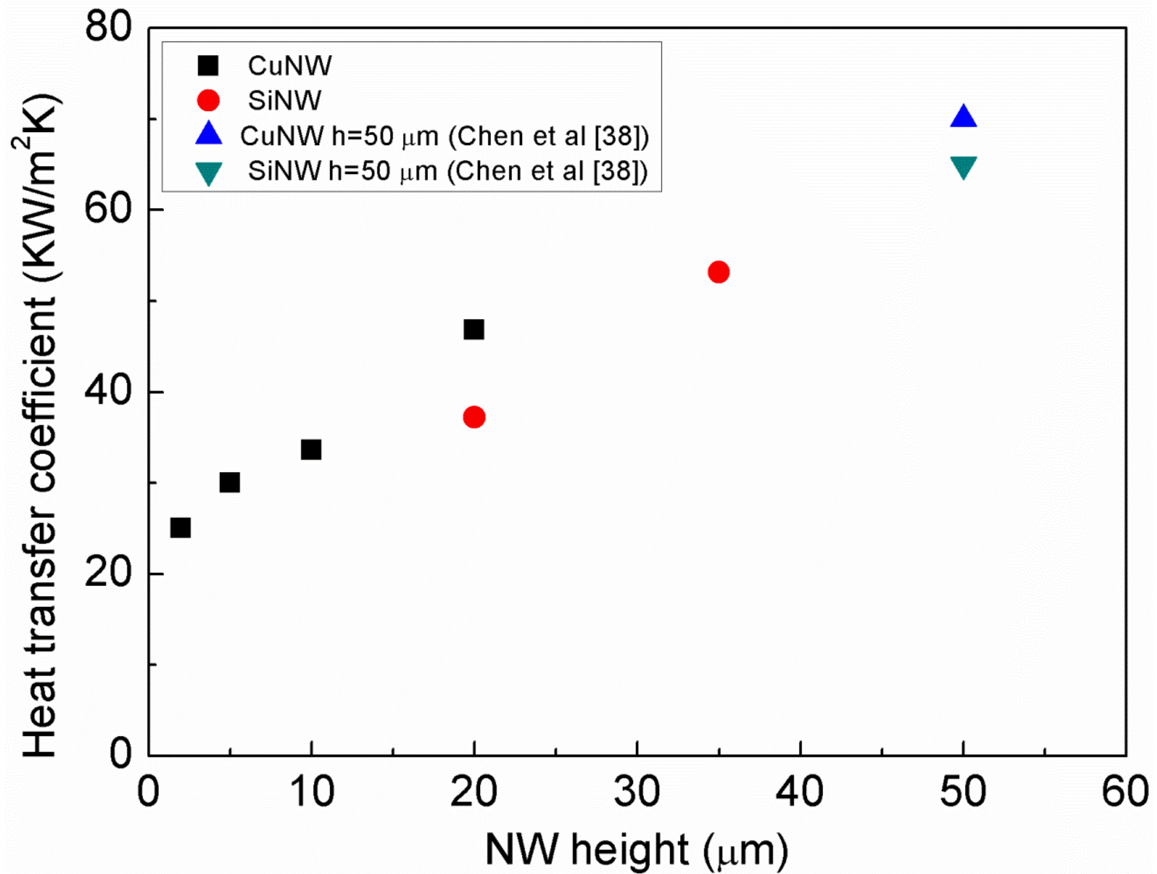


Figure 5.4 Heat transfer coefficients of the samples with CuNW and SiNW (incorporated with Chen's results [38]) at given wall superheat (25K)

and the higher ones are not preferred due to increased flow resistance on the surface. For pool boiling with water, although the optimal NW height is not identified yet, our study suggests that the water pool boiling performance can be enhanced by increasing NW height to at least 50 μm.

5.2.1 Surface cavity of SiNW and CuNW surfaces

The surface cavities induced by NW structures play an important role in pool boiling enhancement due to serving as active bubble nucleation site at low wall superheat and tunnels for liquid transport. Most cavities and openings were observed on NW surface with average NW height above 20 μm. For CuNW, the cavities were primarily crated during the AAO removal process, in which the surface tension of the etchant caused the NW arrays to bundle together. Non-uniform distribution of the NW height, caused by the growth rate variation of CuNW across the substrate, also leaded to the cavity formation. The non-uniform NW height distribution became the surface waviness at a larger scale and may also promote bubble nucleation. As a result, the sample with longer NW arrays had better boiling performance than the ones with shorter arrays, as shown in Fig. 5.2, as the former provided more active nucleation sites and wider passage for liquid transport. A post-imaging process was conducted on the SEM images (Fig. 2.4 and Fig. 3.3) for surface cavity characterization. The SEM images were first converted to binary by thresholding, and then the segmentation between the NW area and cavity was made. By defining the NW diameter, the individual NW can be distinguished from ambient cavity. In this way, the area percentage, the size of cavity and NW density can be measured. The imaging processing of one SEM sample image was shown in Fig. 5.5 (a) and (b), and from the results of all NW samples, Fig. 5.6 was drawn and it showed that the cavity density and average size change as NW height increases. The cavity density of 20 μm CuNW is 58% and for 35 μm SiNW, it is 65%. The maximum cavity size also increases as NW height increases, the maximum cavity was found on the 35 μm SiNW

surface, with a size of 2.5 μm. This explains how NW height affects the boiling performance.

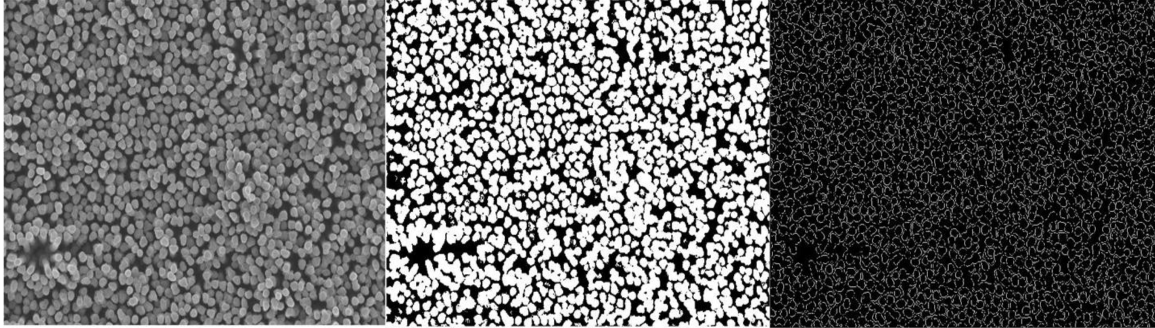


Figure 5.5 (a) Original SEM image, (b) images with pre-set contrast threshold for cavity calculation and (c) image for single NW counting and density calculation

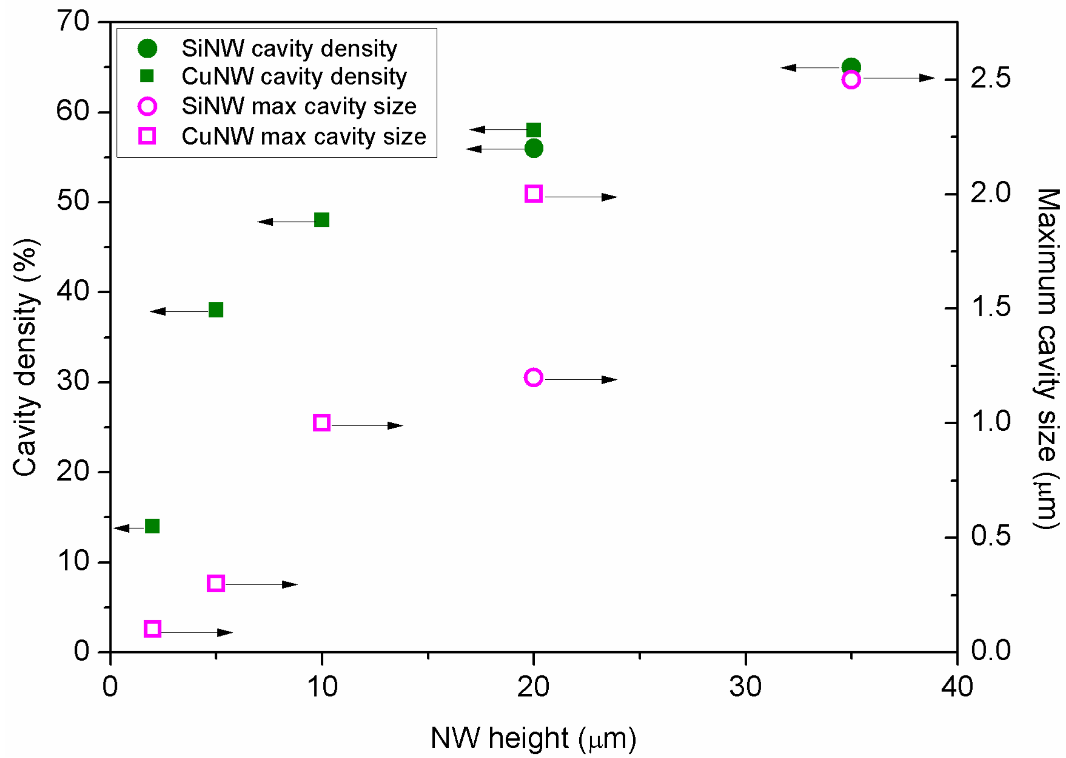


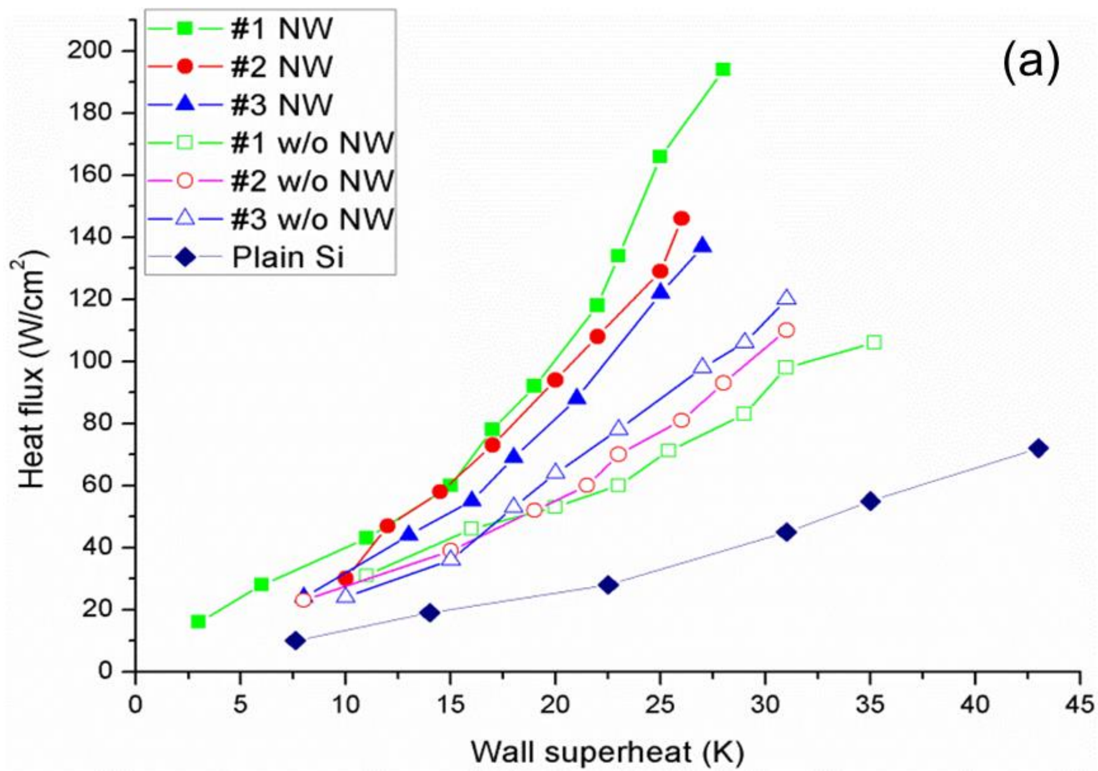
Figure 5.6 Cavity density and maximum size of NW samples with different heights

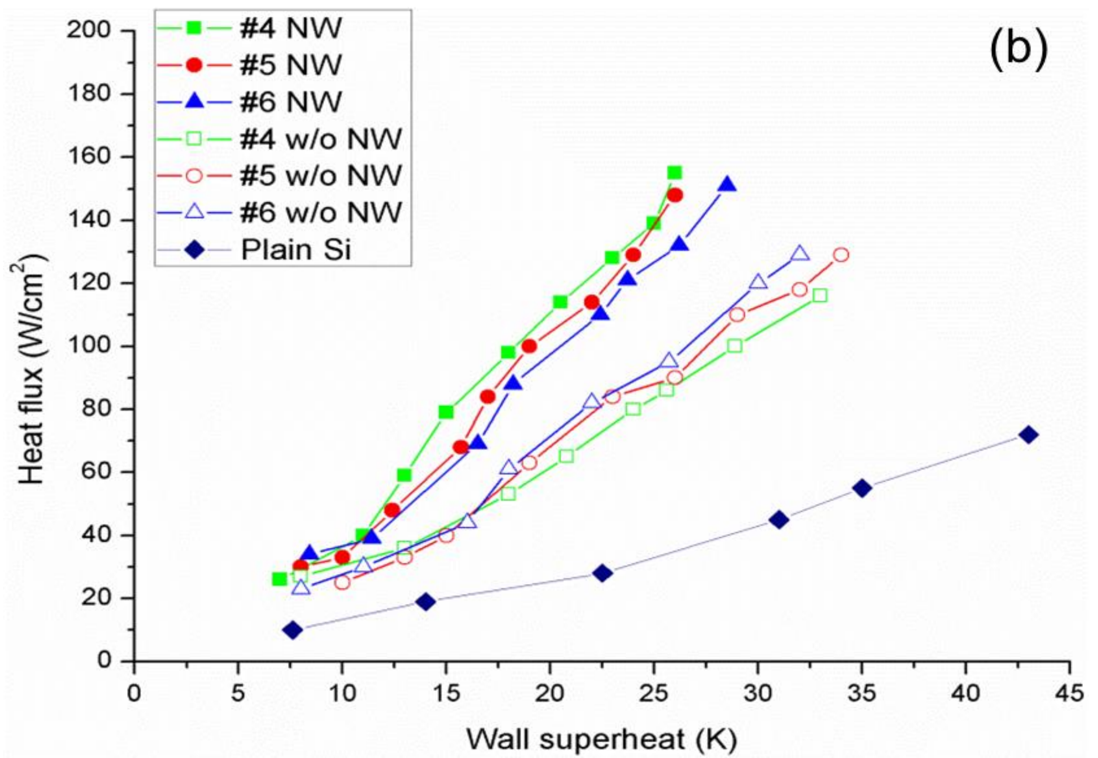
5.3 Pool boiling test of SiNW on 3D Si microchannel surfaces

9 different patterns of Si microchannel were first compared in pool boiling performance and the effect of mircochannel geometry on pool boiling was investigated. The SiNW coated microchannels were also tested and compared in the same manner. In addition, the bubble dynamics of SiNW coated microchannel during nucleate boiling was studied and the microbubble emission boiling was introduced.

5.3.1 Comparison of microchannel with different patterns

The boiling characterization of micro/nano hierarchical structure in the microchannel heat sinks is depicted in Fig. 5.7 (a)-(c). The heat flux value was calculated based on the projected microchannel area. Nine samples were separated into three groups, each of them share the same fin width, as indicated in Table 3.2 from Chapter 3. Basically, the active heat transfer area of samples decreases as the channel width increases. Boiling on the plain Si substrate served as the primary control for comparing boiling performance. The results were consistent with experimental results reported previously [36]. Significant boiling heat transfer enhancement was observed on all SiNW samples compared to the plain microchannel samples. The enhancement ratio varies according to microchannel geometry.


(a)
#1 NW
#2 NW
#3 NW
#1 w/o NW
#2 w/o NW
#3 w/o NW
Plain Si
Heat flux (W/cm^2)
Wall superheat (K)
0
20
40
60
80
100
120
140
160
180
200
0
5
10
15
20
25
30
35
40
45


(b)
#4 NW
#5 NW
#6 NW
#4 w/o NW
#5 w/o NW
#6 w/o NW
Plain Si
Heat flux (W/cm^2)
Wall superheat (K)
0
20
40
60
80
100
120
140
160
180
200
0
5
10
15
20
25
30
35
40
45

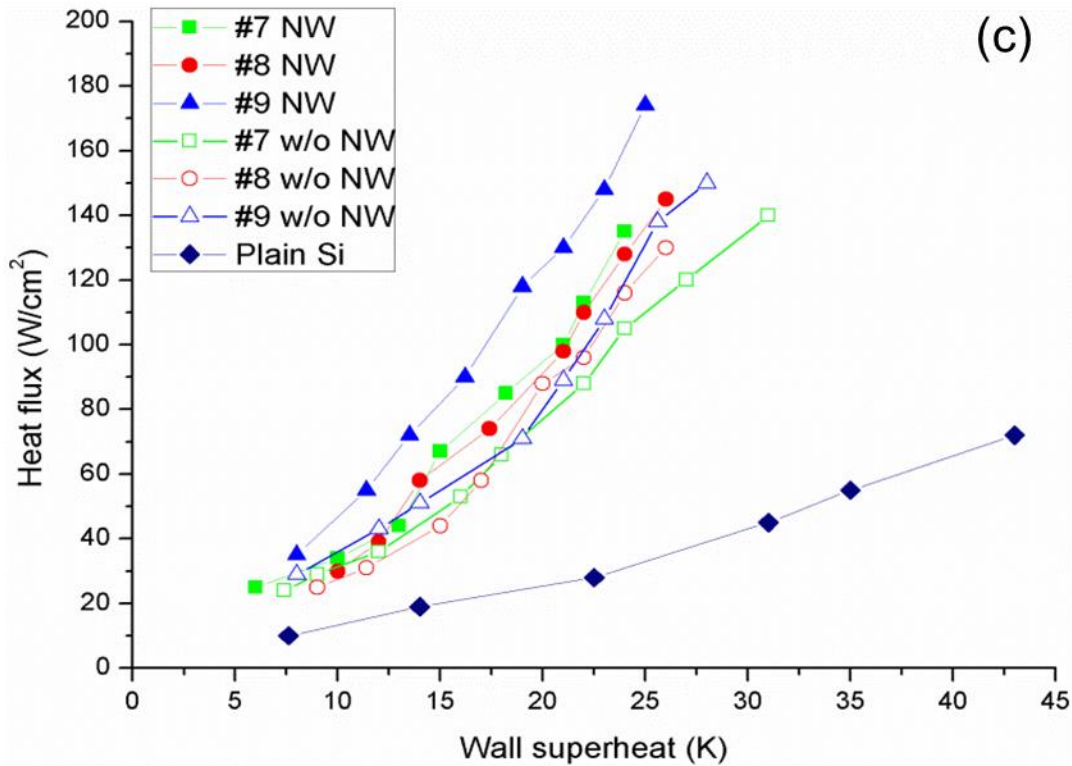


Figure 5.7 Boiling curves for microchannels with and without SiNW: (a) sample# 1-3, (b) sample# 4-6 and (c) sample# 7-9.

For microchannel-only surface, the boiling curves suggest that for a given channel depth of 150 μm, the heat transfer is increased at a given wall superheat when the channel width is increased from 100 μm to 300 μm. In addition, reducing the fin pitch also increases the heat transfer performance from the structure. As seen from Fig. 5.7(c), sample # 9 yielded a heat flux of 150 W/cm^2 at 27.5 K wall superheat. In contrast, the lowest performing sample #1 reached only 114 W/cm^2 at 35 K wall superheat, as this sample has the largest fin pitch and smallest channel width.

The physical reason for wider channels providing more heat transfer in this study seems to be related to the bubble generation and dynamics. Bubbles primarily generated at the bottom of the channel due to its proximity to the heat source. The wider channels

seem to result in more bubble nucleation sites. Also, increasing channel width makes it easier for water to flow into the microchannels feeding the nucleation sites, thereby preventing dry out in the channel. This finding is also consistent with a previous study on the effect of open microchannel geometry on pool boiling performance [125]. By incorporating SiNW in the microchannel heat sink, the boiling incipient wall superheat on the surface was found to be much lower than that on the microchannel-only surface. Particularly, the boiling enhancement ratio was directly related to the overall surface area.

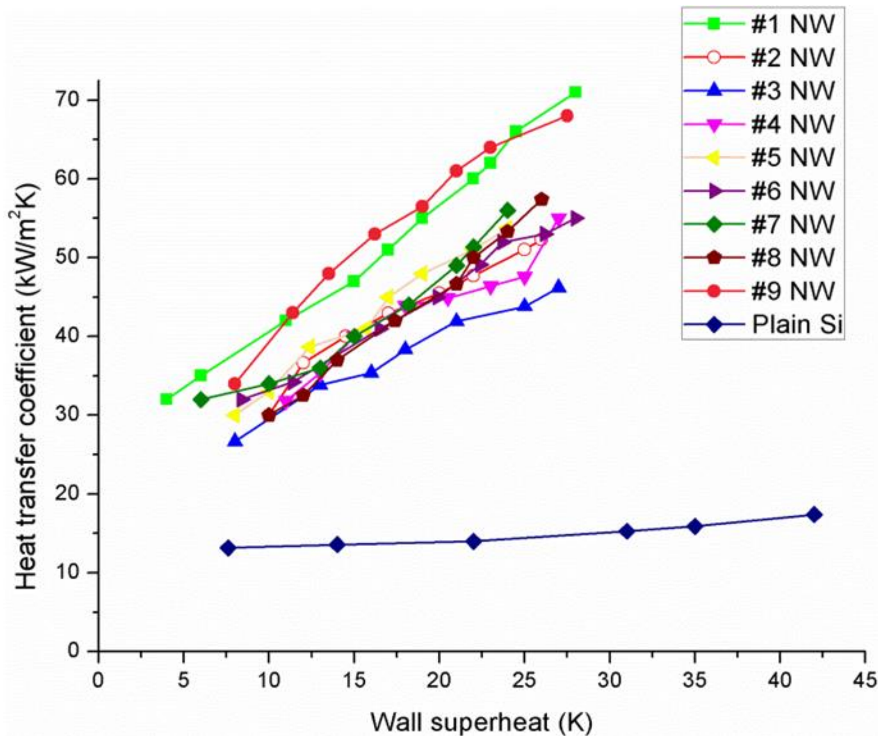


Figure 5.8 Heat transfer coefficient for the SiNW samples and plain surface

The enhanced surface area of each sample was represented by surface area augmentation factor shown in Table 5.3. Samples with more active heat transfer area benefitted more from the SiNW structures. The maximum heat flux was observed in the present experiments on sample #1, which reached 194 W/cm^2 at 28K superheat, and the

actual CHF was beyond 200 W/cm^2 (not observed due to safety considerations). In order to compare the heat transfer performance in a more quantitative way, a plot of the heat transfer coefficient (HTC) against wall superheat of all the samples, including plain Si surface, is shown in Fig. 5.8.

For the microchannel samples coated with SiNW surfaces, the maximum HTC was observed on sample #1, which has a surface area augmentation of 2.05. At a given wall superheat (25 K), the heat flux of sample #1 is improved by 120% over the microchannel-only surface, and its HTC is more than 4 times higher than that of plain Si surface, as shown in Table 5.3, Fig. 5.7(a) and Fig. 5.8. The sample with the lowest surface augmentation factor (#9) has only 27% improvement in heat flux even though it has high heat fluxes. The result suggests that the microchannels with higher surface area would benefit more from nanostructures for heat transfer enhancement. It may be noted that the chosen microchannel pattern may not be the best configuration for boiling performance; the boiling performance is expected to improve further by optimizing the microchannel configuration.

It is worth mentioning that many earlier studies have successfully applied nanowire structures on plain surfaces for the enhancement of pool boiling heat transfer. At 25 K ~ 30 K wall superheat region, the reported maximum heat flux in those studies ranges from 100 ~ 150 kW/cm^2 [38, 43, 128]. By combining the nanowire structures with microchannel structure, the maximum heat flux is pushed higher to 194 kW/cm^2 at 28 K wall superheat, as shown in Fig. 5.7(c). This finding suggests a promising application of micro/nano hierarchical structures in enhancing pool boiling heat transfer.

Table 5.3: Summary of pool boiling performance of various microchannel samples with and without nanowires

Sample# (SiNW)	**Surface augmentation factor**	**Heat flux @ Δ25K With SiNW(W/cm²)**	**Heat flux @ Δ25K w/o SiNW (W/cm²)**	**Enhancement of heat flux (%)**
1	2.02	168	76	120%
2	1.69	129	80	61%
3	1.50	122	92	32%
4	1.69	139	86	62%
5	1.51	132	90	45%
6	1.48	129	95	30%
7	1.52	142	106	32%
8	1.41	154	117	23%
9	1.35	174	138	27%

5.3.2 Effect of sidewall SiNW structure on pool boiling

To study the effect of sidewall SiNW structure on pool boiling, microchannels with SiNW fabricated on different surface areas were prepared and tested. The geometry of microchannel and the dimension of SiNWs were listed in Table 5.4. The boiling characteristics of microchannel with SiNW on the whole surface area, microchannel with SiNW only on the top and bottom, microchannel without SiNW, plain Si surface with SiNW [42] and plain Si surface were depicted in Fig.5.9.

The heat flux value was calculated, based on the projected microchannel area. Boiling on the plain silicon substrate served as the primary control for comparing boiling performance, the results were consistent with experimental results reported previously [36]. For microchannel only surface, the maximum heat flux recorded is 110 W/cm^2 at 35K wall superheat, which is below the performance of plain Si surface with SiNW, as the smooth microchannel can not provide as many active bubble nucleation cavities as

the later one does, even it possesses more surface areas. By incorporating SiNW in the top and bottom of microchannel heat sink, the boiling incipient wall superheat on the surface was found to be much lower than that on the plain silicon surface as well as on the microchannel-only surface and the maximum heat flux reached 135 W/cm^2 at 28 K wall superheat. The combination of microchannel and SiNW also shows superior performance comparing to SiNW on plain Si surface.

Table 5.4: Summary of microchannel surface parameters

Characterization of Microchannels (before SiNW synthesis)		**Characterization of heated surface**		**Characterization of SiNWs**	
Channel length	100 mm	Heated surface	Silicon	Average height on (100) surfaces	15-20 μm
Channel/fin width	100 μm	Thermal conductivity	104 W/ mK	Average height on (110) surfaces	10-15 μm
Channel height	100 μm	Heat surface area	10×10 mm^2	Average diameter on (100) surfaces	50 nm
Channel number	50	Heated surface thickness	450 μm	Average diameter on (110) surfaces	80-100 nm

When the entire microchannel surface was covered by SiNW, significant enhancement was found at intermediate wall superheat region, yielding a peak heat flux value of 168 W/cm^2 at 24 K superheat and demonstrating an improvement of 60% over the microchannel with SiNW only on the top/bottom surface, 150% over the microchannel-only surface and 400% over a plain silicon surface at given superheat region. The boiling test results suggest that the heat dissipation ability of microchannel heat sink through pool boiling can be greatly enhanced by embedding SiNW on the silicon microchannel surfaces; this result is consistent with the previous study on SiNW on plain surfaces [16].

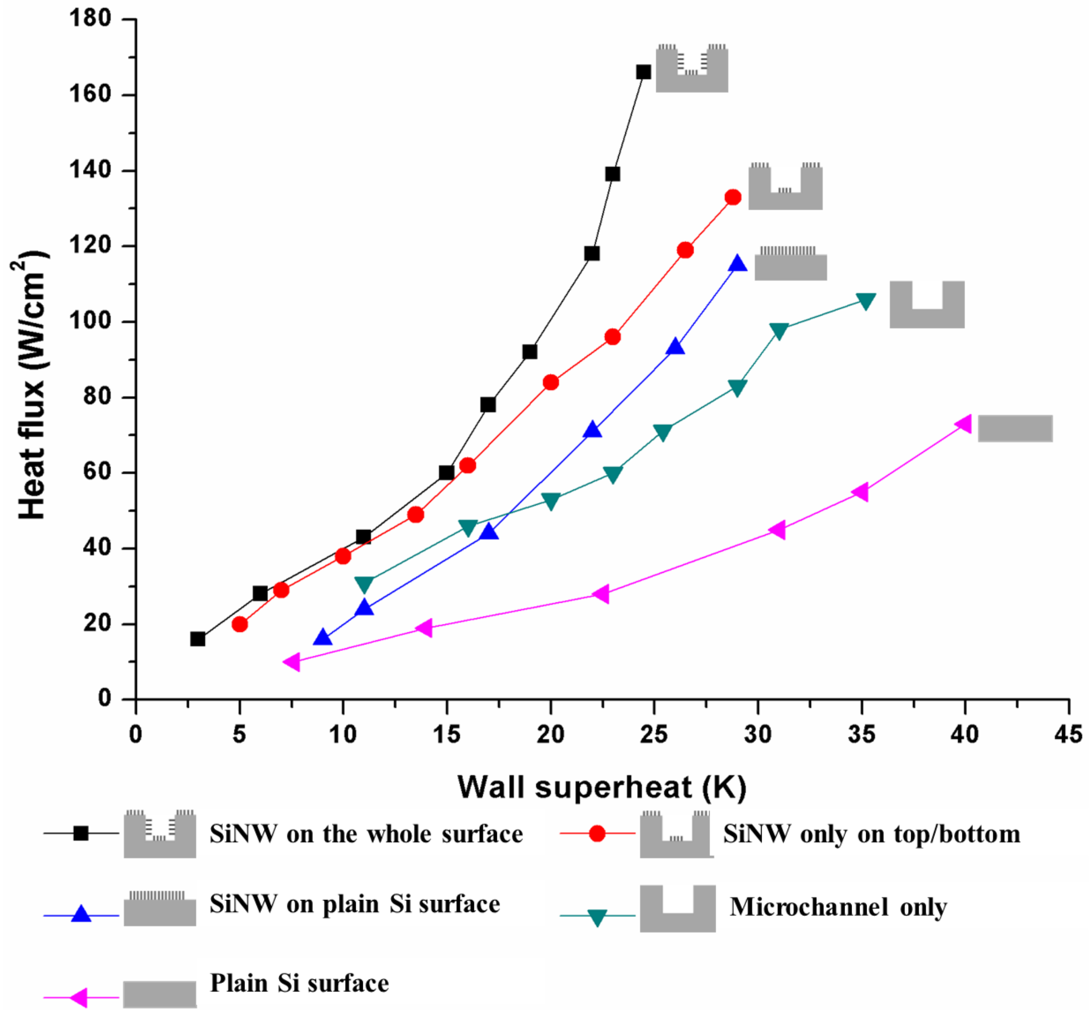


Figure 5.9 Boiling characterization of microchannel with SiNW on the whole surface, microchannel with SiNW on the top/bottom surfaces, microchannel only surface, SiNW on plain Si surface and plain Si surface

In addition, the boiling enhancement ratio is related the surface area covered by SiNWs, as suggested in Table 5.3. At low wall superheat region where only forced convection and conduction heat transfer occurs, the microchannels with SiNWs on the whole surface have similar heat transfer characteristics as the one coated with SiNWs only on top and bottom surfaces. Once the boiling behavior reaches the nucleate boiling stage, bubble dynamics is greatly affected by the sidewall SiNW structures, the microchannel chip with SiNWs on the whole surfaces experiences a dramatic heat flux

increment as wall superheat increases. Moreover, the SiNWs on the sidewall surfaces enhance heat transfer area and surface roughness, resulting in stronger recirculation and flow separation in the microchannel passage. The surface cavities in between bundled SiNWs provide great amount of active bubble nucleation sites. The Sidewall SiNW structure promotes bubble detachment from the surfaces, intensify the flow turbulence and therefore increase the heat transfer coefficient during the nucleate boiling stage. All these factors contribute to the boiling enhancement. At 24 K wall superheat, the calculated HTC of microchannel embedded with SiNW on the whole surface is 69 KW/m^2K, indicating a 42% improvement comparing to the surface without SiNW on the sidewall at the same superheat region.

5.3.3 Bubble dynamics in microchannel surfaces

The bubble nucleation and growth on the sample surfaces were investigated with high speed camera (24,000 frames/sec, Keyence VW-6000). Fig. 5.10 shows the bubble generation event from the samples of microchannel-only and microchannel with SiNW at 0.02 s interval during low heat flux region (10~15 W/cm^2).

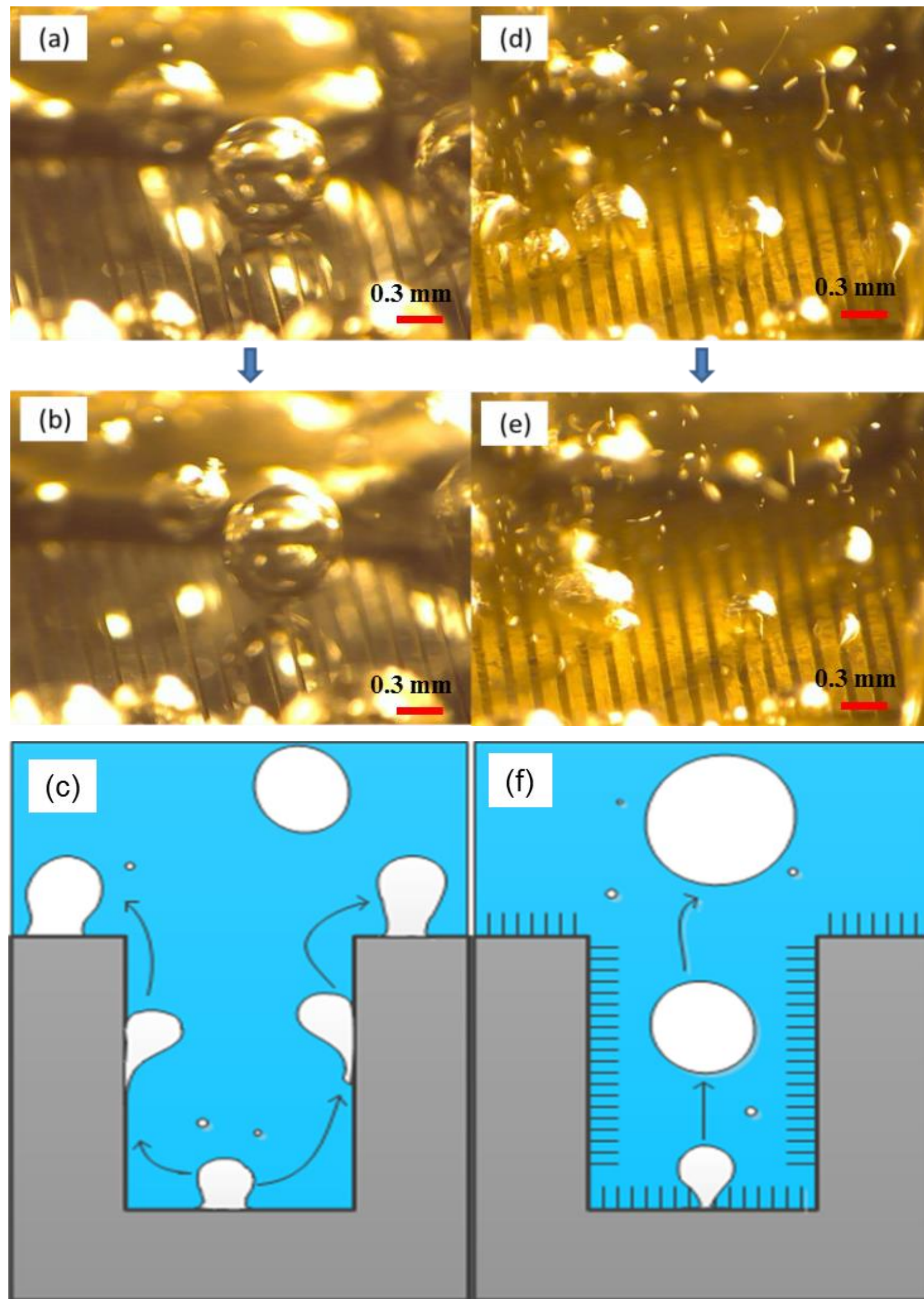


Figure 5.10 Successive images of bubble generation at low heat flux (10~15 W/cm^2) on the samples of (a)-(b) microchannel-only and (d)-(e) microchannel with SiNW at 0.02 second intervals; (c) and (f) illustrate the possible mechanisms of bubble generations on microchannel-only and microchannel with SiNW surface respectively.

Different bubble behaviors were observed on microchannel surfaces with and without SiNW. For the microchannel-only surface at low heat flux, a bubble nucleates at

the bottom and moves to the fin where it attaches itself to the sidewall and then migrates to the top surface and grows. The diameter of the bubble is confined by the channel width but the bubble does not depart from the top of the fin surface until it reaches certain critical departure diameter. However, when the microchannel surface is coated with SiNW, the bubble directly departs from the nucleation sites without sticking on top of the fin surface, resulting in an instantaneous micro-sized bubble generation and a high departure frequency. The SiNW structures create a very high bubble nucleation site density; thus at a given time, large number of small bubbles were observed on microchannels with SiNW samples than that on microchannel-only surfaces.

5.3.3.1 Microbubble emission boiling

At intermediate heat fluxes, microbubble emission boiling (MEB) was observed on microchannel with SiNW surfaces. The MEB phenomenon was first reported by Inada [129] in a study of highly subcooled pool boiling. Subcooled flow boiling with microbubble emission has been investigated Suzuki [130] . The MEB regime usually occurs in the beginning of subcooled transition boiling, when the instability of bubble interface is accelerated in the subcooled liquid and the interface collapses to form many microbubbles. Because MEB promotes liquid-solid contact and increases heat flux, it significantly enhances boiling performance by maintaining high heat flux while preventing the dryout. In the boiling test of microchannel with SiNW samples, it is found that at intermediate heat fluxes, the coalesced bubbles generated on the heated surface were broken to many microbubbles after contacting with the surrounding liquid. The bubbles stably and continuously generated and sprayed from active nucleate site to form jet flows in the liquid (Fig. 5.11.a-d). While at high heat fluxes, the coalescing bubble

size increased dramatically, as shown in Fig. 5.11(e-h). Because the details of MEB generation is not yet fully understood, the bubble behavior at different heat flux region may be attributed to some unique characteristics of SiNW, as MEB was not observed on microchannel-only samples. The commencement of MEB however, may explain the superior boiling performance of microchannel with SiNW surfaces at intermediate heat fluxes.

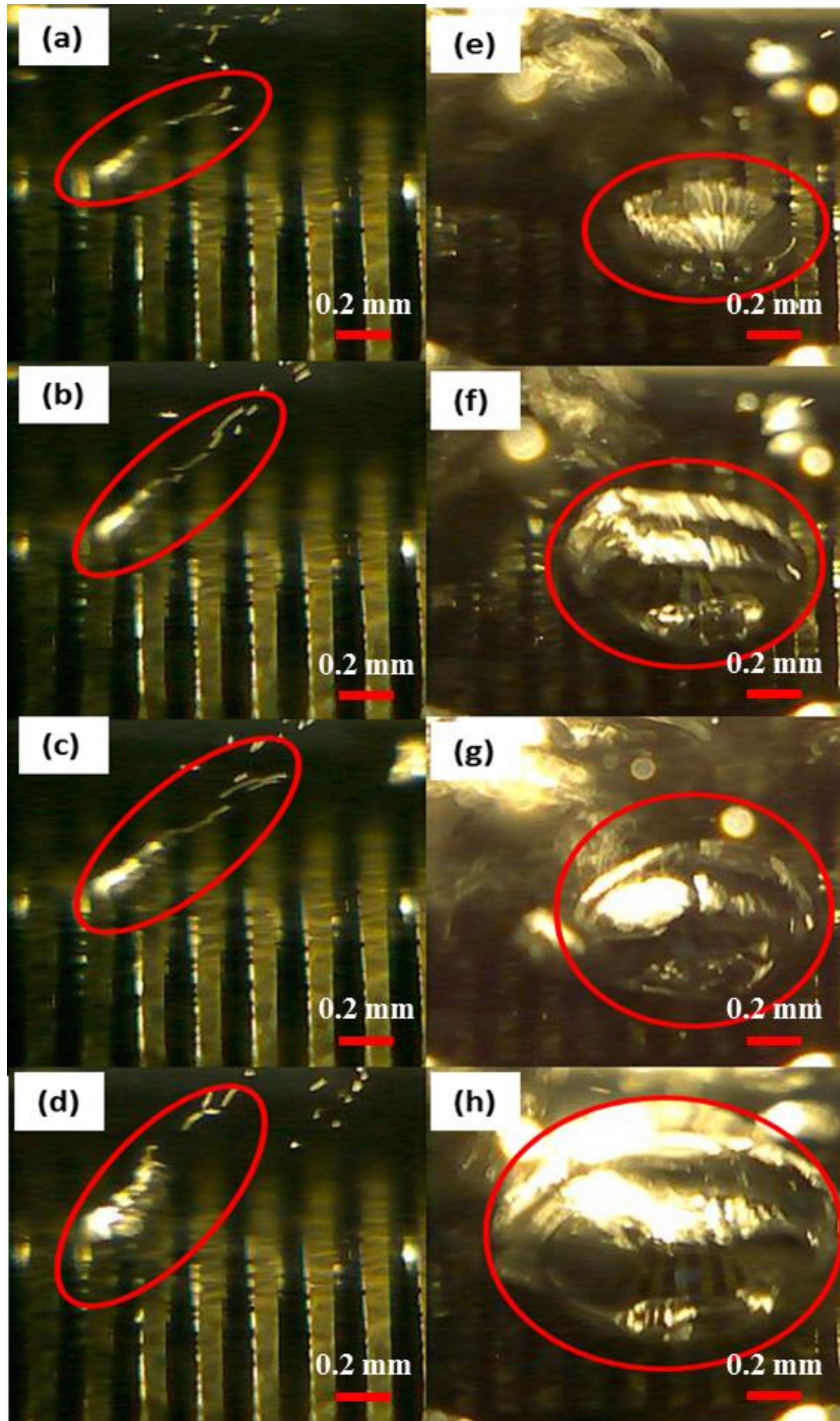


Figure 5.11. Successive images of (a-d) microbubble emission boiling at intermediate heat flux (60~80 W/cm^2) at 0.1s interval and (e-h) large bubble generation at high heat flux (120~140 W/cm^2) at 0.02s interval for microchannel with SiNW surface

5.4 Summary

In this chapter, pool boiling tests were conducted on CuNW on copper chip, CuNW on Si chip, SiNW on Si chip and SiNW on Si microchannel heat sink, respectively. The results have shown that NW structure can significantly enhance pool boiling performance in that both CHF and HTC of NW coated surface are improved comparing to surfaces without NW structure. Several factors that may attribute to boiling enhancement are demonstrated in experimental data. Those factors include surface cavity, surface wettability and bubble dynamics. More details will be discussed in the following chapter.

In addition, the testing of micro/nano hieratical structure on Si microchannel heat sink suggests that 1) For microchannel without SiNW, the pool boiling performance was primarily affected by microchannel geometry, as surface with wider channel size and smaller fin pitch demonstrate superior boiling performance; 2) after incorporating with SiNW, the enhancement ratio is only related to the area covered by SiNW, which suggests that more surface area covered by SiNW, the higher enhancement the surface would possess; 3) the sidewall structure of microchannel plays a very important role in boiling process, as the heat flux difference between microchannel with sidewall SiNW and the same one without sidewall SiNW can be as high as 42%, as indicated in the testing results. This finding may provide insight for advanced cooling technique in 3D IC architecture development.

CHAPTER 6

DISCUSSIONS AND CONCLUSIONS

The Pool boiling experiments conducted on 2D/3D substrates with/without NW structures suggested that the nanowire structure would significantly improve the pool boiling heat transfer, regardless of the heating surface property and geometry. In this chapter, the mechanism of the enhancement was investigated and summarized, followed by a discussion on the fabrication merits and the major findings from this work.

6.1 Enhancement mechanism

Through the boiling tests, several special behaviors of NW surface were noted which contribute to the enhancement. Firstly, it is observed that surface cavities created by NW structures serve to increase the active bubble nucleation sites, and the average NW height directly affect the cavity size and density. Fig. 5.6 shows that the cavity density of 20 μm CuNW is 58% and for 35 μm SiNW, it is 65%. The maximum cavity size also increases as NW height increases, the maximum cavity was found on the 35 μm SiNW surface, with a size of 2.5 μm. This may explain why substrate with 35 μm SiNW demonstrates the best pool boiling result. The surface cavity with large opening size can enhance nucleation from the larger embryonic bubbles, increase thin film evaporation due to the large surface area of the nanowires, and two-phase convection within the cavities. During the nucleate boiling, the vapor embryos exhilarate bubble generation in cavity mouth at comparatively less superheat. In addition, the increase in surface cavity would also affect the bubble dynamics. Fig. 5.4 shows that the Nanowired surface generates

smaller sizes of bubbles with higher departure frequencies compared to the plain surface. The consistent contributing factor to nucleate boiling enhancement using the NW structure is the increase in the bubble departure frequency, which is caused by the increase in both single site frequency and nucleation site density. The occurrence of these phenomena would lower the heater surface temperature by reducing the average temperature within the superheated liquid layer that surrounds the heated surface. An increase in single site frequency would reduce the waiting time between bubble generation and departure therefore lead directly to a lower surface temperature. A rise in the number of active bubble nucleation sites would increase the individual bubble influence areas, thus enable the removal of larger amount of superheated liquid and inhibits the growth of the superheated liquid layer, resulting in a lower wall superheat. Since an increase in the average NW height would increase both the number of surface cavity and the cavity size, fabricating high aspect ratio nanowire structures has practical application in boiling heat transfer enhancement.

Secondly, the surface wettability change caused by NW also contributes to the pool boiling enhancement. Surface wettability is a very important parameter in phase change heat transfer situation where liquid surface takes away heat from solid surface. Higher wettability improves the solid-liquid contact that causes better and efficient heat transfer from one to another. In addition, higher wettability suggests a greater affinity towards water thus it can delay the incoming of film boiling and prevent the occurrence of individual hot spot on the heating surface. Therefore, higher wettability is highly desired in boiling and evaporation. The contact angles of water droplet on NW surfaces are significantly lower than that of plain surfaces. As shown in Fig. 2.6 and Fig. 3.4, the

liquid-solid contact angle of CuNW surface is 28˚ and that for SiNW it is 0˚ (completely wetting). The decrease in the evaporation time and the increased CHF are the outcomes of improved wettability of the NW surfaces. Thus, surface hydrophilicity induced by the NW structures is another cause of enhanced pool boiling heat transfer.

In addition, it is found that the surface area of the NW is directly related to the HTC. Taking the microchannel heat sink for example, the surface area of microchannel #1 is about 2.05 times of plain Si substrate (Table 5.3). After SiNW coating, the heat flux is improved by 120% over the same sample without SiNW coating at a given wall superheat and the HTC is more than four times higher than that of plain Si surface. While for microchannel #9, which is about 1.35 times larger than plain Si substrate in surface area, the heat transfer improvement is only 27% after SiNW coating. This result suggests that higher NW coverage could lead to better HTC.

6.2 Fabrication merits

In this study, new fabrication methods were developed to directly grow CuNW on flat Si substrate and grow SiNW on 3D microchannel surface, respectively. Both of them are more advantageous than the conventional fabrication techniques for the application of boiling enhancement. The direct growth of CuNW technique is a simple and controllable method and it can be applied to a variety of substrates. The NW array without any intermediate epoxy layer strengthens the overall mechanical and thermal reliability, therefore it would be beneficial in other applications where large area coverage of metallic nanowires is desired.

The two-step etching for SiNW fabrication on Si microchannel heat sink is the first attempt on creating uniform NW structures on non-flat substrates through wet etching. The first step involves the metal-assisted etching targeting (100) planes of the microchannel (i.e. top and bottom area of microchannel), and the second step is initiated by adding more oxidant in the etching solution to promote the etching at (110) planes of the microchannel (i.e. sidewall area of microchannel). Therefore, by applying different etching conditions for different crystalline direction, the electroless etching is capable of creating uniform SiNW on silicon-based three-dimensional geometry. The as-fabricated SiNW on (100) surface is 50 nm in diameter and 15~20 μm in height, while on (110) surface it is 80~100 nm in diameter and 10~15 μm in height. The geometry difference may be due to the etching duration difference. While incorporated with microchannels, this simple, controllable and low-cost fabrication method can further expand onto applications of nanostructure in advanced heat and mass transfer devices, not limited to the flat substrates.

6.3 Conclusion

This study demonstrates that pool boiling heat transfer in water can be enhanced by applying nanowire structures to heating surfaces. The effects of NW height have been explored, showing that the density and size of surface cavity increase as the NW height increases, and the pool boiling performance is enhanced regardless of the NW material. In addition, a two-step etching method was developed to fabricate uniform SiNW structures on the whole surface area of Si microchannel heat sinks. The main findings and conclusions are summarized as follows:

For NWs fabricated on 2D flat surfaces:

1 A modified synthesis technique is developed to directly grow CuNW on Si surface. With this technique, the durability and interfacial strength of NW structure are enhanced while the thermal resistance between the NW array and the substrate, due to epoxy layer needed in previous methods, is eliminated.

2 The average height of CuNW and SiNW can be controlled by synthesis parameters, and NW height is one of the key characteristics that influence the pool boiling performance. The best pool boiling performance was observed on SiNW with average height of 35 μm, which yield a heat flux of 134 W/cm^2 at 23 K wall superheat, more than 2 times higher than plain Si surface. However, it is believed that there should be a critical value for both cavity density and NW height, below which, the enhancement brought by nanowire structure become trivial.

3 The testing results of NW on 2D substrates suggest that for pool boiling with water on the nanowired surfaces, the heat transfer can be enhanced by increasing the NW height. Large number of cavities and openings were observed on the surface with higher NW arrays, which contribute to the enhanced pool boiling performance by providing more and stable active bubble nucleation.

4 Boiling performance of SiNW and CuNW appear to be similar to each other due to the fact that as heat transfer in boiling is dominated by bubble dynamics rather than heat conduction, the surface morphology plays a more important role in boiling heat transfer.

5 NW structures can significantly improve surface wettability, making heating surface more hydrophilic. The contact angles of water droplet on CuNW and SiNW surface are 28˚ and 0˚, respectively.

For SiNWs fabricated on 3D microchannel surfaces:

1 A two-step synthesis process is developed to create uniform SiNW structures on the orthogonal surfaces of the microchannels, including the (100) surface on the top and bottom, as well as the (110) surfaces on the sidewalls. The average height of the SiNWs is around 15~20 μm, with a diameter between 50~80 nm.

2 The microchannel geometry plays a critical role in pool boiling performance, for microchannels with 150 μm depth, large channel width and small channel pitch are preferred for better boiling performance. However, when SiNW are incorporated, microchannels with more surface area have higher enhancement ratio. A 400% improvement of HTC was observed on the microchannel samples with most surface area after SiNW coating, compared to the plain Si surface.

3 The SiNW synthesis mechanism indicates that uniform SiNW can be created on the surfaces at their own crystalline directions, with controllable morphology. By growing SiNW on the surfaces of the microchannel heat sink for pool boiling applications, the total effective heat transfer surface area increases and the heat transfer performance is significantly enhanced.

4 Microchannel sidewall structure directly affects the boiling behavior, as the incorporation of SiNW on the sidewall surfaces results in a 40% improvement in HTC compared to the microchannel sidewalls without SiNW. The boiling

enhancement induced by SiNW is directly related to the area covered by SiNW, especially for the sidewall surfaces.

5 For SiNW coated 3D substrate (i.e. Si microchannel), a heat flux of 195 W/cm^2 at 28K wall superheat was observed. This result represents a 400% improvement over a plain silicon substrate at the same wall superheat. For SiNW coated 2D substrate (i.e. flat Si surface), the optimal result was obtained on the surface with 35 μm SiNW, which yielded a heat flux of 134 W/cm^2 at 23 K superheat. This heat flux is almost 3 times higher than that of plain Si surface at the same wall superheat region.

Silicon is the most commonly used material in the semiconductor industry. The CuNW, SiNW and micro/nano hierarchical structures employed here are attractive for future semiconductor cooling, thermal management and high-heat-flux energy conversion applications. The study of micro/nano-structures on pool boiling provides a new insight on effectively enhancing boiling heat transfer.

6.4 Recommendations for future work

Additional areas in which this work can benefit from further research include the following:

6.4.1 NW structure aging testing

NW coated surface have demonstrated superior pool boiling performance compared to plain surfaces, however there remains a question that needs to be investigated- “aging”. Many nanostructure / nanomaterials and nanoparticle modified surfaces lose their enhancement characteristics as the surface gets aged. The surface structure may get peeling off or degradation after long hours of operation. It is still

unknown if the same aging problem exists for NW structure, although repeatedly testing shows no derivation on boiling performance of NW coated surfaces. Still, a systematic aging test of all NW structures is recommended as it would provide useful information on the life cycle of the NWs.

6.4.2 Effect of NW geometry on boiling

For flat nanowired surface, so far the 35 μm SiNW surface has the best boiling heat transfer performance, but it is still uncertain if the correlation between the NW height and enhancement will be hold when NW height is even higher (i.e. $h > 50\,\mu m$). In addition, the surface cavity induced by NW structure has proven to be one of the critical factors affecting nucleate boiling and it is directly related to the NW density. By quantifying the surface cavity and building a correlation between NW density and the amount of surface cavity would provide a better understanding for the boiling enhancement mechanism at micro/nano scale.

6.4.3 Verify the hydrodynamic theory

The pool boiling on nanowired surface and plain Si surfaces were both studied and it is found that these two kinds of surfaces represent two extremes: The nanowired surface exhibits a large capillary force (superhydrophilicity) while the plain Si surface has no capillary force at all. CHFs on SiNW coated surface and plain Si surface are consistent with the predictions of the hydrodynamic theory with a higher nucleation site density assumed for the SiNW coated surfaces. This finding indicates that the CHF is a result of pool hydrodynamics while the surface properties modify the corresponding hydrodynamic limits. This hypothesis can also be supported by that HTC in pool boiling

can be generally correlated with a single-phase forced convection process and the dominant thermal resistance comes from the bubble dynamics. The surface dry-out would be much easier to occur when the vapor transportation is not efficient enough. Since the SiNW can be synthesized with controllable morphology, by conducting pool boiling tests on nanowired surfaces with different NW density, the hypothesis can be tested. If the CHF data on those surfaces could be matched by the prediction of hydrodynamic theory with assumed nucleation-site densities, it suggests that the CHF model based on the hydrodynamic theory is universally applied and surface properties modify the corresponding hydrodynamic limits.

6.4.4 Comparison of pool boiling and thin film boiling

In pool boiling the occurrence of CHF could result from pool hydrodynamics whereas there is no such liquid pool present in a thin film boiling. In thin film boiling, the dry-out is primarily due to the capillary limit. A comparison of these two could clarify the effect of liquid pool in pool boiling, especially with the existence of nanostructures.

6.4.5 Applying micro/nano structure in flow boiling

The significant pool boiling enhancement induced by nanowire and micro/nano structure may provide insights on flow boiling enhancement. It is still uncertain how nanowire structure would affect the boiling flow, as it may produce more flow resistance and provide capillary force at the same time. The flow boiling test on nanowired surface would be a very interesting project to work on.

APPENDIX A

Labview VI for the data acquisition

The screen shots of the LabView front panel VI and block diagram are shown below. In order to monitor the steady state for data recording, an indicator was integrated into the VI. This indicator, in the form of a green light, turns on when all thermocouples are only varying by the standard noise, determined as twice the standard deviation from the calibration. Over a course of 12.5 seconds, if the recording temperatures from all thermocouples do not show a derivation beyond the normal nose, the green light will be on indicating the boiling system has reached steady state. For Si-based substrate (400~450 μm in thickness) testing, only thermocouples T_1- T_4 are needed for calculation. For Cu-based substrate (about 3 mm in thickness), an extra thermocouple (T_5) is insert into the sample through the sidewall for extrapolating surface temperature on Cu surface.

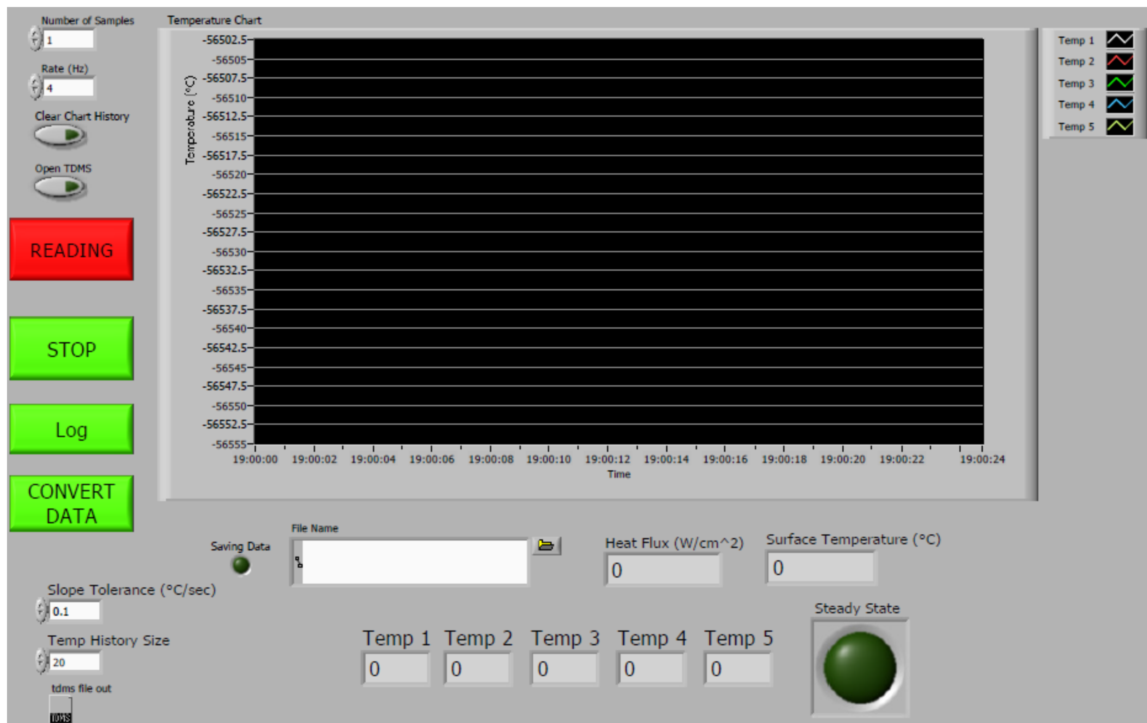


Figure A.1 Screenshot of the front panel for boiling data acquisition

Figure A.1 shows the front panel for the data acquisition, recording date will be automatically saved in a txt file after pressing LOG. The slope tolerance is used for calculating and indicating the steady state of pool boiling and a value of 0.01 is recommended for accuracy in this boiling test.

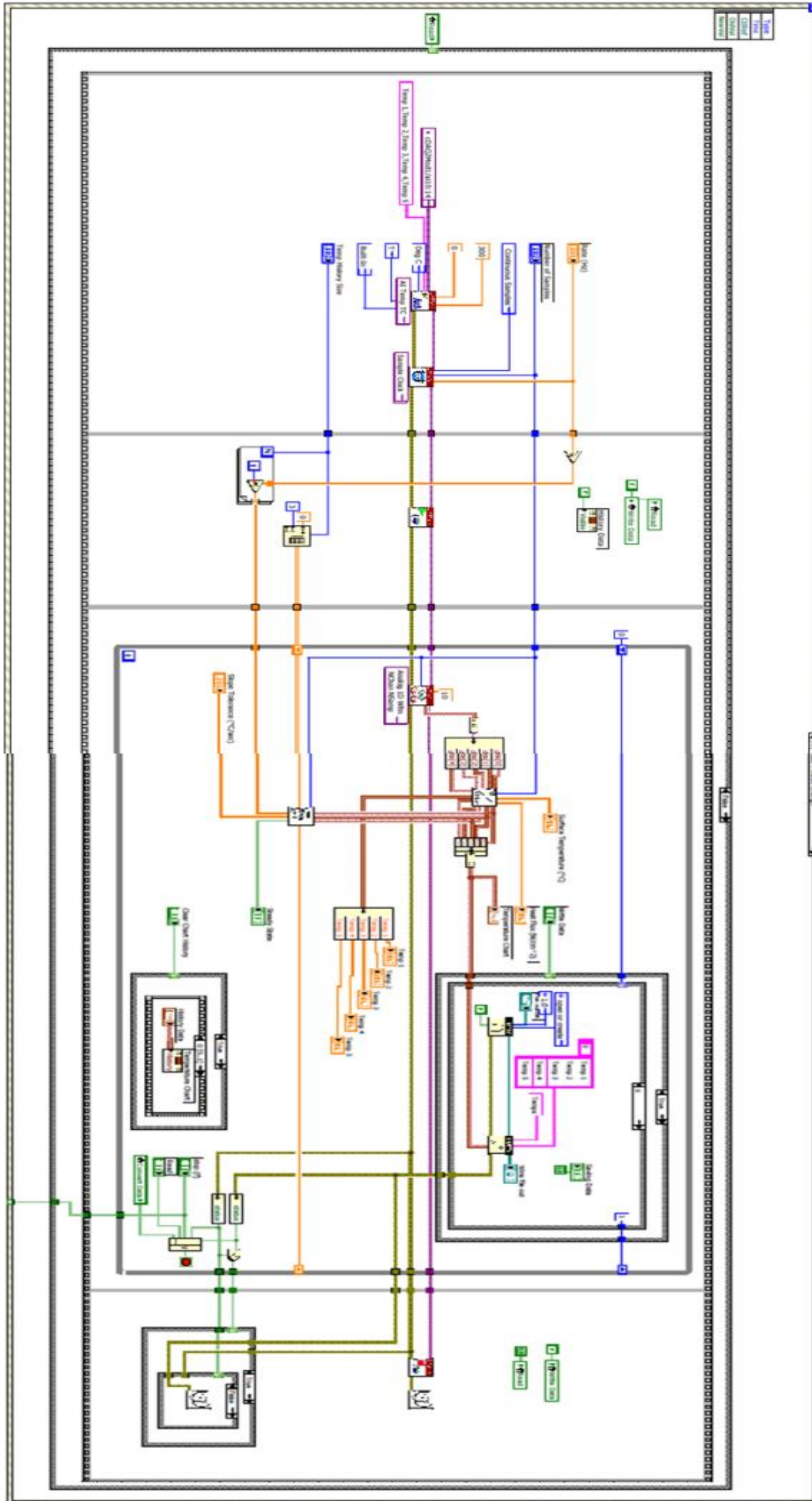


Figure A.2 Overview of the block diagram of the DAQ

The block diagram of the DAQ is divided into two parts shown below for a better view. In figure A.3, the date type terminals and block diagrams responsible for the icon terminals of front panel are defined. The digital data is converted from analog data by the NI-cDaq-9172 hub in channel 10~14 which is connected with a working station by USB connector. The AI Temp TC diagram contains the input data channel, data sources and max/min value of the temperature value allowed in the temperature VS time waveform in front panel shown in figure A.1 (in the diagram, the max and min value of the temperatures are set as 300 and 0 degree C, respectively). The date type of Temp History Size and Number of Samples is 32-bit signed integer numeric, while for the Rate, it is double-precision floating-point numeric. The recording rate is set as 4 Hz for the current boiling tests. In this part, icon terminals such as Read, Write Date, and History Date are also defined.

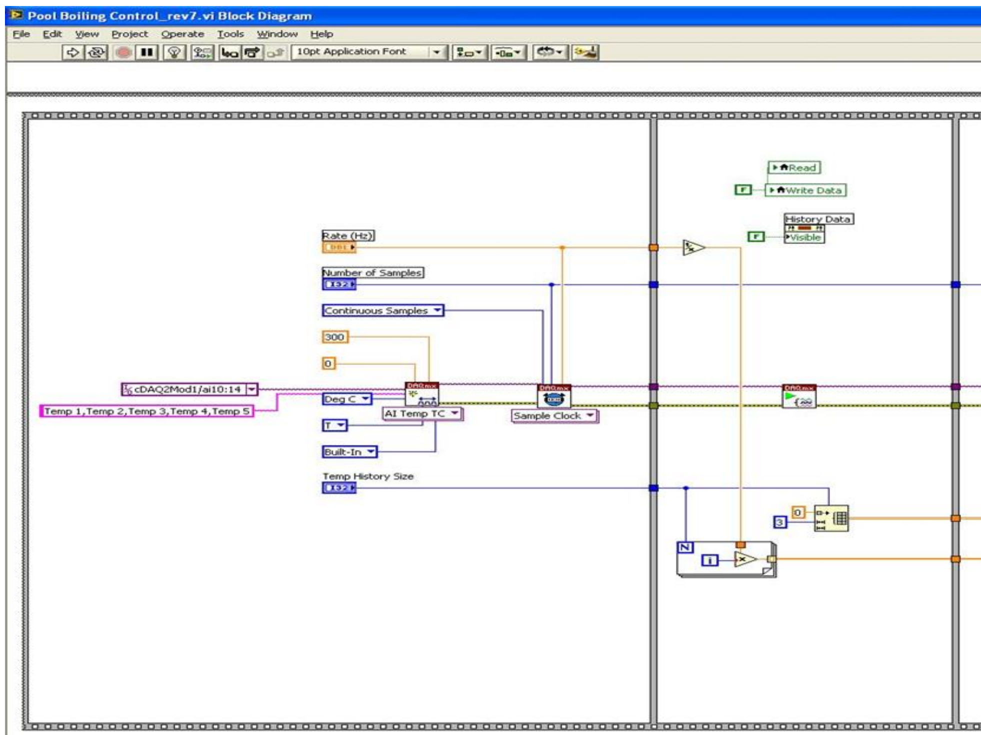


Figure A.3 First part of the DAQ block diagram

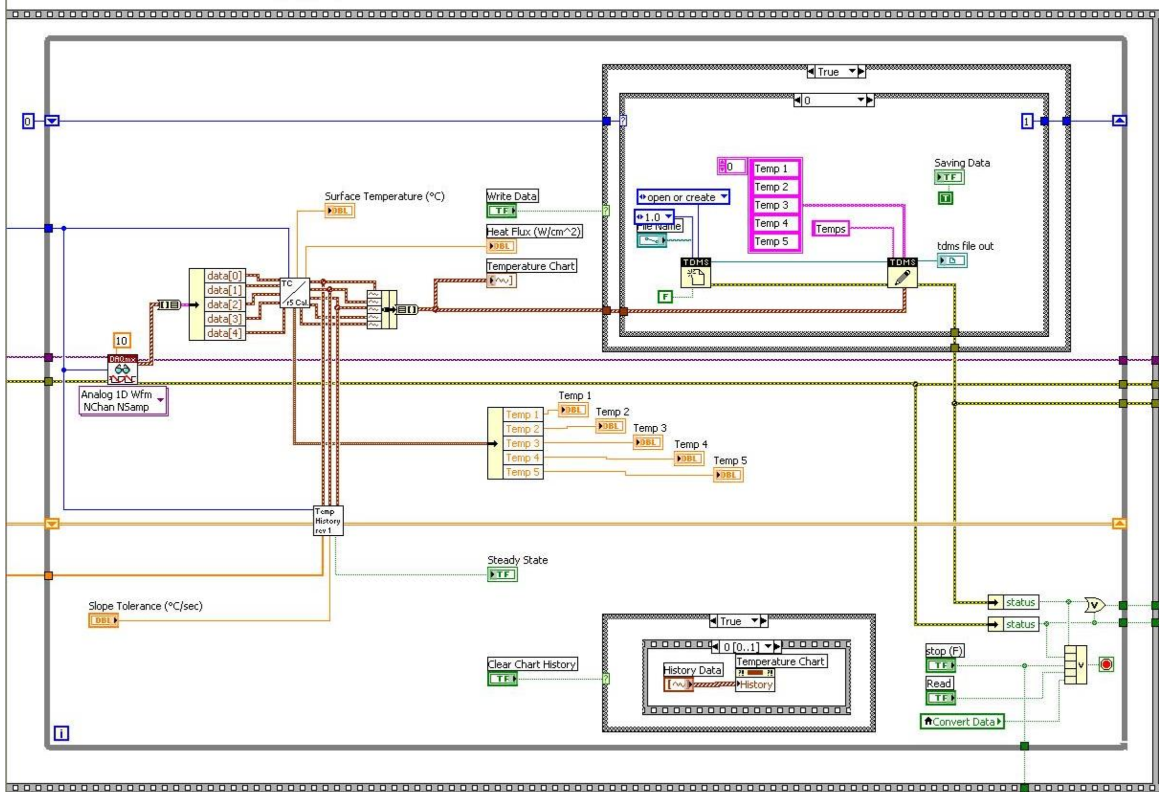
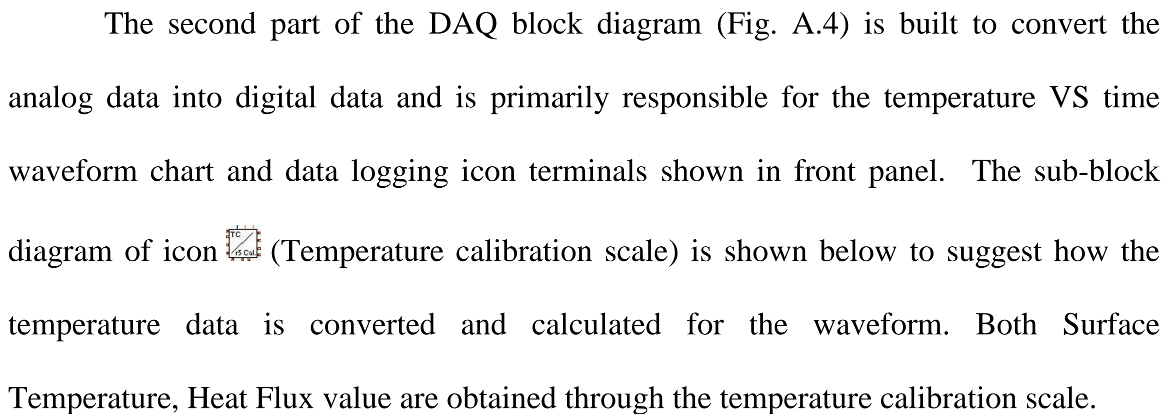


Figure A.4 Second part of the DAQ block diagram



The second part of the DAQ block diagram (Fig. A.4) is built to convert the analog data into digital data and is primarily responsible for the temperature VS time waveform chart and data logging icon terminals shown in front panel. The sub-block diagram of icon (Temperature calibration scale) is shown below to suggest how the temperature data is converted and calculated for the waveform. Both Surface Temperature, Heat Flux value are obtained through the temperature calibration scale.

The date output is realized by the Write Date function (default as True during the tests). When the icon of Log is turned on green in the front panel, a tdms file (default file type) will be automatically generated and the data will be logging in the destined format. The logging data will be checked simultaneously to ensure no error occurs. In the event a date shows unknown data type or exceeds the pre-set limits, an error message will pop-up

and indicate the error type, without interrupting the data logging process. The ions of Clear Chart History, Stop and Read on the front panel are also setup by True/False loop shown in Fig. A.4.

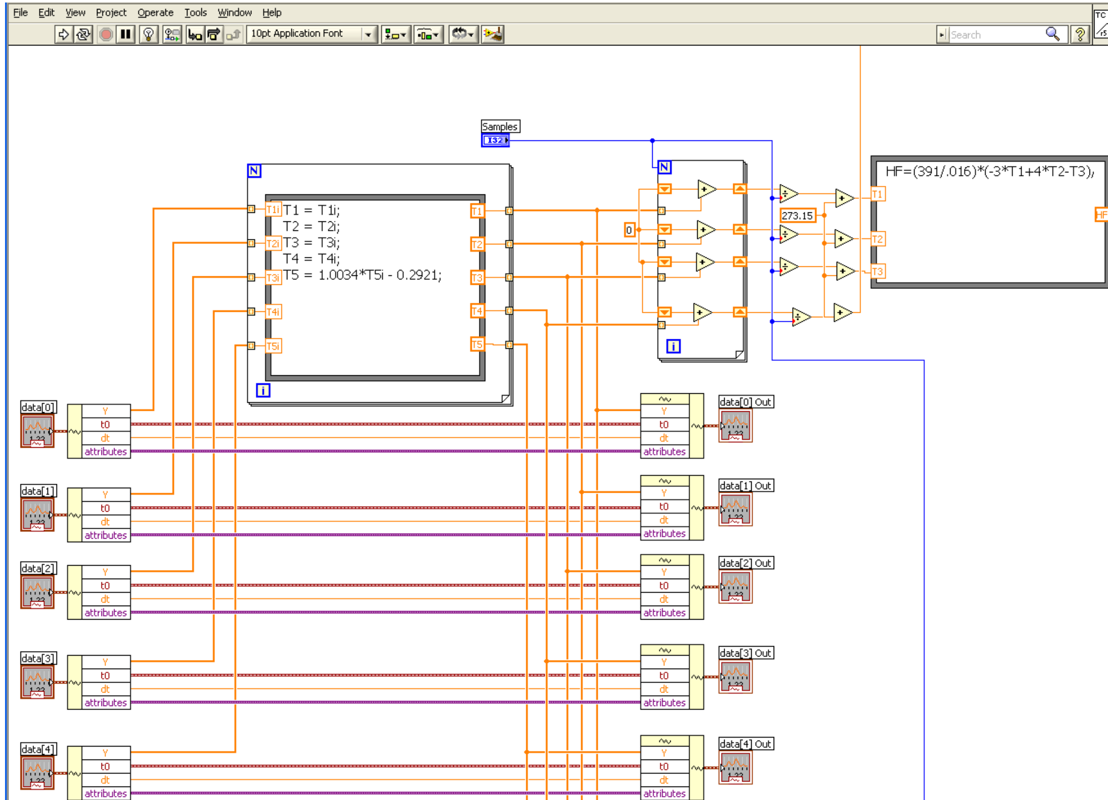


Figure A.5 Sub-block diagram of the temperature calibration scale

APPENDIX B

Matlab program for cavity approximation on NW surface by imaging process [131]

The cavity calculation is realized by converting the grayscale image to binary image. The output image replaces all pixels in the input image with value 1(white) and replaces all other pixels with the value 0 (black). Specify the gray thresh hold value in the range [0,1]. This range is relative to the signal levels possible for the image's class. Because in the SEM images of NW surface, the grayscale of cavity area is always lighter than NW area due to contrast difference, therefore by setting up the gray thresh hold value, the cavity area can be distinguished from NW area.

Matlab code for cavities and NW number count calculation of NW surfaces (fig. 2.5 and fig.3.3)

```
I1=imread('fig.3.3(a).jpg');
figure,imshow(I1)

graythresh1= graythresh(I1)    "computes a global threshold (level 1) that can be used to
                                 convert the image to a binary image with im2bw. Level
                                 is a normalized intensity value the lies in the range
                                 [0,1]."

I11 = ones(size(I1))-im2bw(I1); ; "defines the I11 as an array of the binary matrix"
figure, imshow(I11)
```

```
BW1 = edge(I11,'canny',graythresh1); "Use Canny algorithm to find the edges of objects
                                      in images"

figure, imshow(BW1)

L = bwlabel(BW1);
imshow(label2rgb(L, @jet, [.7 .7 .7]))

return
I1=imread('fig3.2(b).jpg');
figure,imshow(I1)

graythresh1= graythresh(I1)
BW1 = edge(I1,'canny',graythresh1);
figure, imshow(BW1)
Dark_area2 =length(find(I1<graythresh1))/(size(I1,1)*size(I1,2))

I1=imread('fig.3.2(c).jpg');
figure,imshow(I1)

graythresh1= graythresh(I1)
BW1 = edge(I1,'canny',graythresh1);
figure, imshow(BW1)
Dark_area3 =length(find(I1<graythresh1))/(size(I1,1)*size(I1,2))


I1=imread('fig.3.2(d).jpg');
figure,imshow(I1)

graythresh1= graythresh(I1)
BW1 = edge(I1,'canny',graythresh1);
figure, imshow(BW1)
Dark_area4 =length(find(I1<graythresh1))/(size(I1,1)*size(I1,2))
```

```
[Dark_area1 Dark_area2 Dark_area3 Dark_area4]


return
I2=imread('fig.4.1(a).jpg');
figure,imshow(I2)

graythresh2= graythresh(I2)

bw = im2bw(I2,graythresh(I2));
figure,imshow(bw)
BW1 = edge(I2,'canny');
figure, imshow(BW1)
Dark_area2 = length(find(I2<graythresh(I2)*255))/(size(I2,1)*size(I2,2))


I3=imread('fig.3.2(c).jpg');
figure,imshow(I3)

graythresh3= graythresh(I3)

bw = im2bw(I3,graythresh(I3*0.5));
figure,imshow(bw)
BW1 = edge(I3,'canny');
figure, imshow(BW1)
Dark_area3 = length(find(I3<graythresh(I3)*0.5*255))/(size(I3,1)*size(I3,2))


I4=imread('fig.3.2(d).jpg');
figure,imshow(I4)
```

```
graythresh4= graythresh(I4)

bw = im2bw(I4,graythresh(I4)*1.25);
figure,imshow(bw)
BW1 = edge(I4,'canny');
figure, imshow(BW1)
Dark_area4 = length(find(I4<graythresh(I4)*1.25*255))/(size(I4,1)*size(I4,2))

Ia=imread('fig.4.1(a).jpg');
figure,imshow(Ia)

graythresha= graythresh(Ia)

bw = im2bw(Ia,graythresh(Ia));
figure,imshow(bw)
BW1 = edge(Ia,'canny');
figure, imshow(BW1)
Dark_areaA = length(find(Ia<graythresh(Ia)*255))/(size(Ia,1)*size(Ia,2))


Ib=imread('fig.4.1(b).jpg');
figure,imshow(Ib)


bw = im2bw(Ib,graythresh(Ib));
figure,imshow(bw)

Dark_areaB = length(find(Ib<graythresh(Ib)*255))/(size(Ib,1)*size(Ib,2))

[Dark_area1 Dark_area2 Dark_area3 Dark_area4]
```

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