

INTEGRATED INJECTION LOGIC

By

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ABSTRACT

Since Integrated Injection Logic was developed in 1972, it has found applications in LSI memories, microprocessors, digital wrist watches, A/D and D/A converters, and other custom IC's. The characteristics of a typical IIL gate are comparable to those of CMOS devices. Propagation times as low as 63 ns and power consumptions as small as .01 mW per gate have been achieved in well developed IIL processes.

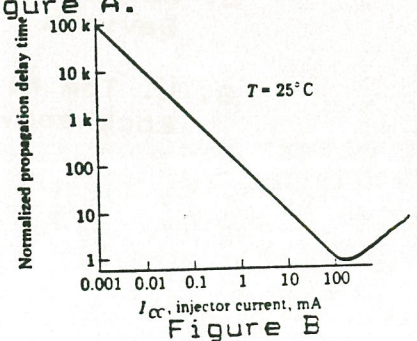
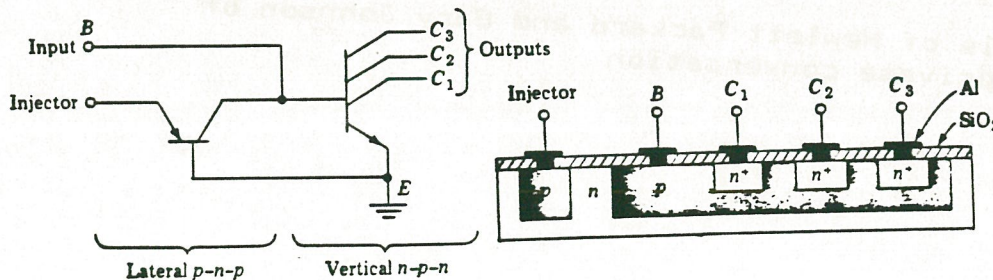
The major benefit that IIL has over other logic families is its relative simplicity. A standard IIL process only requires four masks, (base diffusion, emitter diffusion, contact cuts, and metallization). No isolation is required for an IIL process thus no epitaxial layer is needed nor is ion implantation or localized oxidation.

IIL gates were processed as part of a double diffused bipolar project. Functional tests were performed on NOR and AND gates as to examine aspects of the design and processing. Suggestions for improving device characteristics for future IIL designs are also given.

INTRODUCTION

Integrated Injection Logic is much like Direct Coupled Transistor Logic. In appendix A, Fig. 4.13-1 thru 4.13-4 show the evolution of IIL circuits from DCTL. The major advantage of using IIL over DCTL is that IIL makes use of a merged transistor design that saves real estate on the chip. Also the relative simplicity in circuit design makes the layout of an IIL gate very easy. From figure 4.13-3 to figure 4.13-4 in Appendix A note that the pull up resistors R_b have been replaced with PNP transistors with common emitters and bases. This is done to reduce the large space required to fabricate the resistors on a chip.

Because the circuit design calls for a PNP transistor to be connected to an NPN transistor and since the base of the PNP is connected to the emitter of the NPN and the collector of PNP to the base of the NPN, the two transistors may be merged together and share like diffusions as illustrated in figure A.



The emitter of the lateral PNP is referred to as the injector. It is biased thru an external resistor, R_{INJ} to a positive supply voltage. By adjusting the value of R_{INJ} , the propagation times can be made faster at the expense of power consumption. Figure B shows a plot of propagation delay time as a function of the injector current for the Texas Instrument SBPD400 IIL chip.

THEORY

To have a successful IIL process for LSI circuits where a large number of gates will be cascaded together, it is necessary for each to have a current gain of at least one. Consider the circuit in figure C.

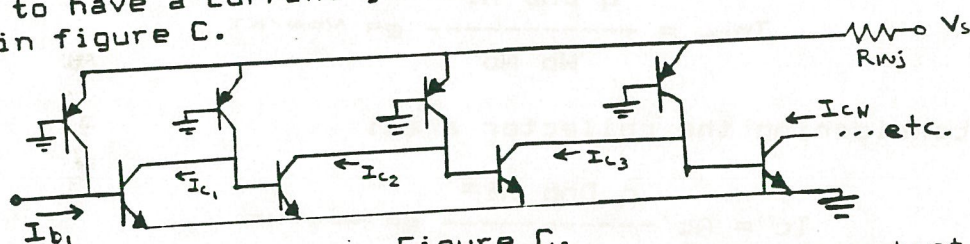


Figure C.

If the PNP lateral transistors are considered as constant current sources then the small signal gain can be expressed as:

$$1. \quad \text{Gain} = \frac{I_{cN}}{I_{b1}} = -\text{Beta}^N$$

Thus if Beta is less than one, the small signal gain of the chain will be degraded with each stage until it cannot be distinguished from the background noise. If Beta is greater than one, then digital operation of the circuit will be from a high state of V_{be} to a low of $-V_{ce \text{ sat}}$, regardless of the number of stages in the circuit. However, the NPN vertical transistors in an IIL circuit operate in reverse mode, so high gains are hard to come by.

Let's examine the gain for a reverse mode NPN vertical transistor. The gain can be found from the minority carrier concentrations under active biasing.

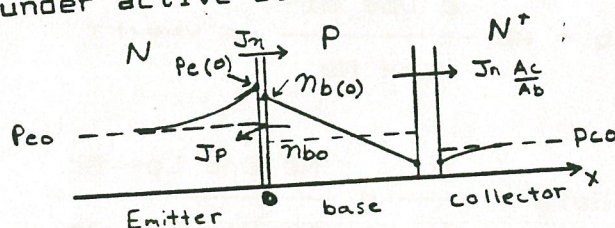


Figure D.

The electron current injected from the emitter into the base can be expressed as:

$$2a. \quad J_n = q D_{nb} \frac{d}{dx} (n_b - n_{b0})$$

Similarly, the hole current flowing from the base into the emitter can be expressed as:

$$3a. \quad J_p = q D_{pe} \frac{d}{dx} (p_e - p_{e0})$$

In the regions where the base width is short, (the width of the base is less than one diffusion length), electrons injected from the emitter into the base will diffuse across the base with no recombination. The electrons are quickly swept away at the base-collector junction by the reverse biased field. Thus the concentration gradient in the base will be linear and since n_{b0} is many orders of magnitude less than $n_b(0)$ under bias:

$$2b. \quad \frac{d}{dx}(n_b - n_{b0}) = \frac{n_b(0)}{W_b} = \frac{n_{b0}}{W_b} e^{q V_{be}/KT}$$

Where $n_{b0} = n_i^2/N_b$

Thus:

$$2c. \quad J_{n_{be}} = \frac{q D_{nb} n_i^2}{W_b N_b} e^{q V_{be}/KT}$$

And considering the collector area:

$$2d. \quad I_c = A_c \frac{q D_{nb} n_i^2}{W_b N_b} e^{q V_{be}/KT}$$

For the hole current in the emitter, since the width of the emitter is greater than the diffusion length, (L_{pe}), the charge gradient at the emitter-base junction can be shown as:

$$3b. \quad \frac{d}{dx}(p_e - p_{e0}) = \frac{p_e(0)}{L_{pe}} = \frac{p_{e0}}{L_{pe}} e^{q V_{be}/KT}$$

Where $p_{e0} = n_i^2/N_e$

Thus:

$$3c. \quad J_{p_{be}} = \frac{q D_{pe} n_i^2}{L_{pe} N_e} e^{q V_{be}/KT}$$

And considering the base area:

$$3d. \quad I_b = A_b \frac{q D_{pe} n_i^2}{L_{pe} N_e} e^{q V_{be}/KT}$$

And

$$4. \quad \text{Beta} = \frac{I_c}{I_b} = \frac{N_e D_{nb} L_{pe} A_c}{N_b D_{pe} W_b A_b}$$

By examining equation 4 one can manipulate the processing conditions to get a good gain. However, since the vertical transistors are operating in reverse mode, the substrate is the emitter and the doping profile will look something like figure E.

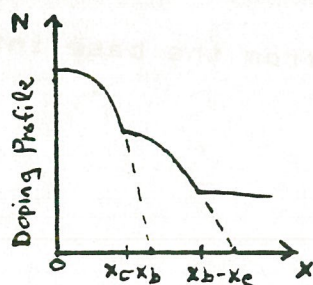


Figure E

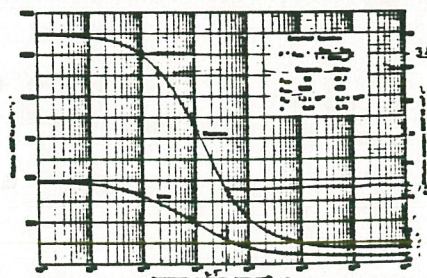


Figure F

Thus, as a consequence of the geometries, N_b must be greater than N_e and N_e/N_b is less than one. However, this should be made as close to one as possible. Note that when a low boron concentration is required, after a long drive-in and subsequent oxidations, the surface in the base region may become depleted of boron. This problem may be avoided by doing a double boron diffusion. After doing the base drive-in, the wafer may be remasked with the base mask and a second, very short, predeposit of boron may be done before proceeding with the process.

Looking at the ratio of D_{nb}/D_{pe} from figure F, shows that the diffusivity ratio is favorable. For $N_e=2.0E15$, $N_b=1.0E16$:

5. $\frac{N_e}{N_b} = 0.2$

$$\frac{D_{nb}}{D_{pe}} = \frac{32}{12} = 2.67$$

L_{pe} is determined by the emitter doping concentration. For $N_e=2.0E15$, The diffusion length L_{pe} is:

6. $L_{pe} = 20 \text{ um}$

How small can we make the base width? The base width is limited by the punch-thru voltage. Punch thru occurs when the depletion width of the B-C junction extends across the entire width of the base. It can be determined as follows.

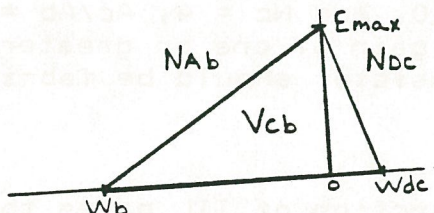


Figure G

7. $\frac{dE}{dx}(\text{base}) = \frac{E_{max}}{W_b} = \frac{q N_b}{\epsilon s i}$ $\frac{dE}{dx}(\text{coll}) = \frac{E_{max}}{W_{dc}} = \frac{q N_b}{\epsilon s i}$

8. $W_{\text{depletion}} = W_b + W_{dc} = \frac{N_c + N_b}{N_c} W_b$

9. $V_{ce} = .5 E_{max} W_{\text{depletion}}$

Thus combining eq. 7, 8, and 9:

10. $W_b \text{ min.} = \frac{2 V_{ce0} \epsilon s i N_c}{q N_b (N_c + N_b)}$

For a 10v source $W_b \text{ min.}$ will be 1.08um. The maximum gain from equation 4 using the values from 5, 6, and 10, will be:

11. $\text{Beta} = \frac{(1) (32) (20) A_c}{(5) (12) (01) A_b} = 10.67$

DESIGN RULES

When designing the physical layout of an IIL gate, one should obey the following ground rules.

1. All collectors should be square.
2. The space between collectors should be Md .
3. The width of the base diffusions should be $Wc + 2Md$.
4. The contacts to the injector rail should be at the end of the injector diffusions so that the base diffusions need not extend beneath the injector metallization.
5. Injector rails should be placed between each base diffusion.
6. The emitter/substrate contact should be N^+ doped and should be made large as to minimize its resistance.

Where: Wc = Topographical collector width
 Md = Minimum dimension allowed

If the Ground Rules are obeyed, the ratio of areas may be found from:

$$A_c/A_b = \frac{Wc}{(Wc + 2Md)[Nc(Wc + Md) + Wc]}$$

For $Wc = 30$, $Md = 10$, and $Nc = 4$, $A_c/A_b = .095$ and $Beta = 1.01$. Therefore to get a gain of one or greater, no more than four collectors per transistor should be fabricated in this process.

EXPERIMENT -

To test the function of IIL gates that had been fabricated as part of EMCR650, the gate shown in figure H was chosen. The circuit consists of a NOR gate and an AND gate. Upon testing the logical operation of the circuit using $R_o = 330K$, $R_{INJ} = 1K$, and $V_s = 5$ volts. The data in figure 6 was obtained.

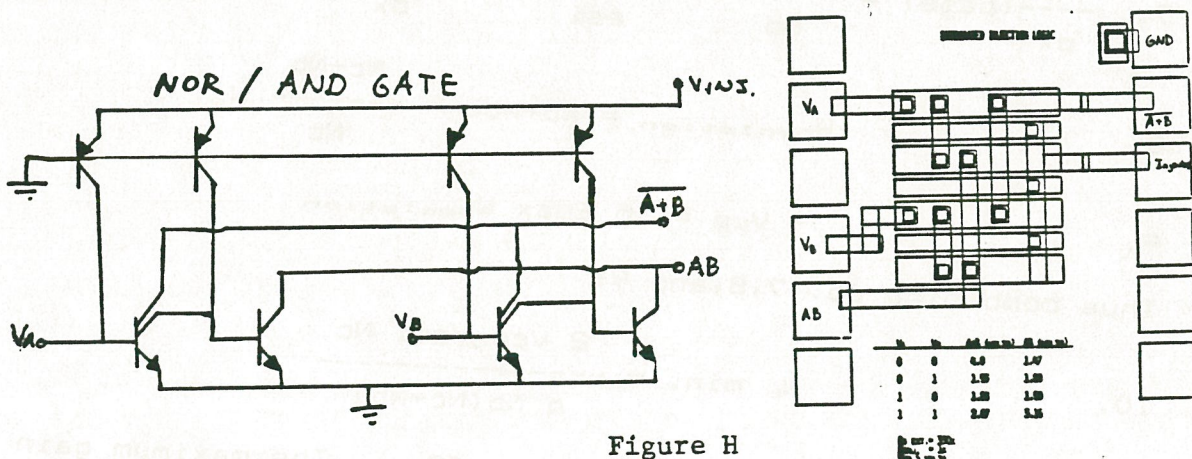


Figure H

RESULTS AND DISCUSSION

The on voltage of the NOR gate was measured to be 4.0 v. This drop of one volt across R_o when the transistor should be

off is due to the NPN transistor leakage current. The higher than expected output of about two volts observed when the output should be low is caused by an internal emitter resistance of 550 ohms. (see appendix B) This was determined by examining V_{ce} at $I_c=0$. At $V_{ce}=0$, $dV_{ce}/dI_b = 550 \text{ OHMS}$. Notice that the collector current is negative until the collector voltage becomes greater than the drop across the internal emitter resistance. This is a big problem and should try to be avoided by making the emitter contact big, N^+ doped, close to the gates, and sintering well. With this emitter resistance present, one can never achieve a low state of zero volts. Also the leakage current is quite significant when a supply voltage of five volts is used because of the low breakdown voltage, $V_{ce0} = 6 \text{ volts}$. The breakdown voltage is low due to the high doping concentration of the base.

The gain of the reverse mode NPN was only .08. So the logical voltage swing is degraded with each stage. This is seen from the voltage swing of the AND gate which is lower than the swing of the NOR gate because the AND gate is a two stage device while the NOR gate a one stage device.

CONCLUSION

The reason why the gain is so low in this circuit is that the doping of the base in those devices was high, about $5.0 \text{ E}16$, and $A_c/A_b = .067$. Appendix C shows the doping profiles as modeled by SUPREM and the gain calculations. Please note that this gate was processed along with discrete transistors with goal of obtaining high forward gains. (Appendix D)

However, the results are encouraging. Although the voltage swings, from logic one to logic zero, are small, they are definitely present and in correlation with the expected operation of these gates. If the IIL gates are more carefully designed and the processing is performed to get high reverse mode gains, functional LSI IIL gates should be no problem.

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J. Lekas: His circuit design used for testing is shown in figure 8
R. Turkman: The affect of A_c/A_b on the reverse mode current gain.
P. George: For helping me put this report together.

APPENDIX A

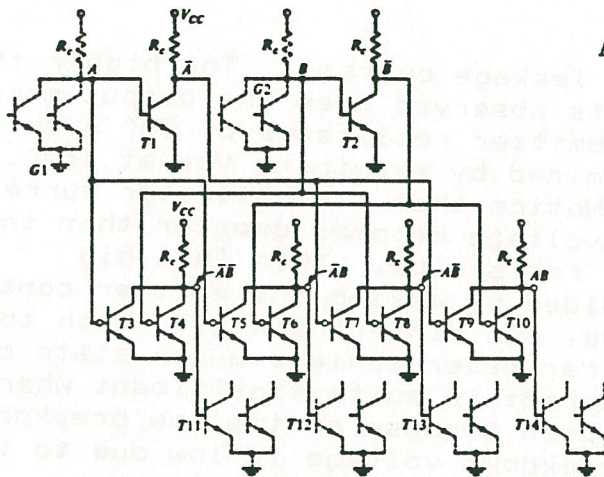


FIGURE 4.13-1
A DCTL gate structure which generates AB , $\bar{A}\bar{B}$, $\bar{A}B$, and $A\bar{B}$ from the logical variables A and B .

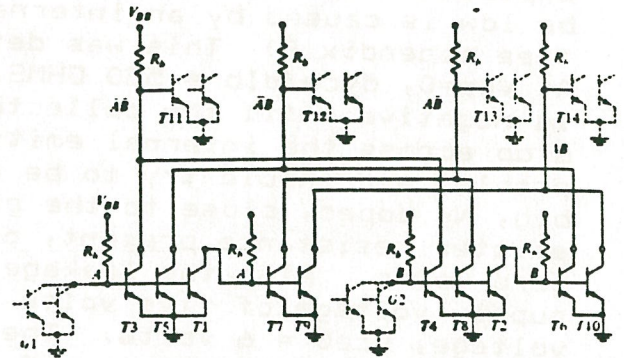


FIGURE 4.13-2
Figure 4.13-1 redrawn to group transistors with common base connections.

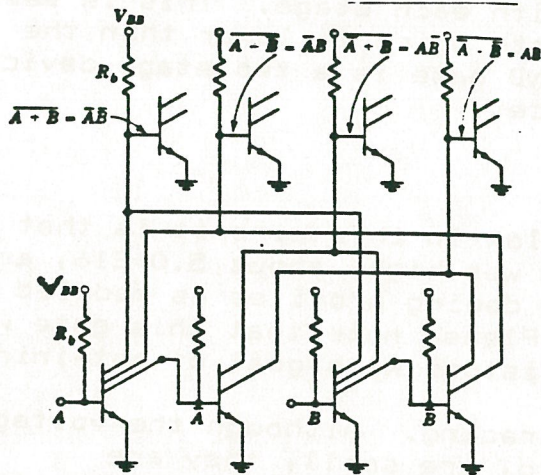


FIGURE 4.13-3
Figure 4.13-2 redrawn with multiple-collector transistors.

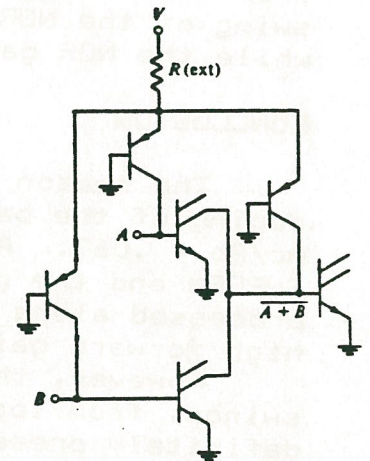
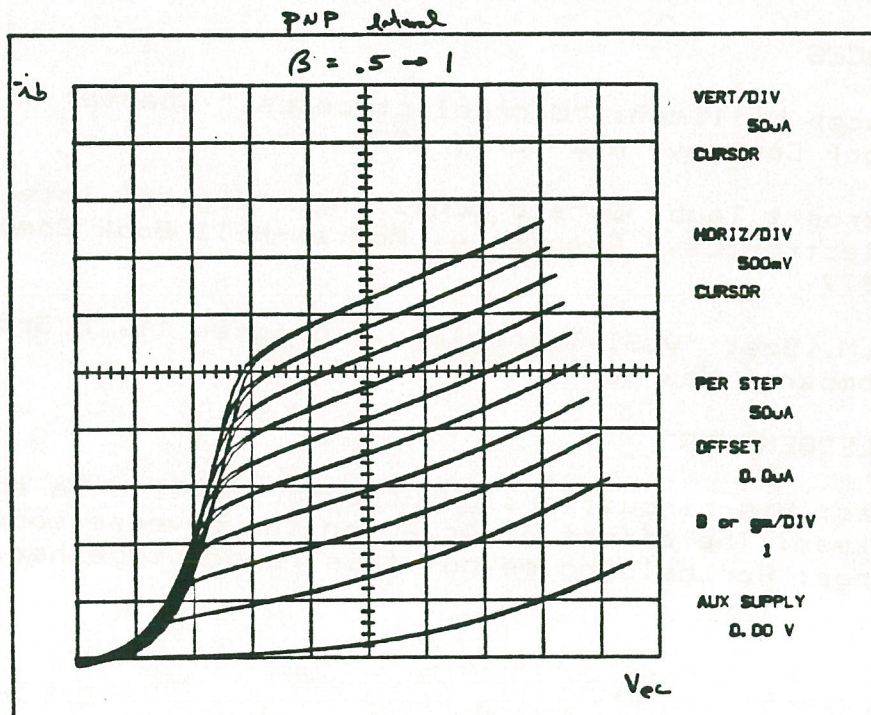
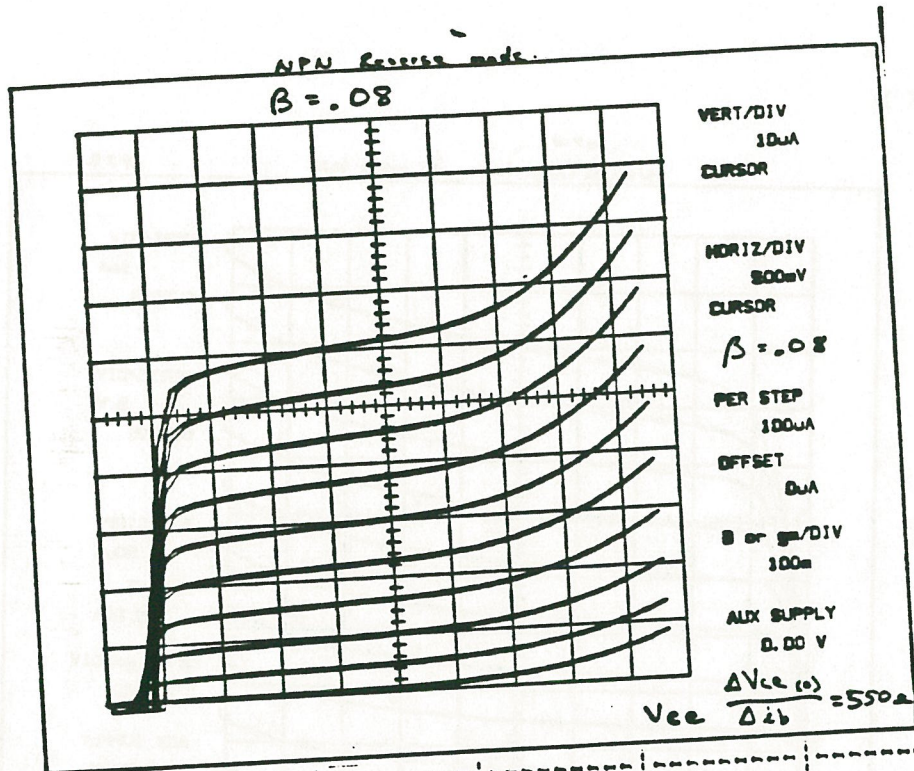


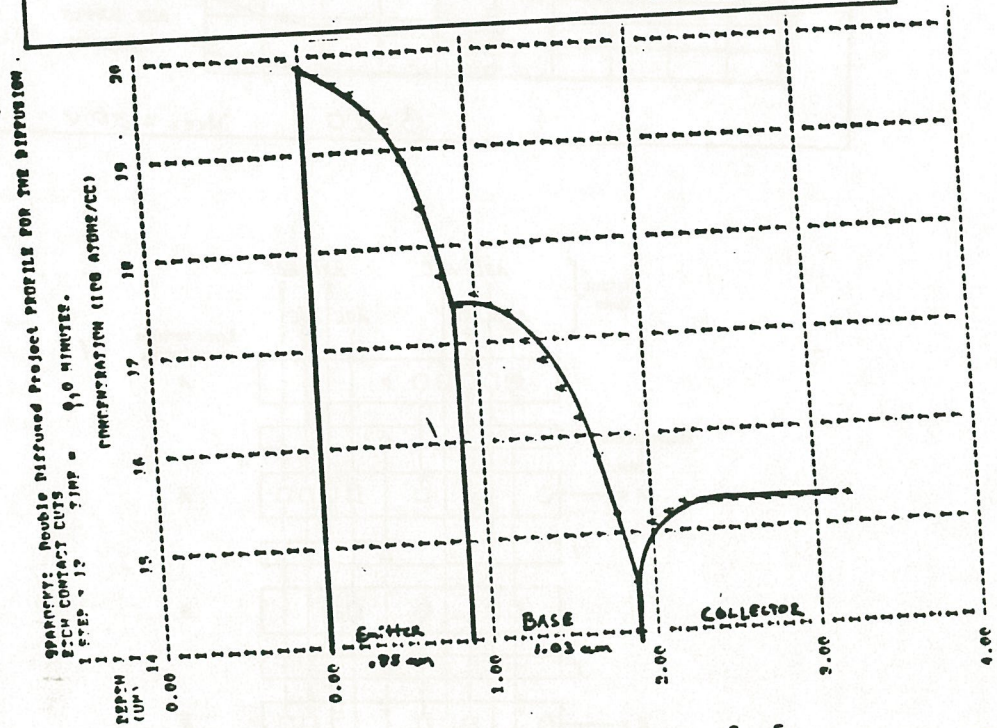
FIGURE 4.13-4
The basic configuration of IIL gates.



APPENDIX B



APPENDIX C



Current Gain for hfe



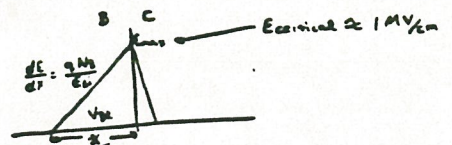
$$J_c = q D_b \frac{dN_b}{dx} \frac{A_c}{A_b}$$

$$J_b = q D_b \frac{dN_b}{dx} \frac{A_b}{A_c}$$

$$\beta = \frac{J_c}{J_b} = \frac{D_b A_b h_{fe} \frac{A_c}{A_b}}{D_b N_b w_b \frac{A_b}{A_c}} = \frac{h_{fe} (A_c)^2}{N_b w_b (A_b)^2}$$

$$\beta = 1.67 \times 10^{-6} = .11$$

$$\beta = 10.67 \times 10^{-6} = .11$$



$$\frac{dE}{dx} = \frac{q N_b}{\epsilon_s} = \frac{E_{cb}}{x} \Rightarrow x = \frac{E_{cb} \epsilon_s}{q N_b}$$

$$V_{cb0} = \frac{1}{2} E_{cb} x$$

$$V_{cb0} = \frac{1}{2} \frac{E_{cb}^2 \epsilon_s}{q N_b}$$

$$V_{cb0} \approx \frac{2.012 \times 10^{17}}{N_b} = 5.62 V \quad N_b = 5 \times 10^{16}$$

$$V_{cb0} = V_{cb0} \left(\frac{1}{1+\beta} \right)^{1/2} = 5.5 V \quad \text{Breakdown}$$

If $N_b = 10^{16}$
 $A = 1$
 $V_{cb0} = 22.1 V$
 $V_{cb0} = 24.5 V$

APPENDIX D

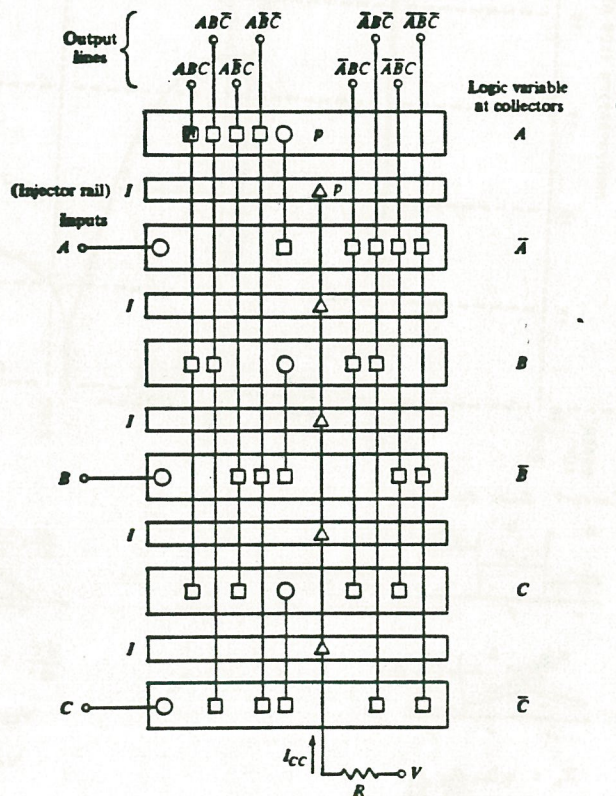
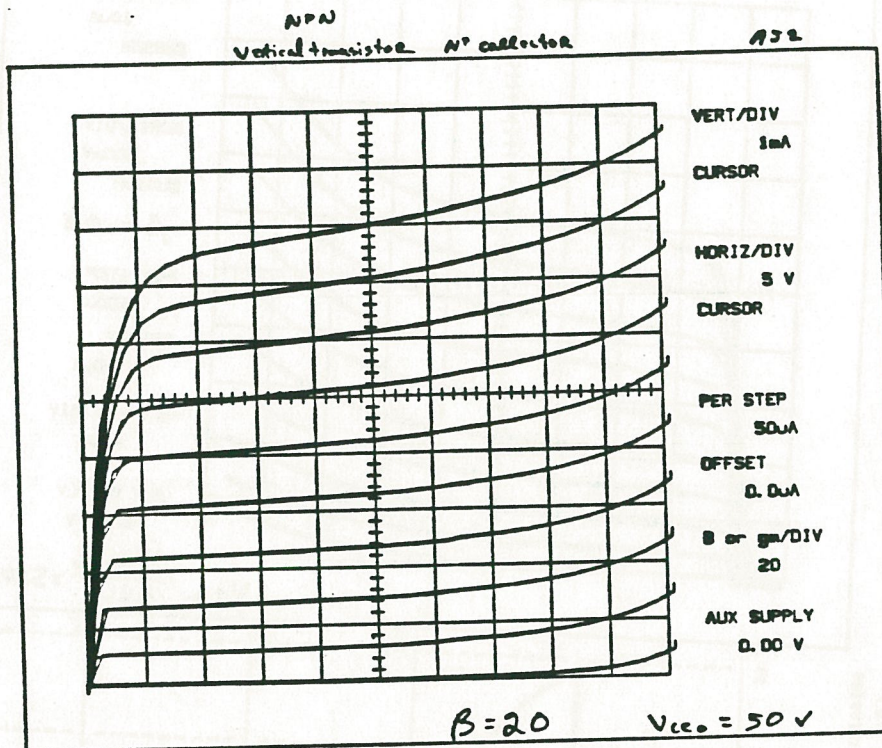


FIGURE 4.15-1
A 3-bit ILL decoder.