IDEAS TO ASICS

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ABSTRACT

The conception/completion/distribution of an integrated circuit idea is the heart of ASIC (application-specific integrated circuits) technology. Completing the transformation of an idea to the design before the market window closes is the designer's greatest concern. The evolution of sophisticated computer-aided design tools has enabled functional simulation of analog and digital together within hours. A description of the latest software methodologies is presented through an example of a possible ASIC implementation.

INTRODUCTION

Sometimes the most perfect ideas come at just the wrong time... and sometimes they don't. In the microelectronics industry, timing is everything. One of those Hewlet Packard "What if's" could be the answer to success. Innovative ideas have a lifespan that technology can take advantage of. There can be no waiting for a response from the patent office, the decision to sell the idea or build a facility to anticipate product demand must be done quickly. Present technology has made it possible to deliver complicated IC's in less than one month- application-specific integrated circuits just waiting for an idea. Engineers can organize parts once available only discretely, into systems uniquely defined to a specific function. A product whose physical size limitations would have made it impracticle previously, can be condensed into a homogeneous unit.

The increasing availability of process technology for building chips with design rules of 1.25 um and less has made available a generation of digital chips that integrate a daunting number of circuit functions. As chips grow more highly integrated, they look more and more like systems than components. Sophisticated design, simulation, and layout tools are required to meet the demands of high density integration. The revolution created by the world of computer-aided design is giving designers far greater flexibility in implementing an idea.

Application-Specific Integrated Circuits (ASIC) are computer-customized semiconductors tailored to the unique applications of customers. Considered the fastest growing segment of the semiconductor industry, ASICs will account for at least $10 billion in sales by 1990, and represent more than 25 percent of the entire semiconductor industry. Continued success in ASICs will be limited to suppliers who recognize the value of computer-aided design (CAD) tools. User-friendly integrated design tools will allow the production of a wide range of circuits- - from a few thousand gates of logic to the integration of complex computer systems (microprocessor, memory, logic) onto silicon.

Three digital ASIC design methods have evolved; metal mask programmable gate arrays, cell-based solutions, and a concept known as silicon compilation, with the object of producing designs from high level description.

Metal mask programmable gate arrays require one masking operation for interconnections by which chip performance is determined. They consist of prefabricated arrays of standard logic gates structured for use as RAMs, ROMs and Multipliers. They are the simplest and quickest to manufacture but usually consume the largest amount of silicon.

Cell-based solutions are usually semi-custom to full custom layouts of each component in the library requiring sophisticated simulation routines to guarantee desired operation the first time. They tend to be most efficient in silicon consumption and are usually limited by process technology or package considerations.

Silicon compilers are knowledge based systems which can incorporate the above solutions into a fluent arrangement. They are distinguished by their flexibility. A designer might need an arithmetic logic unit, a register file, a shifter and other elements to work at a specific clock rate within a number of busses. The compiler would arrange an efficient layout using both gate arrays and cell-based solutions.

All three design methodologies have been incorporated into a Modular Design Environment ™ which accomplishes system-scale integration. This new generation of CAD system integrates schematic entry, behavioral simulation, multi-chip simulation, and floorplanning into a single system design capability.

Schematic entry is probably the most difficult part of the process requiring the user to master a series of commands in order to input the design. VLSI circuits require very accurate modeling of the interconnections. Each first or second level metal segment, via, contact, and polysilicon gate is calculated, and individual interconnection delays must be analyzed. HCMOS (High-performance CMOS) technology can support tens of thousands of sub-nanosecond gates, but interconnection delays can be appreciable with very high circuit speeds, fine line metalization, and large chips.

Behavioral Simulation: Circuits are described and simulated at a higher level than at the individual component level. Simulation times are reduced because system port parameters representing the combined effects of the components require far less storage and compilation time. Physically realizeable networks of macrocells and megacells replace detailed circuit descriptions.

Multichip Simulation: A designer must be able to simulate a number of ICs together. The present high power 32-bit workstations run at 2-5 MIPS (million instructions per second) with a capability of synthesizing an entire system simulation in less than an hour.

Floorplanning: The designer must confirm the feasibility of laying out the design in the desired chip size and verify that the resulting delays are satisfactory.

A designer must choose whether to implement the entire design on one chip or split it up into several chips. The Design Assistant ™ enables the designer to make basic tradeoffs early in the design cycle. The purpose of the Design Assistant is to provide a quick, easy route to developing a product from the basic take-off point—a tool for nonexperts who need expert results.

The Design Assistant:

The Design Assistant has two major components; namely analysis and technology.

Analysis requires the designer to enter the number of supply voltages, the operating frequency and so on. The Design Assistant compiles a list of what is known about a single chip or each chip in a multiple-chip design. This information is passed to a second part which searches the library for possible equivalent cells and package implementations collecting all the information a human expert would need in order to evaluate the range of alternatives.

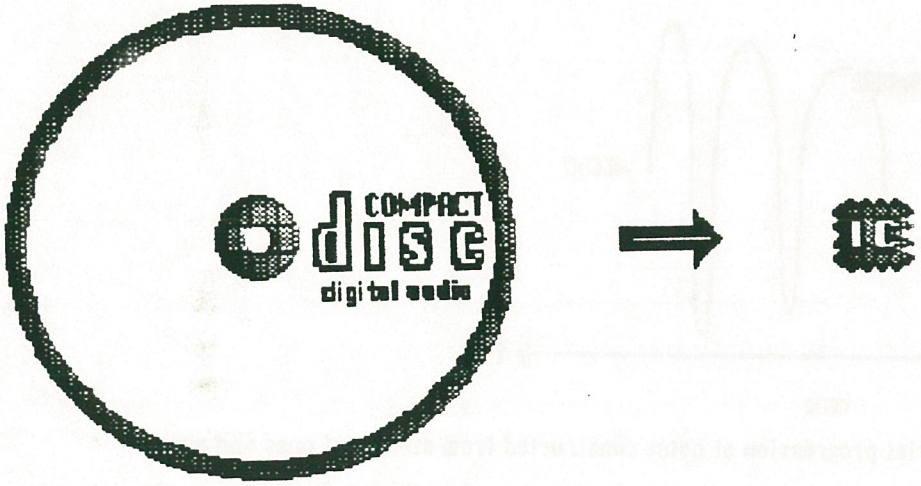
The **Technology** file contains the algorithms for estimating routing, determining which pad sets to use, selecting packages, estimating power dissipation, assessing sizes of various floor plans, and ruling out odd chip configurations.

The Design Assistant "*aids the ASIC designer in making cost and feasibility tradeoffs ... by providing feedback on chip size and power, packaging alternatives, relative cost, and performance*"- Douglas Fairbain, vice president VLSI Technology at San Jose, Calif.

Asic designs which require combinations of analog and digital components have relied on simulation models such as SPICE in conjuction with simulation systems described above. Spice makes a series of approximations as the program models each individual circuit component. When Spice looks at an analog circuit it models the behavior of the devices as if everything is working properly eliminating the ability to identify incorrect input. The program indicates when an approximation converges but this requires days or weeks of computer time for large designs.

Sierra Semiconductor has recently introduced an analog behavioral modeling system which uses a Thevenin equivalent configuration representing complex combinations of analog circuitry. Nodes or pins in digital systems need to represent a 0, 1, unknown or tristate condition. An analog node, by contrast, must possess qualities such as source resistance, load resistance, and continuous values of voltage and current. Thevenin equivalent blocks allow faster simulations of analog and digital networks together.

EXAMPLE:



*The Modular Design Environment is a proprietry CAD system from LSI Logic Corp.

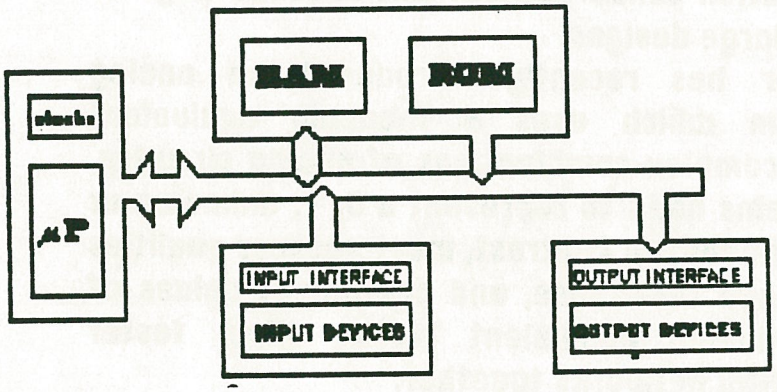
*The Design Assistant is a proprietary CAD system from VLSI Technology Inc.

*The Sierra Simulator is a proprietary CAD component from Sierra Semiconductor

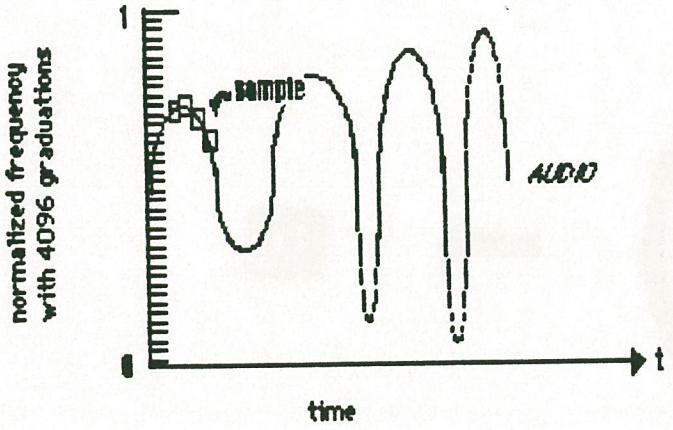
Condensing a compact disc into ultra large scale integration would enable monumetal computing abilities without the bulk of the laser and drive assemblies. This could renovate the audio marketplace by enabling a complete digital audio system to be contained in a cassette case.

Further investigation led to the developement of a mature idea with two major stumbling blocks. Over 2 billion bits of information are required to digitize an average album. Most experts agree that the levels of memory integration will reach 1 billion before the turn of the century. The limitations imposed by present process technology will be improved by direct use of ASICs in the manufacturing environment. The other problem is that few companies can incorporate analog and digital systems together, but confidence in new simulation procedures promise the expedient modeling necessary to insure first time success.

SYSTEM ARCHITECTURE



QUANTIZATION



Digital music is a serial progression of notes constructed from strings of ones and zeroes.

At a stereo sampling rate of 44.1kHz (22.5kHz per channel) with a 12-bit note size:

$$74\ \text{min} \times \frac{60\ \text{sec}}{\text{min}} \times \frac{44{,}100\ \text{samples}}{\text{second}} \times \frac{12\ \text{bits}}{\text{sample}} = 2{,}349{,}648{,}000\ \text{total bits:}$$ 300Mbyte Memory

Summary:

After perusing many publications (see reference list), two competetive companies equipped to design and fabricate application-specific integrated circuits exist. These companies have demonstrated abilities to design and fabricate monolithic application-specific integrated circuits in less than one month using sophisticated user-friendly design tools and state-of-the-art processing. The Modular Design Environment from LSI Logic and the Design Assistant from VLSI Technology can integrate complex computer systems (microprocessor, memory and logic) onto silicon. Sierra Semiconductor, has introduced hardware which can model analog and digital circuitry simulataneously.

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Special Thanks to Bill Guidici of LSI Logic Corporation