TANOS Charge-Trapping Flash Memory Structures

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***Abstract*—This work endeavored to optimize and integrate a process for depositing and patterning the gate film stack of TaN, Al_2O_3, Si_3N_4, SiO_2, Si (TANOS) charge-trapping flash (CTF) memory with an existing complementary metal-oxide-semiconductor process flow. Fabricated capacitance-voltage devices with T-A-N-O thicknesses of 2500Å, 110Å, 75Å, and 30Å respectively show characteristic charge-trapping in subsequent program/erase (P/E) cycles (likely modified Fowler-Nordheim tunneling) with a maximum possible program threshold voltage of 2.7V for 5sec 28V program and minimum erased threshold voltage of -2.5V for 5sec 15V erase, w/ total P/E threshold voltage swing 5.2V. Device wafers are currently at step 22 of 67 and will be continued in the future, eventually demonstrating hot carrier injection P/E schemes.**

***Index Terms*—Charge-Trap, EEPROM, Energy Band Engineering, Flash, Fowler-Nordheim Tunneling, Gate Stack, HEI, MANOS, Nitride, TANOS, Tantalum**

I. Introduction

THE integration of flash memory into CMOS processes has helped advance the state of non-volatile, low-power memory for portable device applications. However, electronically-erasable programmable read-only memory (EEPROM), which has been the standard for many years, is reaching it's limits in terms of scalability (notably bit/area). CTF devices, which replace the conductive floating gate of EEPROM with a charge-trap rich insulating storage layer, have found notable success owing to decreased program/erase (P/E) voltages, faster P/E, and improved reliability [] and have been roadmapped as a production replacement for EEPROM by the ITRS []. Integration of such devices into existing CMOS processes is therefore of the utmost importance.

II. Theory

A. Charge-trapping vs. Floating gate EEPROM

The flatband voltage, and thereby the threshold voltage, of a MOSFET is modified by the addition or removal of charges between the gate (control gate, CG) and channel. In EEPROM, these charges are stored in a floating gate of polysilicon isolated from the control gate and channel, usually by SiO_2 (see figure 1a). In Si-SiO2-Si3N4-SiO2-Si (SONOS) CTF the floating gate is replaced with silicon nitride (see figure 1b), which is insulating and charge-trap rich. Charge injected into the nitride, either by Fowler-Nordheim (FN) tunneling or by hot-carrier-injection (HCI, holes or electrons), is stored in it and acts to modify the threshold voltage of the device. [1] The nitride, when programmed by HCI, can also store charge in two distinct locations along the channel, sensed best by the change in GIDL by each, and makes CTF memory very desirable due to a decreased required area per bit. [2] More recently, TANOS and other so-called "band-engineered" CTF devices have replaced the oxide (barrier oxide) between control gate and storage layer with Alumina (see figure 1c) which, due to it's higher dielectric constant and potential barrier, helps suppress erase saturation and improves lifetime by preventing charge leakage from storage layer to control gate over long periods of inactivity. [3] The use of TaN as control gate improves gate control over degenerately doped polysilicon due to it's higher work function. [3]

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III. Experimental Procedure - Film Optimizations

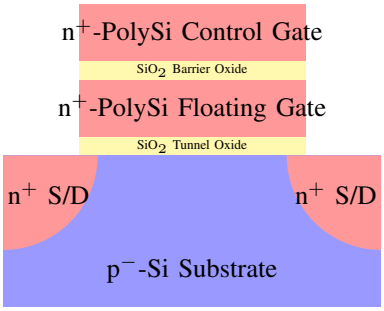
Design of processes for the deposition and patterning of the films of the CTF gate stack was an imperative part of this project. The tunnel oxide film thickness required for reasonable tunneling by FN and HCI is far thinner than previous recipes had been designed for. Similarly, the storage layer thickness must be kept thin enough so as not to impair gate control but also must not be so thin that charge is not able to be adequately stored on it. Such thin nitride demonstrated here was a first for RIT. The thicknesses in parentheses in the titles of the following sections are the target thickness levels of those films (factors) deposited on the nMOS CTF device wafers for full-factorial experimental design, investigating the impact of tunnel and barrier oxide thicknesses on device performance.

A. SiO_2 - Tunnel Oxide (30, 50, 70Å)

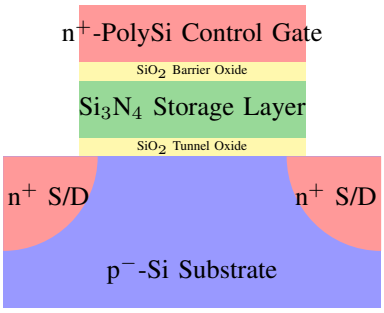
Dr. Lynn Fuller developed, and uses in his "Adv-CMOS" process, a Bruce furnace dry oxide recipe which incorporates nitrogen into the oxide during the first half of growth by using equal soaks of N_2O and O_2 at 900°C, targeting a 100Å film. By adjusting total soak time and keeping both soaks equal, it was found that the oxide growth can be modeled with a linear function of total soak starting from native oxide (≈15Å), shown in figure 2. Each point taken represents measured film thickness of two 6" Si wafers loaded into the Bruce Furnace without dummies, spaced equally from the ends of the boat and one another. The Woolam variable-angle spectroscopic ellipsometer (VASE) was used to measure thickness and optical properties of the film for each soak and showed ±.5Å thickness variation across wafers and between wafers for each run. The optical properties were consistent with a pure thermal oxide film.

B. Si_3N_4 - Storage Layer (100Å)

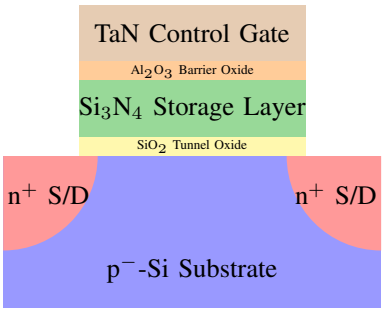
In order to deposit a pure and very thin nitride film, the SMFL Low Pressure Stoichiometric Nitride Recipe in the



(a) EEPROM



(b) Charge-Trapping Flash (SONOS)



(c) Charge-Trapping Flash (TANOS)

Fig. 1: Different charge-storage memory structures.

ASM LPCVD Tube 2 was employed with a soak time of only 1 minute. Two 6" Si wafers were loaded for each run in a similar fashion to the oxide deposition (no dummies). The test recipe deposited a 91.8Ånitride film (as measured on the VASE) with optical properties which match Si_3N_4.

C. Al_2O_3 - Barrier Oxide (100, 130Å)

Alumina is most easily deposited (at RIT) by evaporation in the CHA E-beam Evaporator. However, for such thin films the offset of the crystal film thickness monitor in the tool and the deposited thickness becomes significant. 6" wafers were loaded into the rotating platen, Al_2O_3 source in a carbon crucible was loaded, and after achieving a base pressure of at least 1×10^{-6} Torr the alumina was evaporated with a .14A beam current (after centering), stopping at the desired thickness readout on the Inficon monitor. As seen in figure 3, the measured thickness (VASE) is consistently about 1.5

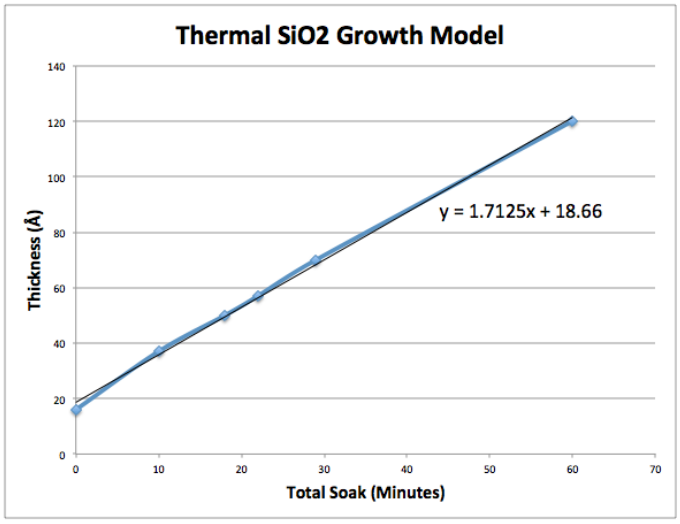


Fig. 2: Linear Growth model as a function of total soak time (minutes).

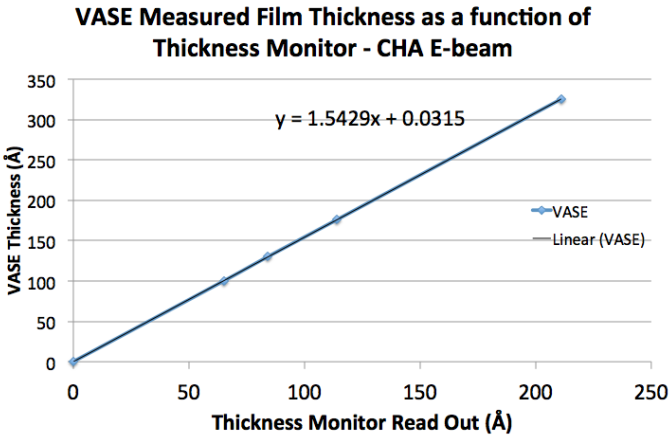


Fig. 3: Plot of measured thickness vs. Inficon monitor reading.

times the thickness monitor. Stop points to obtain desired film thicknesses were determined from this offset.

D. TaN - Control Gate

Tantalum Nitride was first reactively sputtered in the CVC601 on 2 silicon wafers and glass slides from 4 Tantalum target under 15% N2 partial pressure (16.5sccm Ar, 12.8sccm N2) at 300W DC power in 16mTorr deposition pressure with a base pressure of 1E-5 Torr. This sputter exhibited a deposition rate of ~651 angstroms/minute for Tantalum Nitride and reasonable optical properties, figure 4, describing a film of stoichiometric TaN.

IV. Experimental Procedure - C/V Device Fabrication

Three fresh 6" silicon wafers were first blanket doped with an 8E13 B11 80KeV Implant in the Varian Ion implanter and annealed in Bruce Tube 1 using the "Adv-CMOS" well-drive recipe. Following an RCA clean, SiO_2 was deposited

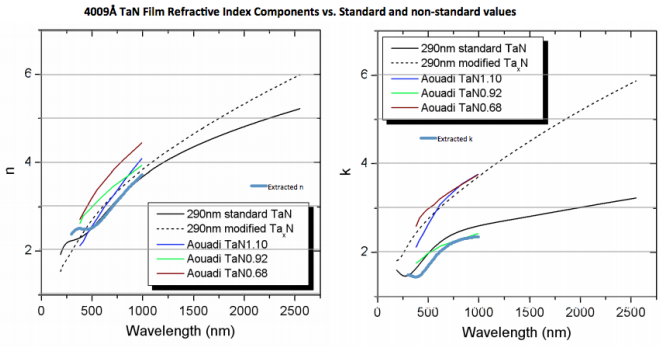


Fig. 4: Extracted (light blue on plot) real and imaginary parts of the refractive index of TaN films deposited in this study, overlayed on a plot taken from [4].

at one of three levels (with measured thicknesses of 38, 57, and 68Å each) with one wafer at each level, using appropriate soak times of the dry oxide recipe discussed in section III-A. Using the film deposition processes outlined in section III, Si_3N_4 was deposited and measured 75Å, Al_2O_3 was deposited measuring 95Å, and TaN was deposited measuring 2345Å. 5000Å Aluminum was then deposited in the CHA Flash Evaporator. All measurements of thickness were performed with VASE and optical properties remained consistent with experimental films throughout. The wafers were coated with OiR620 resist on the SSI Wafertrack using the CoatMtl recipe, exposed on the GCA stepper with the clear-field C-V mask, and developed on the SSI Wafertrack with DevMTL recipe (140°C hard bake). After wet aluminum etching, 9 minute Drytech quad etching using the Tantalum etch recipe to etch TaN, and PRS-2000 solvent photoresist strip, the wafers were completed. Since the oxide, nitride, and alumina layers are all insulating, they did not need to be patterned. Solvent strip was employed because plasma ashing after Tantalum dry etch can lead to accidental deposition of very thin Ta_XO_Y films that are extremely difficult to remove.

V. Experimental Procedure - nMOS CTF Device Fabrication

TANOS is integrated into an existing CMOS process by replacing the 4000Åpolysilicon gate of the "Adv-CMOS" with the gate stack of TANOS CTF (defined in previous sections). Subsequent etch steps for patterning of the gate are then employed (see Appendix A) to define the gate. Finally, the polysilicon reoxidation for LDD spacer must be replaced with a thin Nitride deposition. pMOS CTF are not targeted because of the difficulty of program by hot hole injection, therefore many pMOS steps are omitted. These changes alone are enough to adequately fabricate TANOS CTF in a CMOS process.

VI. Discussion of Results

A. C-V Devices

The .006cm^2 C-V devices on the wafer (seen in figure 5) with 38Åtunnel oxide exhibited P/E by FN tunneling with a

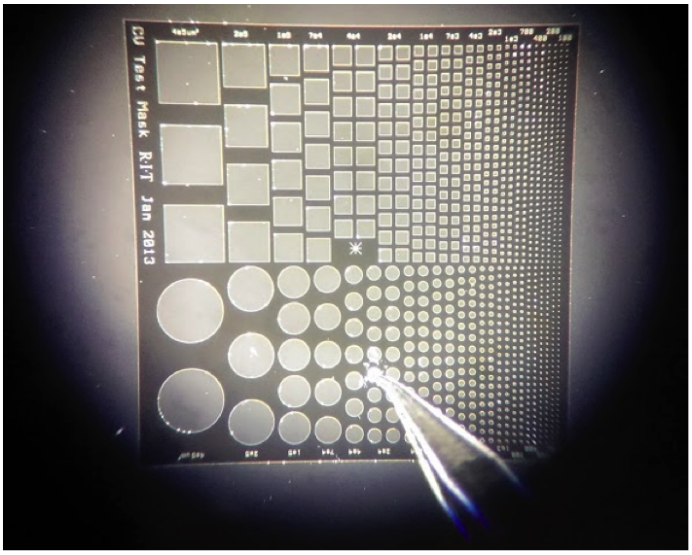


Fig. 5: Image of the C-V die patterned on the wafer on the C-V probe station with the probe on the .006cm^2 device.

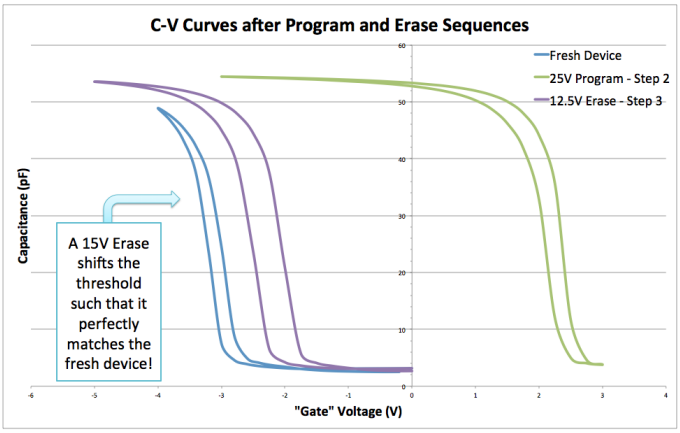


Fig. 6: C-V Plot showing maximum program and erase shifts and native device C-V.

maximum program threshold voltage of 2.6V (program voltage of 25V) and a minimum erase threshold voltage of -2.5V (erase voltage of -15V), shown in figure 6. This demonstrates, for the first time at RIT, charge trapping in TANOS devices.

B. nMOS CTF Devices

Currently the nMOS device wafers are at step 22 of 67 (see Appendix A) and would, if completed, likely yield far more efficient P/E, by merit of HCI programming and erasing mechanisms, than the C-V devices. Thereafter, the contributions of device size, tunnel oxide thickness, and barrier oxide thickness on P/E and other device characteristics would be extracted.

VII. Conclusion

For the first time at RIT, charge-trapping TANOS memory structures have been fabricated and demonstrate good operation with a total P/E threshold voltage swing of 5.2V. A process flow which integrates TANOS nMOS fabrication into

an existing CMOS process has been developed and partially completed.

APPENDIX A
DEVELOPED CMOS-INTEGRATED TANOS NMOS-CTF PROCESS FLOW

(1) Ox05 Pad Oxide 500, Tube 4
(2) CV02 1500 Nitride (LPCVD)
(3) PH03 Level 1 STI (ASML & SSI)
(4) ET29 Nitride Etch (Lam 490)
(5) ET07 Ash (Gasonics)
(6) CL01 RCA
(7) OX04 First STI Oxide Tube 1 (Bruce)
(8) ET06 Oxide Etch (Wet, HF Bench)
(9) OX04 - 2nd Oxide Tube 1 (Bruce)
(10) ET19 Hot Phos Nitride Etch (Wet, Phos Bench)
(11) PH03 P-Well Level 3 (ASML & SSI)
(12) IM01 8E13 B11 80KeV (Varian)
(13) ET07 Ash (Gasonics)
(14) OX06 Well Drive, Tube 1 (Bruce)
(15) PH03 NMOS Vt (ASML & SSI)
(16) IM01 3E12, P31, 30KeV (Varian)
(17) ET07 Ash (Gasonics)
(18) ET06 Etch 500 Pad Ox (10:1 BOE, 45Secs, Rinse SRD)
(19) CL01 Pre-Gate RCA Clean
(20) ET06 Pre-Gate HF Etch
(21) TANOS GATE
  a) 30, 50, 70 Oxide, Tube 1 (Bruce) 3 runs, 2 wafers each
  b) 75 Nitride, (LPCVD) all wafers, equal spacing
  c) 100, 130 Alumina, (CHA E-Beam) 2 runs, 3 each
  d) 375nm TaN, (CVC 601) all wafers
(22) PH03 Level 6 Poly Gate (ASML & SSI)
(23) ET08 Plasma or 4-step Gate Etch (Drytech/LAM490/LAM4600)
(24) ET07 Ash (Gasonics)
(25) CL01 RCA
(26) OX05 Gate Stack Re-Ox, 500, Tube 4 (P-5000?)
(27) PH03 Level 8 N-LDD (ASML & SSI)
(28) IM01 4E13, P31, 60KeV (Varian)
(29) ET07 Ash (Gasonics)
(30) CL01 RCA Clean
(31) CV01 Nitride Spacer Dep (LPCVD)
(32) ET39 Sidewall Spacer Etch (Drytech)
(33) PH03 Level 9, N+ D/S (ASML & SSI)
(34) IM01 4E15, P31 60KeV (Varian)
(35) ET07 Ash (Gasonics)
(36) PH03 Level 9, P+ D/S (ASML & SSI)
(37) IM01 4E15, B11 50KeV (Varian)
(38) ET07 Ash (Gasonics)
(39) CL01 RCA Clean
(40) OX08 DS Anneal, Tube 2, 3 (Bruce)
(41) ET06 Silicide Pad Ox Etch (Wet)
(42) ME03 HF Dip & Ti Sputter (50:1 HF Dip, CVC601 Sputter)
(43) RT01 RTP 1 min, 800C (AG610 RTP TISI1.RCP, 1min, 650C)
(44) CV03 TEOS, (P-5000)
(45) PH03 Level 11 CC (185mJ/cm^2, DEVFAC.RCP)
(46) ET06 CC Etch (Drytech FACCUT)
(47) ET07 Ash (Gasonics)
(48) CL01 RCA Clean
(49) LPCVD Tungsten Plugs?????
(50) ME01 Aluminum Sputter (.5um, CHA Flash Evap)
(51) PH03 Level 12-metal 1 (ASML & SSI)
(52) ET15 Al Etch (Wet Al Etch)
(53) ET07 Ash (Gasonics)
(54) CV03 TEOS P-5000
(55) PH03 Via (ASML & SSI)
(56) ET26 Via Etch
(57) ET07 Ash
(58) Tungsten Plugs????
(59) ME01 Al Deposition Metal 2 (CVC601 or PE4400)
(60) PH03 - Metal 2
(61) ET15 - Al Etch (LAM4600)
(62) ET07 Ash (Gasonics)
(63) SI01 Sinter

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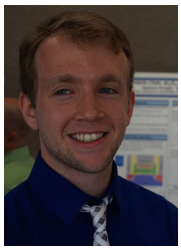

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