Ferroelectric HfO2 for Emerging Ferroelectric Semiconductor Devices

Karine Florent
kxf5974@rit.edu

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KARINE FLORENT   Dr. SANTOSH KURINEC *Advisor*

R·I·T | KATE GLEASON
College of ENGINEERING

Department of Electrical and Microelectronic Engineering

Kate Gleason College of Engineering

Rochester Institute of Technology

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Karine Florent

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Approved By:

Prof. _____
Dr. Santosh Kurinec *Advisor*

Prof. _____
Dr. Dhireesha Kudithipudi *Committee Member*

Prof. _____
Dr. Karl Hirschman *Committee Member*

Prof. _____
Dr. Michael Pierce *Committee Member*

Prof. _____
Dr. Robert Pearson *Program Director*

Prof. _____
Dr. Sohail Dianat *Department Head*

Department of Electrical and Microelectronic Engineering

Kate Gleason College of Engineering

Rochester Institute of Technology

Rochester, New York

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Because dreams do come true...

Abstract

The spontaneous polarization in ferroelectrics (FE) makes them particularly attractive for non-volatile memory and logic applications. Non-volatile FRAM memories using perovskite structure materials, such as Lead Zirconate Titanate (PZT) and Strontium Bismuth Tantalate (SBT) have been studied for many years. However, because of their scaling limit and incompatibility with CMOS beyond 130 nm node, floating gate Flash memory technology has been preferred for manufacturing. The recent discovery of ferroelectricity in doped HfO_2 in 2011 has opened the door for new ferroelectric based devices compatible with CMOS technology, such as Ferroelectric Field Effect Transistor (FeFET) and Ferroelectric Tunnel Junctions (FTJ).

This work began with developing ferroelectric hysteresis characterization capabilities at RIT. Initially reactively sputtered aluminum doped HfO_2 films were investigated. It was observed that the composition control using co-sputtering was not achievable within the existing capabilities. During the course of this study, collaboration was established with the NaMLab group in Germany to investigate Si doped HfO_2 deposited by Atomic Layer Deposition (ALD). Metal Ferroelectric Metal (MFM) devices were fabricated using TiN as the top and bottom electrode with $Si:HfO_2$ thickness ranging from 6.4 nm to 22.9 nm. The devices were electrically tested for P-E, C-V and I-V characteristics. Structural characterizations included TEM, EELS, XRR, XRD and XPS/Auger spectroscopy.

Higher remanant polarization (P_r) was observed for films of 9.3 nm and 13.1 nm thickness. Thicker film (22.9 nm) showed smaller P_r. Devices with 6.4 nm thick films exhibit tunneling behavior showing a memristor like I-V characteristics. The tunnel current showed decrease with cycling indicating a possible change in either the structure or the domain configurations. Theoretical simulations using the improved FE model were carried out to model the ferroelectric behavior of different stacks of films.

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List of Symbols

Term	Description	Units/Value
P_s	Spontaneous polarization	µC/cm^2
P_r	Remanent polarization	µC/cm^2
E_c	Coercive field	kV/cm^2
E_g	Band gap energy	eV
ϵ_r	Relative permittivity	
ϵ_0	Vacuum permittivity	8.854×10^{-14} F/cm^2
D	Displacement vector	C/m^2
ρ_V	Free volume charge density	C/m^2
ϵ_k	Relative permittivity of material k	
E_k	Electric field of material k	kV/cm
P_k	Polarization of material k	µC/cm^2
C_k	Capacitance per area of material k	F/cm^2
Q	Surface Charges per area	C/cm^2
ψ_s	Semiconductor surface potential	V
V_k	Voltage dropping in the material k	V
t_k	Thickness in the material k	cm
V_g	Gate Voltage	V
V_c	Coercive Voltage	V
V_{FB}	Flatband Voltage	V
k	Boltzmann's constant	8.617×10^{-5} eV/K
T	Temperature	K
q	Elementary charge	1.602×10^{-19} C

Term	Description	Units/Value
N_A	Acceptor concentration	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
$V_{g,eff}$	Effective gate voltage	V
C_{total}	Total capacitance per area	F/cm^2
C_{stack}	Stack capacitance per area	F/cm^2
t_{dm}	Maximum width of the surface depletion layer	cm
C'_{ox}	Oxide capacitance per unit area	F/cm^2
$\mathcal{E}$	Electric field	V/cm
n_i	Intrinsic carrier concentration	cm^{-3}

Chapter 1

Introduction and Motivations

In the last several decades, the efforts in the field of microelectronics enabled the miniaturization of portable electronic devices used on a-day-to-day basis, while improving their overall performance. These achievements result from the discovery of new technologies, such as non-volatile semiconductor memories (NVSMs). They are more robust and compact, have faster access times and consume less power due to their non-volatile data storage aspect, compared to magnetic and optical mass storage devices. Floating-gate technology, in which the data is stored in form of charges into a conductive layer, encapsulated in the gate stack of a field effect transistor, is currently used in NVSMs. Its performance and capability to scale in accordance with CMOS technology, driven by Moore's law, stating that the number of transistors on an integrated circuit doubles every 18 months, made it a technology of choice until now. However, further scaling to sub-20 nm, will become challenging as tunnel oxide thickness scaling is limited by charge retention [1]. Other drawbacks of this technology are the large applied voltage (15-17 V), necessary to inject electrons to the conductive layer, and the relatively long program/erase times (micro- to milliseconds) [2]. Recently, new memory concepts have been studied to replace floating gate technology. Charge-trapping memories, magnetic Random Access Memories (RAM), phase change RAM, resistive RAM and ferroelectric memories are seen, among the emerging memory devices, as the most promising candidates by the International Technology

Roadmap for Semiconductors (ITRS) [2]. These last devices are of particular interest in this study.

Ferroelectricity is the property of certain dielectrics of having a spontaneous polarization, which can be reversed by applying an electric field. This property was discovered for the first time by Joseph Valasek in 1921 during studies of Rochelle salt [3]. Since then, materials showing ferroelectric properties have been extensively studied. Ferroelectric Random Access Memories (FRAM) and ferroelectric Field Effect Transistor (FeFET) are two types of devices using ferroelectric material. FeFET in particular offers many advantages compared to the other alternatives by combining fast operation and non-destructive readout. With the discovery of the memristor, two terminal memristive devices have gained significant research attention in the last decade as devices that can emulate the behavior of biological synapses. This comportment is particularly attractive in the neuromorphic community, which is searching for circuits and architectures that can achieve low-power, massively parallel, and intelligent computing systems. Ferroelectric tunnel junction (FTJ) and ferroelectric memristor are two devices, which are able to mimic synapses.

Until now, the current technology involving ferroelectricity has been based on materials such as Lead Zirconate Titanate (PZT) and Strontium Bismuth Tantalite (SBT) [4, 5]. Unfortunately, due to their unstable ferroelectric properties at thin film thickness and their incompatibility with standard IC processing, alternative materials need to be explored. An appealing material is hafnium dioxide (HfO_2). This material has been fully integrated in IC technology as the gate dielectric in transistor. Recently, ferroelectricity in doped HfO_2 has been reported with dopants such as yttrium [6, 7], silicon [8, 9, 10, 11, 12] and aluminum [13]. Silicon doped hafnium dioxide (Si:HfO_2) has shown promising results with a low dielectric constant (~ 30 versus 200-300 for PZT/SBT) and a stronger coercive field (1 MV/cm versus 50 kV/cm for PZT/SBT) [10] and has been successfully integrated in FeFET device [14]. The focus

has been mainly centered on silicon as dopant and very little publications report the use of aluminum.

The emphasis of this work is on studying the effect of dopants ('X') into thin layer of hafnium dioxide. Most of the publications report the use of atomic layer deposition (ALD) to deposit the thin ferroelectric layer. In this study, physical vapor deposition (PVD) and ALD were employed to get the desired film properties in collaboration with Nanoelectronic Materials Laboratory (NaMLAb) in Dresden, Germany. The amount of dopant in PVD films was modulated by varying the thickness of the films. Two different approaches were studied: a stack approach (HfO_2/Al/HfO_2/Al/HfO_2) and a solid source dopant approach, in which the dopant was deposited on top of HfO_2 and then annealed. Si:HfO_2 ALD films were deposited in NaMLab and studied using capacitor structures. Structural and electrical measurements were carried out. The influence of annealing temperature and film thickness was studied. In parallel, ferroelectric simulations based on Miller *et al.* [15] and Lue *et al.* [16, 17] models were developed. These investigations will lead to the development of ferroelectric HfO_2 for subsequent implementation into FTJ and FeFET devices.

Chapter 2

In this chapter, polarization and ferroelectricity will be first explained. The origin of the ferroelectricity in hafnium oxide will be then described.

2.1   Polarization

A dielectric is an electrical insulator. A perfect insulator does not allow charge to pass through. However, it can be polarized by an applied field: electric charges shift from their equilibrium positions resulting in a dielectric polarization (Figure 2.1a) .

Among these materials, some of them have special properties and are classified accordingly: piezoelectricity, pyroelectricity and ferroelectricity (Figure 2.1b). These characteristics, explained in the next paragraphs, are closely linked to the crystalline nature of these materials.

Depending on the lattice structure and crystal symmetry, crystalline material can be classified according to 32 crystal classes [18]. The presence of polarization charges through mechanical strain, also called piezoelectricity, is predictable due to the presence of electrically charged particles. When a crystal is subjected to a mechanical constraint, the shape of the crystal changes and the centers of gravity of positive charges separate from the negative charges at each crystal lattice, producing a dipole moment: it is called piezoelectricity effect. To give a piezoelectric effect,
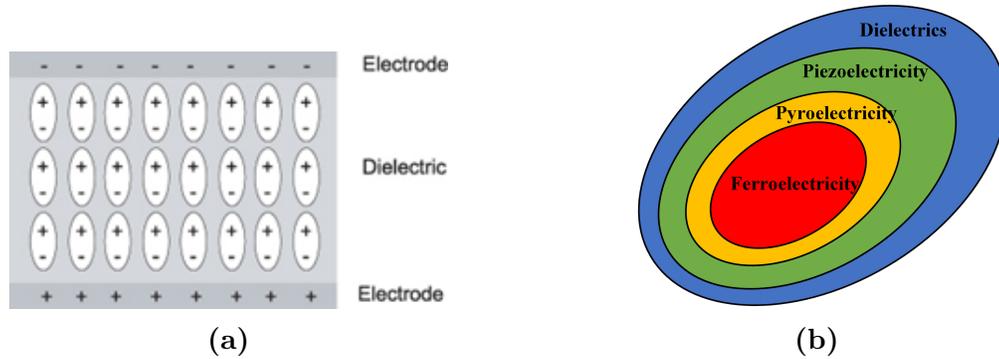
Figure 2.1: (a) Schematic of a dielectric with the application of an electric field. (b) Classification of dielectrics

it was established that the crystal must not have a center of symmetry. 21 classes correspond to this definition, but one of them does not produce a dipole moment. Among these 20 classes, 10 are pyroelectric, which means that they have a spontaneous polarization, whose amplitude can be modulated with temperature.
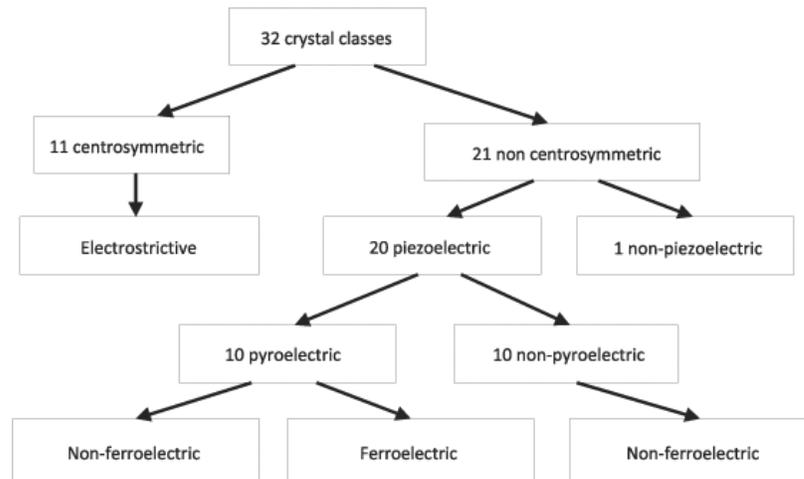
Figure 2.2: Crystal structures and ferroelectricity

Finally, the spontaneous polarization of some of these pyroelectrics can be reversed by the application of an electric field. These crystals are called ferroelectric. Figure 2.2 summarizes the crystal classes according to their properties.

2.2 Ferroelectric properties

A material is defined as ferroelectric if it has a spontaneous remanent electric dipole (pyroelectric) and if this spontaneous polarization can be reversed by an electric field. In ferroelectric materials, the polarization possesses two equilibrium states (Figure 2.3), which can be obtained by the application of a strong electric field [19]. These states, up or down, can be seen as two logic states "1" or "0". This situation of two thermodynamically stable configurations can be represented as a diagram of energy against polarization with a double-well shape, *i.e.* there are two equal energy minima for the system, which have equal and opposite polarizations, called remanent polarization P_r, separated by a potential barrier [20]. Either one of these configurations are energetically more stable than a non-polar configuration ($P = 0$). In the presence of an external electric field, the potential barrier is lowered, so that the central ion can change its position, reversing the polarization.
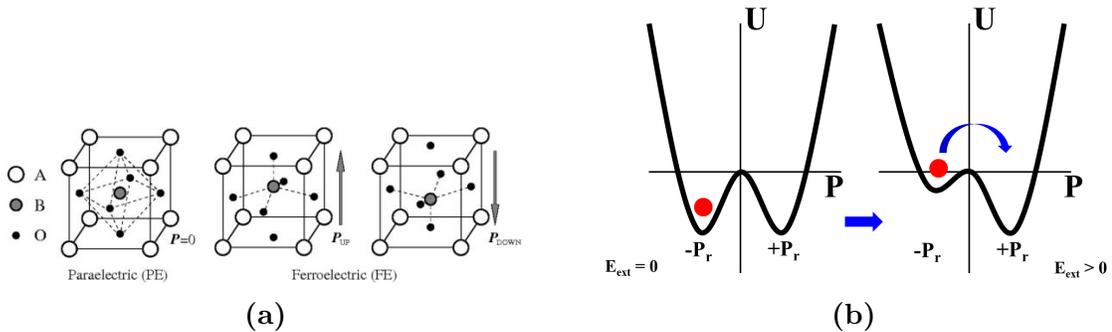
Figure 2.3: (a) Equilibrium states in a unit cell of a PZT crystal in the tetragonal ferroelectric phase: A = Pb,B = Ti/Zr and O = Oxygen [21]. (b) Energy as a function of polarization for ferroelectric materials, with and without an external electric field.

The polarization in such material is far from uniform. Many reasons can explain the presence of domains, regions of the crystal with uniformly oriented spontaneous polarization, including the thermal and electrical history of the sample [19]. In the presence of an external electric field, domains with polarizations similar to the electric field nucleate, generally at the electrode interface or grain boundaries, and then

grow vertically and laterally [22]. Each region is separated by a domain-wall, 1 to 10 nm thick for PZT, in which the polarization changes from one domain to another continuously but steeply (Figure 2.4) [23]. If the spontaneous polarization has a random direction or is distributed in such a way as to lead to zero net macroscopic polarization, this material does not exhibit ferroelectric effects.

| (a) | (b) |
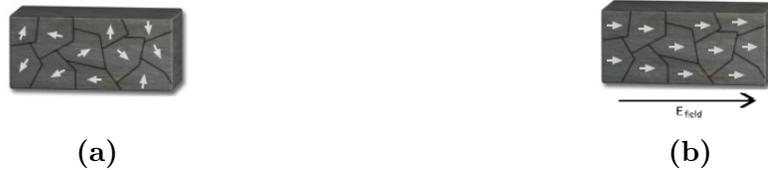
Figure 2.4: (a) Domains before the presence of an electric field. (b) Domains with the presence of an electric field.

By applying an electric field to this material, especially ceramic, a polar state can be obtained: dipole moments rotate to align themselves along the electric field direction, which reorient the domains. This process, called poling or polarization reversal by a field, is possible only in ferroelectric materials. Once the poling field is removed, the ferroelectric material possesses a polarization called remanent polarization P_r at zero electric field.

The polarization reversal by an electric field is characteristic of ferroelectric material. The application of an electric field reduces or can even remove domain walls. The ferroelectric Polarization - Electric field/Voltage (P-E/V) hysteresis loop is a consequence of the domain-wall switching. At small value of the electric field, the polarization increases linearly with the electric field, segment AB in Figure 2.5. The field is not strong enough to switch domains. As the field increases, the polarization of domains with unfavorable direction of polarization starts to switch along the direction of the electric field or, if crystallographically limited, as close as possible to it (segment BC). It is not a linear behavior anymore. At point C, all domains are aligned and the material acts as a linear dielectric (segment CD). When the field starts to decrease, some of the domains switch back. But, at zero field, there is a remanent polarization

P_r. The zero polarization can be obtained by reversing the field (point F). The field at F is called the coercive field E_c. If the field is further increased in the negative direction, the dipoles realign and there is again saturation (Point G). The field is then reduced to zero and reversed to complete the cycle. Ideally, the hysteresis loop is symmetrical.
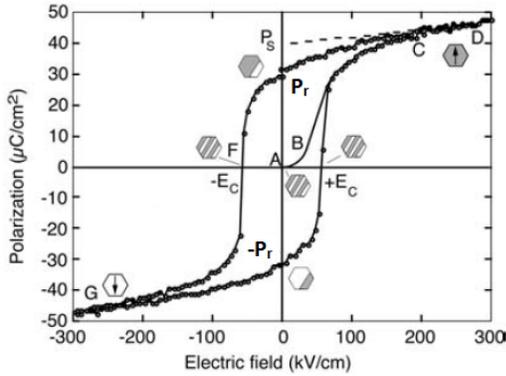
Figure 2.5: Ferroelectric P-E hysteresis loop. The hexagons with gray and white regions represent a schematic of the repartition of two polarization states in the material at different fields [24].

An antiferroelectric crystal has a structure composed of two sublattices polarized spontaneously in antiparallel direction and in which a ferroelectric phase can be induced by applying an electric field. It has a double hysteresis loop (Figure 2.6).
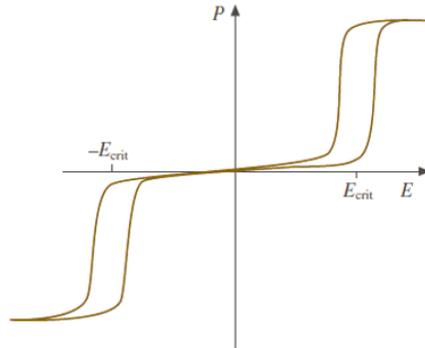
Figure 2.6: Antiferroelectric hysteresis loop with E_{crit}, critical field [25].

Although a P-E hysteresis is a requirement for a ferroelectric material, it is not a sufficient condition. Surface polarization, trapping phenomenon or leakage cur-

rents [14] can also result in the detection of a hysteresis loop. Small-signal capacitance-voltage measurements can give additional information about the true material properties. This measurement will be further analyzed in the next chapter.

Out of the many ferroelectric materials available, two families are mainly used for FeRAMs applications. Lead zirconium titanate $Pb(Zr_{0.5}Ti_{0.5})O_3$, also called PZT, belongs to the perovskite family and is widely used by industry nowadays. The other one is strontium bismuth tantalite $SrBi_2Ta_2O_9$, also called SBT, from the layered perovskite family. SBT offers better reliability than PZT based memories [27]. Figure 2.7a shows a saturated polarization loop for SBT and PZT. Their ferroelectric characteristics can be found in Figure 2.7b.
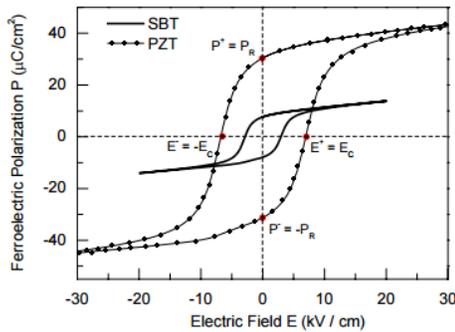
Parameters	PZT	SBT
$P_r \ (\mu C/cm^2)$	32	8
$P_s \ (\mu C/cm^2)$	40	10
$E_c \ (kV/cm)$	70	30
ϵ_r	250	250

(a)   (b)

Figure 2.7: (a) Saturated polarization hysteresis loop for SBT and PZT. (b) Ferroelectric characteristics for thin film SBT and [111]-oriented PZT (30:70) [27].

PZT and SBT have shown excellent ferroelectric properties. However, these ceramic materials have several drawbacks: poor compatibility with standard Complementary Metal-Oxide-Semiconductor (CMOS) fabrication, instable ferroelectric properties at thin film thickness and necessity of a thick buffer layer to prevent the diffusion of Pb, Bi and O. This buffer layer decreases the electrical performance by the presence of a non-desired electric field across the ferroelectric capacitance, depolarizing the film and limiting the data retention time [26]. Therefore, alternative materials need to be explored.

2.3 Hafnium dioxide

Hafnium dioxide (HfO_2) is a dielectric widely used in the IC industry due to its high dielectric constant ($HfO_2 \sim 20$, $SiO_2 \sim 3.9$), large band gap (~ 5 eV) and thermal stability. It has become a material of choice as gate dielectric for CMOS processing. Scaling of devices goes with oxide thickness reduction, resulting in degrading effects such as gate leakage. With high dielectric constant, the gate dielectric layer can be thicker, preventing such effects.

Hafnium is a Group 4 transition element in the periodic table [28]. This metal has excellent mechanical properties, however the presence of zirconium influences considerably its properties. These two elements are two of the most difficult to separate and some residue of zirconium is generally found in hafnium. Some compounds can be made from hafnium such as hafnium carbide, the most refractory binary composition known, and hafnium nitride, the most refractory metal nitride. With the presence of oxygen, hafnium forms a stable oxide, hafnium dioxide. The binary diagram under 1 atm of Hf and O can be seen in Figure 2.8a. As it can be seen on this diagram, HfO_2 has three polymorphs: αHfO_2, below 1827 °C, has a monoclinic phase ($P2_1/c$), βHfO_2, from 1827 °C to 2520 °C, has a tetragonal phase ($P4_2/nmc$) and γHfO_2, from 2520 °C to 2800 °C, has a cubic phase (Fm3m) [29]. Structural parameters for the monoclinic, tetragonal and cubic phases of HfO_2 can be found in Appendix A. The change in crystal structure of HfO_2 as a function of temperature is often summarized as: monoclinic $\longrightarrow$ tetragonal $\longrightarrow$ cubic.

By increasing the pressure between 4 to 11 GPa, a orthorhombic phase (OI) can be obtained ($P2_12_12_1$) and at 14-16 GPa, another orthorhombic structure (OII) of the cotunnite type (Pmnb) can be formed [31] (Figure 2.8b). Different papers report that HfO_2 transforms at 10 GPa to a Pbca phase [30, 32] or Pbcm phase [33] (OI phase) and a Pnma phase [30, 32, 34, 35], Pbcm phase [33] or Pmnb [36] phase for OII phase
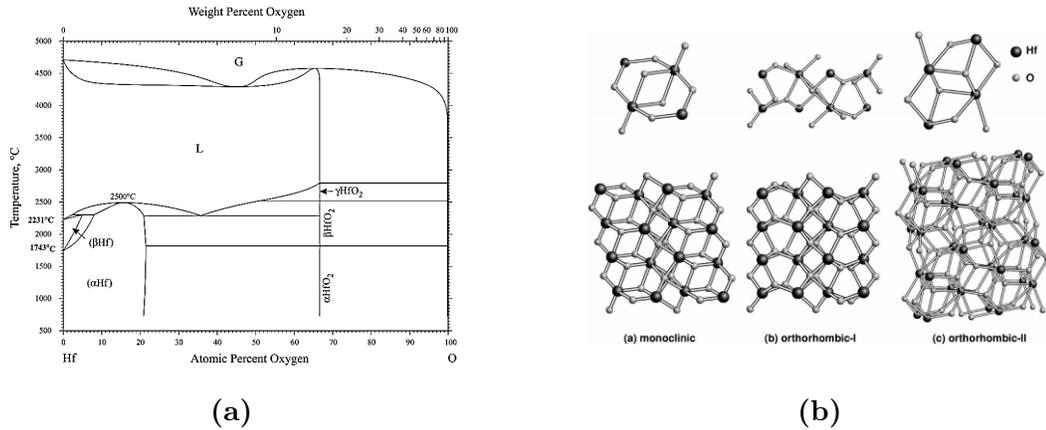
Figure 2.8: (a) Binary diagram of Hf-O [29]. (b) Primitive unit cells and their expanded crystal structure [30].

at higher pressure. The crystal structure of the orthorhombic phases varies following the pressure and the experiment, but all the reported structures are centrosymmetric and therefore are not ferroelectric.

In 1965, Garvie discovered that, in nano-scale crystallites, the stable region of the tetragonal phase extends to lower temperatures due to the surface energy effect [37]. Therefore, the crystallization in thin films tends to proceed in two steps: nucleation in a tetragonal phase and during crystal growth, a martensitic transformation to the monoclinic phase

Electronic studies show that the tetragonal phase has the highest dielectric constant ($\sim$70) [38]. Table 2.1 summarizes the band gaps E_g and averaged dielectric constants reported for HfO_2. The addition of dopants such as SiO_2 (5-10%) is known to stabilize the tetragonal phase [39], leading to higher dielectric constant, particularly interesting for CMOS engineering. Moreover, the presence of a TiN capping layer was found to improve the overall characteristics of an atomic layer deposited HfO_2 after annealing, modifying the structure by reducing the monoclinic phase fraction [40] and leading to an increase in the dielectric constant.

Recently, it was found that the incorporation of dopants in HfO_2 leads to the formation of a ferroelectric material. As has been explained before, only non-

Table 2.1: Band gaps and averaged dielectric constant for crystalline phases of HfO_2

Phase	E_g	ϵ_r
Cubic	5.53[36]	29[38]
Tetragonal	5.79[36]	70[38]
Monoclinic	5.65[36]	16-18[38]
Ortho I	3.75[38]	-
Ortho II	2.94[38]	-

centrosymmetric structure exhibits ferroelectricity. As a reminder, Zr and Hf are difficult to separate from each other. Studies show that ZrO_2 and HfO_2 have very similar crystal structures. The addition of magnesium in ZrO_2 stabilizes the oxide and changes the crystal structure from tetragonal to a rare orthorhombic, with space group $Pbc2_1$, which is non-centrosymmetric, during cooling [41]. Kisi *et al.* [42] discovered in 1989 the presence of a non-centrosymmetric orthorhombic phase in zirconia, but this was forgotten until Boescke *et al.* [10] rediscovered this structure in Si:HfO_2 in 2011. They investigated the influence of mechanical encapsulation (with TiN) of Si:HfO_2 thin films at low Si content by fabricating Metal-Insulator-Metal (MIM) TiN/Si:HfO_2 (10 nm)/TiN capacitors. 5-10 mol% of SiO_2 has been reported to stabilize the tetragonal phase in HfO_2. Their idea was to incorporate low SiO_2 content into the film, with atomic layer deposition, before the complete stabilization of the tetragonal phase occurs. After rapid thermal annealing (RTA), their film shows a ferroelectric behavior (Figure 2.9a) and an orthorhombic phase that they believe is $Pbc2_1$: this was observed using X-ray Diffraction (Figure 2.9b). At high temperature annealing, the initial nucleation is supposed to take place in a metastable tetragonal phase. In the presence of a cap, the shearing of the unit cell is considered to be mechanically inhibited, resulting in an orthorhombic phase (monoclinic $\longrightarrow$ orthorhombic $\longrightarrow$ tetragonal).

The concentration of dopant is critical and an antiferroelectric behavior can also result in case of high doping. Mueller *et al.* have been working on ferroelectric

(a)

(b)
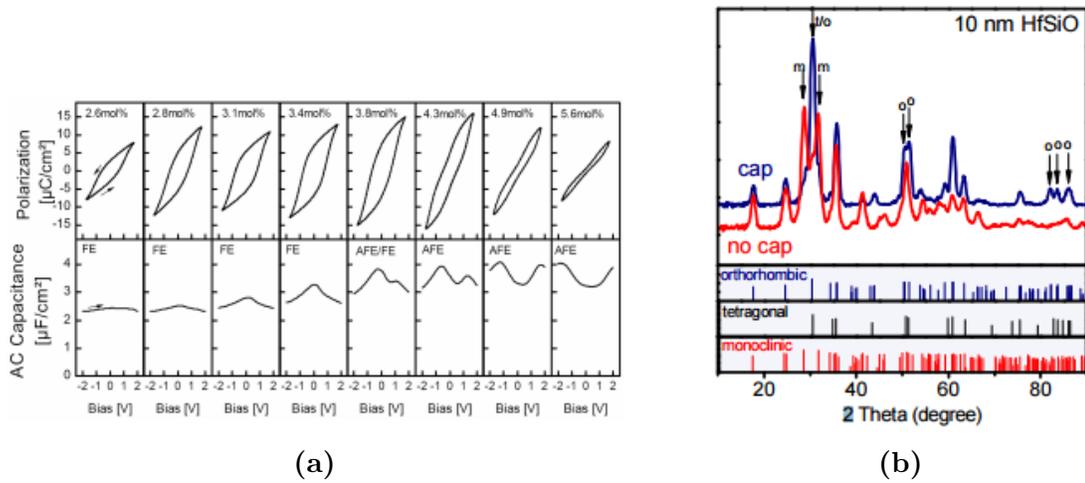
Figure 2.9: (a) Polarization and capacitance-voltage sweeps of a series of capped Si:HfO$_2$ MIM capacitors [10]. (b) XRD measurements of two samples with and without cap [10].

HfO$_2$ by incorporating aluminum [13], yttrium [6, 7] and silicon [8, 9, 10, 11, 12]. They fabricated MIM TiN/HfO$_2$/ TiN capacitors on silicon substrate and obtained hysteresis, confirming the presence of a ferroelectric material. To obtain low and accurate dopant content, they used atomic layer deposition and varied the cycle ratio to obtain the desired ratio. Figure 2.10a summarizes the polarization versus electric field hysteresis for various dopants.

(a)

Dopant < 20 mol%	Ferroelectric properties
Al^{+3}	**confirmed**
Ca^{+2}	expected
Ce^{+4}	expected
Dy^{+3}	expected
Er^{+3}	expected
Gd^{+3}	**confirmed**
Ge^{+4}	expected
La^{+3}	**confirmed**
Sc^{+3}	expected
Si^{+4}	**confirmed**
Sr^{+2}	**confirmed**
Sn^{+4}	expected
Y^{+3}	**confirmed**

(b)
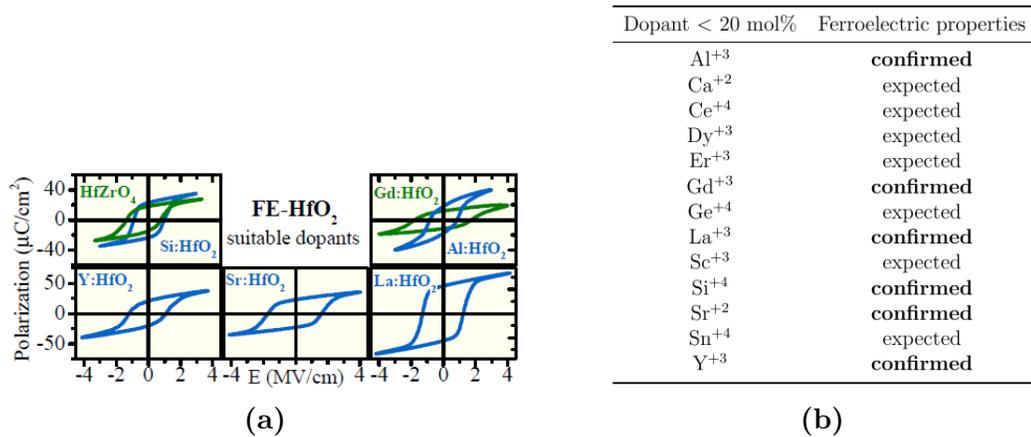
Figure 2.10: (a) P-E hysteresis of TiN/ X:HfO$_2$/TiN capacitors for various dopants X [11]. (b) Existing ferroelectric HfO$_2$ films [12].

ALD is the preferred choice for the deposition of doped HfO$_2$. However, yttrium was successfully co-sputtered into hafnium oxide thin film by Olsen *et al.* [7], confirm-

ing that such films can also be deposited through Physical Vapor Deposition (PVD). The stabilization of the desired tetragonal or cubic phase against monoclinic phase was found to depend on doping, thermal treatments, deposition method, strain as well as mechanical encapsulation provided by electrodes. Since 2011, many attempts have been done to try to get this ferroelectric HfO_2 film using different dopants. Figure 2.10b summarizes the appearance of ferroelectricity in HfO_2 with various dopants [12].

Table 2.2: Comparison of ferroelectric (FE) HfO_2 to the most common perovskite ferroelectrics [12]

	SBT	PZT	FE-HfO_2
Film thickness (nm)	> 25	> 70	5-30
Annealing temp. (°C)	> 750	> 600	450 - 1000
P_r ($\mu C/cm^2$)	< 10	20-40	1-40
E_c (kV/cm)	> 10 - 100	$\sim$ 50	1000 - 2000
ϵ_r	150 - 250	300-3800	$\sim$ 30
ALD capability	limited	limited	mature
CMOC compatibility	Bi, O_2 diffusion	Pb, O_2 diffusion	stable

Advantages of ferroelectric HfO_2 over traditional PZT and SBT are many: thin layer ($\sim$ few nanometers), high annealing temperature, high coercive electric field, ALD capability, CMOS compatibility (Table 2.2). Figure 2.11 summarizes the overall advantages and possible applications of HfO_2.
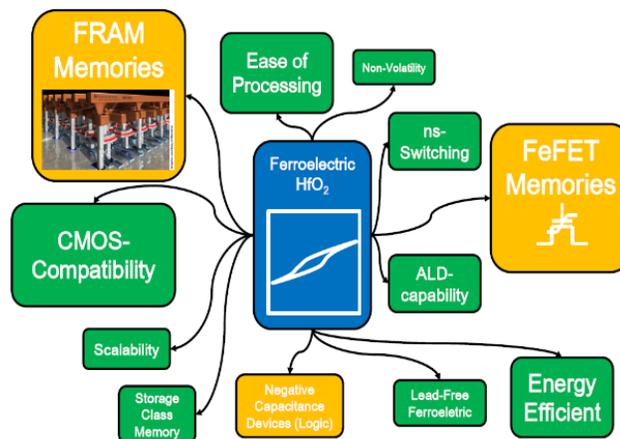
Figure 2.11: Advantages and applications of ferroelectric HfO_2 [43].

Some promising candidates for the use of ferroelectric HfO_2 are Ferroelectric Field Effect Transistor (FeFET), Ferroelectric Tunnel Junction and Ferroelectric Memristor (Figure 2.12). These devices will be described in the following section.
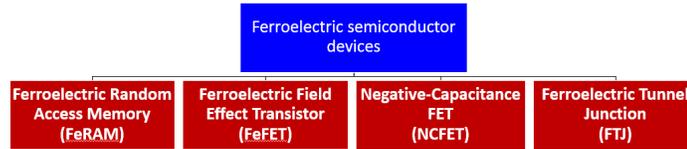
Figure 2.12: Emerging ferroelectric semiconductor devices

Chapter 3

Applications in Memories

Due to the presence of two stable states, ferroelectric materials are particularly attractive for data storage. Two ferroelectric memories have been developed in the recent years: Ferroelectric Random Access Memory (FeRAM) and Ferroelectric Field Effect Transistor (FeFET). They will be described in this chapter, followed by FTJ and ferroelectric memristor.

3.1   Ferroelectric RAM

A FeRAM is composed of a ferroelectric capacitor and a conventional transistor in 1T-1C memory cell (Figure 3.1). It has been widely developed and commercialized. The main drawback of this memory is the destructive readout scheme. To sense the stored memory state, the polarization of the cell is reversed. When a voltage pulse is applied to the capacitor during reading, the polarization either changes or remains same, resulting in a different value of the current. Therefore, the state must be rewritten each time after reading, requiring a high endurance of the ferroelectric material [14]. Additionally, FeRAM reached its scaling limit at 130 nm node.

A ferroelectric capacitor will be now described. Different capacitor structures can be fabricated: Metal-Ferroelectric-Insulator-Semiconductor (MFIS), Metal-Ferroelectric-Semiconductor (MFS) and Metal-Ferroelectric-Metal (MFM), also called MIM.
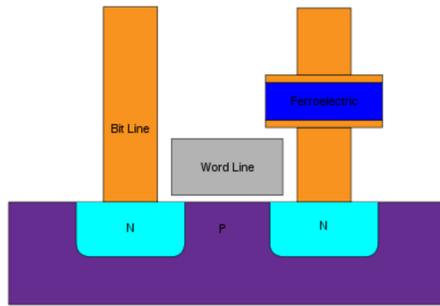
Figure 3.1: Schematic of 1T-1C FeRAM structure.

An insulating interfacial layer is typically added between the ferroelectric layer and the semiconductor to reduce stress and interfacial reaction between materials.

In a standard capacitor, the capacitance of the device is stable (Figure 3.2a). It is not the case for a ferroelectric capacitor because of the spontaneous polarization. A typical Capacitance - Voltage (C-V) plot for a MFM device can be seen in Figure 3.2b. Let's suppose that a voltage is applied to a MFM in a direction opposite of the previous applied voltage. With the increase of an applied voltage, the increase of the dielectric constant, *i.e.* of the capacitance, corresponds to a continuous increase of the amount of domains switching until the number of domains switching simultaneously reaches a maximum. At that point, the majority of the domains have switched; the voltage corresponds to the coercive voltage.
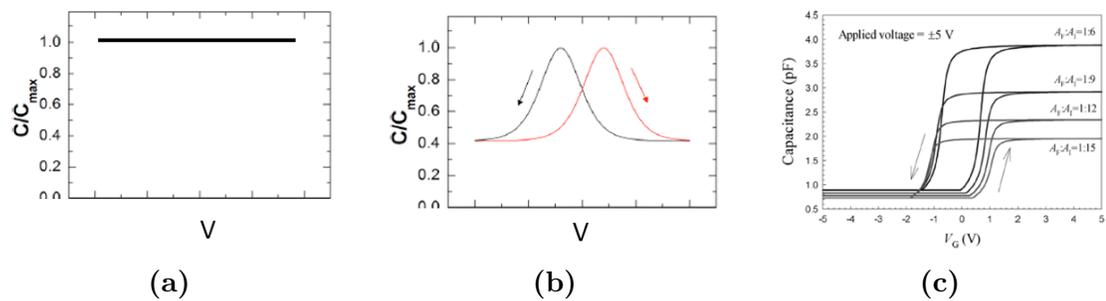
Figure 3.2: (a) Standard capacitor. (b) MFM capacitors [44]. (c) MIS Capacitor [17]

The dielectric constant then decreases continuously, until it reaches the stabilization, due to a continued reduction of the amount of domains that are in the

process of reversing. By reversing the applied voltage, the same behavior is obtained. For a MIS capacitor, a hysteresis can be seen in the C-V measurements, because the polarization influences the threshold voltage (Figure 3.2c).

Therefore, small-signal C-V measurements, a measure of the dielectric constant, can give information about the nature of a material and confirm the ferroelectric properties, in harmony with a polarization-voltage hysteresis.

Miller *et al.* [15] developed a simple quantitative model on the physics of MOS device to explain the ferroelectric capacitor physics. This model will be described in the next chapter.

3.2   Ferroelectric Field Effect Transistor (FeFET)

FeFET is similar to Metal Oxide Semiconductor Field Effect Transistor (MOS-FET) with the gate oxide as ferroelectric material or a stack of dielectrics with one ferroelectric layer. It has both memory and logic functions. PZT and SBT are two ferroelectric materials widely studied and used for FeFET.

In a FeFET, the on- and off-state are defined by the value of the polarization. Figure 3.3 summarizes the operation of a n-channel FeFET. The "on-state" is obtained by applying a positive pulse; the "off-state" is obtained by applying a negative pulse.

The resistance of the channel is regulated by the polarization charge of the ferroelectric layer, controlled by a voltage applied at the gate [14]. If $V_G > V_C$ (Coercive voltage), the polarization vector P is directed toward the semiconductor, *i.e.* positive polarization charge at the ferroelectric/semiconductor interface, there is accumulation of electrons in channel, increasing the channel conductivity: the device is in on-state and I_D-V_G curve is towards lower voltages. If $V_G < -V_C$: the polarization is directed in the opposite direction, electrons are depleted, the channel conductivity increases: the device is in off-state and I_D-V_G curve is shifted towards higher voltages. One of the advantage of this device is that the read out is non-

destructive. By sensing the source-drain resistance or current level, using a voltage less than the coercive voltage but greater than the threshold voltage, it is possible to know the state of the device.
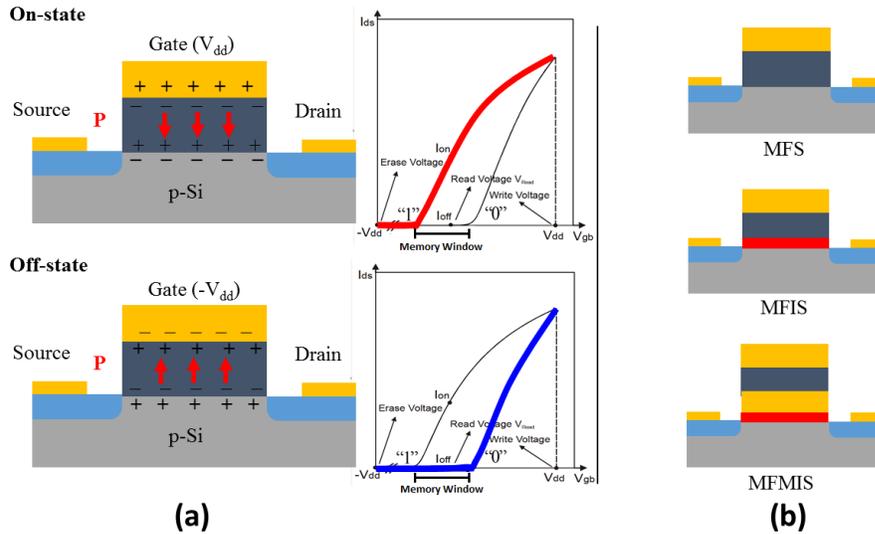
Figure 3.3: (a) Charge motion n-FeFET during one cycle of operation; I_D-V_G characteristics (b) Alternative gate structures. Yellow: metal, Dark blue: ferroelectric materials, Red: insulator, Light blue: doping, Grey: silicon.

FeFET memories are nondestructive readout, nonvolatile and compact (1T). The device must be engineered to assure a sufficient memory window (MW) between both states (Figure 3.3). This window can be estimated as: $MW = V_{TH}^{OFF} - V_{TH}^{ON} = 2E_c t_f$, where V_{TH} is the threshold voltage, E_c is the coercive field and t_f is the thickness of the ferroelectric film [16].

Different structures exist due to challenges at the semiconductor/ferroelectric interface. Indeed, to get the best device, lattice mismatch must be as small as possible, interface states should be small, formation of low-k dielectrics should be avoided and the ferroelectric material must form a pinhole free layer [45]. It is known that perovskite oxides are ferroelectric, but only few of them are suitable for growth on silicon. Therefore, alternative gate structure have been developed: MFS, MFIS and MFMIS (Figure 3.3). Figure 3.4 shows an example of an experimental result of HfO$_2$-based FeFET devices [9].
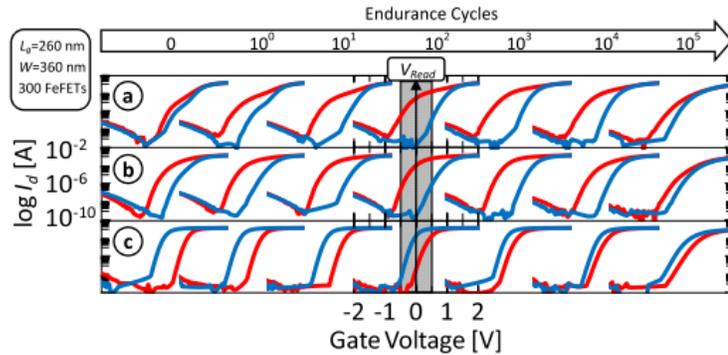
Figure 3.4: Pulsed $I_d - V_g$ characterization for long-channel FeFET. Doping concentration of (a) 3.5 mol%, (b) 4.5 mol%, (c) 5.7 mol%. (a) and (b) show a shift to more negative V_t values after the application of a programming pulse (red) and a shift toward more positive V_t values after the application of a negative erase pulse (blue). (c) shows an inverted memory window showing only trapping related phenomena [9].

3.3 Ferroelectric Tunnel Junction (FTJ)

Electron tunneling phenomenon has been known since the discovery of quantum mechanics. A tunnel junction was first discussed by Frenkel in 1930 [46]. An electron can traverse the potential barrier that exceeds an electron's energy and has a finite probability to be found on the opposite side of the barrier.

Ferroelectric Tunnel Junction (FTJ) was conceptualized by Esaki *et al.* in 1971 [47]. But it is only in 2005 that Tsymbal *et al.* [48] first demonstrated experimentally that the polarization direction of the ferroelectric material can manipulate the quantum mechanical tunneling current and resistance, nondestructively, when an ultrathin ferroelectric film serves as barrier in tunnel junction devices. This effect is called tunneling electroresistance effect (TER). Tsymbal *et al.* established that a change in the electrostatic potential profile across the junction can be produced by reversing the polarization in the ferroelectric, leading to a resistance change. Indeed, in a MFM structure, if the ferroelectric film is sufficiently thin and conserves its ferroelectric properties, the depolarizing electric field in this film is not zero, because the surface charges in the ferroelectric are not completely screened by the adjacent

electrodes. The electrostatic potential associated with this electric field depends on the direction of the polarization. Switching the ferroelectric polarization induces variations of the tunnel resistance, with resistance contrasts between ON and OFF states of several orders of magnitude [49]. Many different FTJ have been reported and some are summarized in Figure 3.5.

Subs.	Electrode 1	FE barrier	d FE (nm)	Electrode 2	Ø (μm)	OFF/ON	Specifications	Year	Ref.
	$SrTiO_3$:Nb	$BaTiO_3$	3.4	Pt	30	>10,000	Barrier width modulation /SC electrode	2013	8
$YAlO_3$	$Ca_{0.96}Ce_{0.04}MnO_3$	T-$BiFeO_3$	4.5	Co	0.18	>10,000	FE domains /transport correlation	2013	7
$SrTiO_3$	$La_{0.7}Sr_{0.3}MnO_3$	$PbZr_{0.2}Ti_{0.8}O_3$	9	Cu	0.22	>1,500	Thermionic injection	2011	36
$NdGaO_3$	$La_{0.7}Sr_{0.3}MnO_3$	$BaTiO_3$	1.6	Co	5	1000	Memristor/oxygen vacancies	2012	40
$NdGaO_3$	$La_{0.7}Sr_{0.3}MnO_3$	$BaTiO_3$	2	Co	0.35	>300	Memristor/FE domains correlation	2012	39
$SrTiO_3$	$La_{0.7}Sr_{0.3}MnO_3$	$PbZr_{0.2}Ti_{0.8}O_3$	1.2-1.6	Co	0.22	300	FE domains	2012	43
$NdGaO_3$	$La_{0.7}Sr_{0.3}MnO_3$	$BaTiO_3$	2	Co	0.50	>100	Fast: 10 ns	2012	37
$DyScO_3$	$SrRuO_3$	$BaTiO_3$	3	Ag	0.02	>100	Small: 20 nm	2012	38
$SrTiO_3$	$La_{0.7}Sr_{0.3}MnO_3$	$BaTiO_3$	3	$La_{0.5}Ca_{0.5}MnO_3$	15	100 at 5 K	Metal/insulator phase transition	2013	42
MgO	Pt	$BaTiO_3$	3	Cr	0.80	30	Transport/potential profile correlation	2013	41

d FE, barrier thickness; FE, ferroelectric; subs., substrate; SC, semiconducting.
The columns contain the following technical details: materials for the subs., bottom (1) and top (2) electrodes, and FE barrier, d FE, effective diameter of the devices (Ø), OFF/ON ratio, specifications, year and reference of publication. The reports are ordered by the OFF/ON ratio amplitude.

Figure 3.5: Survey of experimental reports of tunnel electroresistance with ferroelectric tunnel junctions [49].

Polarization charges are present at the surface of a ferroelectric film and, depending upon their sign, will attract or repel electrons. This happens over a short distance in the electrode. The electrons near the interface screen polarization charges. According to Thomas-Fermi theory, the screening length can be shorter than a tenth of nanometer for very good metal and can reach tenth of nanometer for semiconductor. However, Stengel *et al.* [50] demonstrated that the effective screen length would actually be strongly dependent on the microscopic properties of the ferroelectric/electrode interface, leading to an incomplete screening and resulting in an additional electrostatic potential at this interface. This additional electrostatic potential will be large if the screening length divided by the dielectric constant of the electrode is large.

(a)

(b)
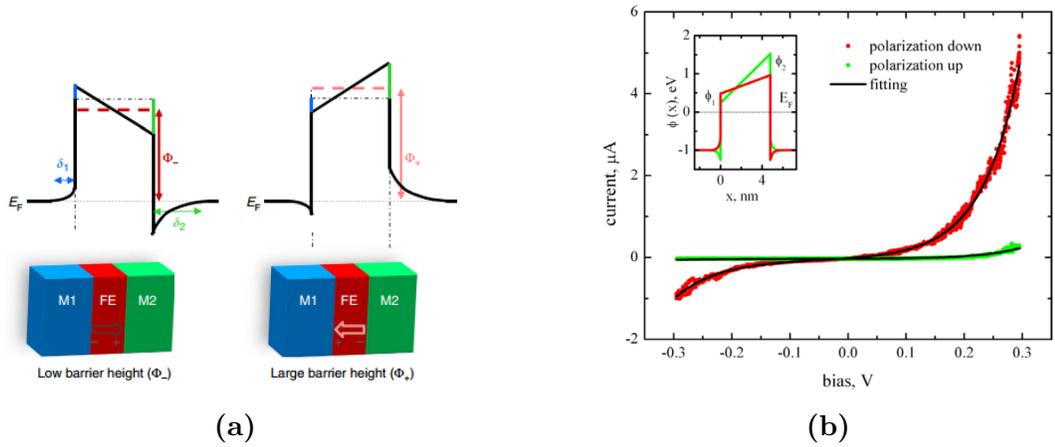
Figure 3.6: (a) Polarization-induced variation of the tunnel barrier height in FTJs and the potential profile across the metal 1 (M1)/ferroelectric/metal 2 (M2) heterostructure for two orientations (right and left) of the ferroelectric polarization (P) [49]. (b) Resistance change depending on the polarization [48].

Let's consider an ultrathin ferroelectric layer sandwiched between two different electrodes with more efficient screening length on the left side than on the right side (Figure 3.6a). To simplify, the initial electronic potential barrier is supposed rectangular, *i.e.* identical barrier heights for the left and right interfaces. An asymmetric modulation of the electronic potential profile is induced by the polarization charges. This asymmetry is reversed when the polarization is reversed. This results in the barrier height being in average higher at one interface than at the other. The tunnel transmission depends exponentially on the square root of the barrier height (see Equation 3.1 [51]) and therefore the junction resistance will depend on the direction of polarization (Figure 3.6b).

$$J = \frac{\alpha}{t^2} \left[\phi\,exp\left(-At\sqrt{\phi} \right) - (\phi + qV)\,exp\left(-At\sqrt{\phi + qV} \right) \right] \qquad (3.1)$$

where $\alpha = \frac{q}{4\pi^2\beta^2\hbar}$, $A = 2\beta\sqrt{\frac{2m}{\hbar}}$, β is a dimensionless correction factor, t is the potential barrier width, q is the elementary charge, k is the Boltzmann constant, T is the temperature, V is the applied voltage, m is the effective mass of the charge, $\hbar$ is the reduced Planck constant and ϕ is the potential barrier.

3.4 Ferroelectric Memristor

3.4.1 Memristor

A memristor has the ability to change resistance with an applied voltage and to maintain this resistance. It was theoretically predicted almost 40 years ago by Chua through the expression:

$$V = M(q) \times I \tag{3.2}$$

where V is the voltage, I is the current and $M(q)$ is the memristance, depending on the charge q.

Devices showing a change of resistance were, up to Chua's discovery, bistable devices, *i.e.* the application of an external bias voltage is necessary to change between ON (low resistance R_{ON}) and OFF (high resistance R_{OFF}) states. However, a memristor is characterized by a continuous change in resistance with the amount of current that has flowed through the device, involving coupled motion of electrons and ions within the material layer under an applied electric field [50]. However, even without current, the device retains its last resistance state and can therefore act as a nonvolatile memory element. The memristance depends on the history of current passing through the element. Chua showed that memristors are part of a broader class of systems called memristive systems described by:

$$V = M(W, I) \times I \tag{3.3}$$

$$\frac{dW}{dt} = f(W, I) \tag{3.4}$$

$$M(W) = W \times R_{ON} + (1 - W)R_{OFF} \tag{3.5}$$

where W is any controllable property and f is some function, which can defined as the equivalent learning rule of the memristor.

In 2008, Strukov *et al.* made the first memristor $Pt/TiO_2/Pt$ [52] (Figure 3.7). Most of the existing memristor prototypes are based on transition metal oxide resistive layers (ex TiOx), phase change, Red-Ox. However, reliability and endurance issues can appear. Moreover, the physical phenomena are complex and difficult to model and understand. A "purely electronic" memristor, *i.e.* a device in which the resistance changes are obtained through charge motion, promises an increase in endurance and reliability, since the structure of the material is preserved. An ideal memristor is small ($< 50 \times 50$ nm^2) and has a large OFF/ON ratio (> 1000). Such a device opens the possibility to build ultra-dense resistive matrices of memristors, called crossbar arrays (Figure 3.7), which can be integrated on top of CMOS [53].
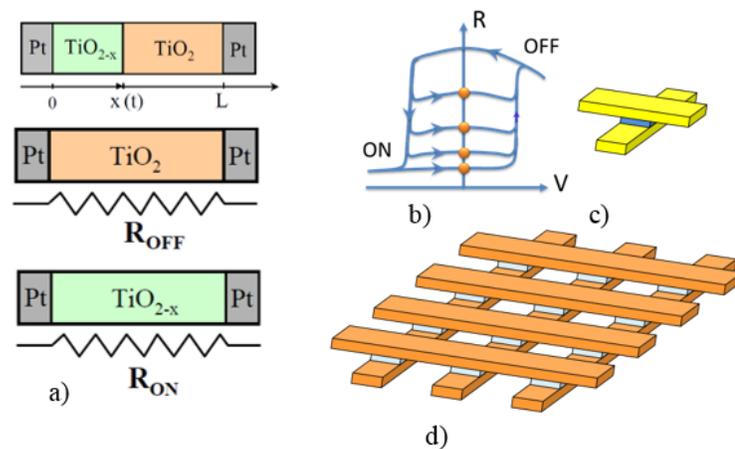
Figure 3.7: a) The first memristor $Pt/TiO_2/Pt$ [54]: top: structure of the device, middle: off state, bottom: on state; b) Example of a characteristic of a memristor; c) A typical memristor structure; d) Crossbar arrays [55].

3.4.2 Ferroelectric tunnel memristor

Kim *et al.* [50] and Chanthbouala *et al.* [55] both demonstrated the memristive behavior of a FTJ using an $Au/Co/BaTiO_3/$ $La_{2/3}Sr_{1/3}MnO_3$ stack. They transformed this binary memory to multi-state, quasi-analog memristors (Figure 3.8). In these devices the switching occurs through non-uniform ferroelectric domain configurations.
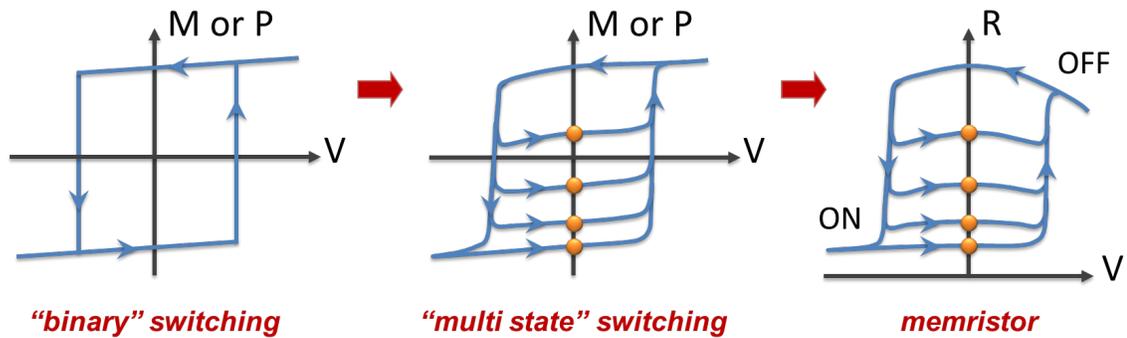
Figure 3.8: Characteristics of a binary memory to a multi-state memory, compared to a memristor [53].

It has been previously discussed that the polarization reversal occurs through the formation and propagation of ferroelectric domains of opposed polarity (Figure 3.9). When this happens, the state is neither ON or OFF, which can lead to multi-resistive states. Moreover, ultrathin $BaTiO_3$ layer is made of very thin ferroelectric domains, resulting in a very fine tuning of the resistance.
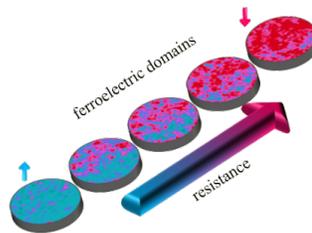
Figure 3.9: Resistance as a function of the ferroelectric domains [53].

The resistance level of the FTJ can be set by an appropriate number of consecutive pulses of a fixed voltage as illustrated in Figure 3.10. Different writing voltages will give different OFF/ON ratios. The large OFF/ON ratios ($> 10^2$), fast switching (below 10 ns) and the purely electronic operation is appealing for using the ferroelectric memristor in neuromorphic applications.
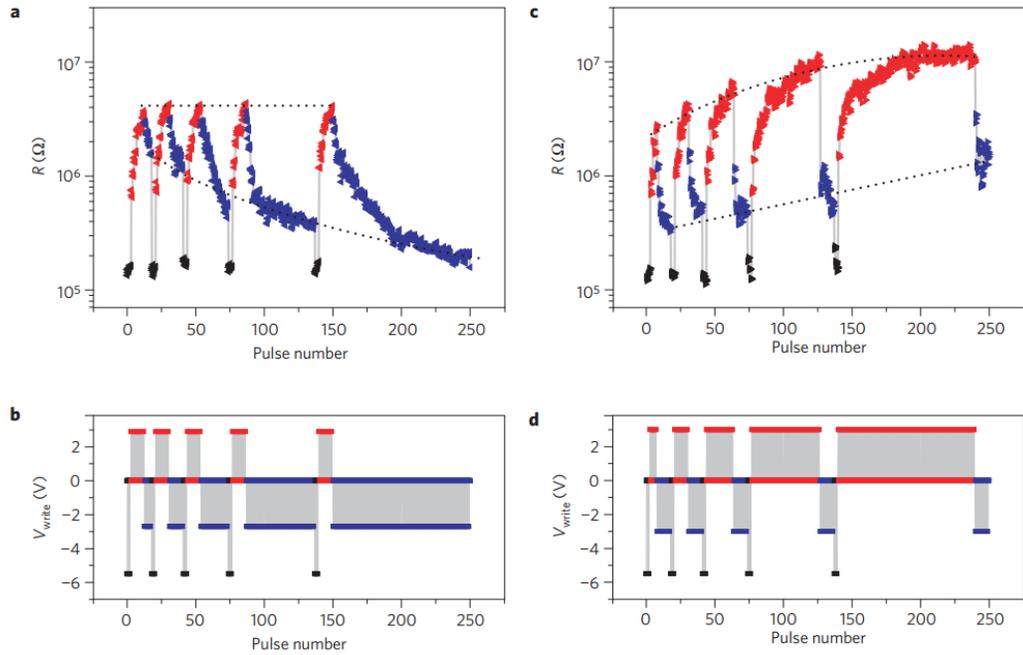
Figure 3.10: Tuning resistance by consecutive identical pulses (a,c); Evolution of junction resistance as a function of the different voltage pulse sequences (b,d) plotted for $V_{write} = +2.9$ V and -2.7 V and for $V_{write} = +3$ V and -3 V [55].

3.4.3 Synaptic plasticity

Memristive devices combined with synaptic plasticity are believed to lead to a new generation of self-adaptive ultra-high density intelligent machines. A biological synapse is the link between pre-synaptic neuron and post-synaptic neuron (Figure 3.11). The pre-synaptic neuron sends an action potential, a spike ($V_{mem-pre}$) travelling through one of its axons to the synapse. During this action, vesicles containing neurotransmitters are released into the synaptic clef. The effect of several pre-synaptic action potentials produces a postsynaptic action potential $V_{mem-pos}$ at the membrane of the post-synaptic neuron, which then propagates through all neuron's terminations [56].

The efficacy of a pre-synaptic spike in contributing to this cumulative action at the post-synaptic neuron is classified as the weight of the synapse. This weight (w) could be understood as the size and/or number of neurotransmitter packages
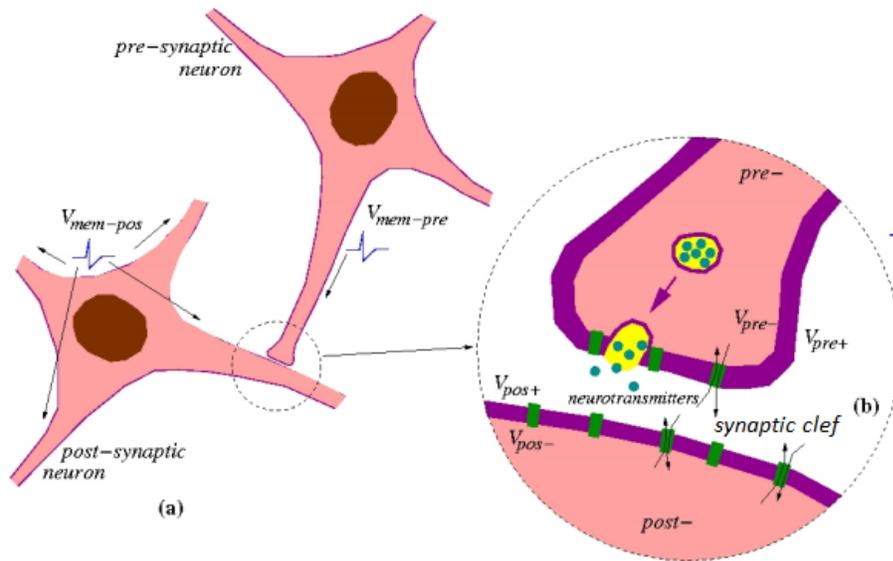
Figure 3.11: Illustration of synaptic action: (a) Two neurons connected, (b) Detail of synaptic junction [56].

released during a spike. The synaptic weight is considered to be non-volatile and of analog nature, but depends on time as a function of the spiking activity of pre- and post-synaptic neurons.

A synapse can be seen as the connection between two neurons. Computer engineers are looking for devices, which can reproduce the synaptic behavior. This behavior can be seen as a change in conductance due to a stimulus. Moreover, the device would be able to "learn" and therefore change conductance depending on the stimulus and remember this change as a function of the stimulus. Memristive devices seem promising candidates due to their variable conductance, which can be seen as the weight of a synapse (Figure 3.12). Ferroelectric tunnel memristors are suitable devices for this application in term of number of states, endurance, reliability and fast switching speed. Resistance change in the memristive device can be achieved through appropriate pulse amplitude and duration to change the ferroelectric domains configuration.
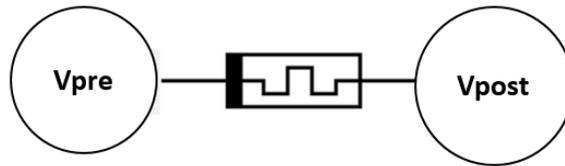
Figure 3.12: Schematic of two neurons connected with a memristor.

3.4.4 Challenges

One of the critical requirements for potential applications of FTJs is a sizeable tunneling electroresistance (TER) effect that is a relative resistance change between ON and OFF states. FTJs composed of $BaTiO_3$ (BTO) (2 nm)/$La_{0.67}Sr_{0.33}MnO_3$ (STO) films have been reported exhibiting tunable tunneling resistance by applying consecutive pulses [50]. However, they are not compatible with the existing microfabrication technologies. It has been shown that, in FTJ with metal electrodes, the TER can be as large as 10^2, which is not large enough for applications [57]. However, Wen *et al.*[58] recently demonstrated a large TER ratio of 10^4, using a semiconductor as electrode. This opens new perspectives for further improvements.

Chapter 4

Structural and Electrical Characterizations

This section gives an overview of structural and electrical characterization methods used in this work. Basic principles of X-ray Diffraction (XRD), X-ray Reflectivity (XRR), X-ray Photoelectron Spectroscopy (XPS), Transmission Electron Microscopy (TEM) and Atomic Force Microscopy (AFM) techniques are described. Electrical characterizations include Polarization-Voltage measurements (P-V), fatigue measurements, PUND measurements as well as Capacitance-Voltage measurements (C-V).

4.1 Structural characterization

4.1.1 X-ray Diffraction (XRD)

X-ray diffraction crystallography is a well-established and widely used method to obtain information about the atomic structure of a material. After the identification of a compound, its crystal structure, unit cell, interatomic distance and many other properties can be established, because each crystalline solid has a unique characteristic X-ray powder pattern.

X-rays are electromagnetic radiation with a wavelength about 1 Å, which is about the same size as an atom [59].

X-rays are produced by the bombardment of electrons from the cathode towards a metallic anode, by the application of a high voltage. When electrons slow down,
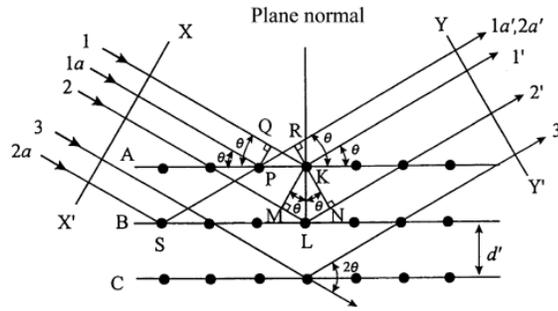
Figure 4.1: Schematic diagram of Bragg condition [59].

continuous X-rays with various wavelengths are emitted. Characteristic X-rays are often generated, when the voltage exceeds the potential necessary to knock out an electron from the K shell, resulting in a fall, into the vacancy, of one of the electrons in L shell. For a copper target, Kα radiations have a wavelength of 1.54 Å. However, most of the kinetic energy of the electrons bombarding the metal target is converted into heat and only 1 % is transformed into X-rays.

The incident X-ray beam is reflected by the atomic planes. It is called diffraction by crystals. When the scattered X-rays from atoms are in phase, they emphasize each other to produce a diffraction beam, which can be detected with a detector. A familiar method to find when this event occurs is called Bragg's law or Bragg condition. The diffraction beam is detected only when this condition is satisfied:

$$2dsin(\theta) = n\lambda \tag{4.1}$$

where n is the order of reflection, θ is the angle of incidence and λ is the wavelength of the incident X-rays, which strike the crystal, where all atoms are placed in a regular periodic array with interplanar spacing d (Figure 4.1).

4.1.2   X-ray Reflectivity (XRR)

X-ray reflectivity measures the intensity of X-rays reflected in the specular direction from a flat surface at low angle (Grazing angle). If the interface is not perfectly

smooth or sharp, the reflected intensity will deviate from the law of Fresnel reflectivity. Density, roughness and thickness can be obtained with this method. At each interface, a portion of X-rays is reflected. Interferences of these partially reflected X-ray beams create a reflectometry pattern. The fringes that appear are called Kiessig fringes in honor to their discoverer (Figure 4.2) [60].
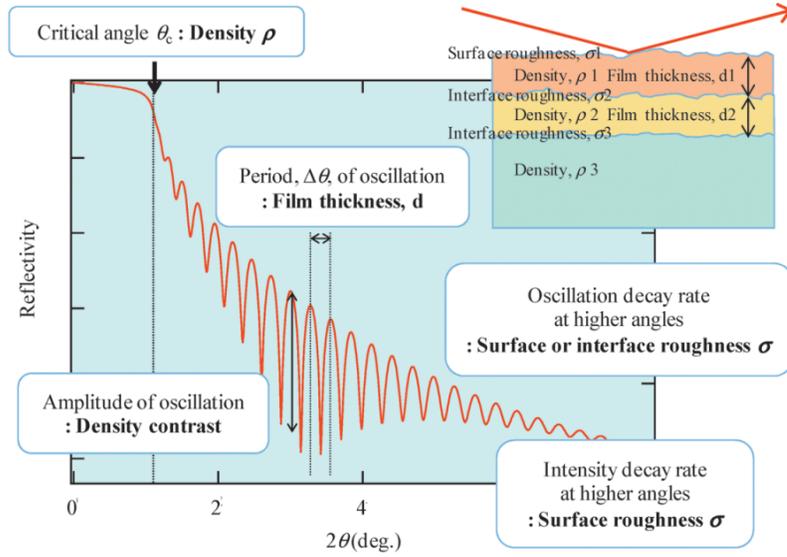
Figure 4.2: Schematic of typical results of XRR [61].

Thickness can be obtained from XRR using Equation 4.2, which is analog to Bragg's law but modified by the influence of refraction.

$$2d\sqrt{sin^2\theta_{im} - sin^2\theta_c} = m\lambda \tag{4.2}$$

where d is the thickness of the layer, λ is the X-ray wavelength (here Cu Kα = 1.54 Å), θ_{im} is the incident angle at which there is an intensity maximum, m is an integer (the fringe order) and θ_c is the critical angle of total external reflection of the layer . If the refraction is neglected, this equation can be approximated as:

$$d \approx \frac{\lambda}{2sin\Delta\theta} \tag{4.3}$$

where $\Delta\theta$ is the difference of angles of two maxima.

For this study, a sealed tube x-ray source with a Huber 4 full circle diffractometer and Cu-Kα radiation was used for XRD and XRR with the help of Dr. Michael Pierce, College of Science, RIT.

4.1.3   X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy is a widely used non-destructive surface analysis technique, which provides quantitative and chemical state information from the surface of the studied material. XPS spectrum is obtained by exposing a solid surface to a beam of X-rays while measuring the kinetic energy and number of photo-emitted electrons from the top 1- 10 nm of the material [62]. The binding energy can be deduced from the kinetic energy. Binding energy and intensity of a photoelectron peak determine the identity, chemical state and quantity of a detected element. Using this technique, the amount of dopant in the film of hafnium oxide can be determined.

XPS measurements were performed using a Physical Electronics UHV system with an x-ray photoelectron spectrometer (XPS) with the help of Dr. Michael Pierce, College of Science, RIT. X-rays were produced with a Mg anode without monochromator.

4.1.4   Transmission Electron Microscopy (TEM) and Electron Energy Loss Spectroscopy (EELS)

Transmission electron microscopy is a microscopy technique capable of imaging at higher resolution than optical microscopes, due to the small de Broglie wavelength of electrons. Sub-nanometer resolution can be obtained with this particular method. Scanning TEM (STEM) differs from conventional TEM by focusing the electron beam into a narrow spot, which is scanned over the sample. It provides a highly local information about a thin specimen (typically 100 nm) [63].

During electron energy loss spectroscopy, a material is exposed to a beam of electrons. During the interaction with the sample, some of the electrons lose energy due to inelastic scattering. EELS involves the analysis of the energy distribution of electrons, giving indication of the material [64].

In this study, TEM/EELS was performed at Micron, Manassas by David McMahon employing a Hitachi HAADF HD-2300A STEM. The sample was prepared using a focused ion beam (FIB).

4.1.5   Atomic Force Microscopy (AFM)

Atomic force microscopy is a high resolution scanning probe microscopy, designed to measure local properties, such as height, roughness, with a probe. AFM operates by measuring force between a probe and the sample.

In this study, AFM was used to get the roughness of the different deposited films with the help of Dr Gupta, College of Engineering, RIT.

4.2   Electrical characterization

4.2.1   Polarization-Voltage measurement (P-V)

Polarization measurements give parameters specific to a ferroelectric material, such as the remanent polarization and the coercive field. It also gives the P-V hysteresis loop, typical of ferroelectric sample. Getting such parameters of a sample means being able to measure its current and charge response due to an applied excitation voltage.

A Sawyer-Tower circuit enables the measurement of ferroelectric characteristics: polarization hysteresis, fatigue, retention, imprint. This circuit was proposed by C.B. Sawyer and C. H. Tower during their studies on the Rochelle Salt in 1929 [65]. Sawyer-Tower circuit is based on a charge measurement method. A reference linear capacitor

and the ferroelectric capacitor are in series between the excitation AC signal and ground (Figure 4.3a). The voltage drop at the reference capacitor is proportional to the polarization charge as defined by :

| (a) | (b) |
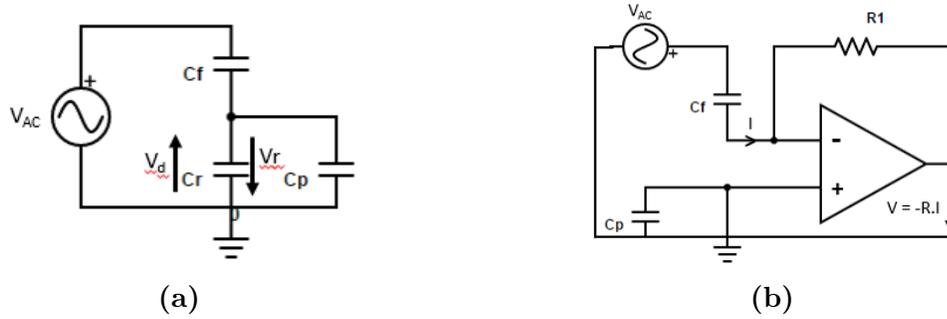
Figure 4.3: (a) Sawyer-Tower circuit. (b) Virtual Ground method

$$P = \frac{Q}{A_f} = \frac{V_r \times C_r}{A_f} \tag{4.4}$$

where V_r is the voltage drop, Q is the polarization charge, C_r is the capacitance of the linear capacitor and A_f is the area of the ferroelectric capacitor. A hysteresis curve results from the plotting of the voltage drop, *i.e.* polarization, versus the total applied voltage. This circuit can be used up for frequencies up to 10^6 hertz and is primarily limited by cable reflections. Although this technique works well and is easy to use, it has some drawbacks: specific frequency window over which it is accurate, small ferroelectric capacitors blinded in the total measured capacitance, parasitic cable capacitance (C_p) and voltage drop back (V_d) across the reference capacitor.

The Shunt measurement technique is another method, in which the reference capacitor of the Sawyer-Tower circuit is substituted with a reference resistor. In this current based method, the switching current is measured as a voltage drop at the resistor and numerically integrated to get the polarization charge $Q = \int I dt$. However, the reference resistance value depends on the sample capacitance and on the frequency. Therefore, the voltage drop increases with increasing frequency. Accurate measurements are possible for large devices but it becomes very difficult for smaller

devices, where the parasitic capacitance starts playing a role.

Finally, the Virtual Ground method uses a current to voltage converter, based on current measurement using an operational amplifier with a feedback resistor. As can be seen in Figure 4.3b, the signal from the ferroelectric capacitor is connected to the inverting input and the noninverting input is connected to ground. Therefore, the inverting input is virtually on ground level, which is very helpful for small capacitors: the cable capacitance becomes electrically ineffective, as both electrodes of the capacitor are kept on the same potential.

Overall, the Virtual Ground method enables the most accurate measurements for ferroelectric capacitors by eliminating the influence of parasitic capacitance and back voltage known from the Sawyer-Tower method.

In a P-V measurement, the test sequence is composed of four pulses: A prepol pulse is first applied, followed by three bipolar triangular excitation signals, each signal is followed by a relaxation time of 1 sec (Figure 4.4a). As the state of the internal polarization of a ferroelectric capacitor is unknown before a test, a preset loop is necessary to preset the internal polarization of the sample. The first signal starts with the same polarity as the preset loop, the last two start with the other polarization state. The final PE loop is usually made by using the second half and the last half of the first and last excitation, respectively, because the polarization measured dynamically is usually different from the one obtained after some relaxation time.

Although a hysteresis curve may indicate the presence of ferroelectricity, it is not a sufficient condition. Leakage currents and surface polarization for example, can also result in a hysteresis behavior. In case of a ferroelectric sample, the current versus voltage plot shows that two peaks should be independent of frequency. They are due to the switching polarization, in which the screening surface charges flow from one electrode to another, resulting in an additional current. The integration of
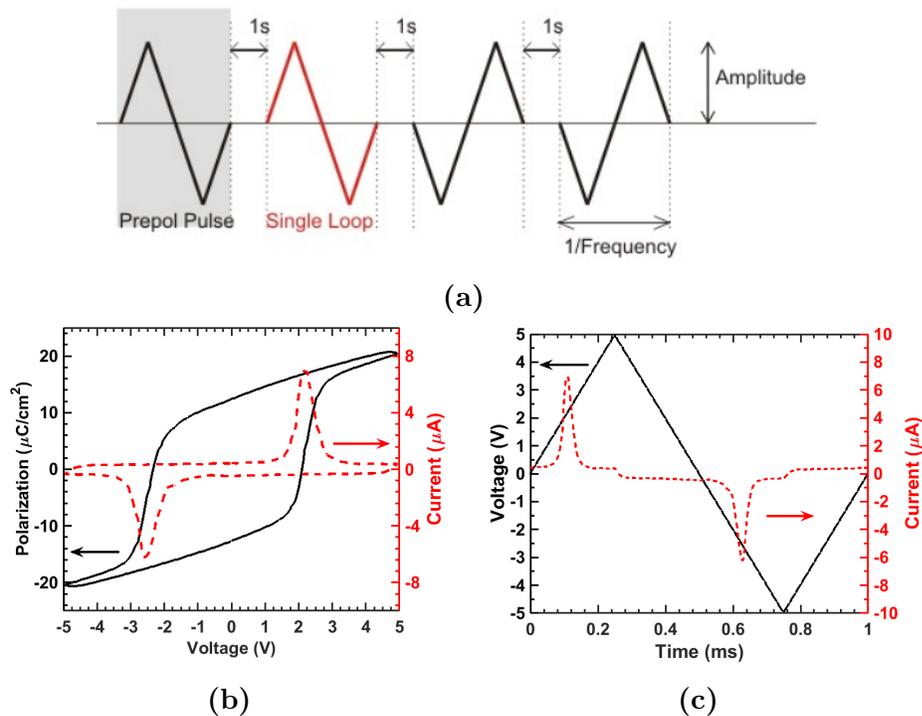
Figure 4.4: (a) P-V parameters used in this study. (b) Current/Polarization versus Voltage and (c) Voltage/Current versus Time in case of a PZT film of 255 nm,measured at a frequency of 1 kHz.

current (Figure 4.4b) over time provides the polarization values (Figure 4.4c).

Polarization Voltage (P-V) measurements were realized with a TF 1000 aix-ACCT Measurement Systems, using the Virtual Ground method. The frequency applied in this study was 1 kHz, except indicated otherwise.

4.2.2 PUND measurement

This measurement records the current response of the device under test. PUND stands for Positive Up Negative Down. A PUND pulse sequence is composed of a preset pulse, followed by two positive and two negative consecutive pulses, using unipolar rectangular pulses (Figure 4.5).

Each pulse will give different information, resulting in more relevant ferroelectric characteristics for memory applications than the standard P-V measurement. The preset pulse, or negative write pulse, will set the initial polarization. The second
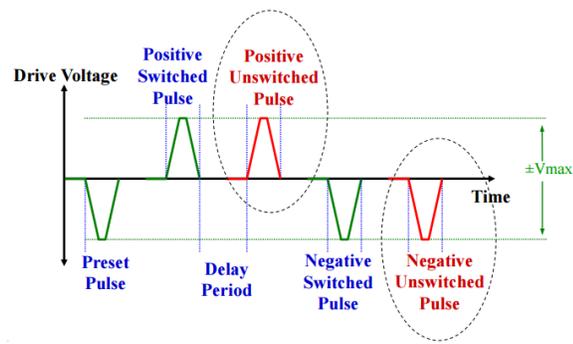
Figure 4.5: PUND sequence
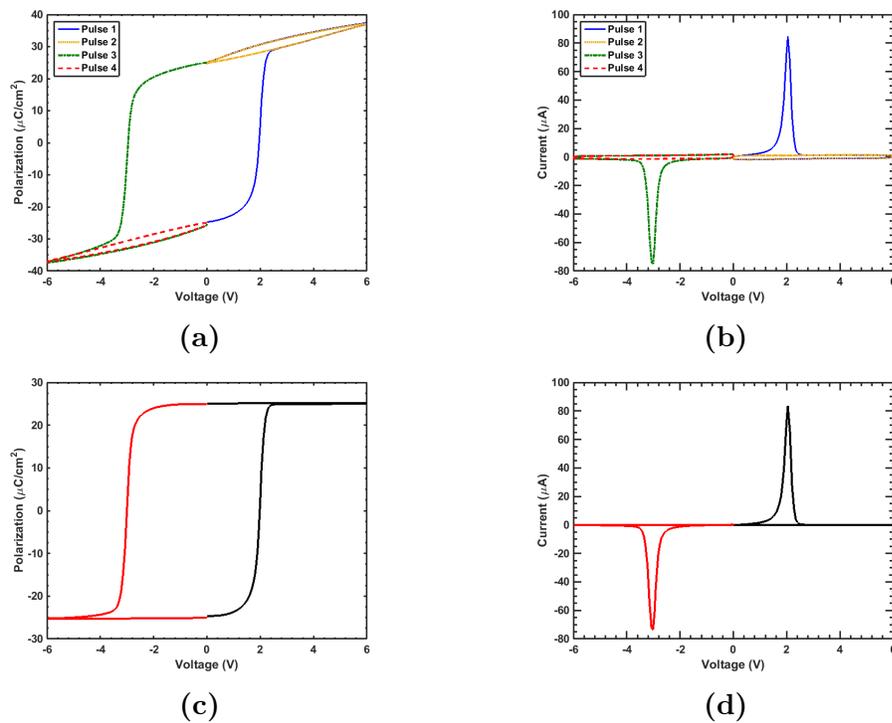
Figure 4.6: (a) PUND measurement of a 255 nm thick PZT film. (b) I-V curves of the same sample. (c) Real P-V and (d) real I-V after subtraction of the non-switching current.

pulse switches the polarization. The third pulse is similar to the second pulse. It is a non-switching pulse, since the polarization has already been switched. Therefore, no switching current should appear. The two last pulses are in the opposite direction, switching the polarization in the other state. Even if no switching current should appear during pulse 2 and 4, a current is observed due to the charging and discharging of the sample and in some case due to the leakage current (Figure 4.6b). A typical

PUND plot can be seen in Figure 4.6a. The subtraction of the non-switching to the switching current in both cases (positive up and negative down) will give the real amount of polarization, *i.e.* without leakage, dielectric charging and trapping contributions (Figure 4.6d). By integrating this current with respect to time, the real amount of charges can be calculated.

4.2.3 Fatigue measurement

Fatigue measurements give an indication about the lifetime of a device. Many cycles are applied to the sample and P-V measurements are realized, to get the ferroelectric characteristics, between each cycle. Any degradation of P_r or E_c is seen as the start of the degradation of the device. After a preset pulse, symmetrical bipolar rectangular pulses are applied, with pulse number going from 1 to 10^9 in this study.

4.2.4 Capacitor-Voltage measurement (C-V)

Besides the standard polarization-voltage hysteresis, capacitance-voltage measurements can be used to confirm the presence of a ferroelectric film, in harmony with a P-V hysteresis. A hysteresis dependence between polarization and electric field is a necessary but not a sufficient condition to confirm the presence of a ferroelectric material, as it has been said previously in section 4.2.1. The dielectric constant of ferroelectric material is very field dependent and its C-V curve presents a hysteresis, as has been discussed in section 3.1.

Capacitance-voltage measurement are performed with an LCR meter. A DC bias voltage is applied across a capacitor, while making the measurements with an AC signal ([66]) . The capacitance for the device under test can be calculated using:

$$C = \frac{I}{2\pi f V_{AC}} \tag{4.5}$$

where I is the magnitude of the AC current through the capacitor, f is the test

frequency, V_{AC} is the magnitude and phase angle of the measured AC voltage. These measurements take into account series (contact issues, high substrate resistance) and parallel (high leakage current) resistance associated with the capacitor as well as the dissipation factor (D). High D is a limiting factor, as the accuracy of the measurement is degraded. Higher frequencies can help solve the problem and eliminate the impact of parasitic parallel resistance.

C-V measurements were performed using a HP 4284A precision LCR meter.

Chapter 5

Modeling Ferroelectric Capacitor Structures

5.1 Theory of MIFIS structure

When engineering a device, simulation is often useful before starting a process or to better understand the device. Also, comparing experimental values to simulated device values can give information on the properties of the material.

In 1992, Miller *et al.* [15] developed a simple quantitative model, combining the switching mechanism of ferroelectric capacitors with the physics of Metal-Oxide-Semiconductor (MOS) FETs, based on the charge sheet approximation model, which assumes that the inversion layer of the silicon can be approximated by a conducting plane of zero thickness.

In this chapter, Miller's work will be detailed for a MIFIS capacitor. The equations can be easily modified for MFIS or MIFS capacitors. The electrostatic equations for the ferroelectric capacitor (Figure 5.1) are derived using Maxwell's equation:
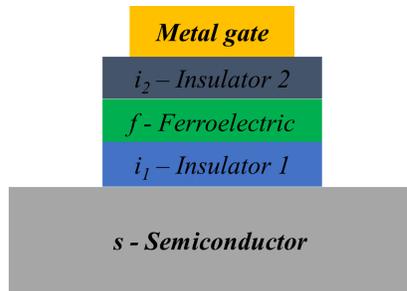
Figure 5.1: Schematic of a MIFIS capacitor

$$\Delta \cdot D = \rho \tag{5.1}$$

and

$$D = \epsilon_k \epsilon_0 E_k + P_k \tag{5.2}$$

where D is the electric displacement, ρ is the charge density, $k = \{f, i_1, i_2, s\}$, f represents the ferroelectric layer, $i_{1,2}$ represent the insulator layers and s represents the semiconductor. P_k corresponds to the polarization and is nonzero only in the ferroelectric layer. E_k is the electric field in the layer k, ϵ_k is the dielectric constant of the layer k and ϵ_0 is the vacuum permittivity $(8.854 \times 10^{14} F/cm^2)$. P_f is a function of the electric field in the ferroelectric layer and will be written $P(E_f)$. The total charge per area in the capacitor can be expressed as:

$$Q_g + Q_{i_1} + Q_s = 0 \tag{5.3}$$

where Q_g, Q_{i_1} and Q_s are the charges in the gate, at the interface between insulator and semiconductor and in the semiconductor respectively. Assuming, no interface charge, $i.e.$ $Q_{i_1} = 0$, this expression becomes:

$$Q_g = -Q_s \tag{5.4}$$

Using Equations 5.2, 5.4 and Gauss' law: $-Q_s = \epsilon_s \epsilon_0 E_s$:

$$-Q_s = \epsilon_s \epsilon_0 E_s = \epsilon_f \epsilon_0 E_f + P(E_f) = \epsilon_{i_1} \epsilon_0 E_{i_1} = \epsilon_{i_2} \epsilon_0 E_{i_2} \tag{5.5}$$

or

$$-Q_s = \epsilon_s \epsilon_0 E_s = \frac{\epsilon_f \epsilon_0 V_f}{t_f} + P(E_f) = \frac{\epsilon_{i_1} \epsilon_0 V_{i_1}}{t_{i_1}} = \frac{\epsilon_{i_2} \epsilon_0 V_{i_2}}{t_{i_2}} \tag{5.6}$$

where $V_{i_{1,2}}$ and V_f are the voltage dropping in the insulators and the ferroelectric

respectively and $t_{i_{1,2}}$ and t_f are the thicknesses of the insulator and ferroelectric layers, respectively. The total gate voltage V_g is given by:

$$V_g = V_{FB} + \psi_s + V_{i_1} + V_{i_2} + V_f \tag{5.7}$$

where ψ_s is the silicon surface potential and V_{FB} is the flat band voltage, which can be written as:

$$V_{FB} = \Phi_{MS} - \frac{Q_{i_1}}{C_{i_1}} = \Phi_M - \left(\chi + \frac{E_c - E_{i_1}}{q} + \phi_F\right) - \frac{Q_{i_1}}{C_{i_1}} \tag{5.8}$$

where Φ_{MS} is the work function difference between the gate metal and the semiconductor, Φ_M is the work function of the gate metal, C_{i_1} is the capacitance of the insulator 1, χ is the electron affinity of silicon, E_c is the conduction band energy, E_i is the intrinsic energy, q is the electronic charge and ϕ_F is the bulk potential expressed as:

$$\phi_F = \phi_t ln\left(\frac{p}{n_i}\right) = -\phi_t ln\left(\frac{n}{n_i}\right) \tag{5.9}$$

where $\phi_t = \frac{kT}{q}$, k is the Boltzmann constant, T is the temperature, q is the electric charge, p and n are the substrate doping, respectively p-type and n-type and n_i is the intrinsic doping of the silicon. As it is assumed that there is no charge at the interface, the flat band voltage is simply equal to the work function ($V_{FB} = \Phi_{MS}$) . Thus, Equation 5.7 can be re-written using Equation 5.6 :

$$V_g = V_{FB} + \psi_s - \frac{Q_s(\psi_s)t_{i_1}}{\epsilon_{i_1}\epsilon_0} - \frac{Q_s(\psi_s)t_{i_2}}{\epsilon_{i_2}\epsilon_0} - \frac{Q_s(\psi_s)t_f}{\epsilon_f\epsilon_0} - \frac{P(E_f)t_f}{\epsilon_f\epsilon_0} \tag{5.10}$$

or

$$V_g = V_{FB} + \psi_s - \frac{Q_s(\psi_s)}{C_{stack}} - \frac{P(E_f)}{C_f} \tag{5.11}$$

where

$$C_{stack} = \left(\frac{t_{i_1}}{\epsilon_{i_1}\epsilon_0} + \frac{t_{i_2}}{\epsilon_{i_2}\epsilon_0} + \frac{t_f}{\epsilon_f\epsilon_0} \right)^{-1} \tag{5.12}$$

$$C_f = \left(\frac{t_f}{\epsilon_f\epsilon_0} \right)^{-1} \tag{5.13}$$

where C_{stack} and C_f are the capacitance per area of the dielectric stack and the ferroelectric layer respectively. The electric field of the ferroelectric layer E_f can be expressed as:

$$E_f = -\frac{Q_s + P(E_f)}{\epsilon_f\epsilon_0} \tag{5.14}$$

The charge in the semiconductor per area, Q_s, is defined for a p-type substrate as:

$$Q_s(\psi_s) = -sgn(\psi_s)\sqrt{2q\epsilon_s\epsilon_0 N_a}\left[\left(\phi_t e^{\left(\frac{-\psi_s}{\phi_t}\right)} + \psi_s - \phi_t \right) + \left(\frac{n_i}{N_a} \right)^2 \left(\phi_t e^{\left(\frac{\psi_s}{\phi_t}\right)} - \psi_s - \phi_t \right) \right]^{(1/2)} \tag{5.15}$$

and for an n-type substrate :

$$Q_s(\psi_s) = -sgn(\psi_s)\sqrt{2q\epsilon_s\epsilon_0 N_d}\left[\left(\phi_t e^{\left(\frac{\psi_s}{\phi_t}\right)} - \psi_s - \phi_t \right) + \left(\frac{n_i}{N_d} \right)^2 \left(\phi_t e^{-\left(\frac{\psi_s}{\phi_t}\right)} + \psi_s - \phi_t \right) \right]^{(1/2)} \tag{5.16}$$

where N_a and N_d refer to the majority carrier concentration of the p-type and n-type semiconductor respectively. If $P(E_f)$ and ψ_s are known, it is therefore possible to solve these equations.

The total capacitance per area C_{total}, obtained from series combination of multi-layered capacitance, can be expressed as:

$$C_{total} = \left(\frac{1}{C_{i_1}} + \frac{1}{C_{i_2}} + \frac{1}{C_f} + \frac{1}{C_s} \right)^{-1} = \left(\frac{t_{i_1}}{\epsilon_{i_1}\epsilon_0} + \frac{t_{i_2}}{\epsilon_{i_2}\epsilon_0} + \frac{t_f}{\epsilon_f\epsilon_0} + \frac{1}{C_s} \right)^{-1} \tag{5.17}$$

where C_{i_1} and C_{i_2} are the capacitances per area of the insulator layers. C_s is the capacitance per area of the semiconductor and is expressed at low frequency as:

For a p-type substrate:

$$C_s = sgn(\psi_s)\sqrt{2q\epsilon_s\epsilon_0 N_a} \frac{\left(1 - e^{\frac{\psi_s}{\phi_t}}\right) + \left(\frac{n_i}{N_a}\right)^2 \left(e^{\frac{\psi_s}{\phi_t}} - 1\right)}{2 \times \left[\left(\phi_t e^{\left(\frac{-\psi_s}{\phi_t}\right)} + \psi_s - \phi_t\right) + \left(\frac{n_i}{N_a}\right)^2 \left(\phi_t e^{\left(\frac{\psi_s}{\phi_t}\right)} - \psi_s - \phi_t\right)\right]^{1/2}}$$

(5.18)

For a n-type substrate:

$$C_s = sgn(\psi_s)\sqrt{2q\epsilon_s\epsilon_0 N_d} \frac{\left(e^{\frac{\psi_s}{\phi_t}} - 1\right) + \left(\frac{n_i}{N_d}\right)^2 \left(1 - e^{\frac{-\psi_s}{\phi_t}}\right)}{2 \times \left[\left(\phi_t e^{\left(\frac{\psi_s}{\phi_t}\right)} - \psi_s - \phi_t\right) + \left(\frac{n_i}{N_d}\right)^2 \left(\phi_t e^{\left(\frac{-\psi_s}{\phi_t}\right)} + \psi_s - \phi_t\right)\right]^{1/2}}$$

(5.19)

At high frequency, the capacitance does not follow Equations 5.18 or 5.19, because the generation rate of the charge carriers from the depletion region cannot follow the rapid change of the applied signal. To get the capacitance per area at strong inversion condition ($\sim \psi_s > 2\phi_F + 6\phi_t$ [67]), Sun *et al.* [68] uses this equation:

$$C_s = \frac{\epsilon_s\epsilon_0}{t_{dm}}$$

(5.20)

where

$$t_{dm} = \left(\frac{4\epsilon_s\epsilon_0\phi_t}{qN_a}ln\left(\frac{N_a}{n_i}\right)\right)^{1/2} = \left(\frac{4\epsilon_s\epsilon_0\phi_t}{qN_d}ln\left(\frac{N_d}{n_i}\right)\right)^{1/2}$$

(5.21)

Using the previous equations and knowing $P(E_f)$, it is possible to get the capacitance as a function of voltage (Figure 5.2), showing a hysteresis behavior.

The width of the hysteresis, which can also be seen as the shift of the flatband voltage ΔV_{FB} or the shift of the threshold voltage for FeFET, as seen in Chapter 3.2, is defined as the memory window of the device and can have a maximum value for the saturated loop defined as [16],:

$$\Delta V_{FB} = 2E'_c t_f \approx 2E_c t_f(1 - 2\delta\epsilon_f\epsilon_0/P_s)$$

(5.22)
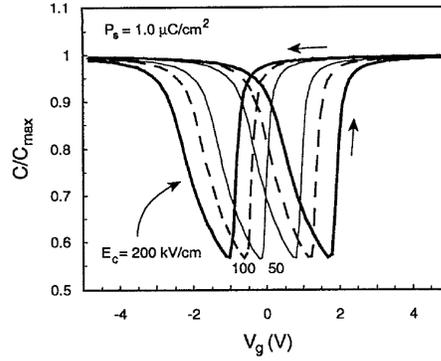
Figure 5.2: Capacitance-Voltage curves for MIFIS capacitors with different coercive field [15].

where $\delta = E_c \left[ln \left(\frac{1 + P_r/P_s}{1 - P_r/P_s} \right) \right]^{-1}$, P_r is the remanent polarization, P_s is the spontaneous polarization and E_c is the coercive field.

Miller *et al.* [15] developed a simple mathematical model to express the dipole polarization. This polarization depends on the previous history of the ferroelectric electric field and is therefore determined by integrating $dP(E_f)/dE_f$. In a P-E hysteresis loop, the dipole polarization approaches asymptotic value of $\pm P_s$, for large electric field value. When all the dipoles are aligned, the polarization is called the saturation polarization P_{sat}. Many mathematical expressions have been proposed to mimic best the hysteresis. In this paper, the hyperbolic tangent function has been chosen as it mimics the phenomenon quite accurately. The saturated polarization hysteresis loop is defined as:

$$P_{sat}^+ = P_s tanh \left(\frac{E_f - E_c}{2\delta} \right) \tag{5.23}$$

where + superscript signifies the positive-going branch of the loop. The negative-going branch is given by:

$$P_{sat}^- = -P_{sat}^+ \tag{5.24}$$

The derivative of the polarization is given by:

$$\frac{dP(E_f)}{dE_f} = \Gamma \frac{dP_{sat}}{dE_f} \tag{5.25}$$

where $\Gamma = 1 - tanh\left[\left(\frac{P(E_f)-P_{sat}(E)}{\xi P_s - P(E_f)}\right)^{1/2}\right]$ and $\xi = +1$ when $dE_f/dt > 0$ and $\xi = -1$ when $dE_f/dt < 0$.

The derivative of the saturated polarization using Equation 5.23 is:

$$\frac{dP_{sat}^+}{dE_f} = \frac{P_s}{2\delta} sech^2\left(\frac{E_f - E_c}{2\delta}\right) \tag{5.26}$$

It has been seen previously with Equation 5.5 that:

$$-Q_s(\psi_s) = \epsilon_f \epsilon_0 E_f + P(E_f) \tag{5.27}$$

Therefore, dE_f can be expressed as:

$$dE_f = -\frac{dQ_s(\psi_s)}{\epsilon_f \epsilon_0 + \frac{dP(E_f)}{dE_f}} \tag{5.28}$$

Numerical evaluation of these equations allows one to solve for P-E and therefore C-V relations. These polarization equations fit well into the P-E relation of the saturated hysteresis, however they cannot accurately describe the nonsaturated, also called minor, situation (Figure 5.3). This happens when the applied voltage is more than the coercive voltage but not high enough to reverse all the domains. Lue *et al.* [16] have developed a new expression for the minor loops using E_m the maximum electric field that the ferroelectric may experience:

$$P^+(E_f, E_m) = P_s tanh\left(\frac{E_f - E_c}{2\delta}\right) + \epsilon_f \epsilon_0 E_f + \frac{1}{2}\left(P_s tanh\left(\frac{E_m + E_c}{2\delta}\right) - P_s tanh\left(\frac{E_m - E_c}{2\delta}\right)\right) \tag{5.29}$$

$$P^-(E_f, E_m) = P_s tanh\left(\frac{E_f + E_c}{2\delta}\right) + \epsilon_f\epsilon_0 E_f - \frac{1}{2}\left(P_s tanh\left(\frac{E_m + E_c}{2\delta}\right) - P_s tanh\left(\frac{E_m - E_c}{2\delta}\right)\right)$$

(5.30)

The polarization as a function of the maximum electric field is defined as:

$$P_d(E_m) = \epsilon_f\epsilon_0 E_m + \frac{1}{2}\left(P_s tanh\left(\frac{E_m + E_c}{2\delta}\right) - P_s tanh\left(\frac{E_m - E_c}{2\delta}\right)\right) \qquad (5.31)$$

To better understand how the hysteresis loop is obtained, the calculations of these equations are used in three steps: first, the ferroelectric is at origin ($P = 0$, $E_f = 0$). An electric field is then applied and the dipole moment will follow the curve $P_d(E_m)$ until the maximum electric field is reached. The polarization will then follow $P^-(E_f, E_m)$ and then $P^+(E_f, E_m)$.
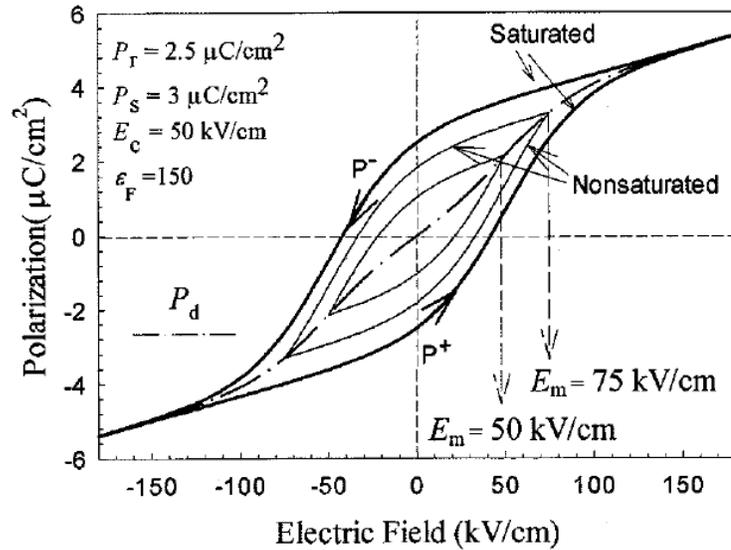
Figure 5.3: P-E for the ferroelectric materials under various maximum electric fields [16].

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5.2 Simulation with Matlab

The software Matlab was used to integrate the equations from Miller's and Lue's theory. A graphical interface was also made to facilitate its use and different options were added such as overlay, save plot or upload of experimental results for comparison and extraction of material properties.

5.2.1 User Interface
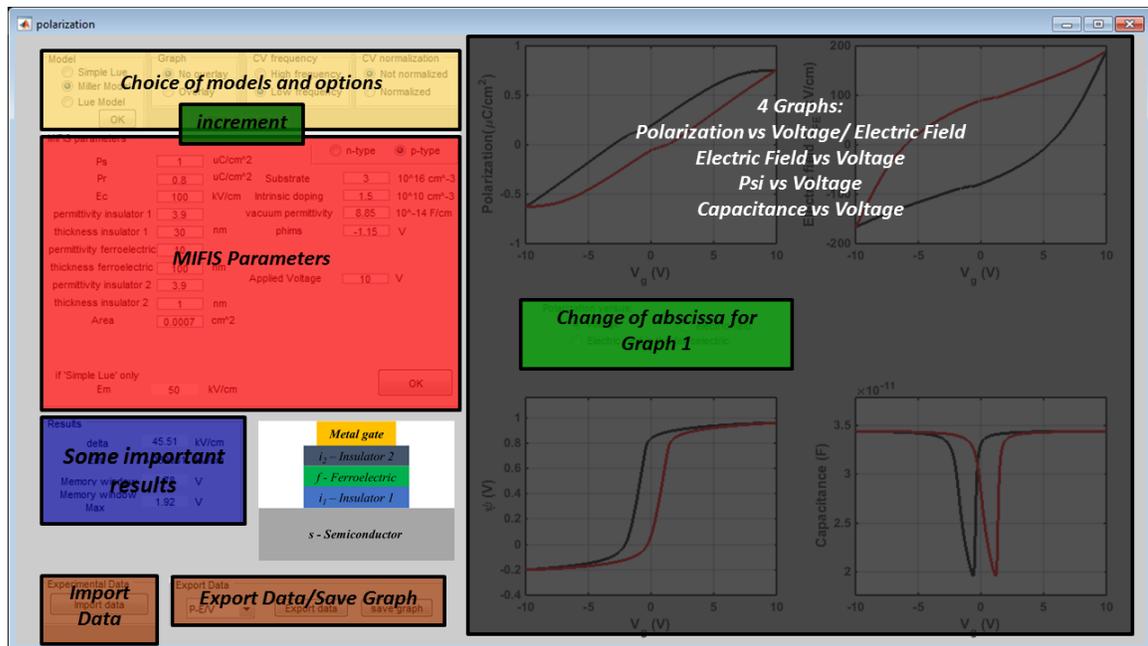
Figure 5.4: Interface of the program

The interface was developed for fast and easy use. Each important part, corresponding to different colors in Figure 5.4, will be developed and explained.

5.2.1.1 Choice of models and options

A) Models:

Three models can be found on the interface: Simple Lue, Miller Model and Lue Model (Figure 5.5). They are arranged by computational time and accuracy of

Figure 5.5: Models and options

the model. Miller model will be first described as it is the original one.

- **Miller Model**

  Miller Model uses the equations described previously in this chapter.

  The first part is the initialization by setting up the initial condition: $V_g = V_{FB}$ and $P(E_f) = 0$. The initial ψ_s is then calculated by solving simultaneously Equations 5.11 and 5.15 (or 5.16 for n-type substrate). The initial Q_s, E_f, P_{sat}, Γ, $\frac{dP_{sat}}{dE_f}$, $\frac{dP(E_f)}{dE_f}$, C_s and C_{total} result from these constants.

  The numerical integration from the initial conditions to a new set of conditions is performed by simultaneously solving Equations 5.11, 5.14, 5.15 (or 5.16 for n-type substrate) and 5.25. ψ_s is varied and for the ith value of ψ_s the polarization can be written as (the subscript f is dropped to avoid confusion):

  $$P(E_i) = P(E_{i-1}) + (E_i - E_{i-1}) \frac{d}{dE} [P(E)]|_{E_{i-1}} \qquad (5.32)$$

  Using Equation 5.14, this equation becomes:

  $$P(E_i) = \frac{P(E_{i-1}) - (Q_s/(\epsilon_f \epsilon_0) + E_{i-1}) \frac{d}{dE} [P(E)]|_{E_{i-1}}}{1 + \frac{1}{\epsilon_f \epsilon_0} \frac{d}{dE} [P(E)]|_{E_{i-1}}} \qquad (5.33)$$

  Now, the ith value of V_g can be calculated, followed by the other values. ψ_s is increased to reach the saturated polarization, then it is decreased to get the negative saturated polarization (negative branch of the hysteresis) and

then increased again (positive branch of the hysteresis). The equations are modified accordingly.

- **Lue Model**

  In this model, the initialization step is similar to Miller's model: V_g, $P(E_f)$ and ψ_s, calculated using Equations 5.11 and 5.15, are necessary to get the initial value of Q_s, C_s and C_{total}. The difference is with the presence of the constant E_m, due to the minor loops. E_m is calculated by solving simultaneously Equations 5.11, 5.27 and 5.31.

  Once the initial values are obtained, ψ_s is increased to get the 'final 'E_m corresponding to the maximum applied voltage. ψ_s is then decreased to follow the negative branch of the hysteresis. The electric field is that time calculated using E_m and by solving simultaneously Equations 5.11, 5.27 and 5.30, the polarization is obtained using Equation 5.30. ψ_s is finally increased and the equations, corresponding to the positive branch of the hysteresis, are used the same way as previously.

- **Simple Lue**

  This model is an easy way to get polarization vs applied voltage/electric field. In Lue's model, if E_m is known, by varying the applied voltage/electric field, the polarization can be found using only Equations 5.29 and 5.30. This model is not suitable if the applied voltage is not symmetrical but it is time-saving in the computer calculation.

B) Graph (Figure 5.5):

An overlay option is possible in this program in order to compare different models or different parameters. By default, each graph is unique and there is no overlay.

C) C-V frequency (Figure 5.5):

The behavior of a Capacitance - Voltage curve of a semiconductor at strong inversion depends on the frequency, as explained previously. The choice is given to the user between low and high frequency. By default, the frequency is high.

D) C-V Normalization (Figure 5.5):

The choice is given to the user to simulate normalized or not normalized C-V curves. To normalize the curve, this equation is applied:

$$C_{i,normalized} = \frac{C_i}{C_{max}} \tag{5.34}$$

By default, the curve is not normalized.

5.2.1.2 Increment

For Miller and Lue's model, ψ_s is the constant, which is incremented. The smaller the increment is set to (also called step here (Figure 5.5)), the more accurate the simulation will be. By varying the silicon surface potential, the other constants can be calculated. To solve two equations simultaneously, the Matlab function *solve(eqn,var)* is used and is the one, which requires computational power. Miller's model needs to use this function only once during the initiation step. Therefore a small increment will not change drastically the time of computation. However, Lue's Model also uses the *solve* function at each step of the iteration to get first E_m, E^- and then E^+. Therefore a compromise is necessary when using this model: an accurate simulation will require a substantial amount of computational time, from a few seconds to a few hours.

For Lue simple model, the electric field is incremented using a constant increment of 10^3, corresponding to 1 kV/cm.
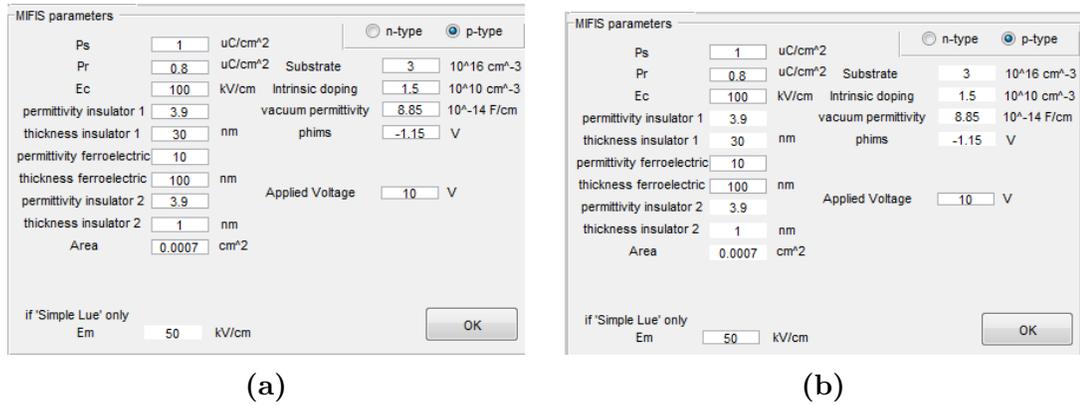
Figure 5.6: (a) Parameters for Miller and Lue's models. (b) Parameters for Simplu Lue model

5.2.1.3 MIFIS Parameters

In this section of the program, the parameters of the device are added (Figure 5.6). A MIFIS device can be simulated. If, for example, only MFIS is wanted, the thickness of the second insulator can just be changed to a very small thickness. If zero is written, the program will crash, as zero thickness corresponds to an 'infinite capacitance '.

- **Parameters shared by all models**

  To simulate a ferroelectric material, the important parameters of the film need to be added: Spontaneous polarization, Remanent polarization, Coercive electric field, Permittivity and Thickness of the layer. The range of voltages is also needed, as it is specific to each simulation.

- **Only Miller and Lue's models** (Figure 5.6a)

  For these models, the stack is important. Permittivity and thickness of each layer should be added. The area of the device, which is assumed to be the same for all layers, the substrate doping and the flatband voltage are required. Intrinsic doping of the substrate and vacuum permittivity can also be changed.

- **Only Simple Lue model** (Figure 5.6b)

The last parameter required for this model is the maximum electric field E_m.

To prevent mistakes, the interface was designed to allow the user to change the parameters, which are required for one model only. By default, the parameters are the one from Miller's paper [15].

5.2.1.4 Some important results

Four important results are given:

- δ, which corresponds to $\delta = E_c \left[ln \left(\frac{1+P_r/P_s}{1-P_r/P_s} \right) \right]^{-1}$ and is used for the calculations of the polarization.

- E_m, which is the maximum electric field, only for Simple Lue and Lue Model.

- Memory window, which corresponds to the shift of the flatband voltage, only for Miller and Lue's models.

- Maximum memory window, which corresponds to the theoretical maximum shift of the flatband voltage (Equation 5.22).

Figure 5.7: Some important results

5.2.1.5 Graphs

For Miller and Lue's models, four graphs can be plotted (Figure 5.8): Polarization vs Voltage/Electric Field/Electric field in the ferroelectric layer (P-V/E/E_{FE}) , Electric field of the ferroelectric layer vs Voltage (E_{FE}-V), ψ_s vs Voltage (ψ_s-V) and

Capacitance vs Voltage (C-V). The black curve corresponds to the negative branch and the red curve corresponds to the positive branch. The abscissa of the P-V/E graph can be changed to voltage or electric field. For Simple Lue model, only P-V/E can be plotted.
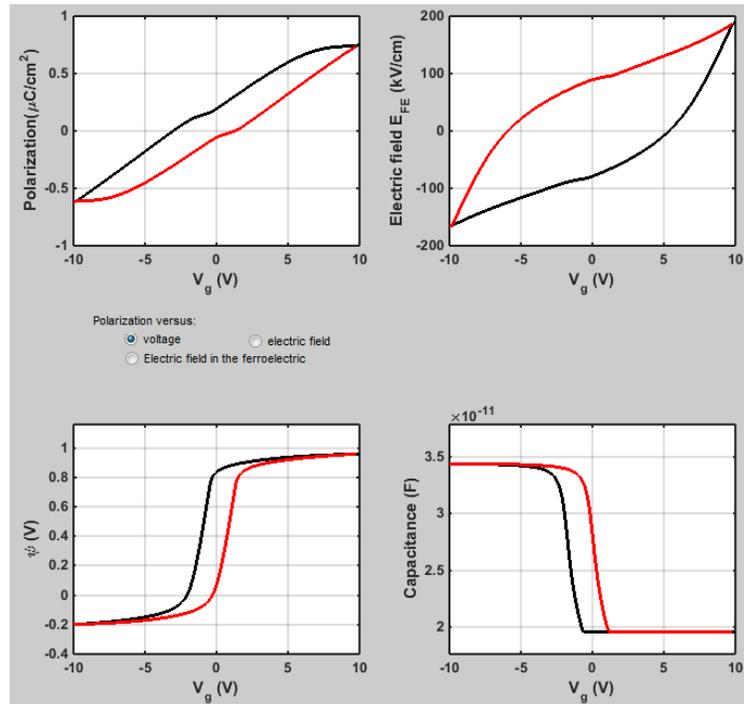
Figure 5.8: Graphs window

5.2.1.6   Import and export data

It is possible to import polarization vs voltage/electric field data (Figure 5.9). When choosing the overlay option, the parameters of the experimental data can therefore be extracted by simulating different models. It is also possible to export the simulated data and to save the graph in different format. For now, the program does not allow for exporting data of an overlay. If overlaid, it will save only the last simulation.
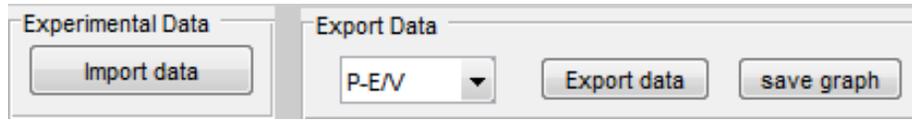
Figure 5.9: Import and export data window

5.2.2 Validation with published data

In this section, devices and conditions described in different papers will be simulated and compared with the published results to validate the program. First, a few papers using Miller's equations will be simulated, then papers using the modified equations, based on Lue's paper [17].

5.2.2.1 Miller Model

A) "Physics of the ferroelectric nonvolatile memory field effect transistor", Miller *et al.* [15]

It seems necessary to start with the paper, which first explained the development of the ferroelectric transistor model. The device parameters can be found in [15] and are also the parameters by default in the MATLAB program: $P_s = 1 \ \mu C/cm^2, P_r = 0.8 \ \mu C/cm^2, E_c = 100 \ kV/cm, t_f = 100 \ nm, t_{i_1} = 30 \ nm, t_{i_2} = 1 \ nm, \epsilon_f = 10, \epsilon_{i_1} = \epsilon_{i_2} = 3.9, N_a = 3 \times 10^{16} cm^{-3}$. Figure 5.10 shows a comparison between P-E graph from the paper and simulated P-E through MATLAB. The color was changed for a better reading of each curve . The other graphs can be found in Appendix B.1. As it can be seen, the two graphs are very similar.

B) "Modeling of metal-ferroelectric-insulator-semiconductors based on Langmuir-Blodgett copolymer films", Reece *et al.* [69]

The authors used Miller's equations to model MFIS structures based on Langmuir-Blodgett copolymer films. Parameters can be found in [69] and are summarized here: $P_s = 10 \ \mu C/cm^2, P_r = 9 \ \mu C/cm^2, E_c = 1250 \ kV/cm, t_f = 20 \ nm, t_i =$
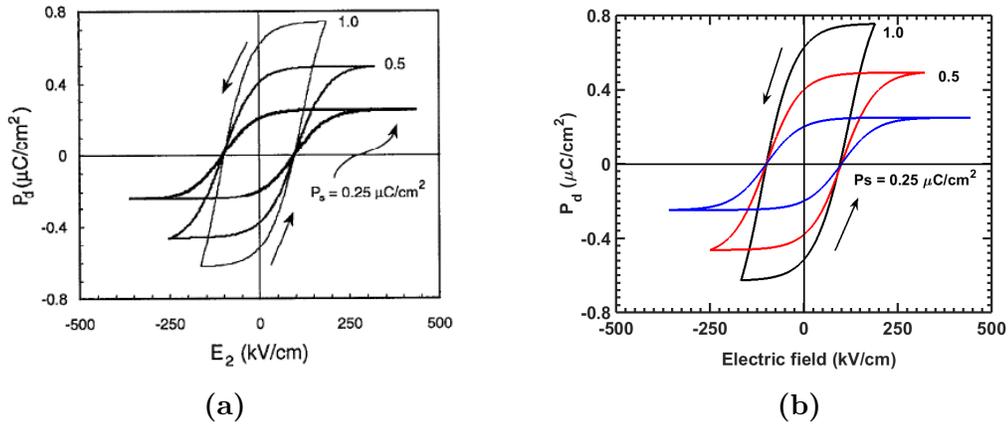
Figure 5.10: (a) P-E$_{FE}$ from Miller's paper [15]. (b) Simulated P-E$_{FE}$.

$10\ nm, \epsilon_f = 10, \epsilon_i = 25, N_a = 10^{16} cm^{-3}$. P-V graphs, from the authors and simulated using MATLAB program can be seen in Figure 5.11. Other graphs can be found in Appendix B.2.
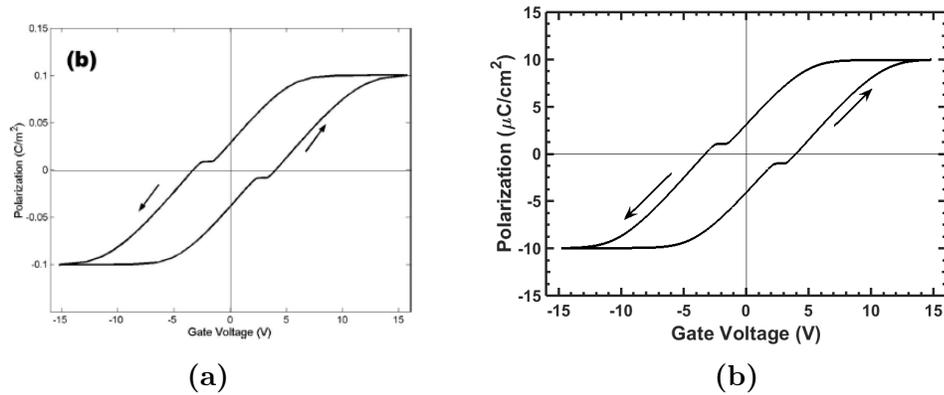
Figure 5.11: (a) P-V from [69] . (b) Simulated P-V using parameters from [69] with hafnium dioxide as the insulator.

5.2.2.2   Lue Model

A) "Device Modeling of Ferroelectric Memory Field-Effect Transistor (FeMFET) ", Lue *et al.* [16]

In the same way as Miller's model, it seems necessary to compare MATLAB program with the original paper. Figure 5.12 shows the P-E graph from the paper and the simulated one using only the Simple Lue model. Parameters are

given on the figure (with $t_f = 200\ nm$).
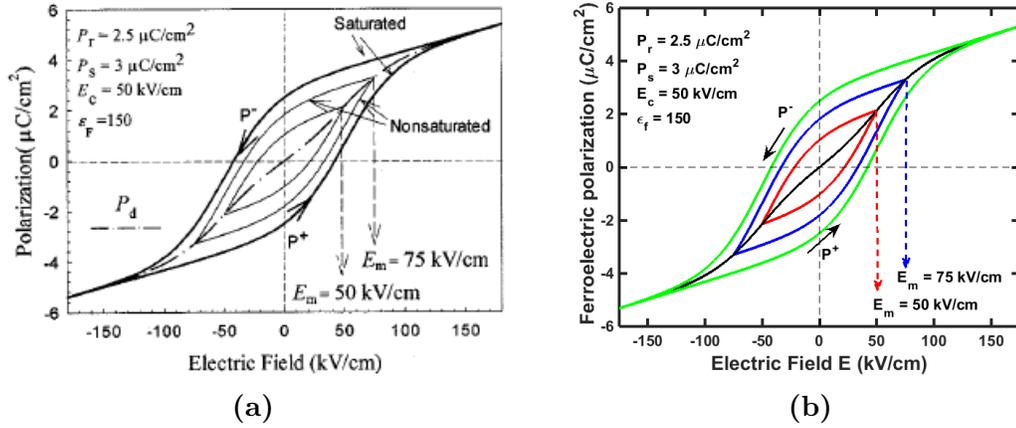
Figure 5.12: (a) P-E from [16] . (b) Simulated P-E using parameters from [16]

C-V graphs of a MFIS capacitor, using the same parameters as previously, are given in Figure 5.13. Additional parameters are: $t_i = 4\ nm, \epsilon_i = 3.9, N_a = 10^{16} cm^{-3}, A = 1\ cm^2$. Once again, both graphs seem identical.
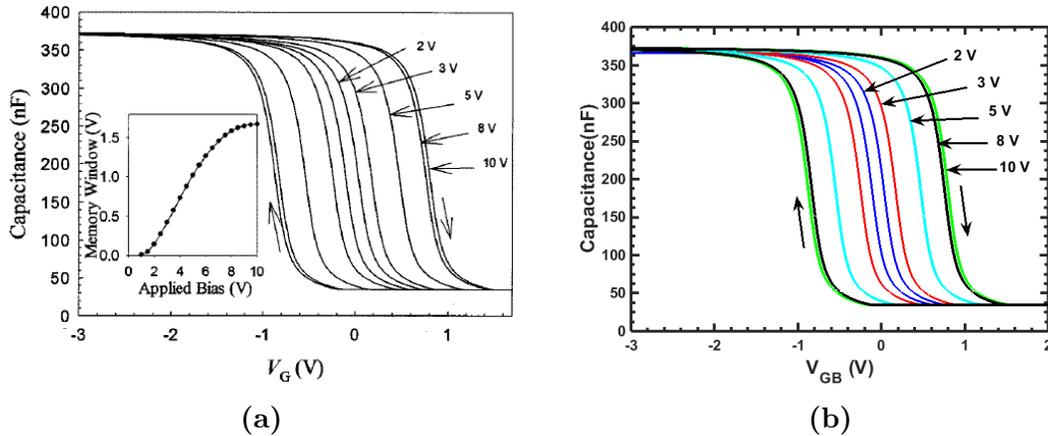
Figure 5.13: (a) P-E from [16] . (b) Simulated P-E using parameters from [16]

B) "Influence of the ferroelectric-electrode interface on the characteristics of MFIS-FETs", Zhang *et al.* [70]

In this paper, the authors proposed a structure using an interface layer between the ferroelectric and the top electrode. The interface layer is changed as a function of the ferroelectric layer: $t_{i_2} = 400\nu\ nm,\ t_f = 400(1-\nu)\ nm,\ t_{i_1} = $

$13\ nm, \epsilon_{i_1} = 22, \epsilon_{i_2} = 42.6, \epsilon_f = 84, P_s = 17\ \mu C/cm^2, P_r = 10\ \mu C/cm^2, E_c = 111\ kV/cm, N_a = 10^{16} cm^{-3}, A = 7 \times 10^{-4} cm^2$. C-V graphs are shown in Figure 5.14 and are comparable.

(a) (b)
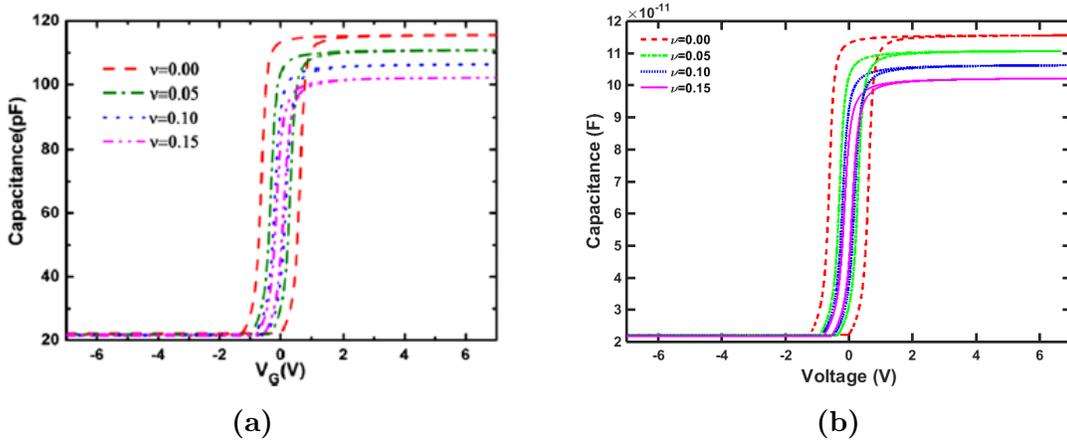
Figure 5.14: (a) C-V from [70] . (b) Simulated C-V

5.2.2.3 Comparison with experimental results

The previous papers were only simulated devices. To validate the model, real data needs to be compared. For this, Mueller *et al.* [71] devices were used. The authors have also done some simulations using Synopsys Sentaurus Device Simulator. Similar parameters were used and resulted in a similar behavior (Figure 5.15).

Finally, some reference capacitors from Radiant Technology were tested using TF 1000 analyzer. These capacitors are made of 255 nm-thick PZT layer. P-V measurements were done with an amplitude of 5 V and a frequency of 1 kHz. Simulations were realized to extract important data such as the remanent and maximum polarizations, coercive field as well as the dielectric constant and compare them with the ones provided by the tool. An overlay of the results can be seen in Figure 5.16. As can be seen in Table 5.1, parameters given by the tool and the simulation are in the same order except for the dielectric constant. The dielectric constant given by the tool is an average and results from capacitance measurement. Thus, it might not
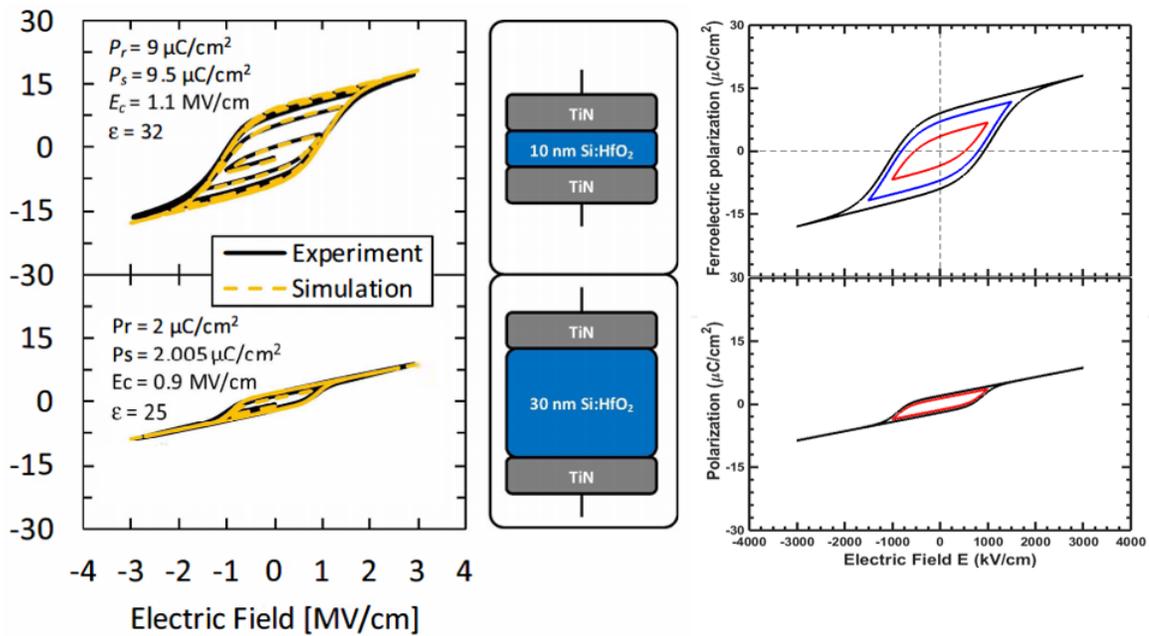
Figure 5.15: Real data simulation using Mueller *et al.* parameters [71].

give an accurate measurement. Other capacitors with a known dielectric constant were tested and it was noticed that the tool was off by a factor of ∼2.5. If the same factor is applied here, it gives a dielectric constant of ∼533, very close to the one obtained by simulation. More experiments with different capacitors need to be done to understand the origin of the error in this factor.
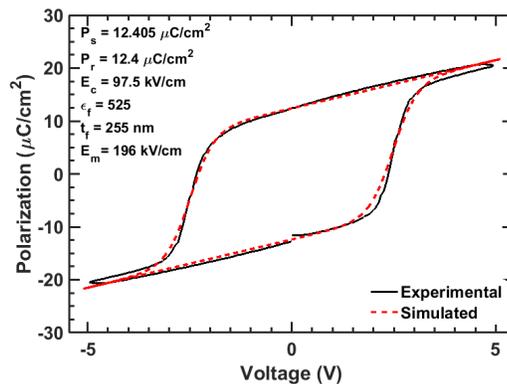
Figure 5.16: P-V graphs of an experimental and simulated PZT capacitor.

Table 5.1: Comparison of PZT parameters between the tool and the one obtained by simulation

	Experimental	Simulated
P_{MAX} (μC/cm^2)	20.5	21.7
P_r (μC/cm^2)	12.5	12.4
E_c (kV/cm)	91.4	97.5
ϵ_r	1333	525

5.3 Discussion

Miller [15] and then Lue [16] developed a model to simulate two and three terminals ferroelectric devices. Their approach uses the switching physics of ferroelectric devices with the physics of MOSFET, based on the charge sheet model. The main difference of these models reside in the expression of the polarization, with Lue's model taking into account the sub-loops, allowing a more accurate simulation.

The MATLAB program developed in this work will be helpful when designing devices. Results using this program were compared with a few published devices and showed a good match between the published and the simulated results.

When comparing results with experimental data, the simulated characteristics were very similar to the one given by the TF 1000. It also showed that the dielectric constant extracted by the tool was off by a factor of $\sim$ 2.5. The charges in the semiconductor, the electric field in the ferroelectric layer and the capacitance of the device can also be derived. Moreover, the influence of thickness and dielectric constant of the ferroelectric or/and insulator layers can be studied for a better understanding on their effect on the P-V loop. Therefore, this tool can be used in one sense, *i.e.* designing a device, but also in the other, *i.e.* getting the film characteristics after testing a device.

C-V graphs of MFM capacitors cannot be simulated at the moment, but equations will be added in a coming update. Finally, the program is limited to two

terminals devices. However, Miller and Lue also described $I_d - V_g$ characteristics for ferroelectric field effect transistor. In Millers model, the calculated drain current is not suitable for a FET operated in saturation and subthreshold regions, assuming that the electric field is independent of the channel position and constant in the ferroelectric film. This assumption is only valid at low drain voltage in the linear region. Lue proposed a more relevant model, including the nonuniform distribution of the field and charge along the channel position, using Pao and Sah's double integral. These equations have not been implemented in this program yet.

Simulation is an integral part of device fabrication. The structure of the device and thickness of ferroelectric films can be simulated to tailor the desired device parameters. This capability is particularly interesting for an academic research lab, such as RIT, where simulation can be used as a teaching tool as well.

Chapter 6

Development of Ferroelectric HfO$_2$ Films

Ferroelectric HfO$_2$ has mainly been deposited using atomic layer deposition [6, 10, 13, 43] and very few papers report the use of physical vapor deposition film [6, 7]. In this study, PVD HfO$_2$ and titanium nitride films have been deposited and studied. To electrically characterize such films, MIM and MIS devices were developed. The process details for the fabrication of capacitors and the development of the films, using aluminum as dopant, will be described in Section 6.1. Section 6.2 will detail the experiments.

6.1 Process development

6.1.1 Substrate

Different substrates were used during this experiment: n-type (2-inch) and p-type (4-inch) silicon wafers and glass slides for process development, 4-inch p-type wafers with resistivity ranging from 1 to 15 Ω.cm and < 0.005 Ω.cm (MIM) for device fabrication. Silicon wafers were initially cleaned using a standard RCA clean to remove organic contaminants (SC-1, 1:1:15 H$_2$O$_2$:NH$_4$OH:H$_2$O at 75 °C for 10 min), native oxide (50:1 H$_2$O:HF for 30 sec) and ionic contaminants (SC-2, 1:1:15 H$_2$O$_2$:HCl:H$_2$O at 75 °C for 10 min).

6.1.2 Films deposition

6.1.2.1 Titanium nitride

As has been discussed previously, the presence of titanium nitride (TiN) seems to enhance the ferroelectricity of hafnium dioxide. TiN is also known to be an excellent conductive barrier to diffusion. Many papers [7, 8, 10, 11] have used TiN as bottom and top electrode for ferroelectric hafnium dioxide capacitor: bottom electrode to prevent diffusion of the metal into silicon and top electrode to help the crystallization of the tetragonal phase of HfO₂.

Titanium nitride was deposited via reactive sputter using CVC 601 DC magnetron sputter tool and a 4-inch titanium target. Once the samples are loaded, the chamber is pumped for several hours to reach a base pressure of ~ 5 μTorr. A presputter was performed to remove any oxides or residue that may have form on the target when loading the samples, since the tool is not a load-lock system. This step was done using an Ar plasma (6 mT, 20 sccm) at 200 W for 300 sec. To not fuse the target to the mount, the maximum power is restrained to 400 W. Various TiN films were sputtered, without a rotating plate, on glass slides at different powers and gas ratio. Results are summarized in Table 6.1.

Table 6.1: TiN deposition study - stationnary plate

Power (W)	Ratio	Ar (mT)	N₂ (mT)	t (Å)	ρ (mΩ.cm)	r (Å/min)
110	**4:1**	**4.8**	**1.2**	**778**	**0.311**	**52**
125	4:1	4.8	1.2	1343	1.15	90
150	4:1	4.8	1.2	1219	1.04	81
175	4:1	4.8	1.2	2545	2.09	170
110	-	6	-	4282	0.0891	285
110	11:1	5.5	0.5	1394	0.637	52
110	3:1	4.5	1.5	946	0.339	63

An Ar/N₂ gas ratio of 4:1 was first chosen, corresponding to a pressure of 4.8 mT and 1.2 mT, respectively and the power was varied. This parameter was

inspired by Kim *et al.* [72]. The power was then fixed at 110 W and the gas ratio was varied. The time and total sputter pressure were kept the same at 900 sec and 6 mT, respectively. Film resistivity was measured using the CDE Resmap and the thickness was determined with a Tencor profilometer.

As can be seen in Table 6.1, at constant gas ratio, the resistivity and deposition rate are the lowest, when the power is 110 W, which justifies the use of 110 W. When the power is kept constant at 110 W, the lowest resistivity is obtained for a gas ratio of 4:1. Low resistivity and deposition rate are primordial for thin conductive layer.

Therefore, during device fabrication, the film was deposited, with a rotary plate, a sputter pressure of 6 mT, a power of 110 W, a deposition time of 1153 sec and an Ar/N$_2$ gas ratio of 4:1 to target a thickness of 10-15 nm. VASE ellipsometer and XRR were used to measure the thickness of the film. Roughness of the film was studied using AFM.
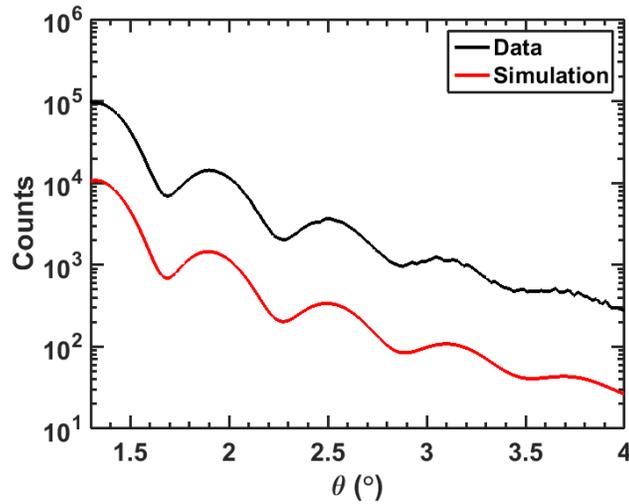
Figure 6.1: XRR TiN comparing real data to simulated data. For a better reading, simulated data curve was offset by a factor 10. Parameters for the simulation: $t_{TiN} = 14$ nm, $\delta_{TiN,Si} = 0.9$ nm, $\delta_{TiN} = 0.1$ nm, $n_{TiN} = 1.58 \times 10^{-5} + i1.02 \times 10^{-6}$ at 8040 eV, $n_{Si} = 7.6 \times 10^{-6} + i1.7 \times 10^{-7}$ at 8040 eV.

VASE ellipsometer measured a thickness of 17 nm, whereas XRR gave a thickness of 14 nm. This thickness was confirmed by simulation (Figure 6.1): minimums

of the fringes have same abscissa on both plots. However, the refractive index might be slightly different between the one chosen in the simulation, from [73] and the one from the sample. This can explained the difference between VASE and XRR results, as well as the fact that VASE calculation used an experimental reference TiN, which is also different from the sample. Finally, AFM measurement gave a roughness of 1.4 nm.

6.1.2.2 Hafnium dioxide

Hafnium dioxide was deposited using the same process tool, CVC 601 DC magnetron sputter tool. The 4-inch Ti target was removed and replaced by a Hf target before loading the samples. Hafnium dioxide was deposited through reactive sputter of argon and oxygen. As only one target is removable in the tool and was already occupied by hafnium, it was decided to use aluminum as dopant, a fixed 8-inch target. Thus, films could be deposited without breaking the vacuum. Loading of the samples and pre-sputter were done similarly to TiN. Design of experiments can be found in Appendix C. From the DOE, the film was deposited for 1028 sec with a power of 100 W, a sputter pressure of 6.8 mT and a gas ratio Ar:O$_2$ of 7:1 to target a thickness of 15 nm. Thickness, measured with VASE ellipsometer and XRR, was 15.5 nm and 14.5 nm, respectively. Roughness of the film was studied using AFM and found to be 1.46 nm. As it can be seen in Figure 6.2, the AFM scan shows the presence of pores in the sample.

Further characterizations, such as temperature of crystallization, were conducted through Time Resolved X-Ray Diffraction (TRXRD) at the National Synchrotron Light Source, Brookhaven National Laboratory and will be presented in the next section.
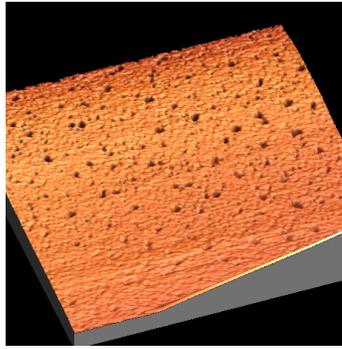
Figure 6.2: AFM HfO$_2$

6.1.2.3   Aluminum

Ferroelectricity was found in Al:HfO$_2$ films with 5 to 10 mol% of aluminum [13]. In case of a 15 nm-thick Al:HfO$_2$ film, 5 mol% of Al corresponds to $\sim$ 3.48 Å of aluminum using parameters of Table 6.2. In order to maximize the uniformity of the films and reproducibility, the deposition rate has to be very low, especially when using an 8-inch target.

Table 6.2: Al and HfO$_2$ information

	Weight $(g.mol^{-1})$	**Density** $(g.cm^{-3})$	**Mole/volume** $(mol.cm^{-3})$
HfO$_2$	210.5	9.68	0.046
Al	27	2.7	0.1

Recipes for depositing aluminum are well established, however for very thin layer, it becomes more challenging. Aluminum was studied and deposited without rotation using an 8-inch target at a sputter pressure of 6 mT under Ar (20 sccm). The time was kept constant to 40 min, in order to get a measurable thickness, with a power of 100 W and 200 W. The power was decreased as much as possible to get a low sputter deposition. Thickness and resistivity were measured using the Tencor P2 profilometer and CDE Resmap, respectively. Results are shown on Table 6.3. The power has a very large influence on the thickness and as 3.5 Å thick films are required, it was decided to use a power of 100 W.

Table 6.3: Aluminum deposition results

Power (W)	Pressure (mT)	t $(\mathring{A})$	$\rho(\mu\Omega.cm)$	r $(\mathring{A}/min)$
100	6	631	10.8	15.77
200	6	1549	6.5	38.73

For top and bottom electrode, 0.6 μm of Al is deposited with evaporation of an Al wire after a base pressure of 2 μTorr is reached.

6.1.2.4   Al:HfO$_2$

Thin ferroelectric layers of HfO$_2$ are generally obtained through ALD. ALD consists of a succession of cycles, alternating HfO$_2$ and Al precursors to deposit the film atom by atom.

Two approaches were investigated to get the ferroelectric film. The first one was to sputter a hafnium oxide stack with several Al layers mixed through its thickness, with an expected total stack thickness of ∼15 nm. The idea was to obtain uniform Al doping throughout the HfO$_2$ layer. HfO$_2$ was sputtered three times for 335 sec each, alternating with Al sputtering for 52 sec each to get 5 mol% of doping (Figure 6.3a).
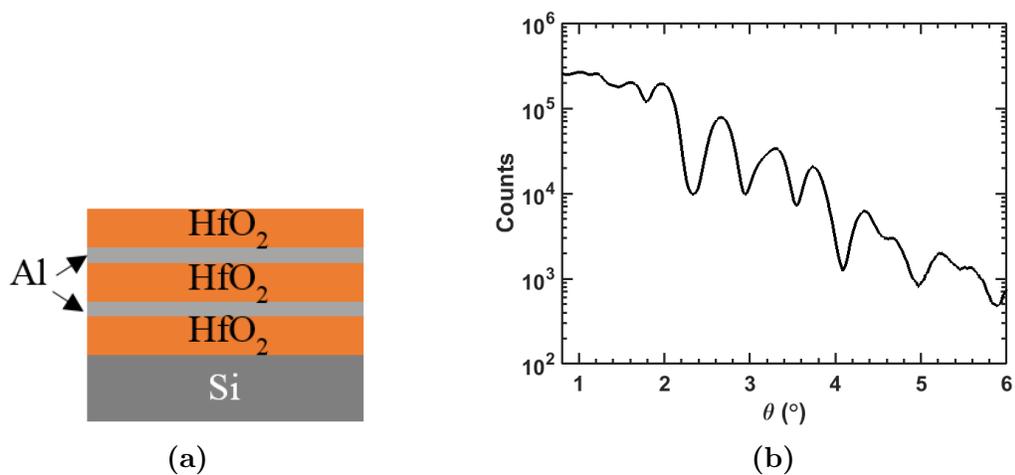
Figure 6.3: (a) 5 mol% of Al in Al:HfO$_2$ stack.(b) XRR of 5 mol% of Al in Al:HfO$_2$ stack.

XRR was used to get the thickness and confirm the presence of interfaces be-

fore annealing. The presence of more than one interface can clearly be seen, as the frequency of the fringes changes and repeats (Figure 6.3b).

The second approach taken was to deposit an Al film on top of HfO$_2$ and attempt to drive in the Al as a solid source dopant. The experiments will be further detailed in Section 6.2.

6.1.2.5   Annealing

Annealing is a crucial part of the fabrication of ferroelectric HfO$_2$ films to get the orthorhombic crystal structure. Annealing was performed with temperatures ranging from 600 °C to 1000 °C and with a duration of 1 sec to 1 hour. For long annealing, a furnace flowing nitrogen was used and for shorter time, less than 60 sec, rapid thermal anneal (RTA) was done. This step was performed before the deposition of the top electrode.

6.1.3   Lithography

To make MIS and MIM devices, a few lithography steps are necessary. TiN and especially HfO$_2$ are not easy to etch and for the development of the ferroelectric film, it was decided to use lift-off resist to avoid etching of these films.

Following a DI H$_2$O rinse and a dehydration bake at 110 °C, resist was spun on the sample using a spin coater. This involves a 500 rpm for 2 sec to spread the resist, followed by a 1 sec ramp up to the resist-specific spin speed, running for 45 sec.

LOR 5A is a lift-off resist, which is not sensitive to light, and therefore requires the presence of an additional light-sensitive resist, such as HPR 504, a positive tone g-line (436 nm) resist used for optical lithography on the GCA g-line stepper. Parameters of the two resists can be found in Table 6.4. TiN, or any other film, can be lifted off in a Remover PG chemistry in an ultrasonic bath. The sample is kept in the solution for 15 min.

Table 6.4: Resist processing parameters

Resist	HPR 504	LOR 5A
Resist Tone	Positive	Lift-off
Spin (rpm)	3000	3000
PAB Temp (°C)	110	140
PAB Time (sec)	60	300
PEB Temp (°C)	-	-
PEB Time (sec)	-	-
Developer	CD-26	Remover PG
Develop time (sec)	60	900

Once the sample is coated, it is loaded onto a paddle. With an exposure of 2.3 sec per die, the run time of the tool depends on the number of dies and can range from a few minutes to 20 min for a 6-inch wafer. No post-exposure bake is required due to the presence of the lift-off resist.

The GCA stepper requires a 5-inch soda lime mask. The mask plate is con-stituted of 4 different levels using the same basic layout but with slight differences. The first two levels are clear and dark field respectively. The last two are similar but bloated by 5 μm. The die is made of capacitors with different shapes and areas, going from 100 μm^2 to 4x10^5 μm^2 (Figure 6.4).
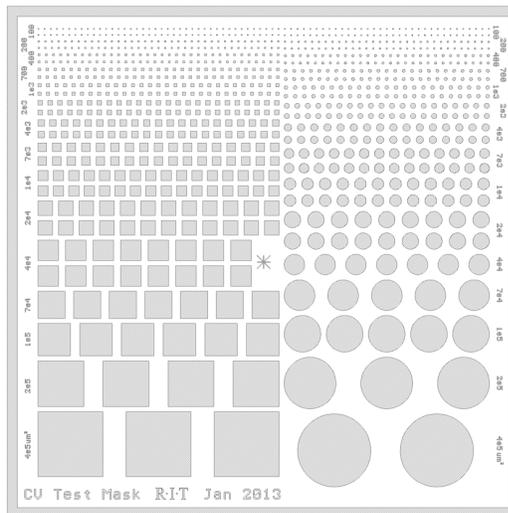
Figure 6.4: Layout of the mask

6.2   Sample description

Different experiments were carried out, starting from the development of sputtered films to the fabrication of complete devices. For a better understanding, samples are named by letters and are summarized in Table 6.5. During device fabrication, monitor wafers were included for characterization of the films. Each sample will be further detailed in this section.

Table 6.5: Summary of experiments

Sample	Purpose	Bot. TiN	Al/HfO$_2$	Top TiN
A	Temp crystal. HfO$_2$	-	0/35 nm	-
B	Temp crystal. Al/HfO$_2$	-	10 nm/35 nm	-
C- MIS	Reference capacitor	-	0/15 nm	15 nm
D- MIM	5mol% Al/HfO$_2$ stack	15 nm	Stack 5 mol%	15 nm
E- MIS	solid source Al dopant	-	5 nm/15 nm	-
F- MIS	solid source Al dopant	15 nm	5 nm/15 nm	-
G- MIS	solid source Al dopant	-	5 nm/15 nm	15 nm
H- MIS	solid source Al dopant	15 nm	5 nm/15 nm	15 nm

6.2.1   Samples A and B

Sample A consists of a 35 nm thick hafnium dioxide film, deposited directly on a silicon substrate, whereas sample B has a 10 nm thick Al on top of HfO$_2$. The samples were sent to the National Synchrotron Light Source, Brookhaven National Laboratory, where Time Resolved X-Ray Diffraction (TRXRD) were conducted to study the impact of aluminum on the crystal structure and temperature of crystallization of HfO$_2$.

6.2.2   Sample C

This sample was prepared to get a reference capacitor with undoped HfO$_2$. 35 nm of HfO$_2$ was deposited on top of two silicon wafers, followed by 15 nm of TiN

through a shadow mask. Each wafer was then rapid thermal annealed at 1000 °C and 850 °C for 20 sec each. 600 nm of aluminum was then evaporated on top of it through a shadow mask. The front of the wafer was then protected with photoresist and immersed into BOE 5.2:1 to remove the native oxide on the backside of the wafer. After a rinse and dry step, the wafers were loaded in the evaporator and Al was evaporated on the backside. The schematic of device is shown in Figure 6.5.

A shadow mask was chosen to shorten the fabrication, however it was abandoned after this run due to the difficulty in aligning the mask to the wafer a second time after RTA.
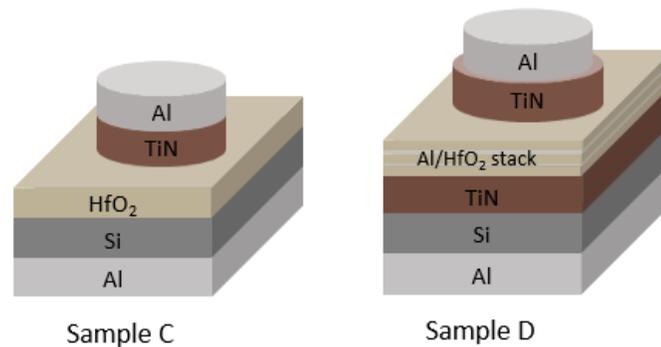
Figure 6.5: Schematic of samples C and D

6.2.3   Sample D

On this sample, the approach of a multi-layers stack was attempted. 15 nm of bottom TiN was sputtered on a cleaned highly doped wafer, followed by a 5 mol% Al/HfO₂ stack without breaking the vacuum. The first lithography step was done using HPR 504, LOR 5A and the bloated dark field level on the mask, followed by a deposition 15 nm of TiN. The layer was then lifted-off. After breaking the wafer, RTA was performed at 1000 °C for 1 sec on one half and at 800 °C for 20 sec for the second half. After another lithography using the non-bloated dark field level, aluminum was evaporated as top electrode. The bottom electrode was done the same way as for sample C. The final device can be seen in Figure 6.5.

6.2.4 Samples E,F,G and H

These samples were prepared using the solid source approach and were processed simultaneously on 5-15 Ω.cm substrate. 15 nm of TiN was first sputtered on samples F and H. Wafers E and G were then loaded into the chamber and 15 nm of HfO$_2$ was deposited. 5 nm of aluminum was finally evaporated. An attempt was also made using the sputter system without breaking the vacuum. However, during the development of the exposed resist, the Al layer was developed away, which could indicate a porous film. This may be because of the low power used to sputter Al. Without sufficient energy to coalesce, the atoms might just have simply hit the wafer and adsorbed, leading to a low quality film. Evaporated Al, on the other hand, has more thermal energy and the atoms can form a dense film. After the first lithography, 15 nm of TiN was sputtered on samples G and H and then lifted-off. Different methods and temperatures of annealing were tried on each sample: 1 h at 600 °C in a nitrogen furnace, 20 sec at 850 °C in RTA and 1 sec at 1000 °C in RTA. The rest of the process is similar to sample D and the final devices schematic can be seen in Figure 6.6 .

Electrical results were measured before and after sintering for samples C to H. Results will be discussed in the next section.
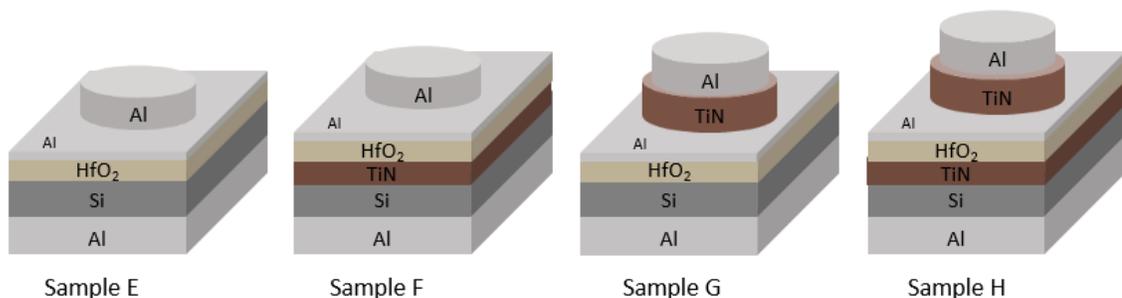
Figure 6.6: Schematic of samples E,F,G and H

6.3 Experimental results

6.3.1 Samples A and B

Time Resolved X-Ray Diffraction (TRXRD) was performed using cobalt wavelength (1.797 Å) at the National Synchrotron Light Source, Brookhaven National Laboratory. The measurements were taken by in-situ annealing with a ramp of 3 °C/s to 800 °C, except indicated otherwise.

The as-sputtered HfO$_2$ is amorphous and crystallization happens at 600 °C. Two distinct peaks can be seen on Figure 6.7 at 0.347 Å^{-1} and 0.399 Å^{-1}, which would indicate the presence of a cubic phase (Fm3m) with a unit cell of 5 Å (calculations using CrystalDiffract software from PDF4 data). Although it seems unlikely to get a cubic phase at such low temperature, studies on surface energies showed that the formation of cubic HfO$_2$ greatly depends on the ratio of Hf:O [74, 75]. Oxygen vacancies can lead to the lowering of the temperature of crystallization of cubic HfO$_2$.
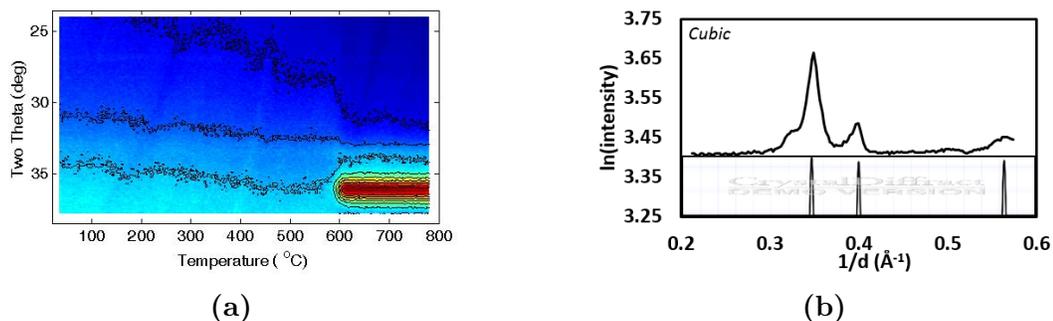
Figure 6.7: (a) 2θ vs temperature curves of sample A. (b) Experimental and fitted XRD

For sample B, the XRD scan before annealing confirms the presence of an amorphous layer (HfO$_2$) and a small aluminum (111) peak. After annealing, crystallization happens at lower temperature (552 °C) (Figure 6.8). A second phase appears at 621 °C (Figure 6.9). The first phase seems to be a monoclinic structure (P2$_{1/c}$) of HfO$_2$ (Figure 6.8). At higher temperature, it seems that Al and O$_2$ react to create Al$_2$O$_3$ (primitive cubic) (Figure 6.9).
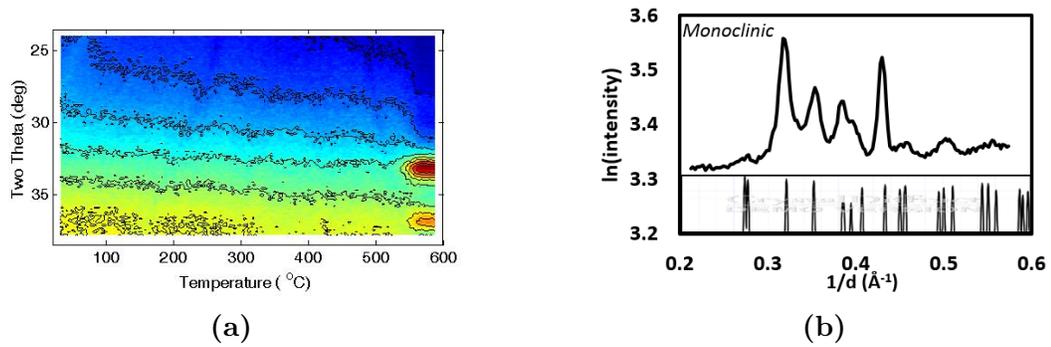
Figure 6.8: (a) 2θ vs temperature measurements of sample B at 600 °C. (b) Experimental and simulated XRD of sample B .
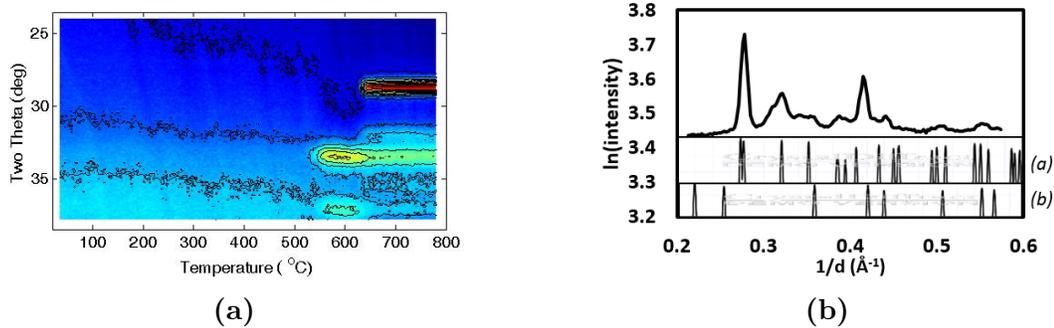
Figure 6.9: (a) 2θ vs temperature curves of sample B at 800 °C. (b) Experimental and simulated XRD of sample B with: (a) Monoclinic HfO$_2$, (b) Cubic Al$_2$O$_3$.

No orthorhombic phase was obtained from these characterizations. No further TRXRD was realized after these samples, as the beam line closed shortly after.

6.3.2 Sample C

C-V measurements were realized at a frequency of 1 MHz and an amplitude of 50 mV. Capacitors with an area of 0.004 cm^2 were tested and results are shown in Figure 6.10.

These wafers show C-V curves without hysteresis, with some non-uniformity for the second wafer. The dielectric constant can be calculated using:

$$C_{ox} = \frac{\epsilon_r \epsilon_0 A}{t_{ox}} \Rightarrow \epsilon_r = \frac{t_{ox} C_{ox}}{\epsilon_0 A} \tag{6.1}$$
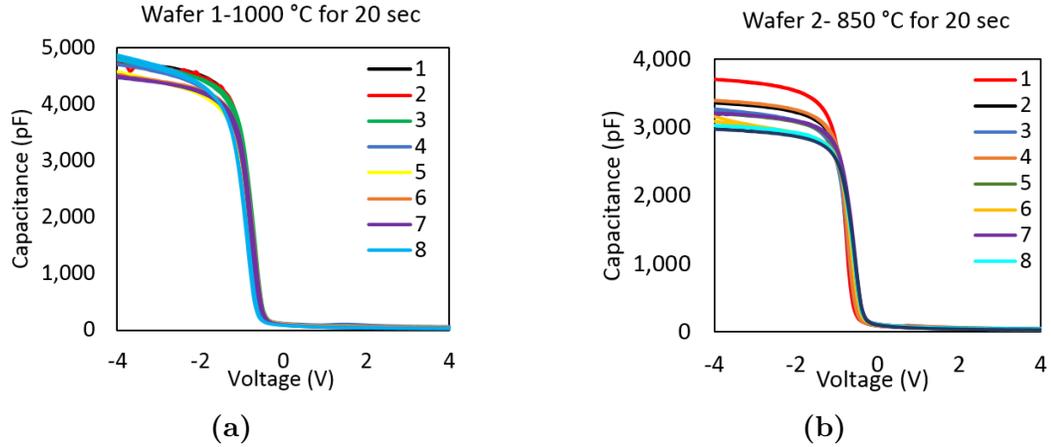
Figure 6.10: (a) C-V characteristics for wafer 1 , (b) C-V characteristics for wafer 2.

where t_{ox} is the oxide thickness, C_{ox} is the oxide capacitance, ϵ_0 is the vacuum permittivity and A is the area of the capacitor.

Calculations give $\epsilon_r(wafer1) = 16.7 \pm 0.65$ and $\epsilon_r(wafer2) = 14.37 \pm 0.93$ with a thickness of 12.9 nm for wafer 1 and 15.5 nm for wafer 2 (XRR).

Dielectric constants of monoclinic, tetragonal and cubic HfO$_2$ have been experimentally found to be 16, 70 and 29 respectively [38]. Thus, these results might indicate the presence of a monoclinic phase for both of these wafers.

P-V measurements were also done. Figure 6.11 shows a typical P-V plot obtained with wafer 1, showing leakage. Pure HfO$_2$ should have a linear behavior.
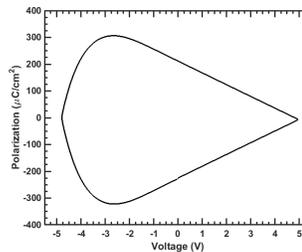
Figure 6.11: P-V measurement for wafer 1

6.3.3 Sample D

Unfortunately for sample D physical film failure was observed under the microscope after annealing. An example is shown in Figure 6.12 after RTA at 600 °C, where the buckling up of the film can be seen. The process was continued and C-V measurements showed the presence of leakage.
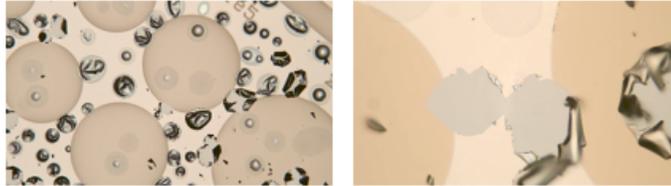
Figure 6.12: High stress observed after RTA at 600 °C .

After these results, an experiment was designed to see if this failure was the result of the presence of TiN layers or if it was the result of the combination of the multistack Al and TiN. TiN/HfO$_2$/TiN layers were deposited on a substrate and annealed at the same temperature. No crack was observed. It is believed that the multi-layered approach taken is the culprit. The presence of multi-films in the stack, and especially aluminum, provides additional stress, whereas the many interfaces provide additional points for failure.

6.3.4 Samples E, F, G and H

Among these samples, samples G and H show promising results, when annealing at 600 °C for an hour. Hysteresis can be seen during C-V measurements. C-V curves don't seem to be dependent on sweep speeds, which would indicate that this is due to ferroelectricity rather than mobile charges (Figures 6.13). In this case, the memory window would be $\sim$ 0.1 V for sample G and $\sim$ 0.25 V for sample H.

These devices were tested using the TF 1000 analyzer. Unfortunately, the depletion capacitance of the MIS structure masked any potential ferroelectric effects.
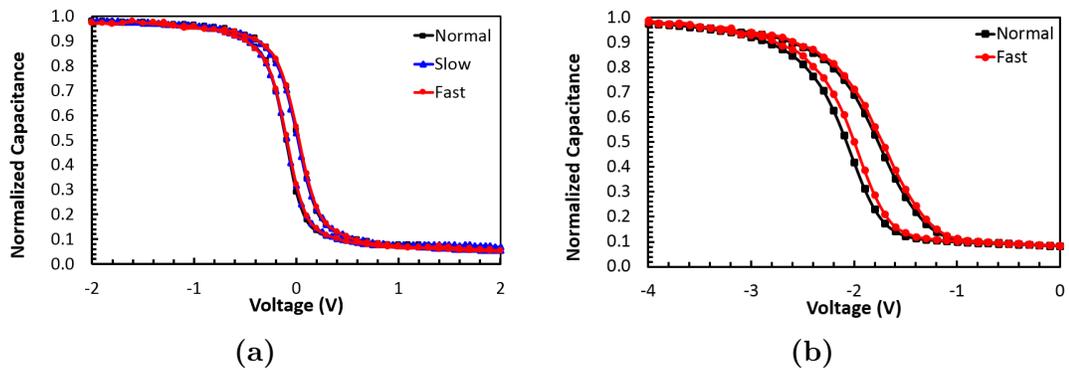
Figure 6.13: (a) C-V of sample G and (b) of sample H annealed at 600 °C for an hour.

MIM capacitors were therefore fabricated using the same process flow on a degenerately doped substrate. However, these samples yielded unmeasurable hysteresis by C-V or P-V measurements. These films have repeatability issues. Further efforts were devoted to developing ferroelectric films using ALD process.

6.4   Discussion

As-deposited HfO$_2$ was confirmed to be amorphous with TRXRD. Crystallization of the film in a cubic phase was observed at 600 °C, probably due to oxygen vacancies, which lower the temperature of crystallization of the cubic structure. The addition of aluminum on top of HfO$_2$ seems to decrease the temperature of crystallization and change the structure to a monoclinic phase. The TRXRD results suggest that the incorporation of aluminum in hafnium dioxide modifies the temperature of crystallization and also the crystal structure. However, it does not seem to give the expected orthorhombic phase with just a layer of aluminum.

Different attempts have been made to create PVD ferroelectric HfO$_2$ using aluminum as dopant. Two different approaches were studied: multi-stack and solid-source dopant. Physical breakdown appeared when the multi-stack approach was attempted. This might be due to a high stress present in this structure. The presence of multi-film layers in the stack, and especially aluminum, provides additional

stress. The thermal coefficient of expansion of aluminum ($22.2 \times 10^{-6} m/(mK)$) [76] is almost twice of the monoclinic HfO$_2$ ($\sim 13 \times 10^{-6} m/(mK)$) [77]. Therefore, during the annealing, aluminum will expand more than hafnium dioxide, resulting in stress if the aluminum is thick. The multi-stack approach needs to be further studied with a smaller target size and a larger gap between the target and the sample to obtain a better film quality.

Finally, solid-source dopant showed some promising results with some C-V hysteresis behavior. However, P-V measurements could not confirm such behavior and the process does not seem to give repeatable results.

To summarize, experiments have been conducted to develop a PVD Al:HfO$_2$ ferroelectric film, however, it seems that a good quality film is necessary to get ferroelectricity. Discussions with NaMLab confirmed that the oxygen content in HfO$_2$ is very critical, as well as the temperature of deposition.

A better approach for PVD would be to deposit the film by co-sputtering using hafnium dioxide and aluminum targets (no reactive sputter). Using a composite target with the right amount of Al and HfO$_2$ could also be an interesting approach.

Chapter 7

Study of Ferroelectric Si:HfO$_2$ MIM capacitors

Since the composition control using co-sputtering was not achievable within the existing RIT capabilities, ferroelectricity in HfO$_2$ was still studied thanks to NaMLab. They provided reference capacitors and deposited ferroelectric films by ALD with different thicknesses. These films, annealed at various temperatures were characterized and results will be detailed in this chapter. Finally, ferroelectric tunnel junction using 6.4 nm thick Si:HfO$_2$ was fabricated and will be discussed at the end of this chapter.

7.1 Samples description

7.1.1 Reference capacitors

Reference capacitors were made at Fraunhofer CNT, Dresden in collaboration with NaMLab. A schematic cross-section of the device can be seen in Figure 7.1. These capacitors were fabricated on highly doped ($< 0.005\Omega.cm$) silicon substrate. 10 nm of TiN was deposited, followed by 9.6 nm of ALD Si:HfO$_2$ with two different compositions to get the ferroelectric and anti-ferroelectric properties. The ferroelectric layer was deposited at 300°C using HfCl$_4$/H$_2$O and SiCl$_4$/H$_2$O precursors. 10 nm of TiN was then grown at 450°C as a capping layer. The samples were spike annealed at 650°C. Ti, as an adhesion layer, followed by 50 nm of Pt was then evaporated through a shadow mask. TiN was then removed by wet etch (mixture of ammonia

Figure 7.1: Reference capacitor

and hydrogen peroxide at 50 °C for 5 min), while Pt served as a hard mask. Finally, 10 nm of TiN was deposited on the backside of the substrate as bottom contact.

7.1.2 MIM capacitors

Highly doped 6-inch wafers were cleaned using a RCA clean. 10 nm of TiN was then sputtered on the samples. The wafers were sent to NaMLab, where ALD Si:HfO$_2$ was deposited with different thicknesses by Claudia Richter using HfCl$_4$/H$_2$O and SiCl$_4$/H$_2$O precursors. Thicknesses were measured after deposition by XRR. 12 nm of TiN was then deposited in a batch furnace using a pulsed chemical vapor deposition process at 450 °C using TiCl$_4$ and NH$_3$ as precursors and N$_2$ as purge gas. Some of the samples were then annealed in NaMLab at 1000 °C for 1 sec. Others received an annealing treatment at RIT. The samples are described in Table 7.1. 400 nm of aluminum was deposited on top of TiN at RIT, followed by a lithography step to form the capacitors. Aluminum and then TiN was dry etched using LAM 4600. Aluminum was etched for 150 sec, with a power of 125 W, a pressure of 100 mT and a mixture of nitrogen (N$_2$, 20 sccm), boron tricholoride (BCl$_3$, 25 sccm), chlorine (Cl$_2$,30 sccm) and chloroform (CFORM,8 sccm). TiN was etched for 2 min with a power of 100 W, a pressure of 300 mT and a mixture of N$_2$ (25 sccm), Cl$_2$ (36 sccm), Ar (84 sccm) and CFORM (15 sccm). The photoresist was then removed and 400 nm of aluminum was evaporated on the backside after a short etch in BOE 5.2:1.

Samples A, B, C and D1 have been annealed at NaMLab and the objective is

Table 7.1: Description of the samples

Sample	Super-cycle	Thickness (nm)	Annealing
A	1	6.4	1 sec/ 1000°C
B	2	9.3	1 sec/ 1000°C
C	3	13.1	1 sec/ 1000°C
D1	6	22.9	1 sec/ 1000°C
D2	6	23.6	-
D3	6	23.6	20 sec/ 650°C
D4	6	23.6	20 sec/ 800°C
D5	6	23.6	120 sec/ 1000°C

to investigate the influence, if any, of thickness on the polarization and endurance. Samples D2 to D5 have been annealed in-house to study the influence of temperature on the polarization and endurance. Sample A was used for FTJ devices and will be detailed at the end of the chapter.

7.2 Experimental results

7.2.1 Ferroelectricity versus antiferroelectricity

The antiferroelectric reference sample was sent for EELS and TEM analysis at Micron. As can be seen in Figure 7.2a, the layers are crystallized, grains can clearly be seen for TiN and Pt. It is less clear for HfO$_2$, but it seems to have partially crystallized. The layers are very uniform and thicknesses are close to the one targeted. EELS confirms the presence of different elements except for the hafnium dioxide doped with silicon. The amount of silicon seems to be too small to be detected by EELS.

P-V measurements were performed at a frequency of 1 kHz and an applied voltage of 3 V, to get an electric field of 3 MV/cm. A hysteresis shape can clearly be seen in Figure 7.3a, typical from a ferroelectric sample. A butterfly curve resulted from the P-V measurement of the antiferroelectric sample (Figure 7.3b). A remanent polarization of 10.3 μC/cm^2, a maximum polarization of 23.7 μC/cm^2 and a coercive voltage
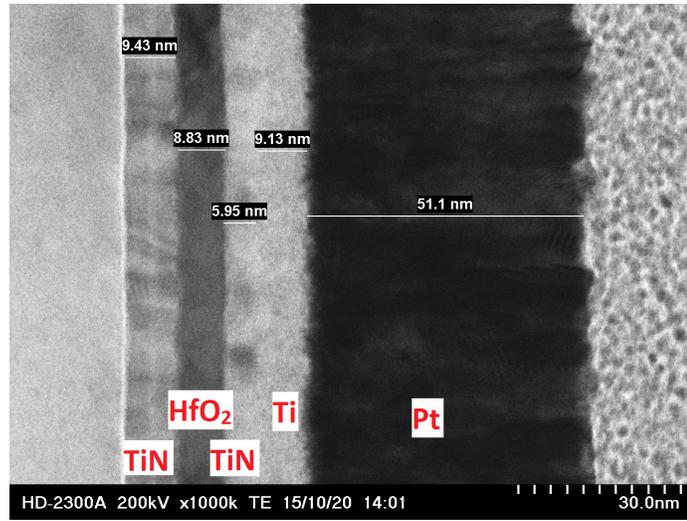
(a)
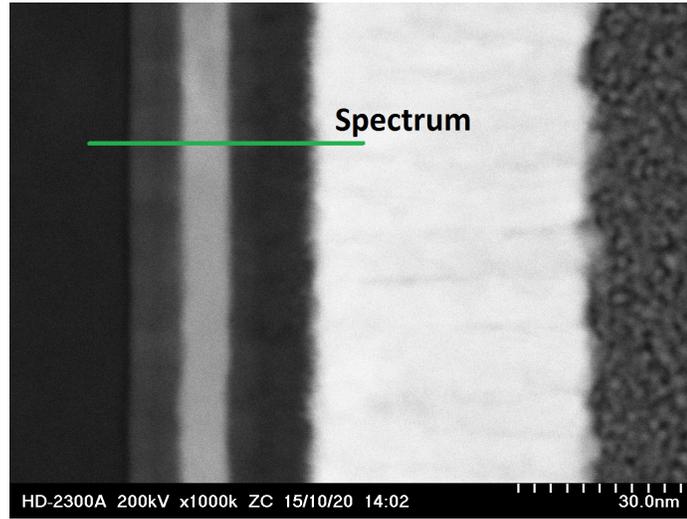
(b)
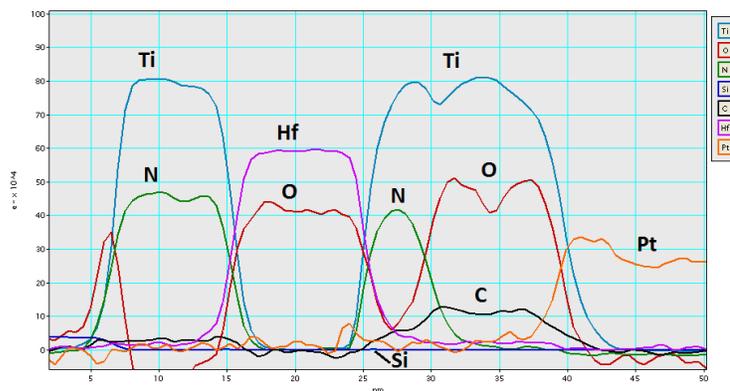
(c)

Figure 7.2: (a) TEM cross-section , (b) Z-Contrast cross section, (c) EELS analysis

of 1.01 V, corresponding to 1.01 MV/cm were extracted from the measurement.
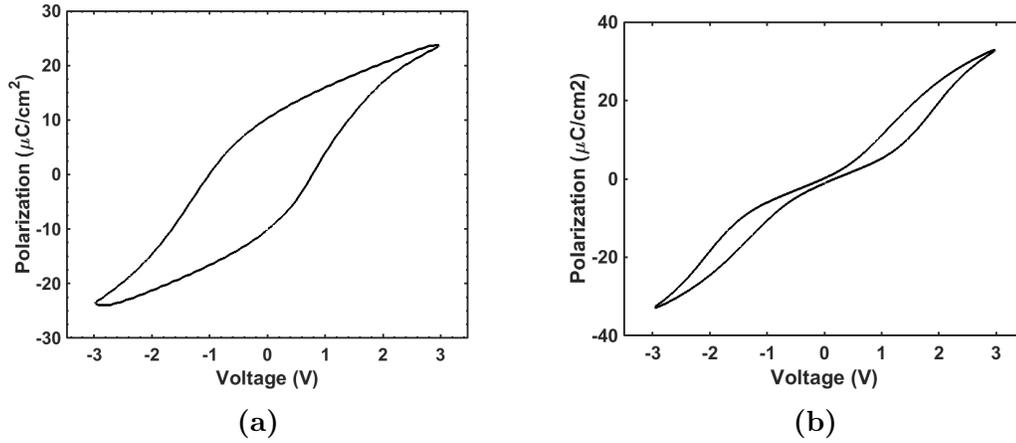
Figure 7.3: (a) Ferroelectric P-V , (b) Antiferroelectric P-V

Using the MATLAB based program, simulations were performed to match experimental data, results are shown in Figure 7.4. The two curves show good match, except for the positive branch, which has a smaller coercive field, as the hysteresis is not perfectly symmetrical.
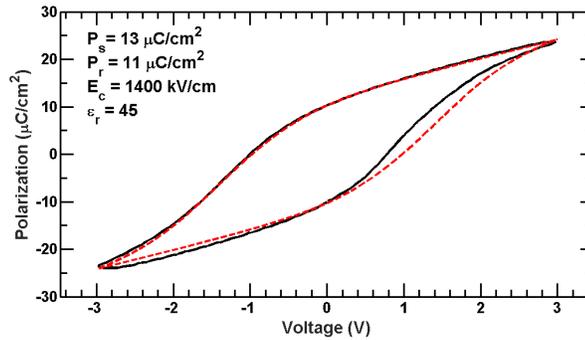
Figure 7.4: (black): experimental P-V hysteresis loop, (red, dash): simulated P-V using P_s=13$\mu C/cm^2$, P_r=11$\mu C/cm^2$, P_{MAX}=24$\mu C/cm^2$, E_c= 1.4 MV/cm and a dielectric constant of 45.

7.2.2 Material characterization of 22.9 nm Si:HfO$_2$

Sample D1 was analyzed using XPS to measure the amount of dopant in the film after annealing. After chemically removing the top TiN, the sample was first analyzed without etching. As it can be seen in Figure 7.5, a small amount of silicon

was detected: 4.2 mol% $\pm 2\%$. These percentages were calculated using tabulated values of sensitivity factors and not from direct determination on this instrument. A small peak of carbon is also present, which was expected as samples are generally contaminated by surface carbon.
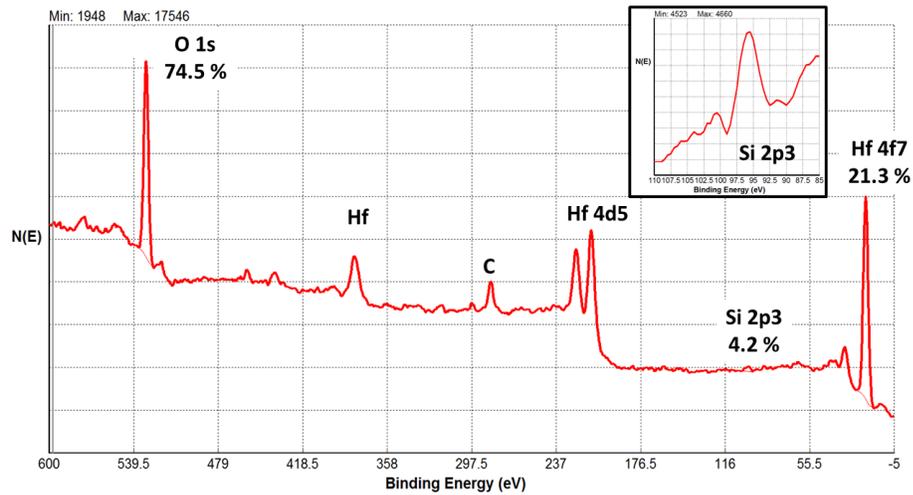
Figure 7.5: XPS scan of sample D1 without etching.

After etching for 5 min, measurements show the disappearance of carbon and silicon peaks. The amount of silicon might be negligible in the ferroelectric layer and does not appear on the graph (Figure 7.6).
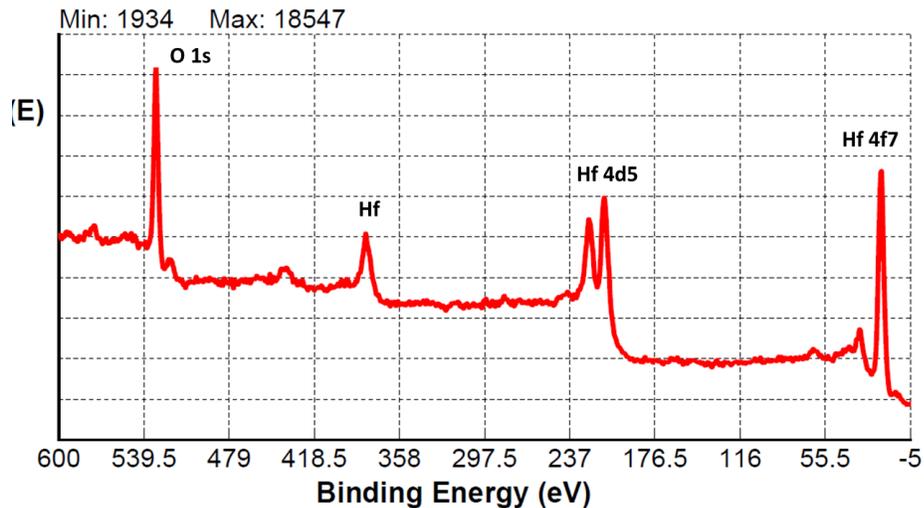
Figure 7.6: XPS scan of sample D1 after etching for 5 min.

Finally, after etching for a longer time to reach to the bottom titanium nitride, Auger measurement was performed, as it is a faster technique (Figure 7.7). At the interface between HfO$_2$ and TiN, results show the presence of Si, HfO$_2$ and TiN. It seems that, after annealing, there is a negligible amount of silicon in the hafnium dioxide layer. However, a certain amount of Si is found above and below it. After further etching in TiN, the signal of TiN increases as well as Si and C. The increase of the silicon peak can result from the substrate, whereas the carbon might come from contamination during sputtering.
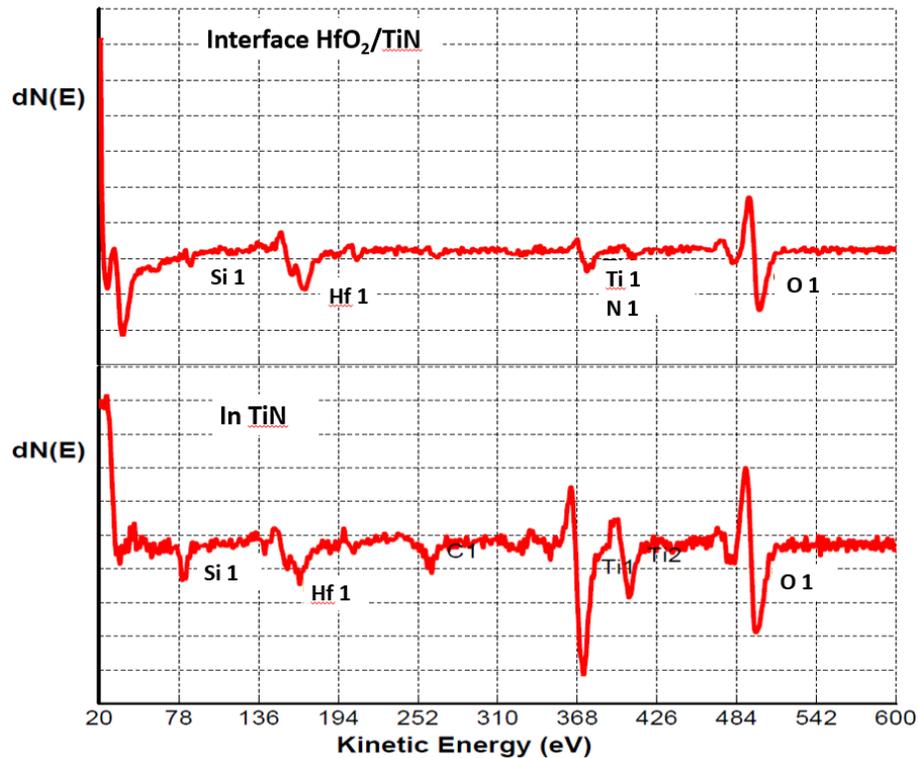
Figure 7.7: Auger scan of sample D1 at the interface HfO$_2$/TiN and in the bottom TiN layer.

XRD measurements confirmed the presence of monoclinic (m) and orthorhombic (o) phases in the sample (Figure 7.8). Calculations using the ratio of the highest intensity peak (orthorhombic) and the one on the left of it (monoclinic), give a m/o ratio of 37/63.
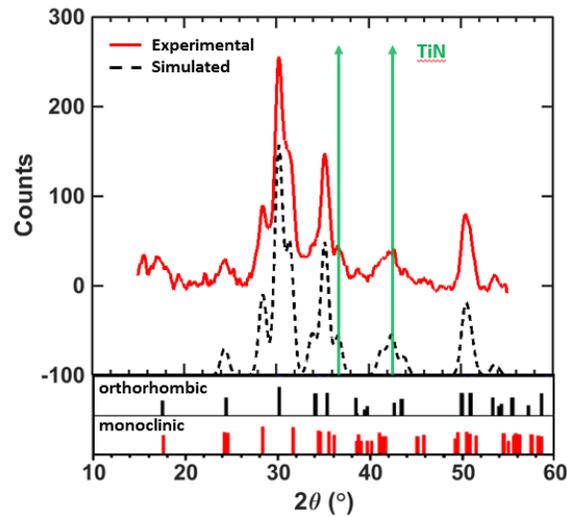
Figure 7.8: XRD of sample D1.

7.2.3 Influence of film thickness

In thin dielectric films, properties can be altered by the thickness. The stabilization of the crystal structure of thin hafnia, that would be metastable in bulk, is thermodynamic in nature [78]. Indeed, the contribution from the surface energy in thin films becomes comparable to the volume energy, modifying the physical properties of the film. It is believed to be due to a high surface-to-volume ratio of each individual grain. Moreover, for thin layers, the tunneling current will become a limiting factor for polarization switching.

P-V measurements were performed on samples A, B, C and D1, all annealed at the same temperature. As it can be seen in Figure 7.9, sample A (6.4 nm) is leaky. The device will be studied further in this chapter and therefore will not be included in this discussion. Polarization hysteresis loops were observed for samples B, C and D1. Moreover the displacement current response exhibit two peaks, associated with domain switching at the coercive voltages.

The hysteresis are not perfectly symmetrical. This can be due to electrodes with different work functions, giving rise to a potential that drops over the film, resulting in a displacement of the P-E curve. Also a broad distribution of switching fields
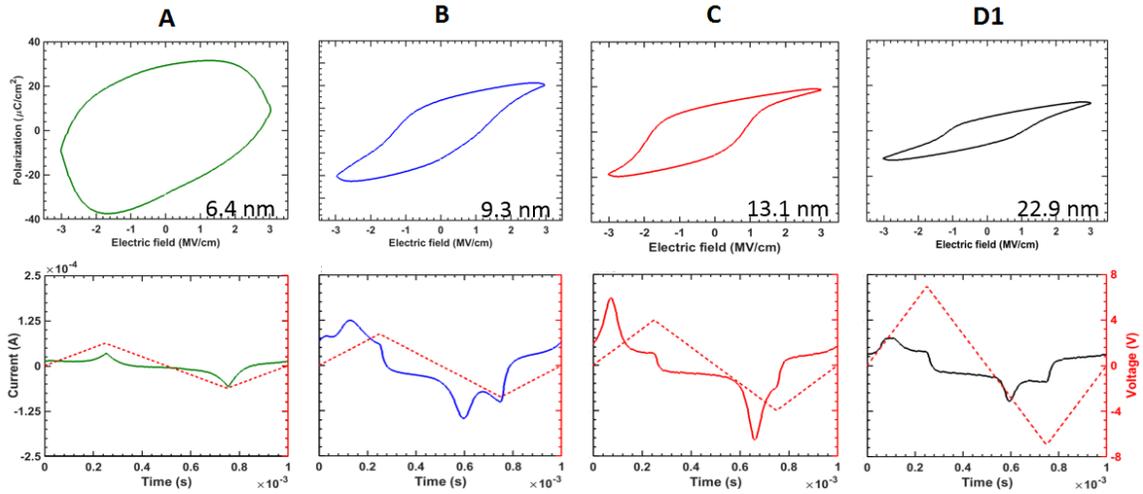
Figure 7.9: P-V and I-T curves of devices with various thicknesses and same area (7e4 cm^2)

compared to E$_c$ results in a strongly rounded hysteresis [79] .

The remanent polarization seems to decrease with the thickness. This is highlighted in Figure 7.10: from 12.3 μC/cm^2 for 9.3 nm film to 5 μC/cm^2 for 22.9 nm film. The coercive field seems to be maximum for the 13.1 nm film. Studies show that thicker films of HfO$_2$ have an increased stability of the monoclinic phase, which therefore inhibits the formation of orthorhombic phase [14]. This was confirmed with the XRD, showing a m/o ratio of 37/63. This is linked to a reduction of the influence of the surface energy, as the film becomes thicker [78]. This could also be the result of a lack of mechanical stress during the annealing step. A stronger mechanical confinement might enhance the ferroelectric properties of thick Si:HfO$_2$ films: it seems that TiN and the amount of Si doping do not induce a sufficient stress to create the orthorhombic phase. This results in a low remanent polarization.

C-V measurements were simultaneously taken and are shown in Figure 7.11 for samples B, C and D1. Dielectric constant versus electric field were extracted and plotted for a better comparison. C-V curves exhibited a butterfly-like shape confirming the presence of true ferroelectric behavior. Ideally, the maximum dielectric constant should coincide with the coercive field in both directions. However, no pre-
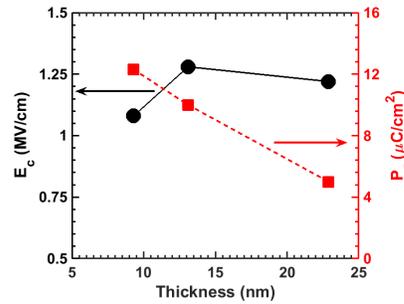
Figure 7.10: Influence of the film thickness on the remanent polarization (P_r) and the coercive field (E_c))

pulse was applied before C-V measurements, which could result in this non-ideality. At zero volts, the polarization is unknown. When the voltage is increased, the domains start to realign but the maximum number of domains switching at the same time does not match with the coercive voltage. Once the maximum voltage is reached, most of the domains, if not all, have switched in one direction. When the voltage is decreased, the domains switch in the other direction and that time, the maximum of the curve is at the coercive field. This explains why there is a gap at 0 V: the remanent polarization is different after a negative voltage. Also, the dielectric constant decreases when the thickness increases, which would suggest the presence of the monoclinic phase, increasing with the thickness.
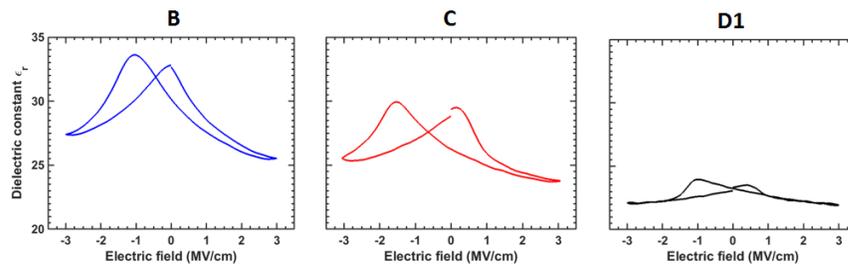
Figure 7.11: Dielectric constant versus electric field extracted from C-V measurements.

7.2.4 Influence of annealing temperature

The influence of the annealing temperature was studied on the 23.6 nm sample in order to see if the ferroelectric characteristics could be thermally enhanced. The

films were studied without annealing (D2) and with 650°C for 20 sec (D3), 800°C for 20 sec (D4) and 1000°C for 120 sec (D5) anneal. As TiN was deposited at 450 °C for a few hours, it is interesting to know if the sample crystallized during the TiN deposition. In Figure 7.12, the sample without annealing shows a linear behavior. This is confirmed by C-V and P-V measurements. It seems that the mechanical confinement without an annealing step was insufficient to form the orthorhombic phase, as it is confirmed with a dielectric constant of 19. The samples annealed at lower temperatures, 650°C and 800°C, show an antiferroelectric behavior. This is confirmed by the double-butterfly shapes obtained from C-V measurements.
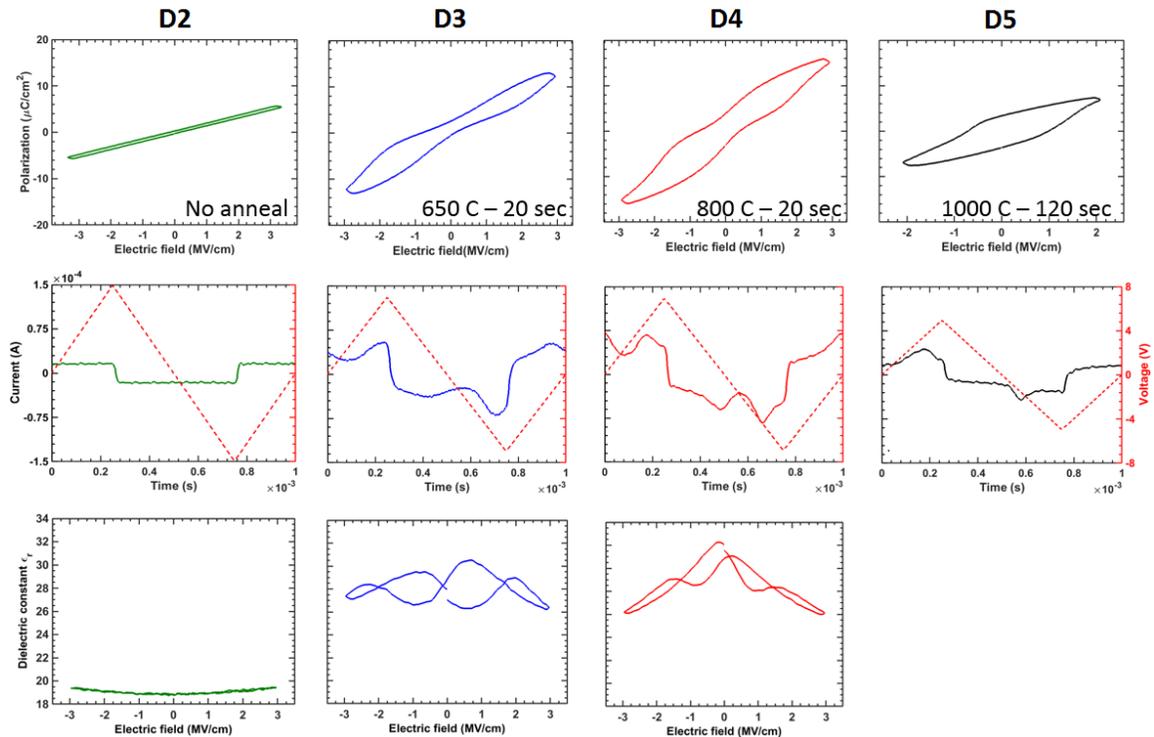
Figure 7.12: P-V, I-T and ϵ_r-E curves of 23.6 nm devices with various temperature of annealing and same area (7e4 cm^2)

However, it does not necessary indicate that it is an antiferroelectric film. Similar behaviors have been reported on ferroelectric materials and several origins have been proposed to explain this pinched antiferroelectric-like hysteresis: space charge accumulation at the grain boundaries, alignment of defect dipoles along the existing

polarization directions and pinning of domain walls by defects due to electric and elastic interactions [23, 14, 80]. This kind of hysteresis appears when multiple domains with antiparallel polarization directions are stabilized. Fortunately, a field cycling, called wake up behavior, allows to recover from such behavior. Finally, sample D5 shows a very small hysteresis loop. C-V measurement could not be performed, as the tool recognized it as a leaky device. The biased voltage was decreased for the last sample as breakdown was occurring for smaller field. This might be due to the exposure of the wafer to a high temperature for a relatively long period, which can degrade the film.

A small cycling, usually 10^3, is known to enhance the ferroelectric characteristics by rearranging defects and charges in the material [14]. Cycling was performed using triangular pulses of alternating polarity with amplitude of 7 V (5 V for sample D5) and frequency of 1 kHz. Figure 7.13 shows the P-V, ϵ_r-E behavior and corresponding transient current characteristics of the previous samples after cycling.
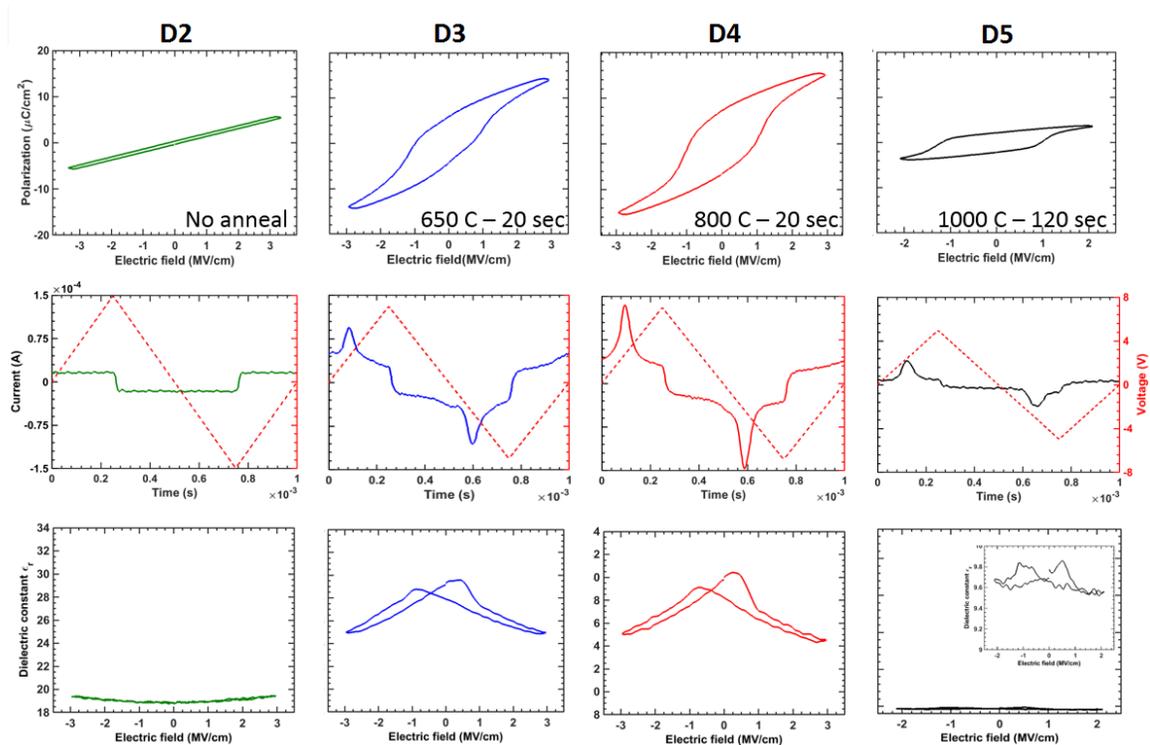
Figure 7.13: P-V, I-T and ϵ_r-E curves of 23.6 nm devices after 10^5 cycles

In this case, 10^5 cycles were needed to obtain a complete ferroelectric behavior. The antiferroelectric-like hysteresis recovered after cycling and showed stable ferroelectric behavior, especially for the sample annealed at 800°C. Sample D5 was also measurable using the C-V instrument after cycling.

The annealing temperature seems to enhance the ferroelectric characteristics when annealed at 800°C for 20 sec. At 650°C, the remanent polarization is a little larger (5.75 μC/cm^2) than the one previously extracted, as it is highlighted in Figure 7.14. However, when it is annealed for a longer time at 1000°C, the remanent polarization is very low: $\sim$2 μC/cm^2. The cycling led to a loss of remanent polarization, a drawback of ferroelectric memory. Here, it is probably due to the degradation of the film during annealing, which aggravated this phenomenon. Concerning the coercive field, it is the opposite, with a smaller E$_c$ at lower temperature (0.6 MV/cm) and a larger at 1000°C (1.01 MV/cm).
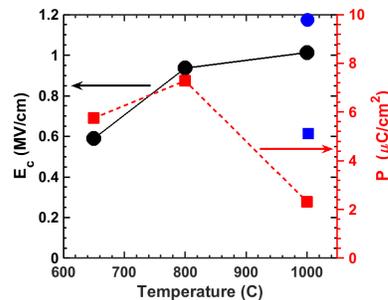
Figure 7.14: Influence of the annealing temperature on the remanent polarization (P$_r$) and the coercive field (E$_c$)). The blue markers correspond to the characteristics for the sample annealed at 1000 °C for 1 sec.

Figure 7.14 summarizes the evolution of the ferroelectric properties with annealing temperature. The blue markers represent the characteristics of the film when annealed at 1000 °C for 1 sec. Sample D5 should not be taken into account for comparison, as the applied electric field was lower to prevent breakdown. It seems that a softer annealing for a longer time on thicker films helped in the crystallization of the orthorhombic structure, resulting in a more pronounced ferroelectric behavior.

7.2.5 Cycling effect

It has been discussed previously that a field cycling improves the characteristics of ferroelectric films and allows the film to recover from an antiferroelectric behavior. The impact of cycling was then studied on sample D4 which showed an antiferroelectric behavior before any cycling (Figure 7.15). The number of cycles was varied from 1 to 10^6 with a frequency of 1 kHz.
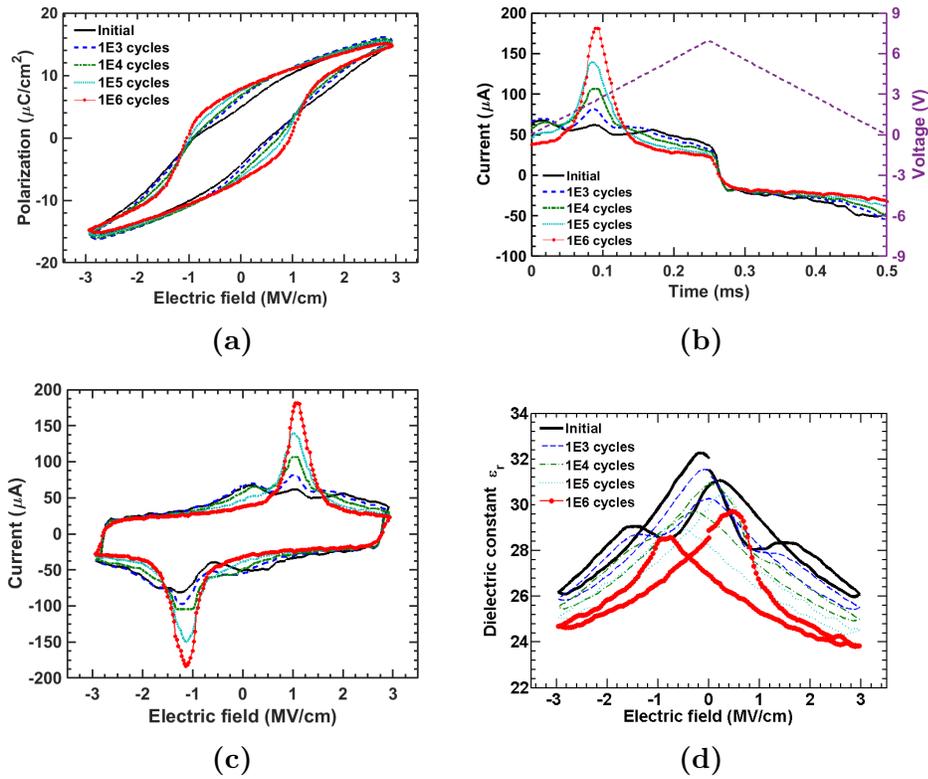
Figure 7.15: Cycling effect on (a) P-E, (b) I-t, (c) I-E and (d) ϵ_r-E characteristics for sample D4 with an anti-ferroelectric behavior initially.

A higher remanent polarization accompanied by a greater stability seems to be the result of the cycling. It is believed that in non-cycled samples, some domain orientations are more favorable, whereas domain wall movements can be at the same time restrained [14].

The transient response is relatively flat initially, but with the increase of cycles, a peak starts appearing, with an increasing amplitude, which implies that the dipoles

are rearranging. Simultaneously, the slope of the P-E hysteresis becomes steeper. This means that more domains are switching almost simultaneously. This steeper slope results in an increase in the remanent polarization.

7.2.6 Fatigue behavior

PZT-based devices exhibit significant polarization fatigue, losing most of their remanent polarization after less than 10^{10} switching cycles in the case where a conductive electrode is used. Otherwise, the degradation of the switching polarization occur between 10^4 and 10^7 cycles [81].

Fatigue characterization was done on samples B and D1 using a frequency of 1 kHz up to 10^8 cycles. The measurement voltage was chosen to get an electric field of 3 MV/cm. Sample B was able to withstand 10^8 cycles without degradation (Figure 7.16).
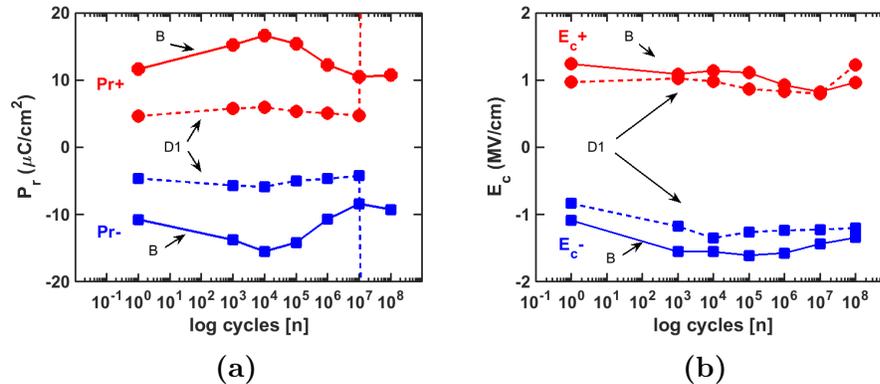
Figure 7.16: Fatigue behavior on samples B and D1

A maximum remanent polarization was obtained after 10^4 cycles, confirming the 'wake-up' behavior when cycling. The coercive field seems to follow P_r trend and is relatively not affected by the cycles. For sample D1, the breakdown of the device happened after 10^7 cycles.

7.3 Study of 6.4 nm devices

The thinnest sample, 6.4 nm, showed a high leakage current due to tunneling, which limits polarization switching. As the TF-1000 analyzer in-house is limited at 1 kHz, the sample was sent to NaMLab for further measurements by Claudia Richter, using a TF-3000 analyzer.

Capacitors with an area of $2x10^4$ μm^2 were first analyzed. Measurements were realized at a frequency of 10 kHz. The initial results (Figure 7.17a) show a paraelectric behavior. The device was then cycled at a frequency of 100 kHz and an applied voltage of 2 V. P-V measurements were performed at a frequency of 10 kHz. A slight increase in ferroelectric behavior can be seen with cycling. However, the leakage current is still high and the breakdown of the device happened at 10^3 cycles.

(a)   (b)
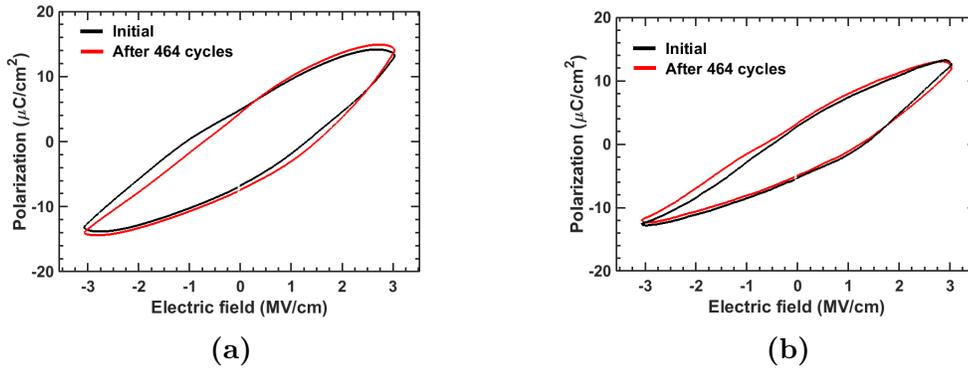
Figure 7.17: (a) P-E loop of a 6.4 nm thick sample with an area of $2x10^4$ μm^2 , (b) Same measurement after leakage current compensation

A method to compensate the leakage current was proposed by Meyer *et al.* [82] in 2005 and was revisited in 2015 by Schenk *et al.* [83]. The final formula of Meyer for the compensated current $i_{comp}(\omega)$ was derived as:

$$i_{comp}(\omega) = \frac{\omega}{\omega_2 - \omega 1} \cdot \left[i_{(\omega_2)} - i_{(\omega_1)} \right] \tag{7.1}$$

where ω is the frequency, ω_1 and ω_2 are two adjacent frequencies with $\omega_1 < \omega_2$

and $i_{(\omega_1)}$ and $i_{(\omega_2)}$ are the current corresponding at these frequencies. Schen *et al.* developed a formula for the compensated polarization $P_{comp}(\omega)$:

$$P_{comp}(\omega) = \frac{1}{\omega_2 - \omega_1} \cdot (\omega_2 P_2 - \omega_1 P_1) \qquad (7.2)$$

where P_1 and P_2 are the uncompensated polarization at frequency ω_1 and ω_2 respectively. P-V measurements were performed at two frequencies, 10 kHz and 12 kHz, and the result after leakage compensation can be seen in Figure 7.17b. The same paraelectric behavior can be observed with a steeper profile.

A device with a smaller area ($1\text{x}10^4 \ \mu m^2$) was tested at the same frequencies of 10 kHz and 12 kHz, an applied voltage of 2.3 V and a cycling frequency of 100 kHz. Figure 7.18 summarizes the results after leakage compensation.
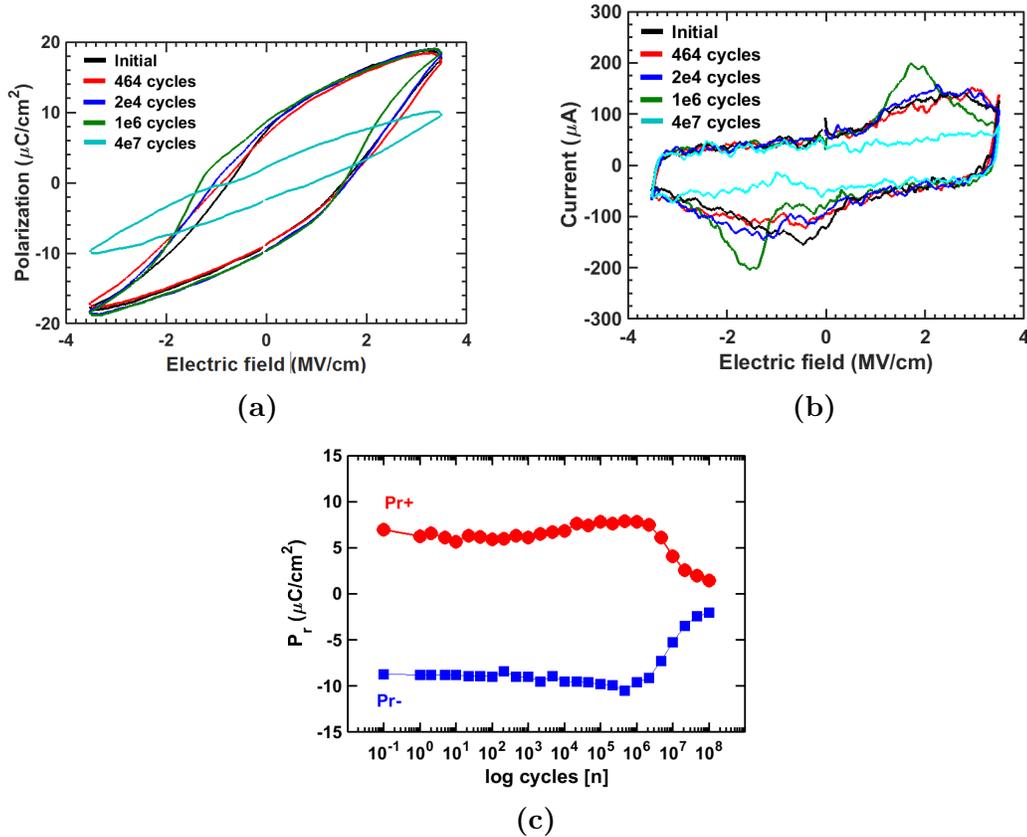
Figure 7.18: (a) P-E loop of a 6.4 nm thick sample with an area of $1\text{x}10^4 \ \mu m^2$ after compensation, (b) I-E response, (c) Fatigue characteristics after a stress at 100 kHz.

The initial hysteresis showed a ferroelectric behavior, which became stronger with cycling. A maximum remanent polarization of 8.8 μC/cm^2 and a coercive field of 1.5 MV/cm was measured. A strong fatigue behavior was also observed (Figure 7.18c). Although a decrease in the remanent polarization starts at 10^6 cycles.
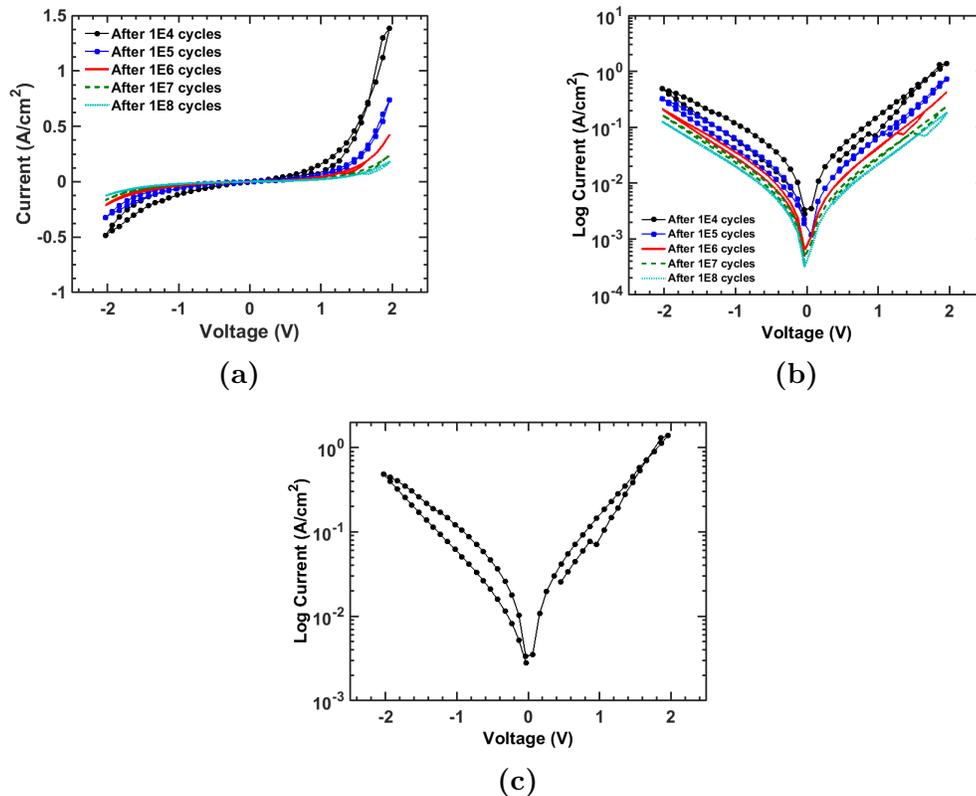
Figure 7.19: (a) I-V characteristics of sample with an area of 1x10^4 μm^2 , (b) I-V curves in log scale, (c) Emphasis on I-V curve after 10^4 cycles.

I-V characteristics were also measured simultaneously on the last sample, after 10^4 cycles, with an applied voltage of 2 V and a step of 0.1 V. Results can be seen in Figure 7.19. The leakage current observed may be attributed to tunneling and to the polycrystalline nature of the layer: the current leaks along grain boundaries. During cycling, the leakage current seems to drop. A possible reason is a change in either the structure or the domain configurations. A memristor characteristic I-V behavior is observed , which suggests resistance change on polarity reversal. This aspect, though not part of this study, certainly needs more further investigations.

7.4 Discussion

Ferroelectric HfO_2 films were studied in order to get a better understanding of the material for transistor and tunnel junction fabrications. The influence of thicknesses and annealing temperatures on the ferroelectric characteristics has been examined. Cycling effect and fatigue behavior were also studied.

XPS/Auger spectroscopy seem to indicate that silicon does not stay in the film but segregates at its interfaces. More characterizations need to be done for a better understanding of the phenomenon.

The film thickness has an impact on the crystallization of the orthorhombic phase. At the same annealing temperature, thick films (22.9 nm) require a stronger mechanical confinement, as the influence of surface energy decreases with thickness, resulting in a higher stability of the monoclinic phase. This was confirmed by XRD with a monoclinic/orthorhombic ratio of 37/63 was calculated. C-V measurements confirmed the presence of true ferroelectric films. Films with a thickness of 9.3 and 13.1 nm exhibited low dielectric constant (~ 30) and high coercive field (> 1 MV/cm) when compared with a PZT sample. A thinner film (6.4 nm) showed the presence of leakage current and a high frequency (10 kHz) combined with a small area ($10\ ^4\mu m^2$) and cycling were necessary to obtain a ferroelectric hysteresis loop with strong coercive field (1.5 MV/cm) and small remanent polarization (8.8 $\mu C/cm^2$)

The influence of annealing temperature was studied on 23.6 nm-thick films. Without annealing, the film showed a linear P-V behavior, confirming the presence of the monoclinic phase with a dielectric constant of 19. Softer annealing resulted in a antiferroelectric-like behavior. This is explained by the presence of defect dipoles in the material. A cycling to 10^5 was necessary to recover from it and to obtain a ferroelectric hysteresis. A softer anneal seem to improve the overall characteristics of the sample with steeper hysteresis and a small increase in the remanent polarization.

From these two investigations, it can be said that 10 nm-thick films seem to be the best thickness in term of ferroelectric performance in comparison to thin (leakage current) and thick (higher stability of the monoclinic phase) films. For thicker films, a softer anneal improved the characteristics. Investigations on the annealing temperatures for 10-nm thick films still need to be performed.

A small cycling is known to improve the overall performance of the material by causing a redistribution of charges and a more homogeneous situation. This was confirmed by studying the effect of cycling on a 23.6 nm-thick sample with a soft anneal. With cycling, the antiferroelectric-like hysteresis became ferroelectric with slopes becoming steeper. This resulted in an increase of the current peaks of the transient current response. A higher peak implies that more domains are switching at the same time.

Fatigue behavior was studied on two different thicknesses, 9.3 and 23.6 nm, by increasing the number of cycles to 10^8, while maintaining a frequency of 1 kHz. The thin sample showed a strong fatigue behavior, without breaking down, while the thickest sample withstood a maximum of 10^7 cycles. Frequency has been found to influence the fatigue behavior of such devices with higher frequencies resulting in a stronger fatigue behavior [14]. Further studies at higher frequencies (1 MHz) and more cycles (10^{12}) need to be performed for a better understanding on the robustness of these devices.

FTJ device was fabricated using a film with a thickness of 6.4 nm. A ferroelectric behavior was obtained for small area and high frequency. The leakage current, through tunneling or/and along grain boundaries, was reduced with cycling, which can be the result of a possible change in the structure of the domain configurations. This film also showed a strong fatigue behavior, up to 10^8 cycles, which is very encouraging for further development. A memristor characteristic I-V behavior was also obtained. However, more investigations need to be done to confirm this observation.

Chapter 8

With the discovery of ferroelectricity in HfO_2, ferroelectric memories are having a second chance for sub-150 nm nodes. However, further investigations are still required to better engineer the film.

In this work, a program has been created using MATLAB based on Miller's [15] and Lue's [16] models. Their approach uses the switching physics of ferroelectric devices along with the physics of MOSFET, based on Brew's charge sheet model. The main difference lies in the expression of the polarization. Both models were computed and compared with simulated data from papers as well as with experimental data. A good match was found between experimental and simulated data, with ferroelectric characteristics similar to the one extracted with the TF 1000 analyzer. This program offers a friendly user interface which can be used to simulate ferroelectric films for FeFET applications.

Physical vapor deposition of aluminum as dopant was studied with multi-stack and solid-source approaches. The first approach was not conclusive, as the physical breakdown of the stack happened during the annealing step. The second approach gave encouraging results, however the lack of repeatability and electrical characterization of the material make it very difficult to use for device application. Additionally, the quality of the film especially the amount of oxygen vacancies in the material, which drastically affects its ferroelectric properties, is not easily controllable using

physical vapor deposition.

The collaboration with NaMLab, Dresden, inventor of the ferroelectric HfO$_2$ films, opened new perspectives. Silicon doped hafnium oxide films deposited using ALD were further investigated for ferroelectric behavior. This film was deposited at NaMLab and further processing was done at RIT. MIM capacitors were fabricated with different oxide thicknesses. It was established that thinner films (6.4 nm) require additional cycling to decrease the leakage current by rearranging the charges in the material. These films exhibit a strong coercive field of 1.5 MV/cm. Thicker films showed a temperature dependent orthorhombic phase. This was confirmed by an improvement of the ferroelectric characteristics when these films were annealed for a longer time at a lower temperature (from P$_r$ = 5 $\mu C/cm^2$ to 8 $\mu C/cm^2$). With cycling, recovery from an initial antiferroelectric-like hysteresis was observed. However, a fatigue behavior can be a result of further cycling. Thin films of 10 nm-thick Si:HfO$_2$ showed low dielectric constant ($\sim$ 30) and high coercive field ($>$ 1 MV/cm). Further analyses on the impact of annealing temperature on thinner films need to be performed for integration in transistor.

Finally, thin film (6.4 nm) was studied for FTJ applications. A memristor like current-voltage curve was observed after 10^4 cycles. Further investigations are necessary to confirm the true memristive behavior of this device.

This work may lead to the fabrication of FeFET and FTJ devices.

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Appendix A

Structural parameters of monoclinic, tetragonal and cubic

phases of HfO$_2$ [84]

	Present work	[39] US-PP, PW	[40] NC-PP, PBE	[41] NC-PP, PBE	[42] US-PP, PBE	Exp.[a]	Exp.[b]
Monoclinic volume	35.13	34.81	36.39	38.01	34.81	34.62	34.67
a	5.148	5.128	5.215	5.291	5.132	5.117	–
b	5.191	5.191	5.293	5.405	5.189	5.175	–
c	5.334	5.297	5.350	5.366	5.307	5.291	
β	99.69	99.71	99.73	97.92	99.78	99.22	
B	238	152	–	–	–	–	282, 145
ΔE	0.0	0.0	–	–	–	–	
E_g	4.10	3.80	3.6	–	4.1	5.7	
Tetragonal volume	33.72	33.30	34.82	37.74	33.12	35.07	
a	3.591	3.578	3.655	3.747	3.578	3.642	
c	5.228	5.200	5.220	5.373	5.181	5.289	
c/a	1.455	1.453	1.428	1.434	1.448	1.452	
δ	0.055	0.055	0.033	0.041	0.051	–	
B	244	201	183	–	–	–	
ΔE	0.163	0.156	0.135	–	0.160	–	
E_g	4.85	4.45	–	–	–	–	
Cubic volume	32.71	32.45	34.10	36.15	32.49	32.77	
a	5.076	5.063	5.148	5.248	5.070	5.080	
B	258	260	257	–	–		
ΔE	0.260	0.237	0.169	–	0.240		
E_g	3.95	3.70	–	–	–	5.6–6.0	

[a] See [43] for monoclinic, [44] for tetragonal (high-temperature results at $T = 1800\,°C$), [45] for cubic HfO$_2$. Bandgap of monoclinic phase after [46], of the cubic phase after [47].
[b] See [48, 49] for monoclinic HfO$_2$.

Appendix B

Simulations: Comparison with results from papers

B.1 "Physics of the ferroelectric nonvolatile memory field effect transistor", Miller *et al.* [15]
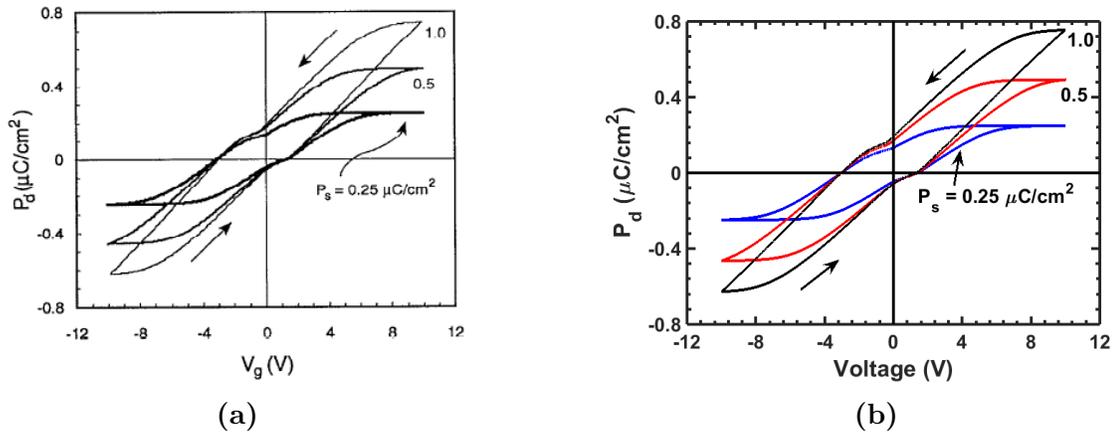
Other published and simulated graphs.

(a)   (b)

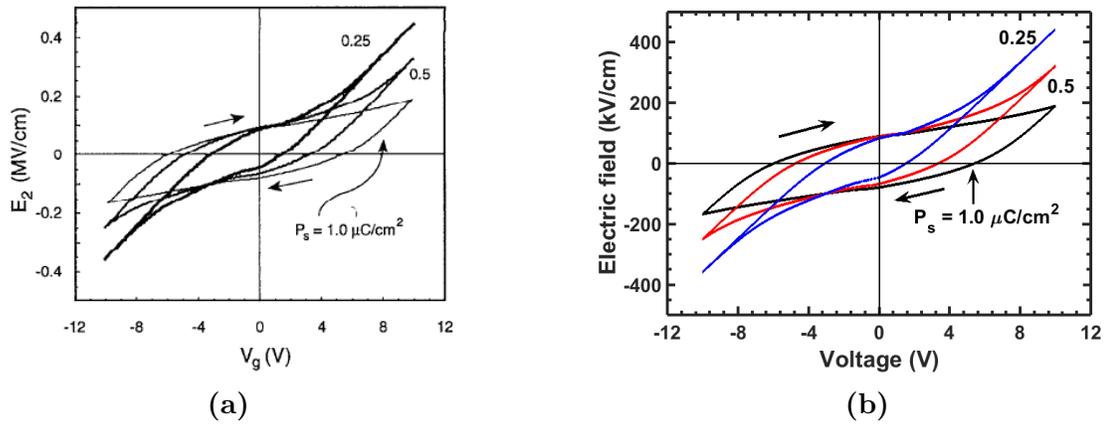**Figure B.1:** (a) P-V from Miller's paper , (b) Simulated P-V
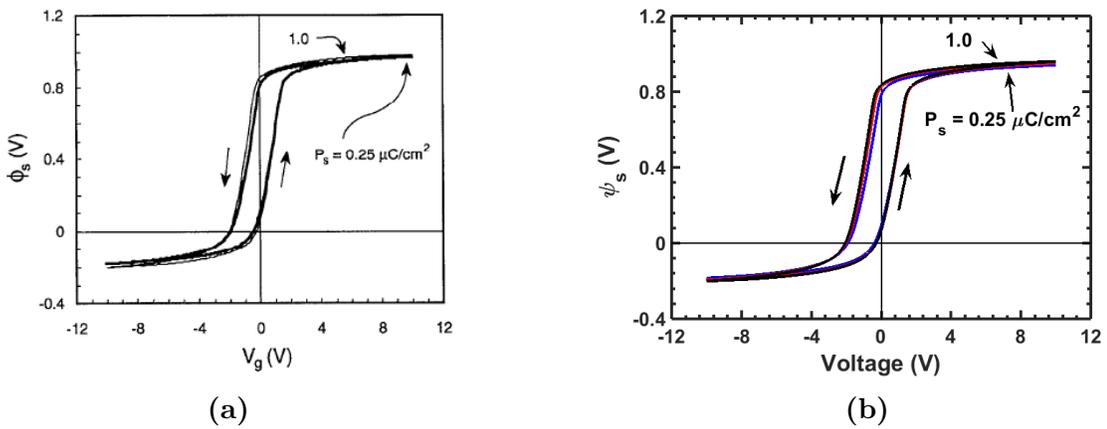
Figure B.2: (a) E-V from Miller's paper , (b) Simulated E-V

Figure B.3: (a) ψ-V from Miller's paper , (b) Simulated ψ-V
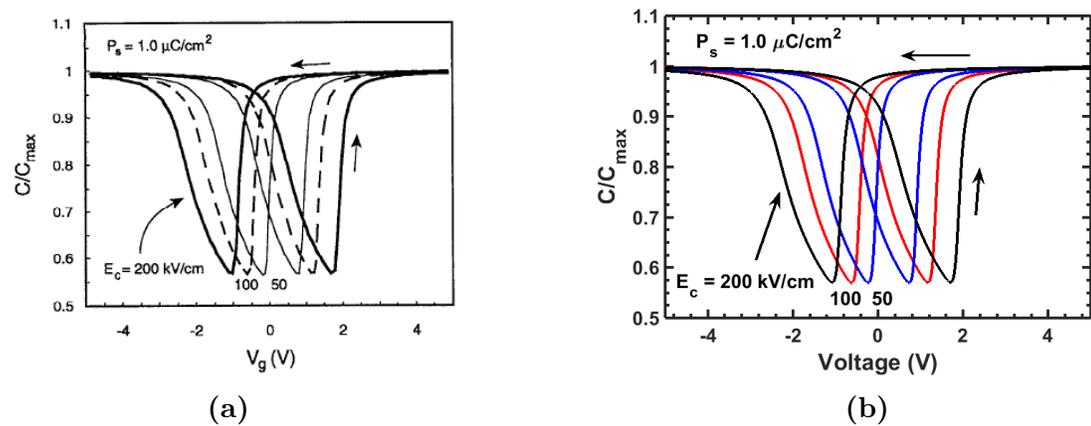

Figure B.4: (a) Normalized C-V from Miller's paper , (b) Simulated normalized C-V

B.2 "Modeling of metal-ferroelectric-insulator-semiconductors based on Langmuir-Blodgett copolymer films", Reece *et al.* [69]
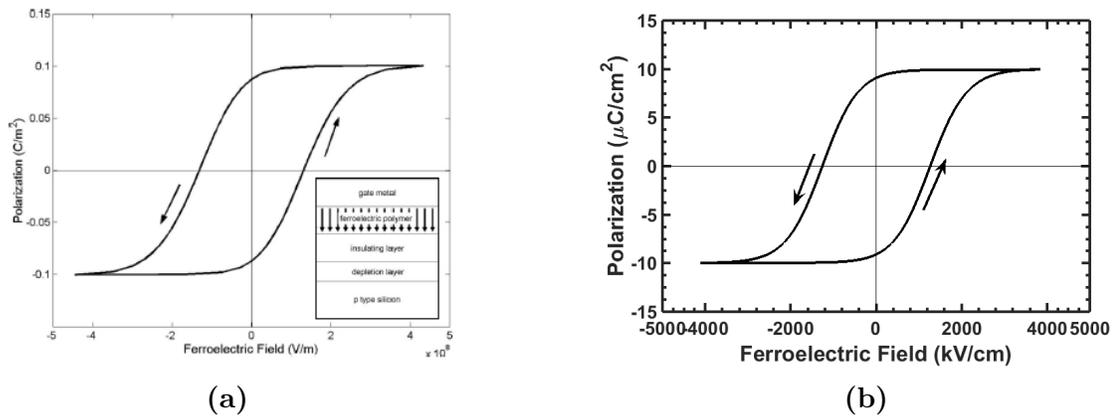
Other published and simulated graphs.

(a)   (b)

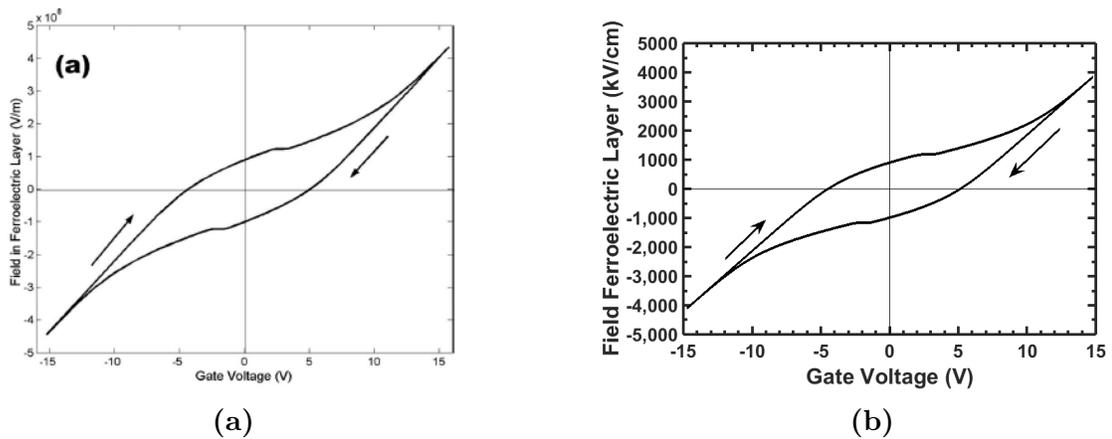**Figure B.5:** (a) P-E from Reece's paper , (b) Simulated P-E
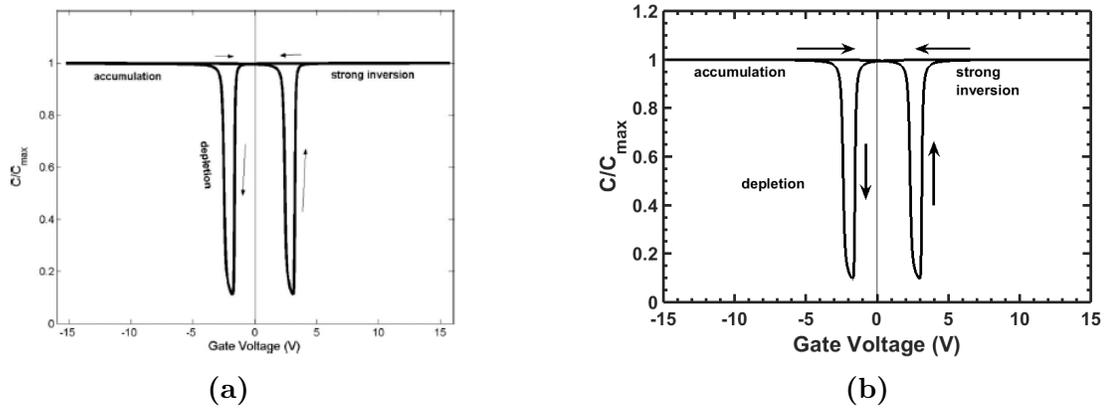

(a)   (b)

Figure B.6: (a) E-V from Reece's paper , (b) Simulated E-V

(a)   **(b)**

Figure B.7: (a) C-V from Reece's paper , (b) Simulated C-V

Appendix C

Design of experiments of HfO₂

Sample	Process Parameters					Measurements		
	SP *(mT)*	Ar:O$_2$	Ar *(mT)*	O$_2$ *(mT)*	t *(Å)*	t-σ *(Å)*	n	n-σ
1	9	5:1	7.5	1.5	502	25.8	1.955	0.048
2	6	3:1	4.5	1.5	546	33.8	1.895	0.052
3	12	7:1	10.5	1.5	548	22	1.91	0.041
4	6	7:1	5.25	0.75	521	26.8	1.955	0.047
5	9	5:1	7.5	1.5	486	4.5	1.993	0.019
6	12	3.8:1	9.5	2.5	494	6.4	1.98	0.023
7	9	5:1	7.5	1.5	473	14.7	1.976	0.03
8	12	7:1	10.5	1.5	521	22.7	1.958	0.046
9	12	3:1	9	3	524	26.8	1.905	0.047
10	9	-	9	-	-	-	-	-