DESIGN OF AN ION IMPLANTATION PROCESS MONITORING CHIP ON I.C.E. AND PROVIDE A METHODOLOGY FOR EVALUATION OF TESTING RESULTS.

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ABSTRACT

A test chip has been designed for experimental use in determining and maintaining the operation of an Ion Implanter. The structures on this chip provide information on the Implant processing and post Implant annealing. Implant dose will be monitored using van der PAUW [1] structures, implanted resistors and comparison of threshold adjusted MOSFET with adjacent non adjusted MOSFET. Surface effects and annealing information will be taken from analysis of gated diodes [2].

INTRODUCTION

Ion Implantation is the introduction of accelerated high energy dopant ions into a semiconductor substrate. Subsequent annealing is needed to diffuse these impurity ions and restore the crystal quality. Ion Implantation is an alternate and more controllable method of introducing impurities into a silicon substrate than diffusion. It differs from solid, gas and spin-on sources in that the impurities are not introduced at the solid solubility limit of the impurity. Aside from the greater control of doping, Implantation offers higher purity and dose levels than conventional solubility techniques. This improved method of introducing impurities requires testing and monitoring of implant dose controllability and post Implant Annealing effects.

A test chip has been designed and layed out on I.C.E. (Integrated Circuit Editor)(*) to characterize an Ion Implanter(**). This chip contains devices to monitor resistivity, which indicates dose, and surface effects such as capture cross section of surface generation and recombination sites, charge storage in the oxide, bulk regions and interfaces and depletion region effects. The chip will be used to determine the capability of the Implanter upon start-up , to determine the processing capabilities enabled by the Implanter and provide a means for future experiments involving Implantation at RIT.

* I.C.E. is an in house computer system for the generation of masks

** Rochester Institute of Technology recently received a Varian Ic Implanter from EASTMAN KODAK CO in March 1987.

CHIP DESIGN

The test chip contains devices to monitor three primary parameters for Ion Implant processing. These three parameters are surface effects, sheet resistivity and low dose implants.

The first parameter is surface effects. A gated diode [2] as shown in Figure 1 will be reversed biased and the reverse leakage current as a function of gate bias characteristics (Figure 2) will be used to determine the optimum anneal. In Figure 2 we see an additional current contribution, I(s). This added current to the metallurgical leakage current, I(m), is a result of the depletion of the bulk region under the metal gate. This depletion of the bulk region allows additional trap sites and imperfections in the lattice to contribute to the reverse leakage in the diode. A design of experiment involving different anneal processing to minimize the I(s) current addition would optimize the anneal. As seen in Figure 1 the n-bulk region is an implanted region. This is to ensure the depletion of a region that has been implanted and damaged by the high energy ions. The two diode regions can be reversed to see the effect of anneal on p-type bulk regions.

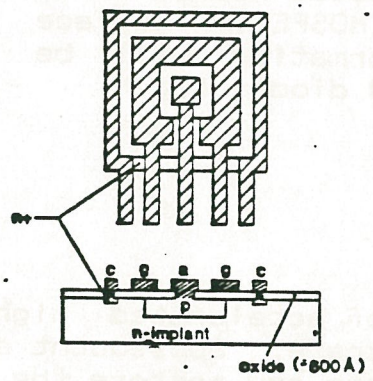


Figure 1 - Gated Diode

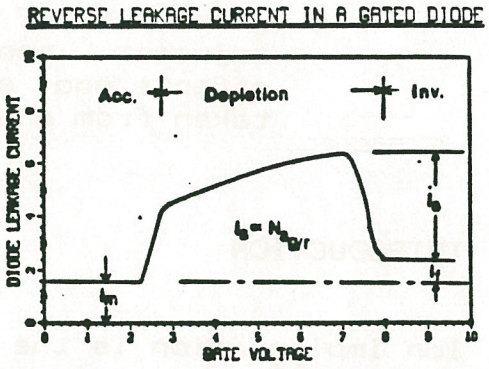


Figure 2 - Reverse Current Through A Gated Diode

The second parameter to be monitored is the effect of a low dose implant. Often times it is very difficult to control and even detect a low dose implant. The method proposed on this chip is to place two p-type MOSFETs (Figure 3) "back-to-back", use a low dose implant to do a threshold adjust on one of the transistors and monitor the capacitance-voltage shift between the two devices.

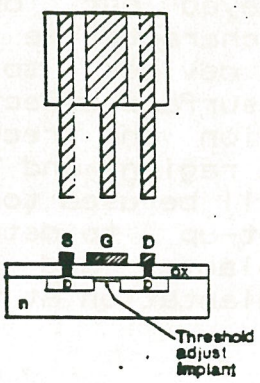


Figure 3 - MOSFET

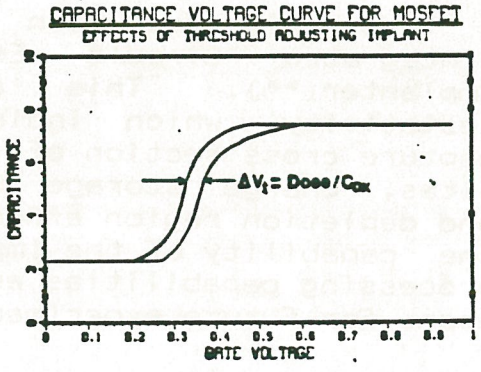
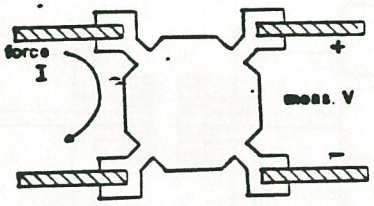


Figure 4 - Capacitance Voltage Plot For FET

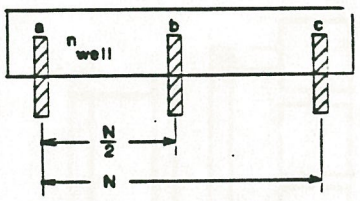
The reason the two devices are placed in close proximity is to eliminate any difference in resistivity of the bulk region. The expected capacitance-voltage curves and the equation relating the voltage shift to the implant dose are shown in Figure 4. The oxide capacitance can be measured or calculated from the oxide thickness.

The final parameter to be monitored is the sheet resistivity. This will be done using two different devices. The first is the van der PAUW [1] structure as shown in Figure 5. A known current is forced the leads and the voltage is measured on the opposite side. The equation given is basically a "V=IR" with a pi/ln2 term which relates to the mathematically derived spreading resistance of the symmetrical device. The "k" is a constant that will be determined and is a function of the I.C.E. generated van der PAUW and the actual processing of the structure (i.e. It is a fine tune of the equation). This "k" value can be determined using a center-tap resistor as shown in Figure 6. The equation given shows the sheet resistivity to be equal to the difference in resistance from the full length of the resistor and half the length of the resistor, multiplied by two and divided by "N" which is the number of squares from points "a" to "c". These structures are designed such that the number of squares from points "a" to "b" are half that of "a" to "c". This resistivity can be compared to the van der PAUW resistivity to determine the value of "k".



$$RHO_s = \frac{k\,\Pi}{\ln 2} \cdot \frac{V}{I}$$

Figure 5 - Van Der PAUW



$$RHO_s = 2\,[R_{ac} - R_{bc}] / N$$

Figure 6 - Center Tap Resistor

In addition to these structures implanted resistors , a vertical NPN transistor and a lateral PNP transistor are included to monitor the effects on actual device yield. For example, as the anneal is optimized the gain of vertical NPN transistors may shift as a result of different heat cycles at anneal.

RESULTS

Figure 7 is a diagram of the I.C.E. generated Implant test chip.

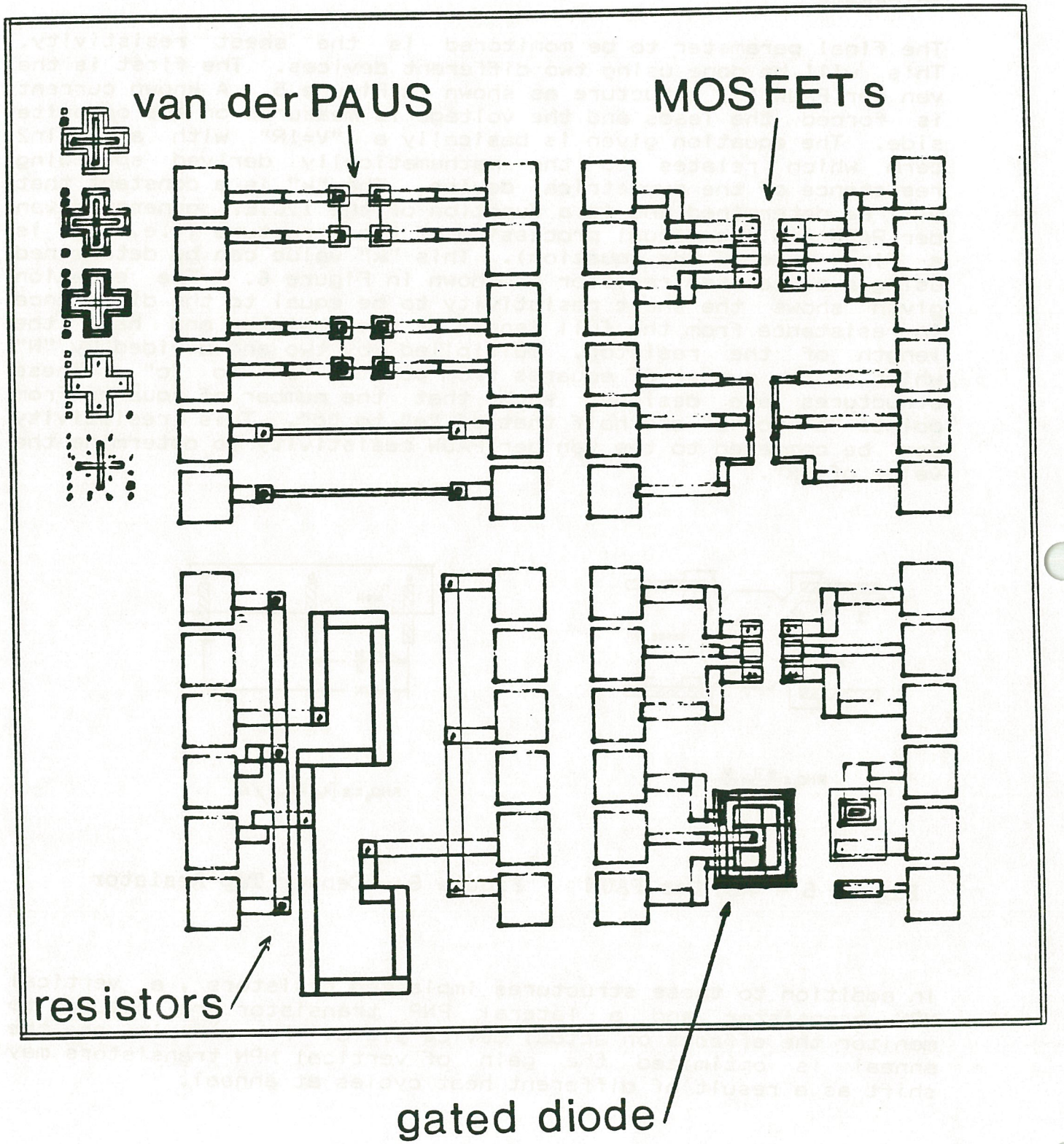


Figure 7 – Ion Implanter Test Chip

CONCLUSIONS

A chip design has been provided to monitor the Ion Implantation processing. This chip will be used to determine the capability of the Implanter upon start up, to be stepped in on product wafers using the implanter to monitor the Implant processing effect on product yield ,in future labs at RIT to introduce students to Implant processing and process monitoring and control and finally for research.

ACKNOWLEDGEMENTS

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REFERENCES

[1] van der PAUW, L. J., "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape", Philips Research Reports, NY, Feb. 1958.

[2] Kamins and Muller, Device Electronics for Integrated Circuits, John Wiley and Sons, NY, 1977 .p 331-333.